RF2908

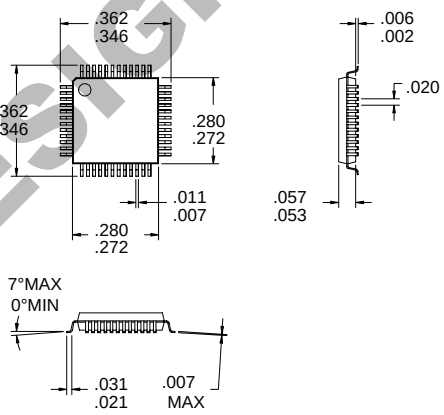
915MHZ SPREAD SPECTRUM RECEIVER WITH PLL FREQUENCY SYNTHESIZER

Typical Applications

- Digital Cordless Telephones
- Secure Communication Links
- Wireless LANs
- Inventory Tracking
- Wireless Security
- Battery Powered Applications

Product Description

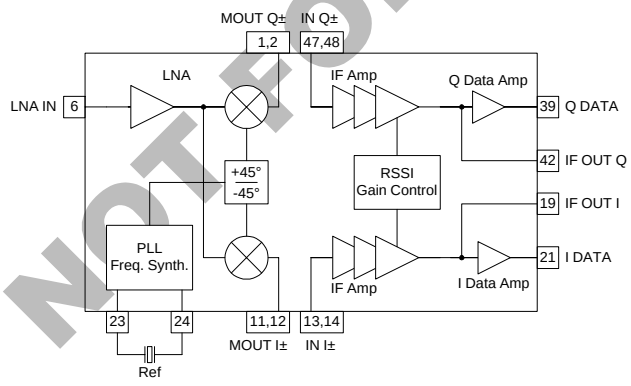
The RF2908 is a monolithic integrated circuit specifically designed for direct-sequence spread-spectrum systems operating in the 902MHz to 928MHz ISM band. The part includes a direct conversion receiver, quadrature demodulator, dual IF amplifiers with gain control and RSSI, on-chip programmable baseband filters, dual data comparators, and a serially programmable 86-channel PLL frequency synthesizer. Two cell or regulated three cell (3.6V maximum) battery applications are supported by the part. The part is also designed to operate in compliance with FCC Part 15.247. The device is provided in 48-lead plastic LQFP packaging.



Package Style: LQFP-48

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☑ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Refer to the Detailed Functional Block Diagram for description of full functionality

Functional Block Diagram

Features

- FCC Part 15.247 Compliant
- Direct Conversion Receiver
- On-Chip 86 Channel Frequency Synthesizer
- On-Chip Selectable IF Bandwidths
- 2.7V to 3.6V Operation

Ordering Information

RF2908	915MHz Spread Spectrum Receiver with PLL Frequency Synthesizer

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Absolute Maximum Ratings

Parameter	Ratings	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Control Voltages	-0.5 to +3.6	V_{DC}
Input RF Level	+20	dBm
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.6V, Freq=915MHz
Frequency Range		902 to 928		MHz	
Cascaded Voltage Gain		100		dB	
Cascaded Noise Figure		6.0	8.0	dB	
Cascaded Input IP_3		-12		dBm	High Gain
		+5.5		dBm	Low Gain
RX Sensitivity		-100		dBm	IF BW=960kHz, Freq=915MHz, S/N=8dB
LO Leakage		-65		dBm	At LNA IN
RSSI DC Output Range		0.35 to 3.1		V	R_{LOAD}=51kΩ
RSSI Sensitivity		30		mV/dB	
RSSI Dynamic Range	60	65		dB	
LNA and Mixer					
Operating Frequency Range		902 to 928		MHz	
Voltage Gain		22		dB	
Noise Figure		6.0	8.0	dB	
RF Input Impedance		50		Ω	
RF Input VSWR			2:1		
Input IP_3	-20	-12		dBm	At maximum gain. ATTN=LOW
		+5.5		dBm	At minimum gain. ATTN=HIGH
Quadrature Phase Balance		±3	±5	°	With expected LO amplitude and harmonic content.
Quadrature Amplitude Balance		±1		dB	
Mixer Output Impedance	150	200	250	Ω	Differential
DC Current Consumption	26	33	39	mA	Operating at a 3.3V supply voltage.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
IF and Data Amplifiers					
IF Frequency Range	Note 1		9.6	MHz	
Voltage Gain	77	80	83	dB	
Noise Figure		5		dB	At maximum gain setting
		35		dB	At minimum gain setting
Input IP3		-65		dBm	At maximum gain setting
		+2		dBm	At minimum gain setting
Output DC Offset		0	25	mV	
Gain Control Range	65	70		dB	
Gain Control Voltage Range	1.2		2.0	V	
Gain Control Sensitivity		-0.08		dB/mV	
VGA Output Voltage		500		mV_{PP}	
VGA DC Output Voltage		1.7		V	
Output P1dB	1	1.64		V_{PP}	Driving a 5kΩ load
RSSI Range		60		dB	At maximum gain setting
RSSI Output Voltage Compliance	55	0.5 to 2.4		V	Maximum RSSI is 2.5V or V_{CC}-0.3, whichever is less.
Input Impedance	1.5	2	2.5	kΩ	Differential
					Note 1. The lower cutoff frequency is a function of: a) input DC blocking cap size; b) DC feedback capacitor; and, c) gain setting. But, recommended component values will yield a cutoff of <10kHz.
Filters					
Characteristics		Five pole Bessel			Five pole Bessel internal LPF. Three pole external LPF.
Bandwidth		1, 2, 4, 8		MHz	Selectable from 1, 2, 4, and 8MHz. Refer to "IF Bandwidth Response" chart.
Passband Ripple			1	dB	
Group Delay			100	ns	At 8MHz, increasing as bandwidth decreases.
Ultimate Rejection	80	100		dB	
Data Amplifiers					
Voltage Gain		100		dB	
Bandwidth	10			MHz	
Rise and Fall Time		2	5	ns	
Logic High Output	V_{CC}-0.3V			V	Can sink/source 1mA and maintain these logic levels.
Logic Low Output			0.3	V	Can sink/source 1mA and maintain these logic levels.
PLL, Synthesizer, VCO and LO					
VCO Tuning Range		800 to 1200		MHz	
VCO Sensitivity	20	30	40	MHz/V	Determined by external resistor.
Charge Pump Current		100		µA	KPD=100µA/2π=0.0159ma/2π rad
Reference Frequency Crystal		9.6	20	MHz	
Reference Crystal Rs		60	80	Ω	
Phase Noise		-66		dBc/Hz	10kHz offset.
		-96		dBc/Hz	100kHz offset.
LO Output Level		-10		dBm	Into 100Ω differential load
Lock Time		1.5		ms	From sleep mode.
Step Size		300		kHz	86 channels in the 902MHz to 928MHz ISM band.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Power Down Control					
Logical Controls “ON”	V_{CC}-0.3V		V_{CC}+0.3V	V	Voltage supplied to the input
Logical Controls “OFF”	0		0.3	V	Voltage supplied to the input
Control Input Impedance		>1		MΩ	
Turn On Time		1		ms	Reference Crystal=9.6MHz. Dependent on reference crystal. Higher frequencies reduce turn on/off times.
Turn Off Time		1		ms	Reference Crystal=9.6MHz. Dependent on reference crystal. Higher frequencies reduce turn on/off times.
RX to TX and TX to RX Time		100		µs	
Power Supply					
Voltage	2.7	3.3	3.6	V	
Current Consumption		50	62	mA	V_{CC}=3.3V; RX ENABL=HIGH; PLL ENABL=HIGH
		50		µA	V_{CC}=3.3V; Sleep Mode
		45	57	mA	V_{CC}=3.3V; RX ENABL=LOW; PLL ENABL=HIGH

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Pin	Function	Description	Interface Schematic
1	MOUT Q-	The complementary quadrature phase signal output from the front-end mixer. See pin 2.	
2	MOUT Q+	The quadrature phase signal output from the front-end mixer.	
3	MIX VCC	Supply voltage for the front-end quadrature mixers.	
4	MIX GND	Ground connection for the front-end quadrature mixers.	
5	LNA GND	Ground connection for the low noise amplifier (LNA).	
6	LNA IN	Input to the attenuator and LNA.	
7	SW GND	Ground connection for the input attenuator.	
8	LNA VCC	Supply voltage for the LNA.	
9	SW GND2	Ground connection for the input attenuator.	
10	ATTN	Input attenuator control point. When connected “high”, the attenuator adds 20dB of series attenuation. When connected “low”, the attenuator adds 0dB of series attenuation.	
11	MOUT I+	The in-phase signal output from the front-end mixer.	
12	MOUT I-	The complementary in-phase signal output from the front-end mixer. See pin 12.	
13	IN I+	Input for the in-phase IF channel.	
14	IN I-	Complementary input for the in-phase IF channel.	
15	GND2	Ground for VCC2.	
16	DCFB I	DC feedback capacitor for in-phase channel.	
17	VCC2	Power supply for VGA amplifier 3, differential to single-ended converter, and post filter.	
18	GND3	Ground for VCC3.	
19	IF OUT I	Analog signal IF output for in-phase channel.	
20	VCC3	Power supply for data amplifier.	
21	I DATA	Logic-level data output for the in-phase channel. This is a digital output signal obtained from the output of a Schmitt trigger.	
22	RSSI I	Received signal strength indicator for the in-phase channel.	
23	OSC B	Base connection point for external reference crystal. The reference crystal is connected between this pin and ground.	
24	OSC E	Emitter connection point for external reference crystal. Feedback capacitors are connected between this pin and ground.	
25	LE	Latches data entered into the serial port. Data is clocked into the latch on the rising edge of LE. See table and timing diagram.	
26	PLL CLK	PLL shift register clock. The rising edges of this clocking signal load in the serial data present at the PLL DATA input pin into the internal latch. See table and timing diagram.	
27	PLL DATA	Input data for loading the counters. Clocked, serial data at this port is presented to the shift register, then to the latch, and finally to the counter. Each clock transition sends a single bit to the on-board 7-bit shift register. The MSB is loaded first. See table and timing diagram.	
28	PLL GND	Ground connection for the PLL.	
29	PLLD VCC	Supply voltage for the PLL.	
30	LO OUT B	Complementary local oscillator output. See pin 33.	
31	RESNTR+	This port is used to supply DC voltage to the VCO as well as tune the center frequency of the VCO.	
32	RESNTR-	This is the complementary port to pin 31. Refer to pin 31.	
33	LO OUT	Local oscillator output.	
34	DO	Connection point for the loop filter.	

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Pin	Function	Description	Interface Schematic
35	PLL ENABL	This pin is used to power up or down the VCO and PLL. A logic high (PLL ENABL>2.0V) powers up the VCO and PLL circuitry. A logic low (PLL ENABL<1.0V) powers down the PLL and VCO.	
36	RX ENABL	Enable pin for the receiver circuits. RX ENABL>2.0V powers up all receiver functions. RX ENABL<1.0V turns off all receiver functions except the PLL functions and the RF mixer.	
37	BW SEL2	Bandwidth select logic input. Pin 37 and pin 38 provide a two bit control word for the setting of the IF bandwidth. See Table1.	
38	BW SEL1	Bandwidth select logic input. Pin 37 and pin 38 provide a two bit control word for the setting of the IF bandwidth. See Table1.	
39	Q DATA	Logic-level data output for the quadrature channel. This is a digital output signal obtained from the output of a Schmitt trigger.	
40	RSSI Q	Received signal strength indicator for the quadrature channel.	
41	VREF	Gain control reference voltage.	
42	IF OUT Q	Analog signal IF output for quadrature channel.	
43	VGC	Gain control voltage.	
44	VCC1	Power supply for bias circuits and VGA amplifiers for both the in-phase and quadrature channels.	
45	DCFB Q	DC feedback capacitor for quadrature channel.	
46	GND1	Ground for VCC1 for both the in-phase and quadrature channels.	
47	IN Q-	Minus input for quadrature channel	
48	IN Q+	Plus input for quadrature channel	

Table 1: Bandwidth Selection Controls

BWSEL1	BWSEL2	IF_{-3dB} Frequency
0	0	1MHz
0	1	2MHz
1	0	4MHz
1	1	8MHz

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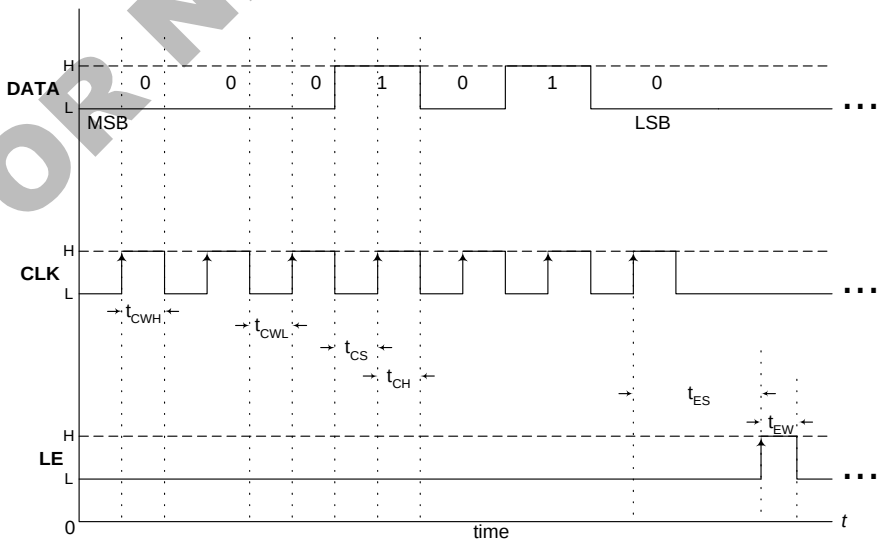
Table 2: Channel Plan

Data	f, MHz	Data	f, MHz	Data	f, MHz	Data	f, MHz
0	902.4	22	909	44	915.6	66	922.2
1	*	23	909.3	45	915.9	67	922.5
2	903	24	909.6	46	916.2	68	922.8
3	903.3	25	909.9	47	916.5	69	923.1
4	903.6	26	910.2	48	916.8	70	923.4
5	903.9	27	910.5	49	917.1	71	923.7
6	904.2	28	910.8	50	917.4	72	924
7	904.5	29	911.1	51	917.7	73	924.3
8	904.8	30	911.4	52	918	74	924.6
9	905.1	31	911.7	53	918.3	75	924.9
10	905.4	32	912	54	918.6	76	925.2
11	905.7	33	912.3	55	918.9	77	925.5
12	906	34	912.6	56	919.2	78	925.8
13	906.3	35	912.9	57	919.5	79	926.1
14	906.6	36	913.2	58	919.8	80	926.4
15	906.9	37	913.5	59	920.1	81	926.7
16	907.2	38	913.8	60	920.4	82	927
17	907.5	39	914.1	61	920.7	83	927.3
18	907.8	40	914.4	62	921	84	927.6
19	908.1	41	914.7	63	921.3	85	927.9
20	908.4	42	915	64	921.6		
21	908.7	43	915.3	65	921.9		

*Data 1 is invalid.

Timing Diagram



Example: Load Sequence for Channel #10 (905.4 MHz)

Decimal 10 = 0 0 0 1 0 1 0 Binary

MSB LSB

Minimum Times:

t_{CWH} = 143 ns
t_{CWL} = 143 ns
t_{EW} = 74 ns
t_{ES} = 143 ns
t_{CS} = 36 ns
t_{CH} = 36 ns

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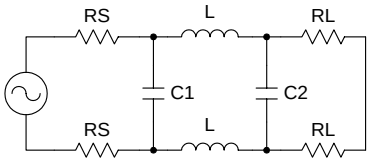
Differential Filter Design Information

Butterworth Response



$$C1 = \frac{C1bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; C2 = \frac{C2bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; L = \frac{Lbw \cdot RL \cdot 10^{6}}{2 \cdot \pi \cdot fc}$$

$$C1bw = 4.5325; C2bw = 13.5691; Lbw = 0.1743$$

$$RS = 125; RL = 1000; \frac{RS}{RL} = 0.125$$

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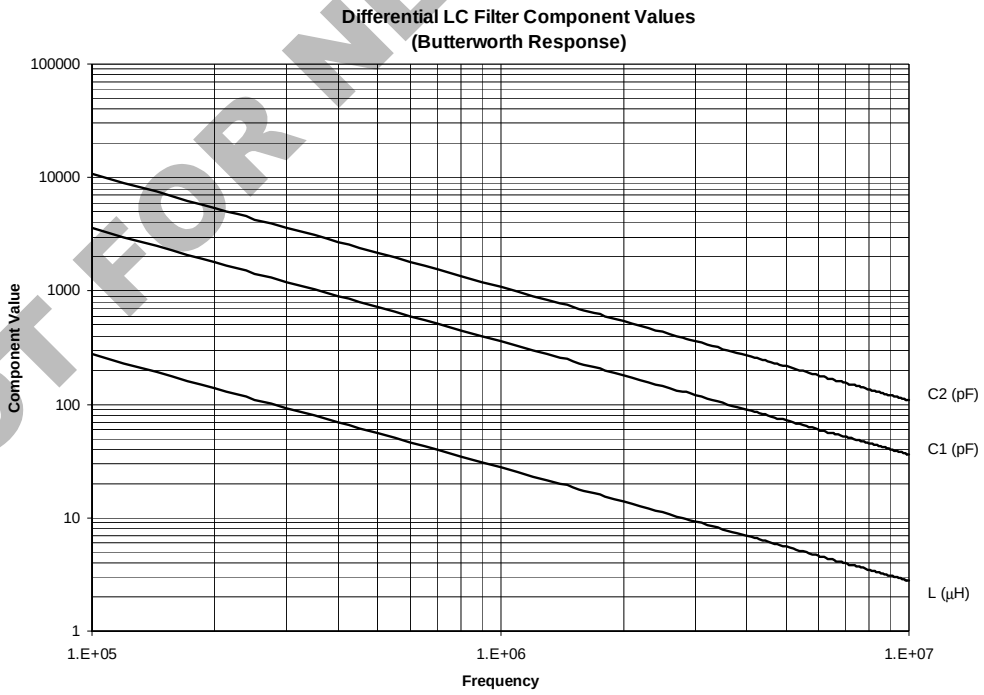
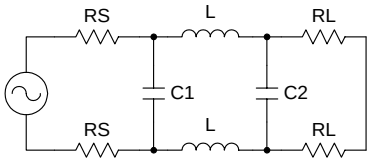


Differential Filter Design Information (Cont.)

Bessel Response



$$C1 = \frac{C1bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; C2 = \frac{C2bw \cdot \frac{1}{2} \cdot 10^{12}}{2 \cdot \pi \cdot fc \cdot RL}; L = \frac{Lbw \cdot RL \cdot 10^{6}}{2 \cdot \pi \cdot fc}$$

$$C1bw = 2.6163; C2bw = 13.6373; Lbw = 0.1083$$

$$RS = 125; RL = 1000; \frac{RS}{RL} = 0.125$$

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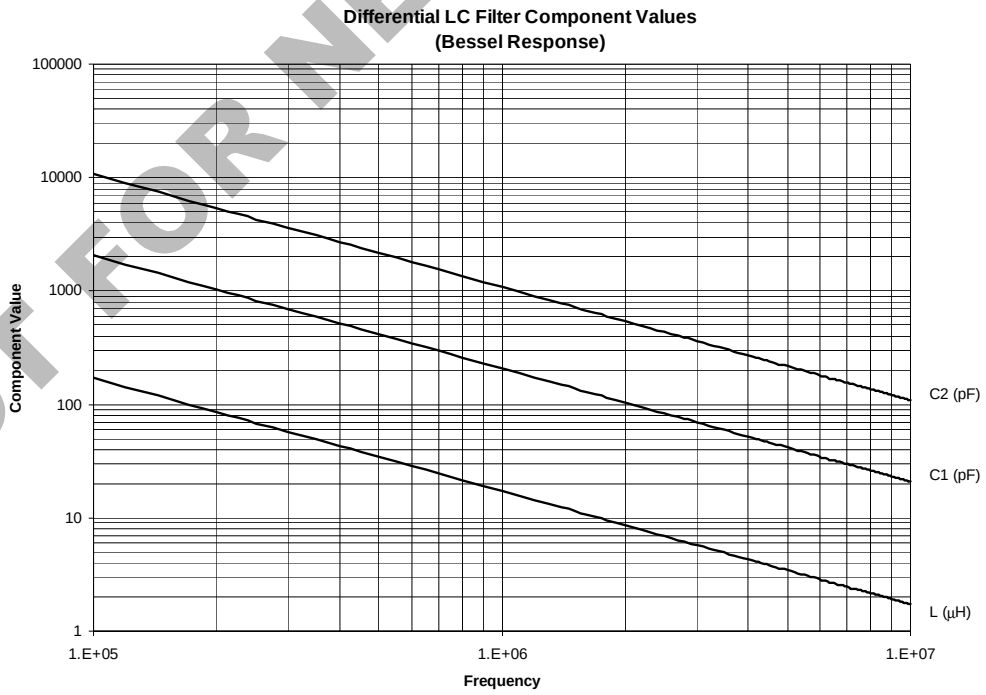
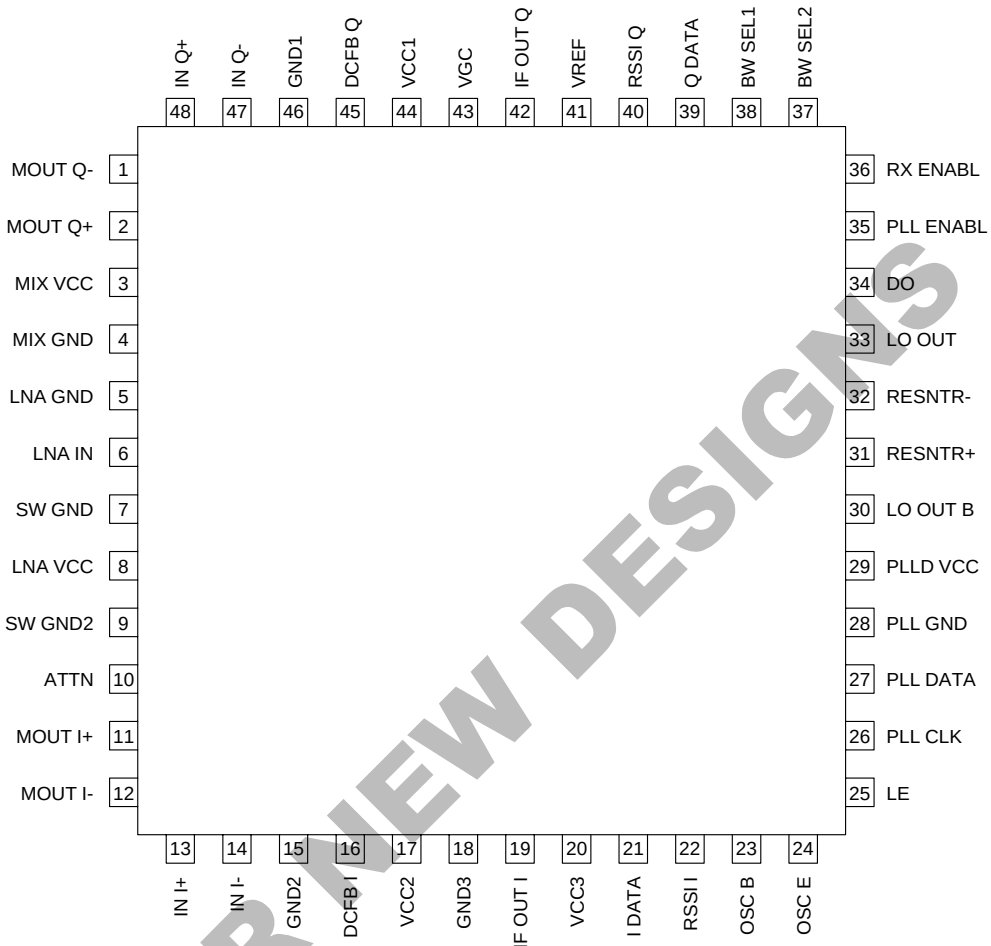


Pin Out



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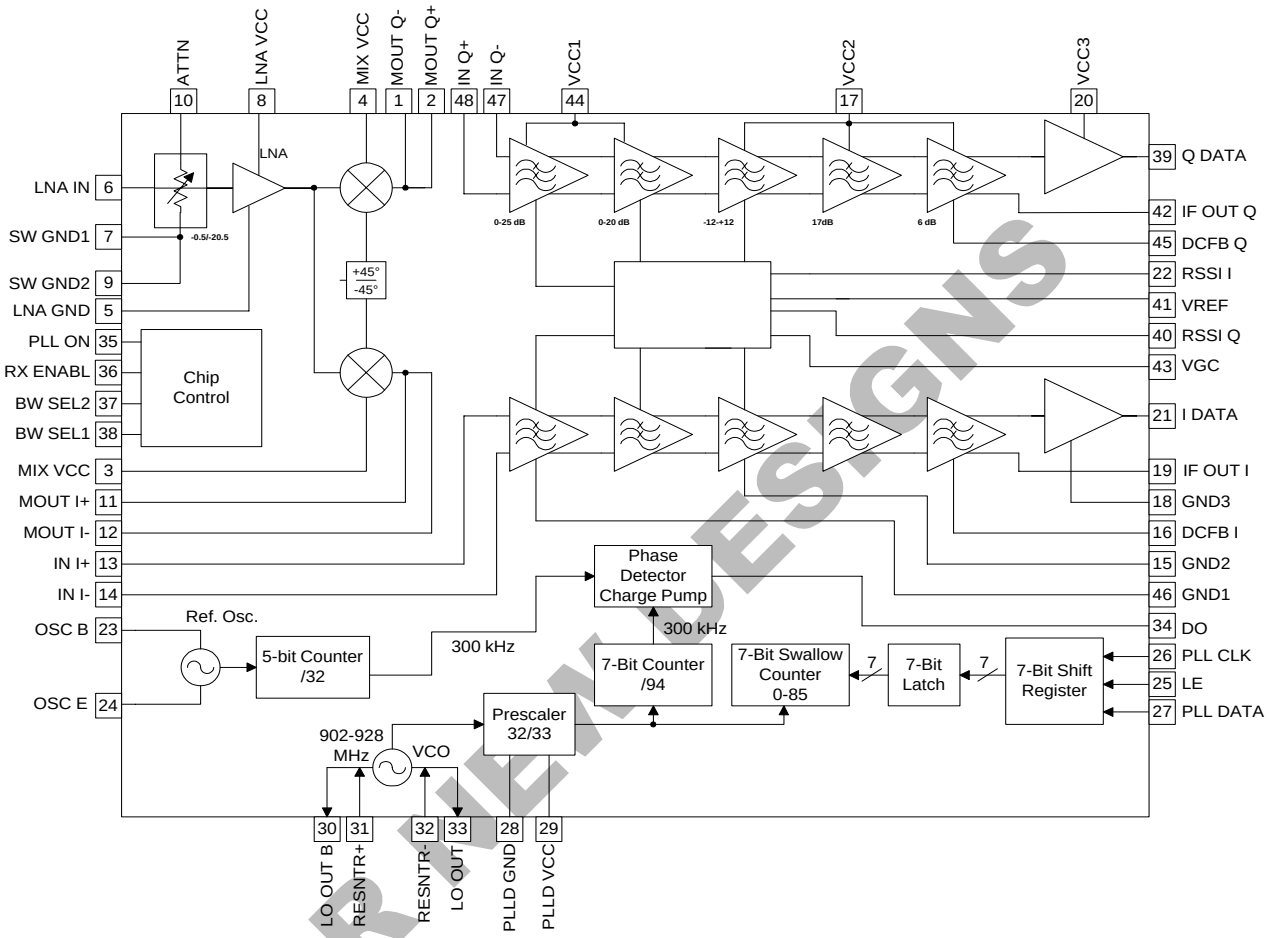
Detailed Functional Block Diagram



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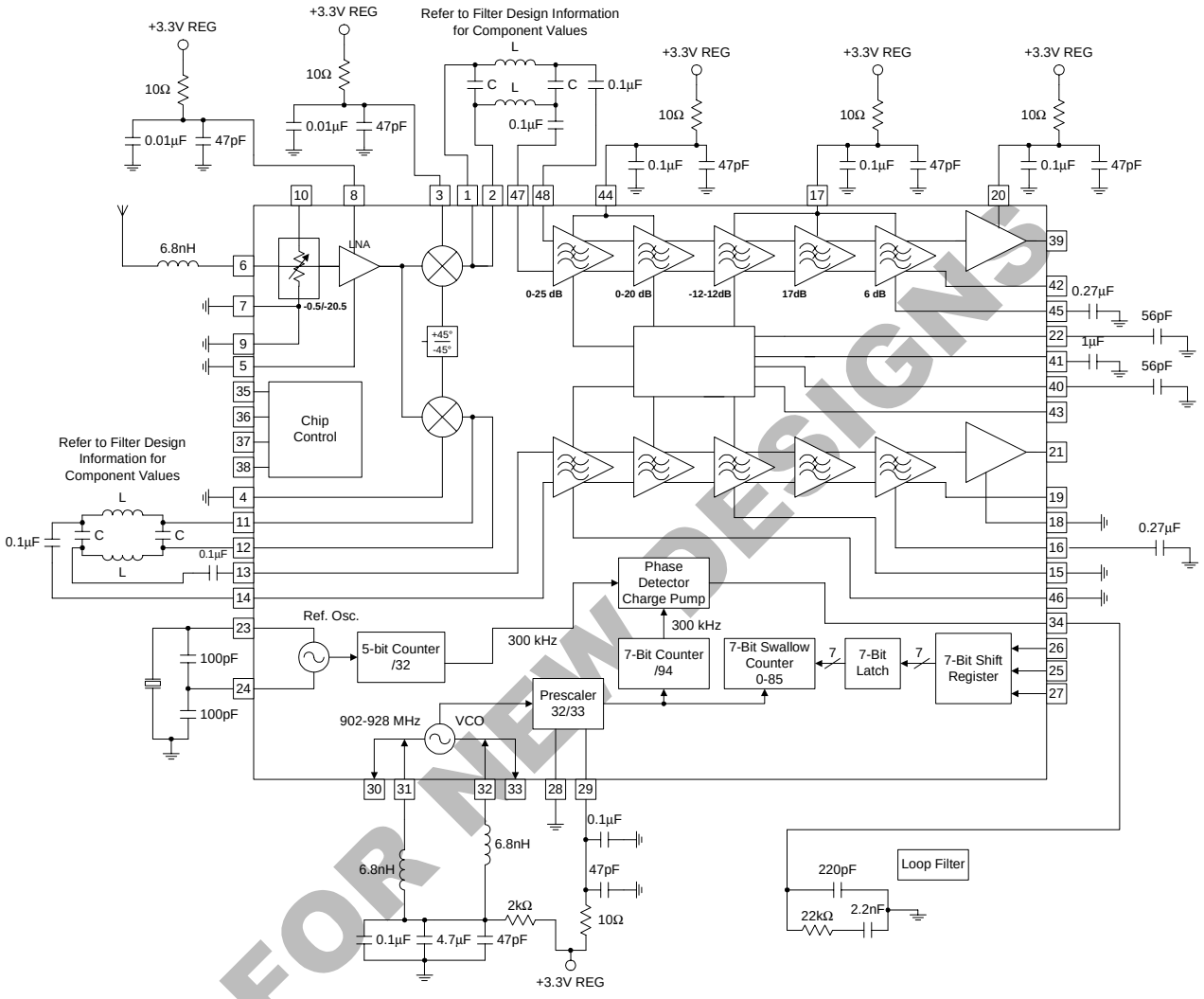
Application Schematic
915MHz



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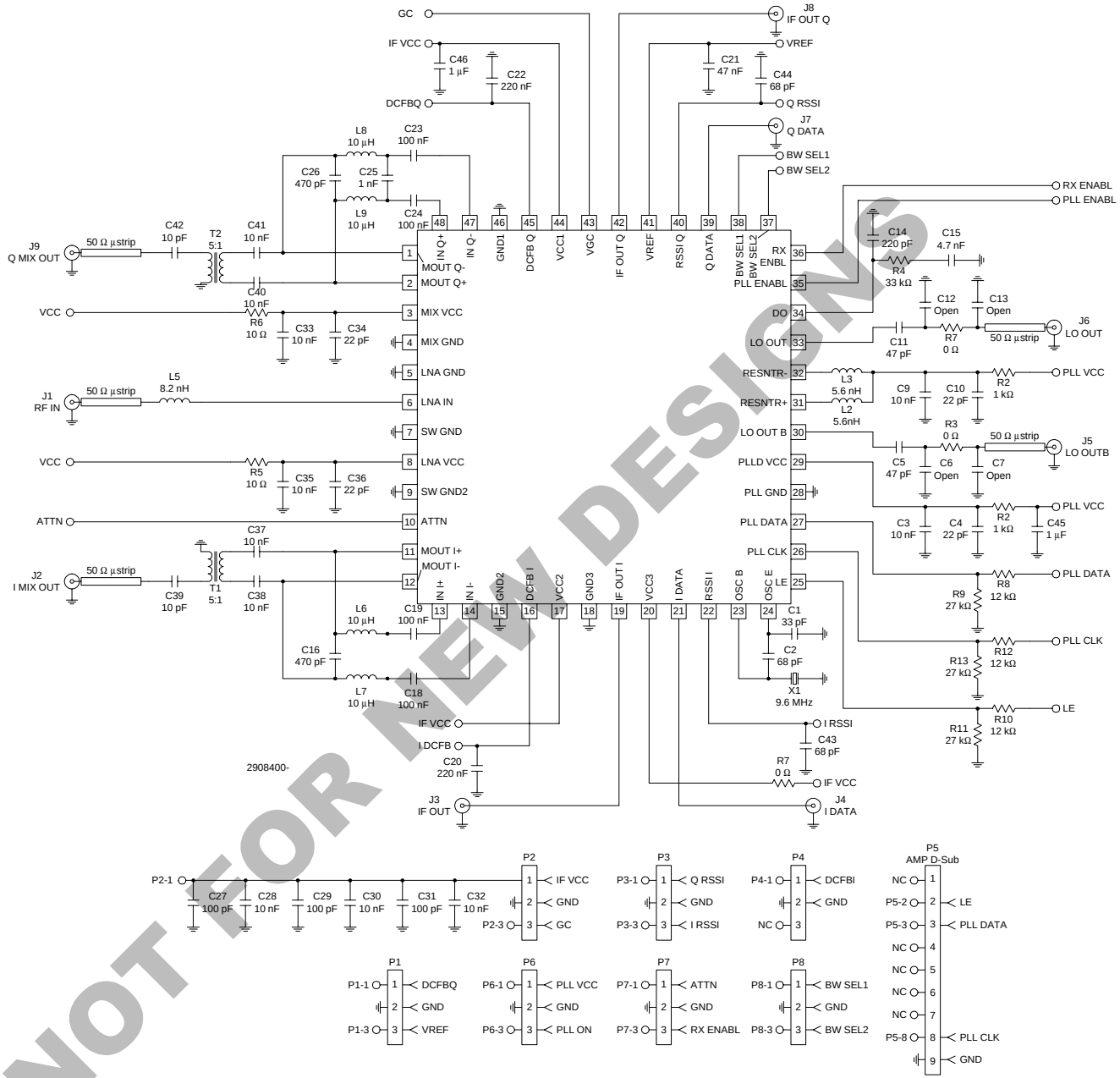
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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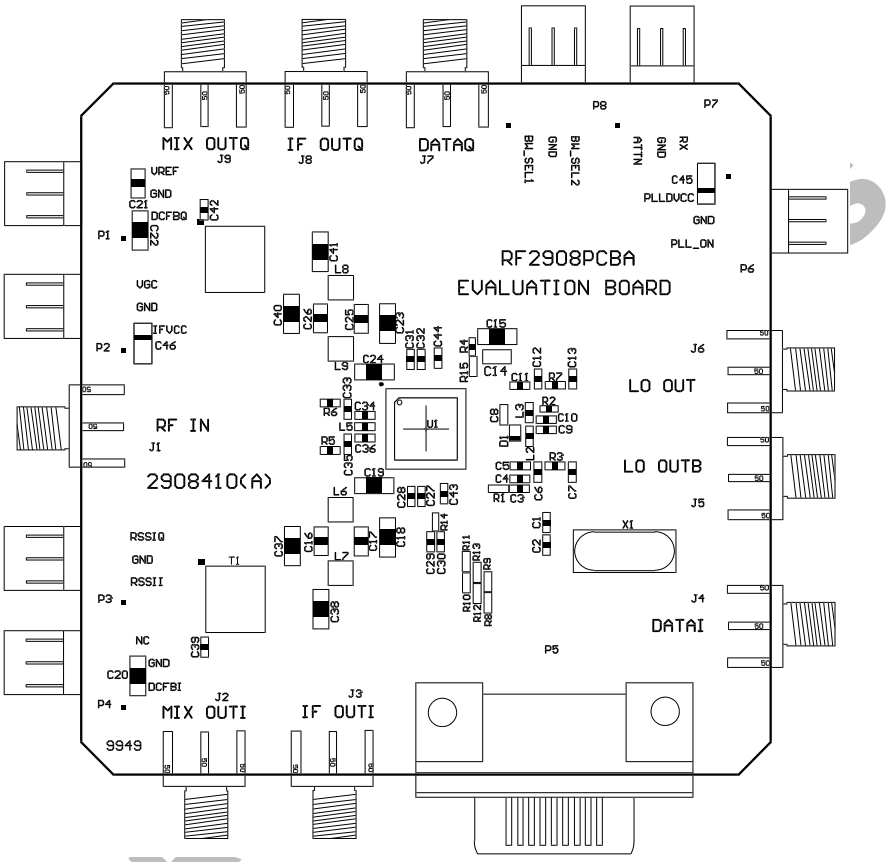
Evaluation Board Layout
Board Size 3.050” x 3.050”

Board Thickness 0.032”, Board Material FR-4, Multi-Layer Assembly



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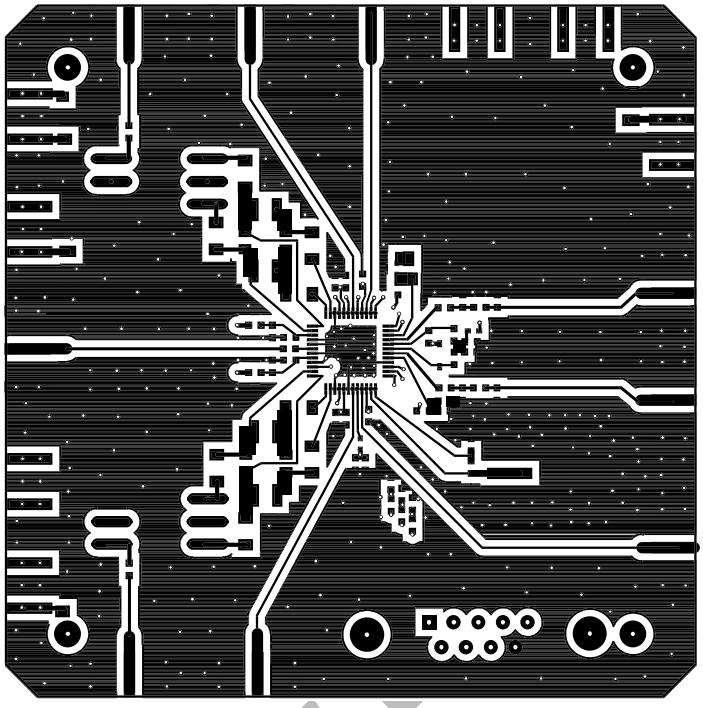
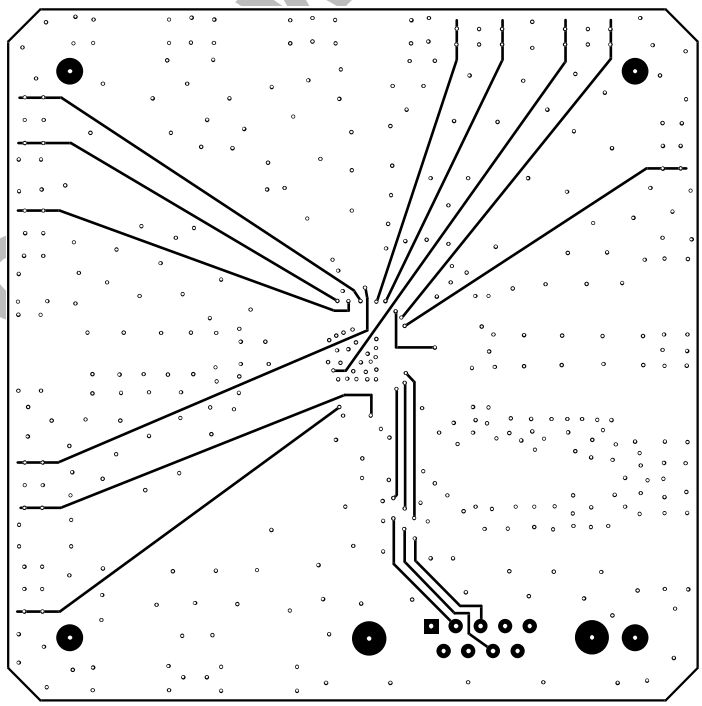
Top



Mid 1



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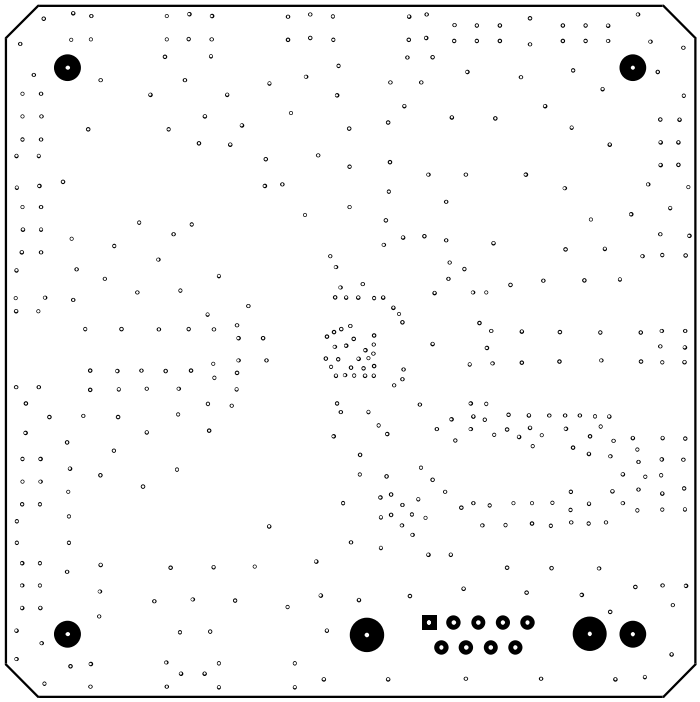
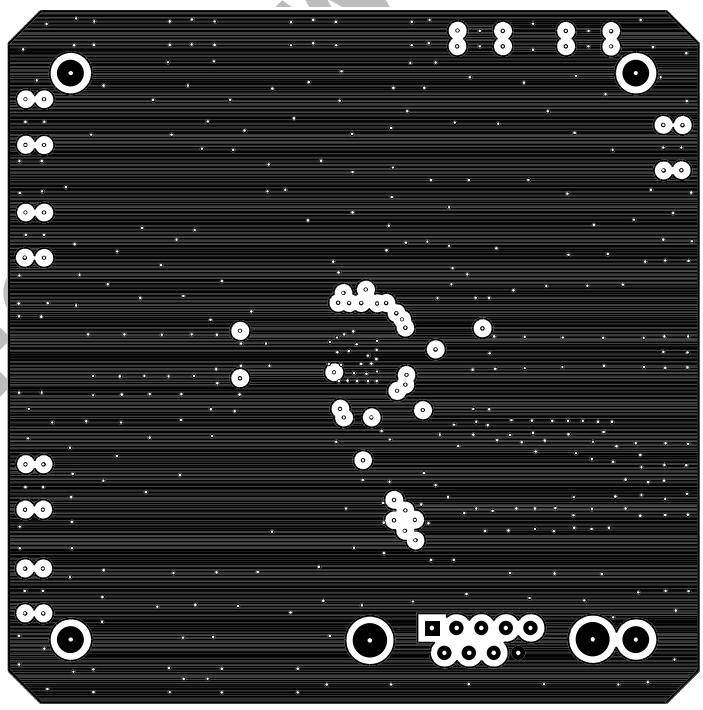
Mid 2



Back



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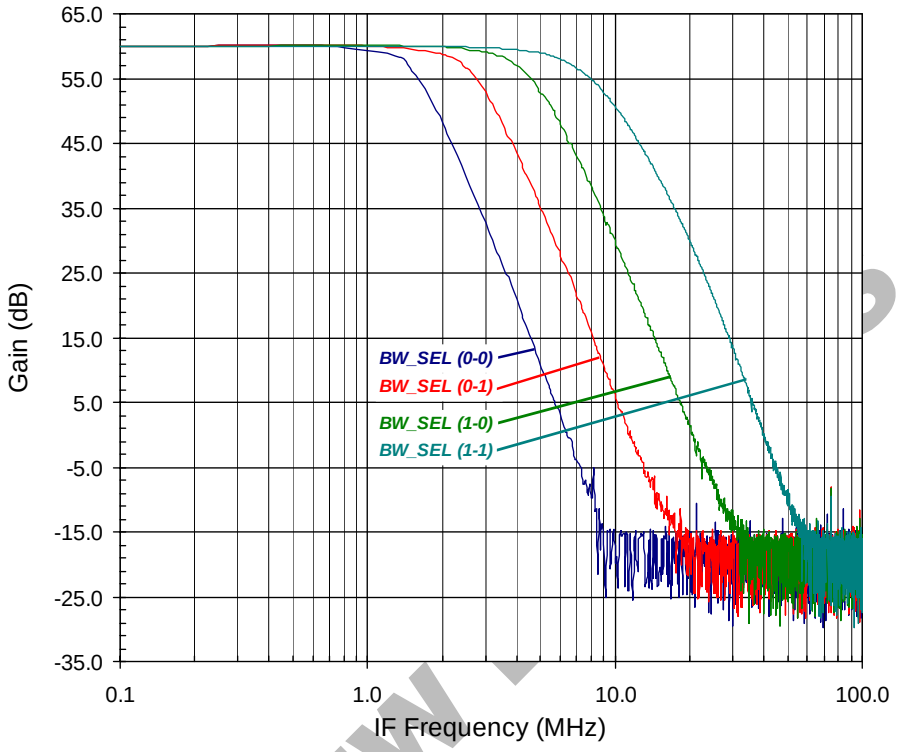
RF2908 IF Bandwidth Response



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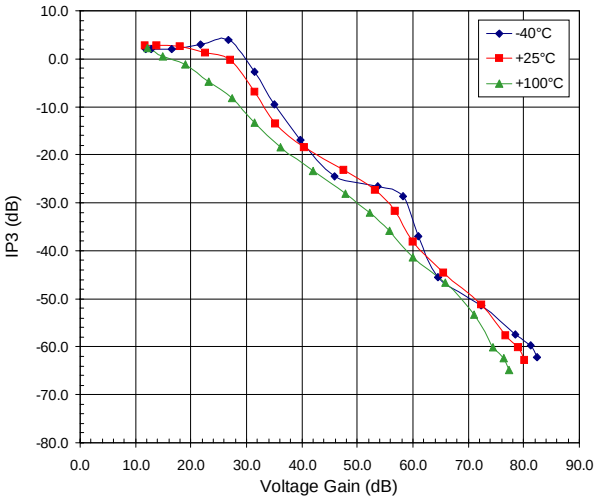
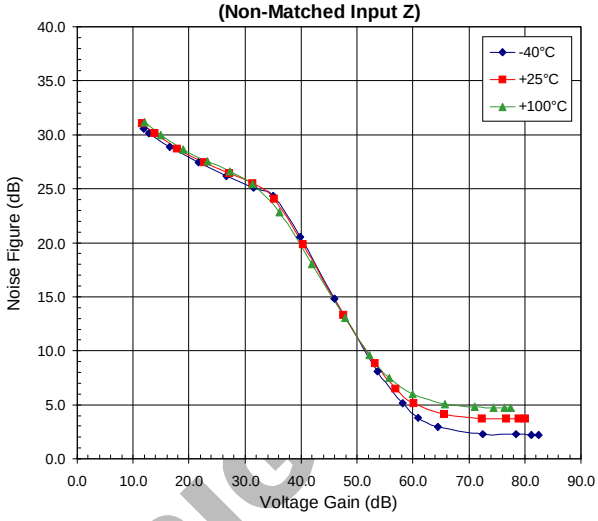
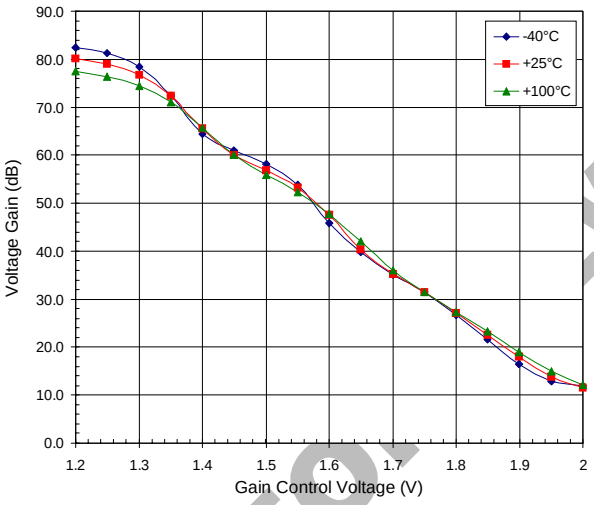
IIP3 versus Voltage Gain



Noise Figure versus Voltage Gain (Non-Matched Input Z)



Voltage Gain versus Gain Control Voltage



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