National Semiconductor

June 1999

# CLC5956
# 12-bit, 65 MSPS Broadband Monolithic A/D Converter

## General Description

The CLC5956 is a monolithic 12-bit, 65 MSPS analog-to-digital converter subsystem. The device has been optimized for use in cellular base stations and other applications where high resolution, high sampling rate, wide dynamic range, low power dissipation, and compact size are required. The CLC5956 features differential analog inputs, low jitter differential PECL clock inputs, a low distortion track-and-hold with DC to 300 MHz input bandwidth, a bandgap voltage reference, TTL compatible CMOS output logic, and a proprietary 12-bit multi-stage quantizer. The CLC5956 is fabricated on the ABIC-IV 0.8 micron BiCMOS process. The part features a 73 dB spurious free dynamic range (SFDR) and 67 dB SNR. The wideband track-and-hold allows sampling of IF signals to greater than 250 MHz. The part produces two-tone, dithered, spurious-free dynamic range of 83 dBFS at 75 MHz input frequency. The differential analog input provides excellent common-mode rejection, while the differential PECL clock inputs permit the use of balanced transmission to minimize jitter in distributed systems. The 48-pin TSSOP package provides an extremely small footprint for applications where space is a critical consideration. The CLC5956 operates from a single +5V power supply over the industrial temperature range of −40˚C to +85˚C. National thoroughly tests each part to verify full compliance with the guaranteed specifications.

## Features

- Wide dynamic range
- IF sampling capability
- 300 MHz input bandwidth
- Small 48-pin TSSOP
- Single +5V supply
- Low cost

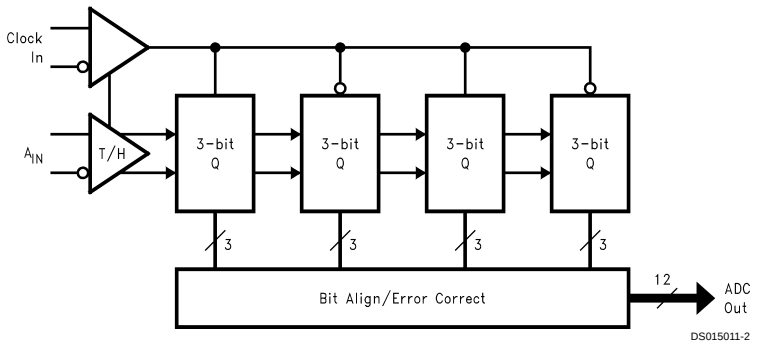
## Key Specifications

| | |
|---|---|
| Sample Rate | 65 MSPS |
| SFDR | 73 dBc |
| SFDR with dither | 85 dBFS |
| SNR | 67 dB |
| Low power consumption | 615 mW |

## Applications

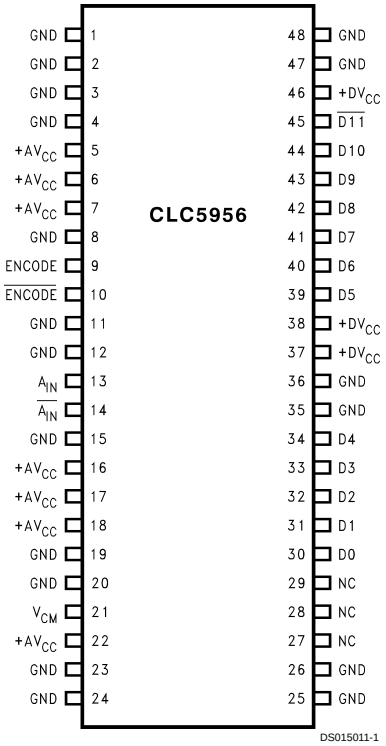
- Cellular base-stations
- Digital communications
- Infrared/CCD imaging
- IF sampling
- Electro-optics
- Instrumentation
- Medical imaging
- High definition video

## Block Diagram




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## Pin Configuration




DS015011-1

## Ordering Information

| | |
|---|---|
| CLC5956IMTD | 48-Pin TSSOP |
| CLC5956IMTDX | 48-Pin TSSOP (Taped Reel) |
| CLC5956PCASM | Evaluation Board |

## Pin Descriptions

| Pin Name | Pin No. | Description |
|---|---|---|
| $A_{IN}$ / $\overline{A_{IN}}$ | 13, 14 | Differential input with a common mode voltage of +2.4V. The ADC full scale input is 1.024 $V_{PP}$ on each of the complimentary input signals. |
| ENCODE / $\overline{\text{ENCODE}}$ | 9, 10 | Differential clock where ENCODE initiates a new data conversion cycle on each rising edge. Logic for these inputs are a 50% duty cycle differential PECL signal. |
| VCM | 21 | Internal common mode voltage reference. Nominally +2.4V. Can be used for the input common mode voltage. This voltage is derived from an internal bandgap reference. |
| D0–$\overline{\text{D11}}$ | 30–34, 39–45 | Digital data outputs are CMOS and TTL compatible. D0 is the LSB and $\overline{\text{D11}}$ is the MSB. MSB is inverted. Output coding is two's complement. |
| GND | 1–4, 8, 11, 12, 15, 19, 20, 23–26, 35, 36, 47, 48 | Circuit ground. |
| $+AV_{CC}$ | 5–7, 16–18, 22 | +5V power supply for the analog section. Bypass to ground with a 0.1 µF capacitor. |
| $+DV_{CC}$ | 37, 38, 46 | +5V power supply for the digital section. Bypass to ground with a 0.1 µF capacitor. |

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Positive Supply Voltage ($V_{CC}$) | −0.5V to +6V |
| Differential Voltage between any Two Grounds | <200 mV |
| Analog Input Voltage Range | GND to $V_{CC}$ |
| Digital Input Voltage Range | −0.5V to +$V_{CC}$ |
| Output Short Circuit Duration (one-pin to ground) | Infinite |
| Junction Temperature (Note 6) | 175˚C |
| Storage Temperature Range | −65˚C to +150˚C |
| Lead Solder Duration (+300˚C) | 10 sec. |

## Recommended Operating Conditions

| | |
|---|---|
| Positive Supply Voltage ($V_{CC}$) | +5V ±5% |
| Analog Input Voltage Range | 2.048 $V_{PP}$ diff. |
| Operating Temperature Range | −40˚C to +85˚C |

## Package Thermal Resistance (Note 6)

| Package | $\theta_{JA}$ | $\theta_{JC}$ |
|---|---|---|
| 48-Pin TSSOP | 56˚C/W | 16˚C/W |

## Reliability Information

| | |
|---|---|
| Transistor Count | 5000 |

## Converter Electrical Characteristics

The following specifications apply for $AV_{CC}$ = $DV_{CC}$ = +5V, 52 MSPS, 50% Encode Clock Duty Cycle, $C_L$ = 7 pF. **Boldface limits apply for $T_A$ = $T_{min}$ = −40˚C to $T_{max}$ = +85˚C,** all other limits $T_A$ = 25˚C (Notes 2, 3, 4).

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DYNAMIC PERFORMANCE** | | | | | | |
| BW | Large-Signal Bandwidth | $V_{IN}$ = FS −3 dB | | 300 | | MHz |
| | Overvoltage Recovery Time | $V_{IN}$ = 1.5 FS (0.01%) | | 12 | | ns |
| $t_{DS}$ | Effective Aperture Delay | | | −0.21 | | ns |
| $t_{AJ}$ | Aperture Jitter | | | 0.4 | | ps(rms) |
| **NOISE AND DISTORTION** | | | | | | |
| SNR | Signal-to-Noise Ratio (without harmonics) | $f_{IN}$ = 20 MHz, FS −1 dB | 63 | 66 | | dBFS |
| | | $f_{IN}$ = 5 MHz, FS −3 dB | | 67 | | dBFS |
| | | $f_{IN}$ = 25 MHz, FS −3 dB | | 66 | | dBFS |
| | | $f_{IN}$ = 75 MHz, FS −3 dB | | 64 | | dBFS |
| | | $f_{IN}$ = 150 MHz, FS −3 dB | | 62 | | dBFS |
| | | $f_{IN}$ = 250 MHz, FS −3 dB | | 59 | | dBFS |
| SFDR | Spurious-Free Dynamic Range | $f_{IN}$ = 20 MHz, FS −1 dB | 66 | 70 | | dBc |
| | | $f_{IN}$ = 5 MHz, FS −3 dB | | 73 | | dBc |
| | | $f_{IN}$ = 25 MHz, FS −3 dB | | 70 | | dBc |
| | | $f_{IN}$ = 75 MHz, FS −3 dB | | 68 | | dBc |
| | | $f_{IN}$ = 150 MHz, FS −3 dB | | 58 | | dBc |
| | | $f_{IN}$ = 250 MHz, FS −3 dB | | 55 | | dBc |
| | Spurious-Free Dynamic Range (dithered) | $f_{IN}$ = 19 MHz, FS −6 dB | | 85 | | dBFS |
| IMD | Intermodulation Distortion | $f_1$ = 149.84 MHz, $f_2$ = 149.7 MHz, FS −10 dB | | 68 | | dBFS |
| | | $f_1$ = 249.86 MHz, $f_2$ = 249.69 MHz, FS −10 dB | | 58 | | dBFS |
| | Intermodulation Distortion (dithered) | $f_1$ = 74 MHz, $f_2$ = 75 MHz, FS −12 dB | | 83 | | dBFS |
| **DC ACCURACY AND PERFORMANCE** | | | | | | |
| DNL | Differential Non-Linearity | DC; Full Scale | | 0.65 | | LSB |
| INL | Integral Non-Linearity | DC; Full Scale | | 1.7 | | LSB |
| | Bipolar Offset Error | | | −1 | | mV |
| | Bipolar Gain Error | | | −0.1 | | % FS |
| **ANALOG INPUTS** | | | | | | |
| $V_{IN}$ | Analog Diff Input Voltage Range | | | 2.048 | | $V_{PP}$ |
| $R_{IN}$ (SE) | Analog Input Resistance (Single-Ended) | | | 500 | | Ω |

## Converter Electrical Characteristics (Continued)

The following specifications apply for $AV_{CC}$ = $DV_{CC}$ = +5V, 52 MSPS, 50% Encode Clock Duty Cycle, $C_L$ = 7 pF. **Boldface limits apply for $T_A$ = $T_{min}$ = −40˚C to $T_{max}$ = +85˚C,** all other limits $T_A$ = 25˚C (Notes 2, 3, 4).

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **ANALOG INPUTS** | | | | | | |
| $R_{IN}$ (Diff) | Analog Input Resistance (Differential) | | | 1000 | | Ω |
| $C_{IN}$ | Analog Input Capacitance | | | 2 | | pF |
| **ENCODE INPUTS** | | | | | | |
| $V_{IL}$ | Logic Input Low Voltage | | **3.0** | | **3.5** | V |
| $V_{IH}$ | Logic Input High Voltage | | **4.0** | | **4.5** | V |
| $I_{IL}$ | Logic Input Low Current | | | 1 | **5** | µA |
| $I_{IH}$ | Logic Input High Current | | | 16 | **25** | µA |
| **DIGITAL OUTPUTS** | | | | | | |
| $V_{OL}$ | Logic Output Low Voltage | | | | **0.4** | V |
| $V_{OH}$ | Logic Output High Voltage | | **2.4** | | | V |
| **TIMING** | | | | | | |
| $F_s$max | Maximum Conversion Rate | | | 65 | | MSPS |
| $F_s$min | Minimum Conversion Rate | | | 10 | | MSPS |
| PWH | Pulse Width High | | | 7.7 | | ns |
| PWL | Pulse Width Low | | | 7.7 | | ns |
| | Pipeline Delay (Note 5) | | | | **3.0** | CLK Cy |
| | Output Propagation Delay | | | 1.6 | | ns |
| **POWER REQUIREMENTS** | | | | | | |
| $I_{CC}$ | Total Operating Supply Current | 65 MSPS | | 123 | 150 | mA |
| | Power Consumption | 65 MSPS | | 615 | 750 | mW |
| | Power Supply Rejection Ratio | | | 64 | | dB |

**Note 1:** "Absolute Maximum Ratings" are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

**Note 2:** Limits are 100% tested at 25˚C.

**Note 3:** Typical characteristics are the mean values of the distributions of deliverable converters at 25˚C.

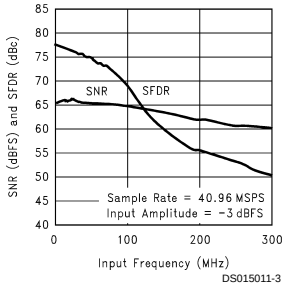
**Note 4:** Outgoing quality levels are determined from tested parameters.

**Note 5:** Max pipeline delay rating is based upon product characterization and simulation.

**Note 6:** The absolute maximum junction ($T_J$max) temperature for this device is 175˚C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($\theta_{JA}$), and the ambient temperature ($T_A$), and can be calculated using the formula $P_D$max = ($T_J$max – $T_A$)/$\theta_{JA}$. For the 48-pin TSSOP, $\theta_{JA}$ is 56˚C/W, so $P_D$max = 2.68W at 25˚C and 1.6W at the maximum operating ambient temperature of 85˚C. Note that the power dissipation of this device under normal operation will typically be about 625 mW (615 mW quiescent power + 10 mW due to 1 TTL load on each digital output). The values of absolute maximum power dissipation will only be reached when the CLC5956 is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

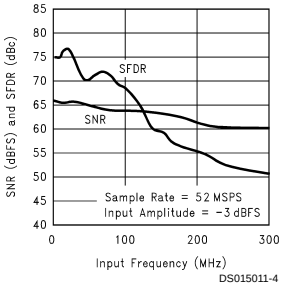
## Typical Performance Characteristics ($AV_{CC}$ = $DV_{CC}$ = +5V)

**SNR and SFDR vs Input Frequency**



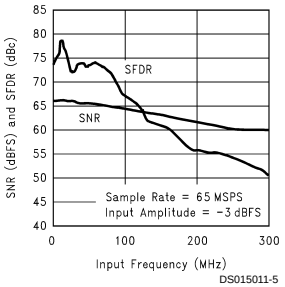
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**SNR and SFDR vs Input Frequency**



DS015011-4

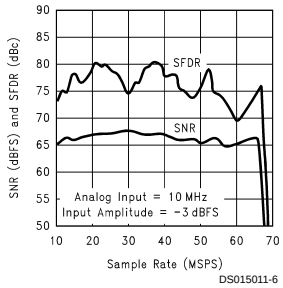
**SNR and SFDR vs Input Frequency**



DS015011-5

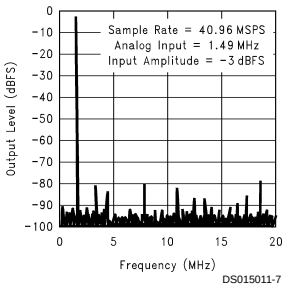
## Typical Performance Characteristics ($AV_{CC}$ = $DV_{CC}$ = +5V) (Continued)

**SNR and SFDR vs Sample Rate**



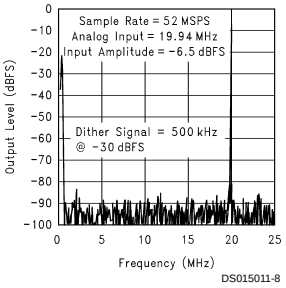

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**Single Tone Output Spectrum**



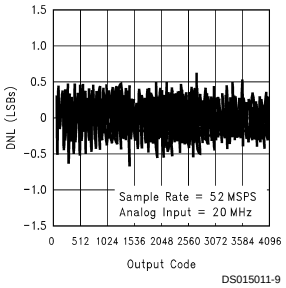

DS015011-7

**Single Tone Output Spectrum (with Dither)**



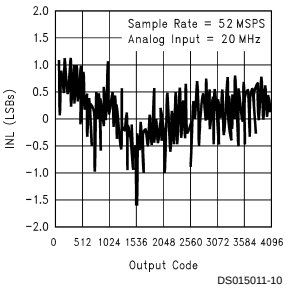

DS015011-8

**Differential Non-Linearity**



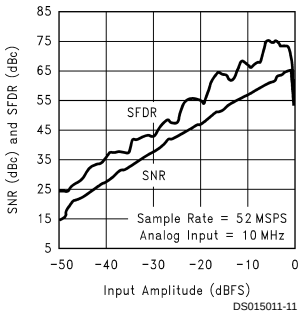

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**Integral Non-Linearity**



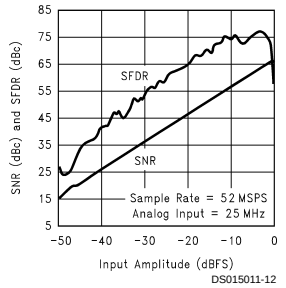

DS015011-10

**SNR and SFDR vs Input Amplitude**



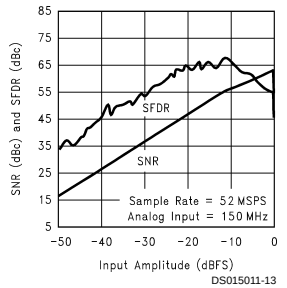

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**SNR and SFDR vs Input Amplitude**



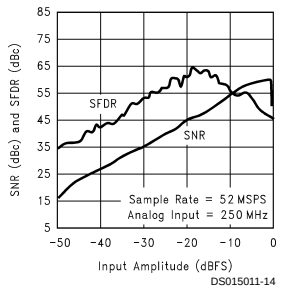

DS015011-12

**SNR and SFDR vs Input Amplitude**



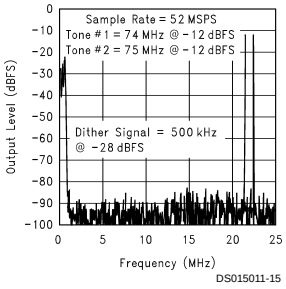

DS015011-13

**SNR and SFDR vs Input Amplitude**



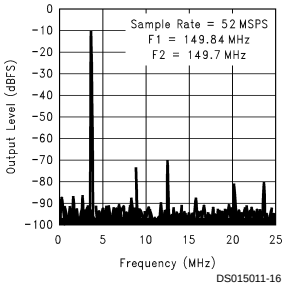

DS015011-14

**Two Tone Output Spectrum (with Dither)**



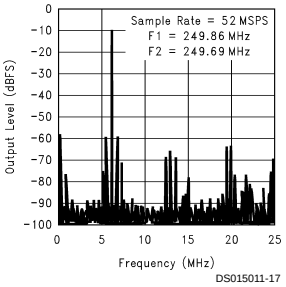

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**Two Tone Output Spectrum**




DS015011-16

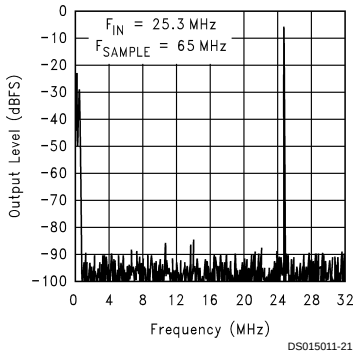
**Two Tone Output Spectrum**




DS015011-17

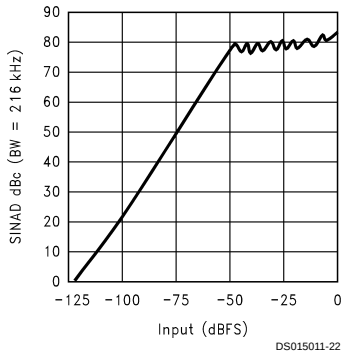
## Typical Performance Characteristics ($AV_{CC}$ = $DV_{CC}$ = +5V) (Continued)

**Spectral Response**



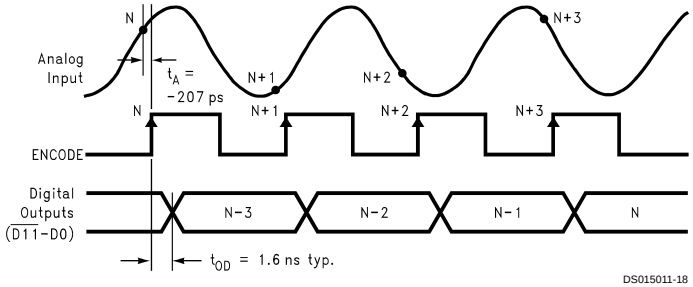

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**SINAD vs Input Level**



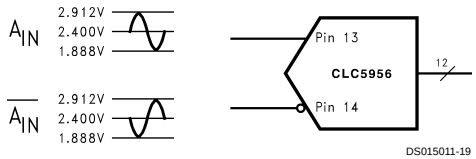

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## Timing Diagram



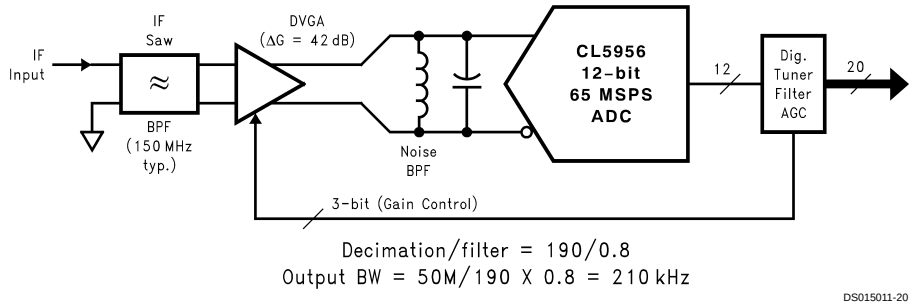

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## Full Scale Analog Input Levels



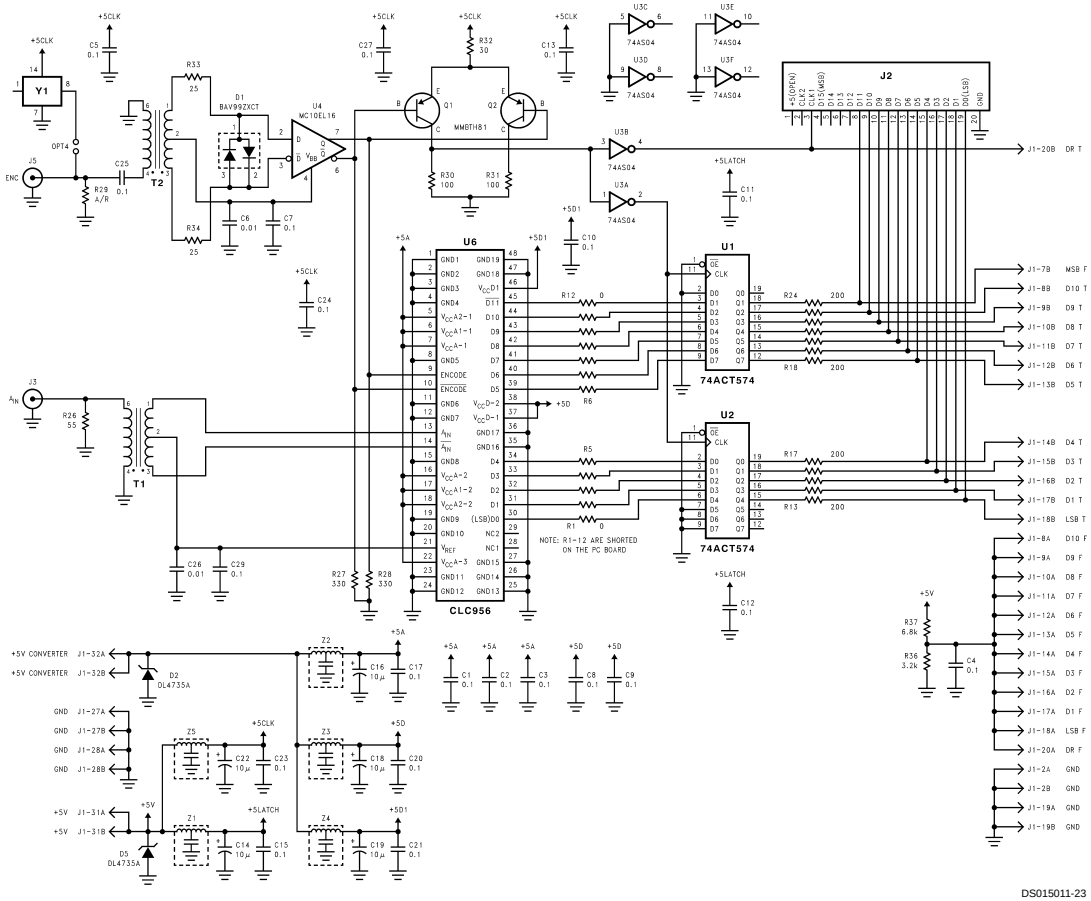

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## Single IF Down Converter



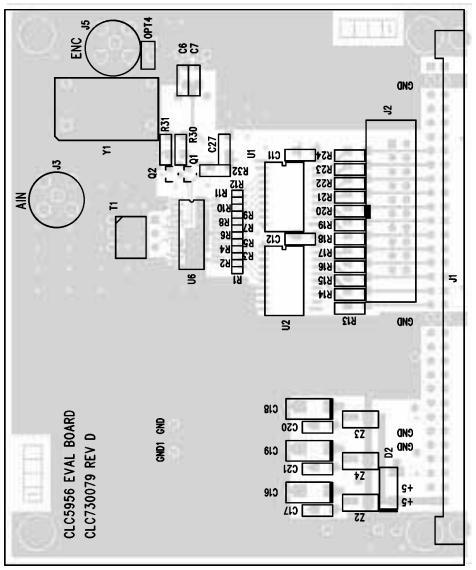

DS015011-20

## Evaluation Board



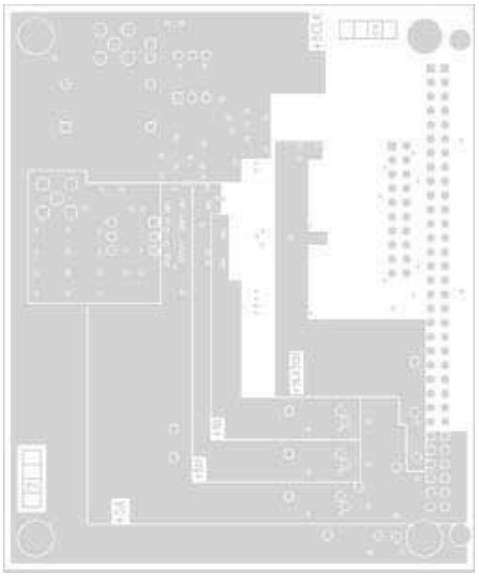

**Evaluation Board Schematic**

## Evaluation Board (Continued)



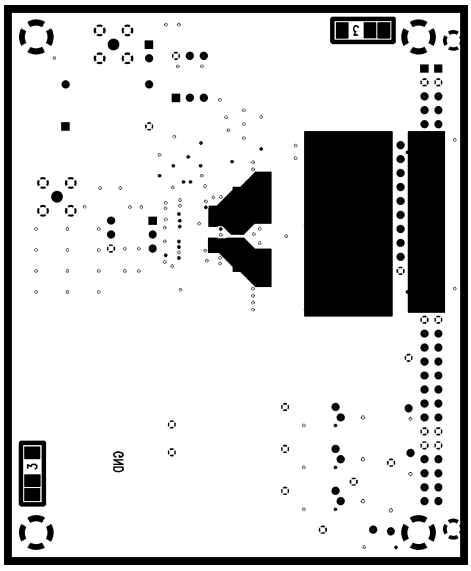

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**CLC730079 Layer 1**



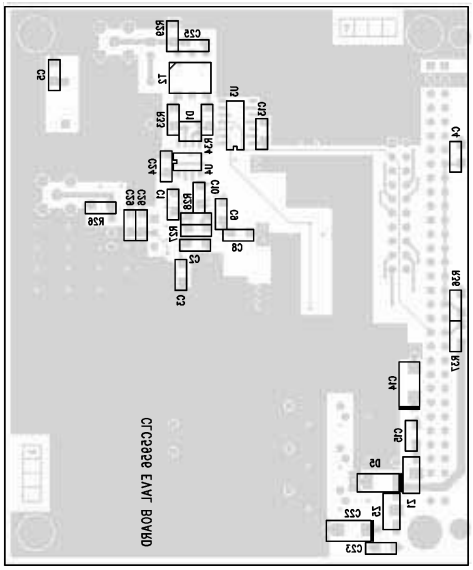
DS015011-26

**CLC730079 Layer 2**




DS015011-25

**CLC730079 Layer 3**




DS015011-27

**CLC730079 Layer 4**

## Evaluation Printed Circuit Board

The Evaluation board for the CLC5956 allows for easy test and evaluation of the product. The part may be ordered with all components loaded and tested. The order number is the CLC5956PCASM. The user supplies an analog input signal, encode signal and power to the board and is able to take latched 12-bit digital data out of the board.

## ENCODE Input (ENC)

The ENCODE input is an SMA connector with a 50Ω termination. The signal is converted from single to differential and its **frequency is divided by four** to produce a low jitter, symmetrical encode signal for the CLC5956. The user should provide a sinusoidal or square wave signal of 10 dBm to 16 dBm amplitude at **four times the converter's desired sample rate**. It is recommended that the source be low jitter to maintain best performance. The transformer will pass signals in the 40 MHz to 260 MHz range which allows sample rates of 10 Msps to 65 Msps.

## Clock Option

The CLC5956 board is configured for a 4x clock input to provide optimal performance with some (i.e., HP8662) synthesizers. The HP8662 output has lower jitter above 160 MHz. Using a 208 MHz clock to sample at 52 MHz minimizes the effect of the synthesizer on the measurement.

To use a 1x clock, replace the divide-by-4 sine-to-PECL converter (U4, MC10EL33D) with an MC10EL16D. The MC10EL16D sine-to-PECL converter does not divide the clock. This approach would be suitable for use with a synthesizer that has optimal jitter performance at 52 MHz (i.e., HP8643 or HP8644).

The best ADC performance is obtained with a low-jitter crystal oscillator module installed at Y1 on the evaluation board. U4 should be replaced with an MC10EL16D. Placing the clock source on the evaluation board reduces ground loop issues and thus improves performance.

## Analog Input (AIN)

The analog input is an SMA connector with a 50Ω termination. The signal is converted from single to differential by a transformer with a 5 MHz to 260 MHz bandwidth and approximately one dB loss. Full scale is approximately 11 dBm or 2.2 $V_{PP}$. It is recommended that the source for the analog input signal be low jitter, low noise and low distortion to allow for proper test and evaluation of the CLC5956.

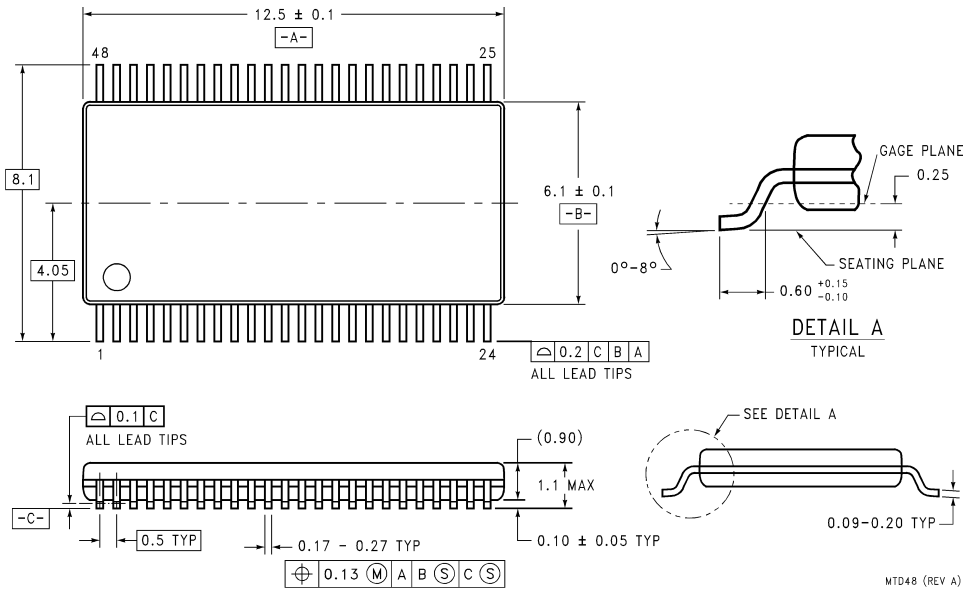
## Supply Voltages (J1 pins 31 A&B and 32 A&B)

The CLC5956PCASM is powered from a single 5V supply connected from the referenced pins on the Eurocard connector. The recommended supplies are low noise linear supplies.

## Digital Outputs (J1 pins 7A ($\overline{\text{MSB}}$, $\overline{\text{D11}}$), 8B (D10) through 18B (LSB) and 20B (Data Ready)

The digital outputs are provided on the Eurocard connector. The outputs are buffered by 5V CMOS latches with 50Ω series output resistors. The rising edge of Data Ready may be used to clock the output data into data collection cards or logic analyzers. The board has a location for the HP 01650-63203 termination adapter for HP 16500 logic analyzers to simplify connection to the analyzer.

## Physical Dimensions inches (millimeters) unless otherwise noted




**48-Lead TSSOP (Millimeters Only)**
**Order Number CLC5956IMTD**
**NS Package Number MTD48**

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