- **3:21 Data Channel Expansion at up to 163 Million Bytes per Second Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **3 Data Channels and Clock Low-Voltage Differential Channels In and 21 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply and 250 mW (Typ)**
- **5-V Tolerant $\overline{\text{SHTDN}}$ Input**
- **ESD Protection Exceeds 4 kV on Bus Pins**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Open-Circuit Receiver Fail-Safe Design**
- **Inputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the DS90C562**

DGG PACKAGE
(TOP VIEW)

D17	1	48	V_{CC}
D18	2	47	D16
GND	3	46	D15
D19	4	45	D14
D20	5	44	GND
NC	6	43	D13
LVDSGND	7	42	V_{CC}
A0M	8	41	D12
A0P	9	40	D11
A1M	10	39	D10
A1P	11	38	GND
$LVDSV_{CC}$	12	37	D9
LVDSGND	13	36	V_{CC}
A2M	14	35	D8
A2P	15	34	D7
CLKINM	16	33	D6
CLKINP	17	32	GND
LVDSGND	18	31	D5
PLLGND	19	30	D4
$PLLV_{CC}$	20	29	D3
PLLGND	21	28	V_{CC}
$\overline{\text{SHTDN}}$	22	27	D2
CLKOUT	23	26	D1
D0	24	25	GND

NC – Not Connected

description

The SN75LVDS86 FlatLink receiver contains three serial-in 7-bit parallel-out shift registers, a 7× clock synthesizer, and four low-voltage differential signaling (LVDS) line receivers in a single integrated circuit. These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, ’83, ’84, or ’85, over four balanced-pair conductors and expansion to 21 bits of single-ended low-voltage TTL (LVTTL) synchronous data at a lower transfer rate.

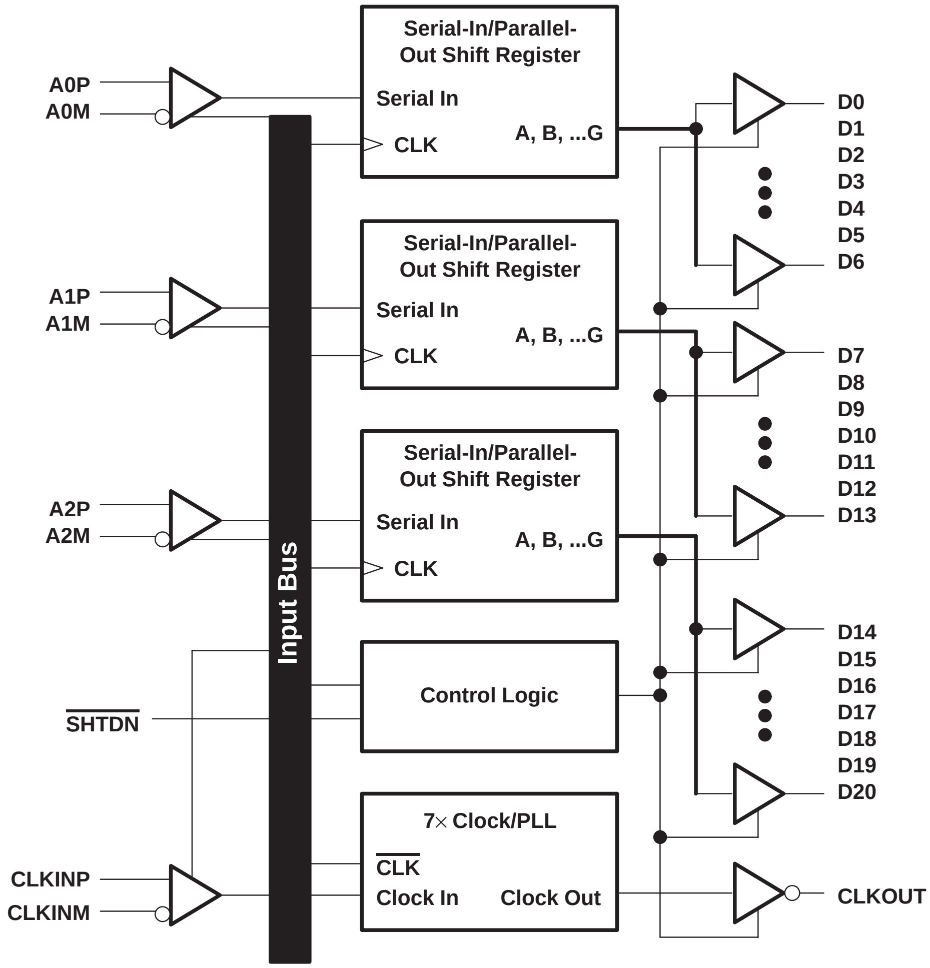
When receiving, the high-speed LVDS data is received and loaded into registers at seven times the LVDS input clock (CLKIN) rate. The data is then unloaded to a 21-bit wide LVTTL parallel bus at the CLKIN rate. A phase-locked loop clock synthesizer circuit generates a 7× clock for internal clocking and an output clock for the expanded data. The SN75LVDS86 presents valid data on the falling edge of the output clock (CLKOUT).

The SN75LVDS86 requires only four line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user(s). The only possible user intervention is the use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

The LVDS receivers of the SN75LVDS86 include an open-circuit fail-safe design such that when the inputs are not connected to an LVDS driver, the receiver outputs go to a low-level. This occurs even when the line is differentially terminated at the receiver inputs.

The SN75LVDS86 is characterized for operation over ambient free-air temperatures of 0°C to 70°C.

functional block diagram



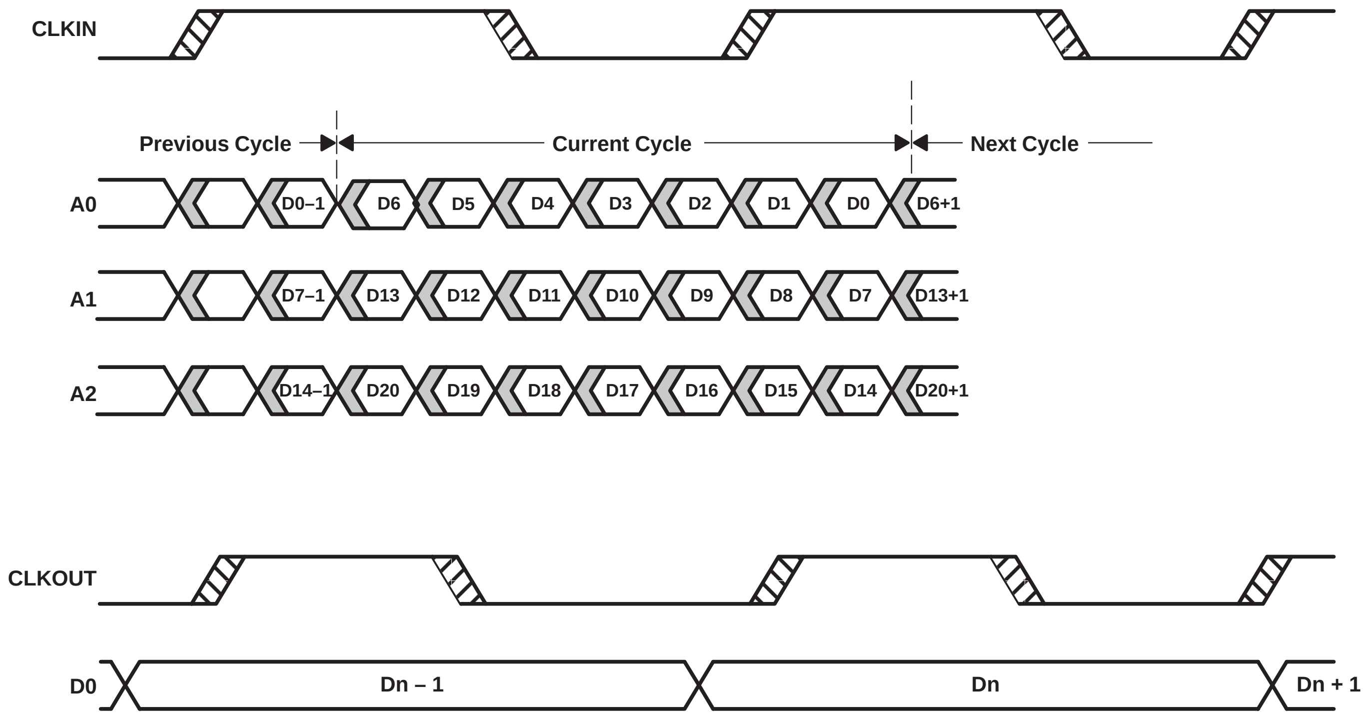
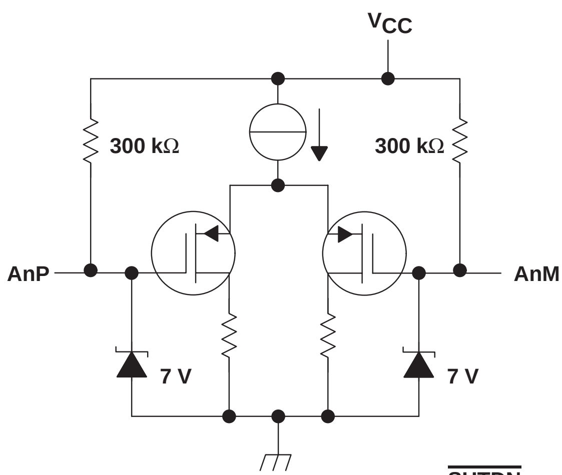
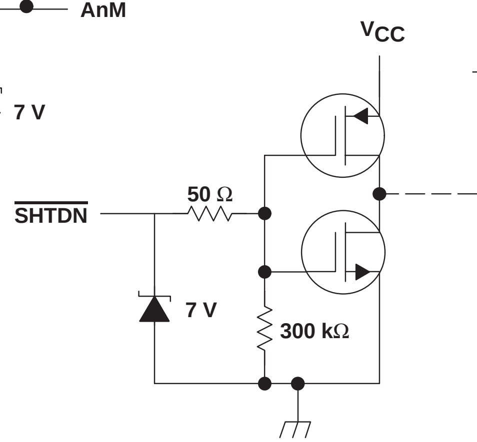


Figure 1. SN75LVDS86 Load and Shift Timing Sequences

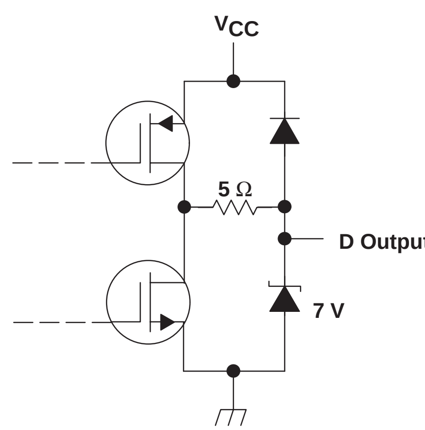
equivalent input and output schematic diagrams



INPUT



INPUT



OUTPUT

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 4 V
Output voltage range, V_O (Dxx terminals) . . . . –0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (any terminal except $\overline{\text{SHTDN}}$) . . . . –0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I ($\overline{\text{SHTDN}}$) . . . . –0.5 V to 5.5 V
Continuous total power dissipation . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING
DGG	1316 mW	13.1 mW/°C	726 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

recommended operating conditions (see Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH} ($\overline{\text{SHTDN}}$)	2			V
Low-level input voltage, V_{IL} ($\overline{\text{SHTDN}}$)			0.8	V
Differential input voltage, $\lvert V_{ID}\rvert$	0.1		0.6	V
Common-mode input voltage, V_{IC} (see Figure 2 and Figure 3)	$\frac{\lvert V_{ID}\rvert}{2}$		$2.4 - \frac{\lvert V_{ID}\rvert}{2}$	V
			V_{CC} – 0.8	
Operating free-air temperature, T_A	0		70	°C

timing requirements

		MIN	NOM	MAX	UNIT
t_c	Cycle time, input clock§	14.7	t_c	32.4	ns
t_{su1}	Setup time, input (see Figure 7)	600			ps
t_{h1}	Hold time, input (see Figure 7)	600			ps

§ Parameter t_c is defined as the mean duration of a minimum of 32 000 clock cycles.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage					100	mV
V_{IT-}	Negative-going differential input threshold voltage‡			–100			mV
V_{OH}	High-level output voltage	I_{OH} = –4 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA				0.4	V
I_{CC}	Quiescent current (average)	Disabled,	All inputs open			280	μA
		Enabled, AnM = 1.4 V,	AnP = 1 V, t_c = 15.38 ns		58	72	mA
		Enabled, C_L = 8 pF, Grayscale pattern (see Figure 4), t_c = 15.38 ns			69		mA
		Enabled, C_L = 8 pF, Worst-case pattern (see Figure 5) t_c = 15.38 ns			94		mA
I_{IH}	High-level input current ($\overline{SHTDN}$)	$V_{IH} = V_{CC}$				±20	μA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	V_{IL} = 0				±20	μA
I_I	Input current (LVDS input terminals A and CLKIN)	$0 \le V_I \le 2.4$ V				±20	μA
I_{OZ}	High-impedance output current	V_O = 0 or V_{CC}				±10	μA

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{su2}	Set up time, D0 – D20 valid to CLKOUT↓	C_L = 8 pF, See Figure 6	5			ns
t_{h2}	Hold time, CLKOUT↓ to D0 – D20 valid		5			ns
t_{RSKM}	Receiver input skew margin§ (see Figure 7)	t_c = 15.38 ns (±0.2%), |Input clock jitter| < 50 ps¶,	490			ps
t_d	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	t_c = 15.38 ns (±0.2%), C_L = 8 pF		3.7		ns
$\Delta t_{c(o)}$	Cycle time, change in output clock period#	$t_c = 15.38 + 0.75 \sin(2\pi 500E3t) \pm 0.05$ ns, See Figure 8		±80		ps
		$t_c = 15.38 + 0.75 \sin(2\pi 3E6t) \pm 0.05$ ns, See Figure 8		±300		
t_{en}	Enable time, $\overline{SHTDN}$↑ to Dn valid	See Figure 9		1		ms
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off state	See Figure 10		400		ns
t_t	Transition time, output (10% to 90% t_r or t_f)	C_L = 8 pF		3		ns
t_w	Pulse duration, output clock			0.43 t_c		ns

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

§ The parameter $t_{(RSKM)}$ is the timing margin available to the transmitter and interconnection skews and clock jitter. It is defined by $\frac{t_c}{14} - t_{su1}/t_{h1}$
¶ |Input clock jitter| is the magnitude of the change in input clock period.
\# $\Delta t_{c(o)}$ is the change in the output clock period from one cycle to the next cycle observed over 15 000 cycles.

PARAMETER MEASUREMENT INFORMATION

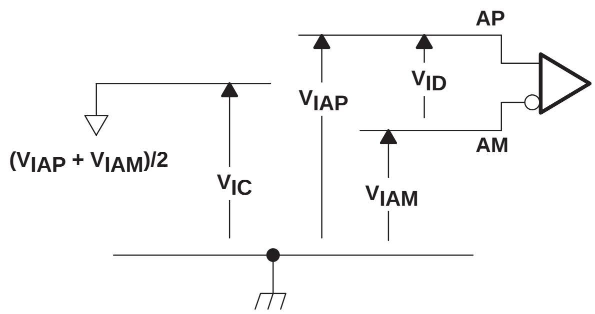


Figure 2. Voltage Definitions

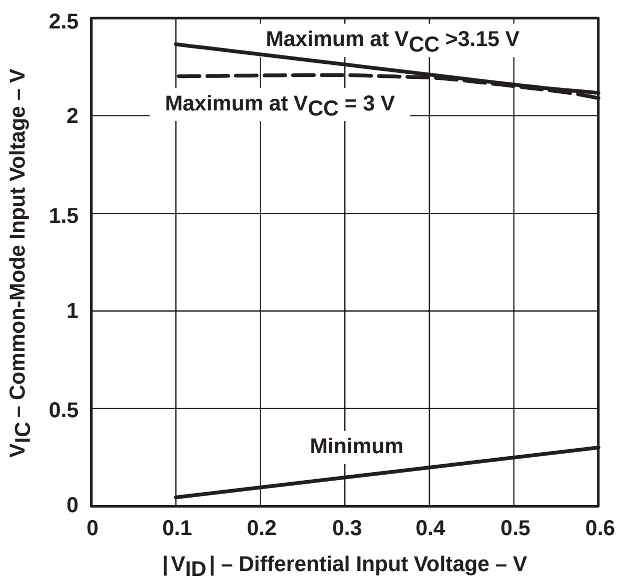
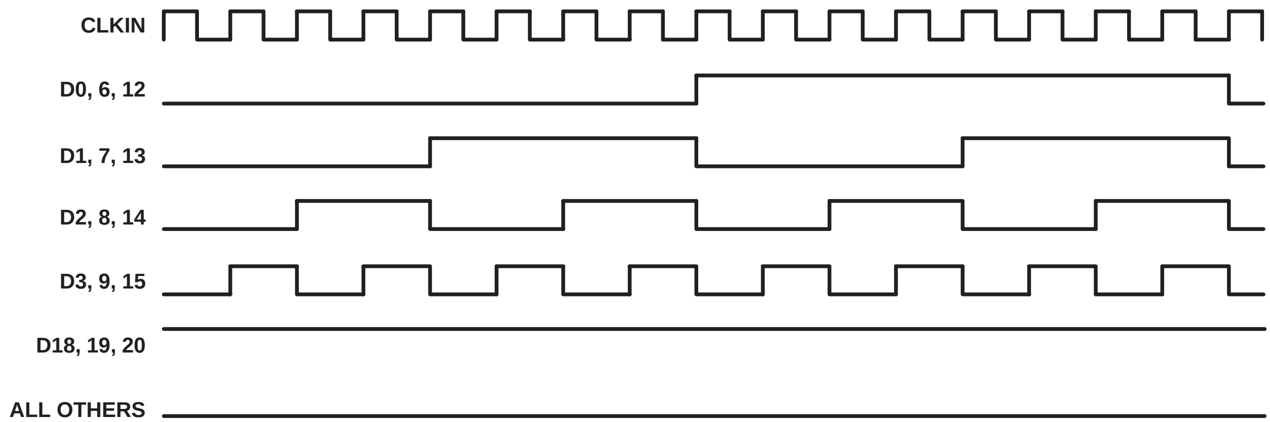


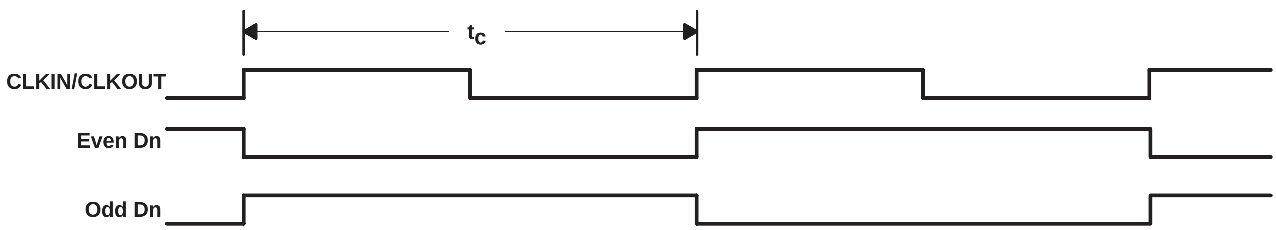
Figure 3. Maximum Common-Mode Input Voltage Vs Differential Input Voltage and V_{CC}

PARAMETER MEASUREMENT INFORMATION



NOTE A: The 16-grayscale test-pattern test device power consumption for a typical display pattern.

Figure 4. 16-Grayscale Test-Pattern Waveforms



NOTE A: The worst-case test pattern produces nearly the maximum switching frequency for all of the LVTTL outputs.

Figure 5. Worst-Case Test-Pattern Waveforms

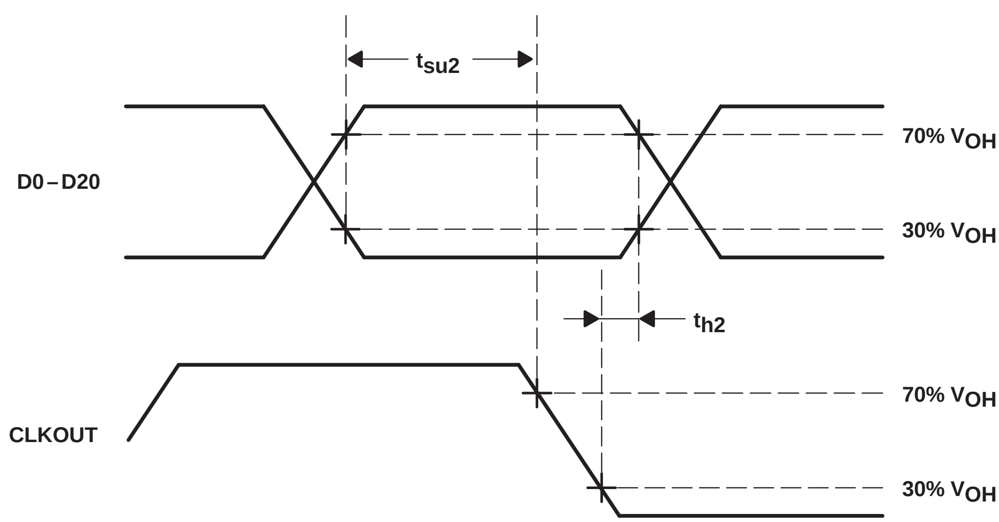
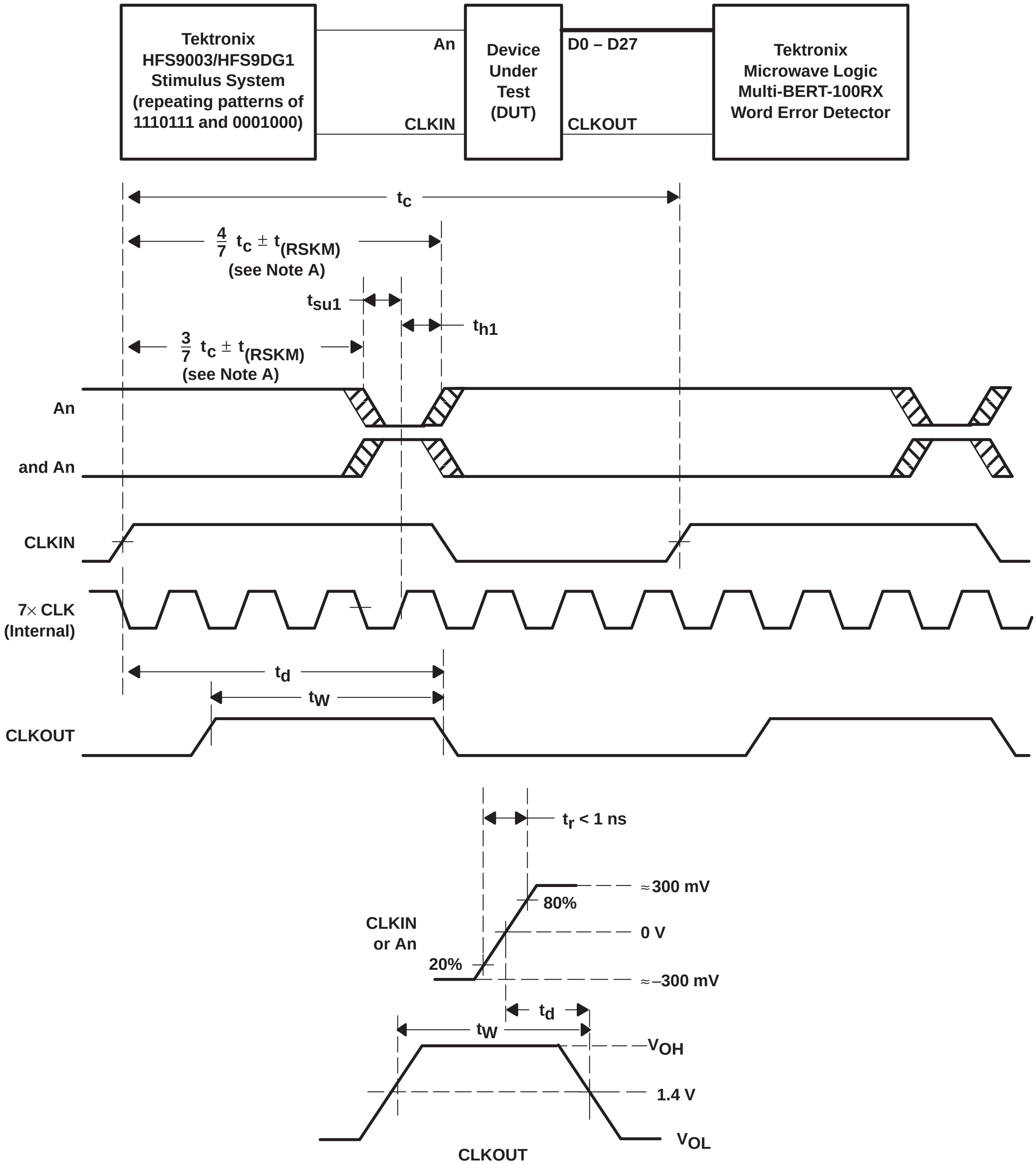


Figure 6. Setup and Hold Time Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The advance or delay is then reduced until there are no data errors observed. The magnitude of the advance or delay is $t_{(RSKM)}$.

Figure 7. Receiver Input Skew Margin, Setup/Hold Time, and Delay Time Definitions

PARAMETER MEASUREMENT INFORMATION

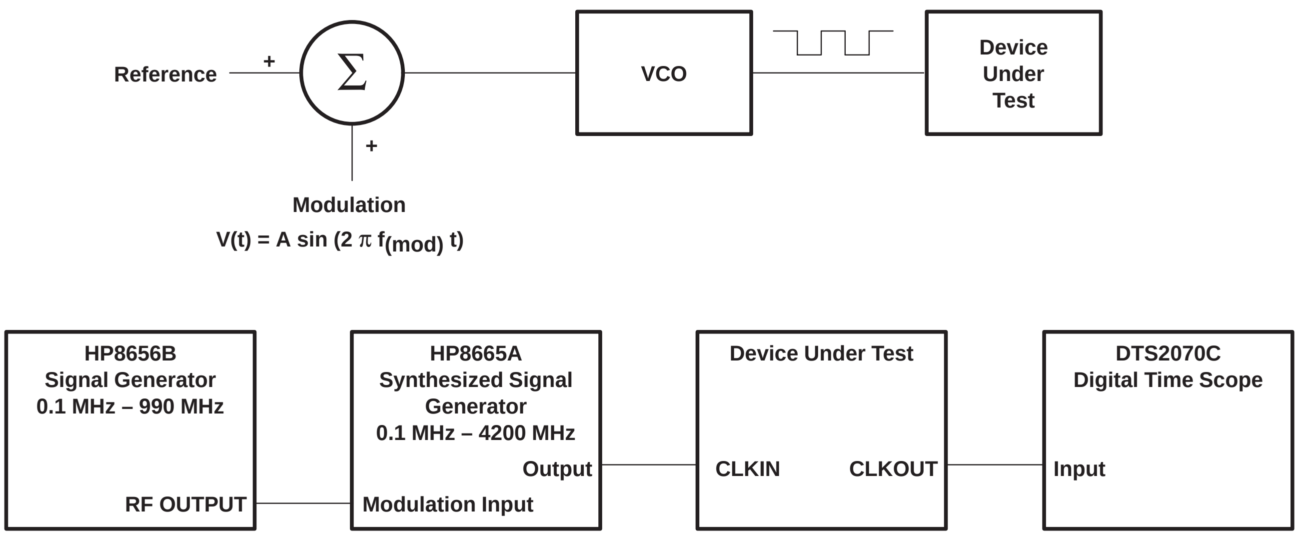


Figure 8. Output Clock Jitter Test Setup

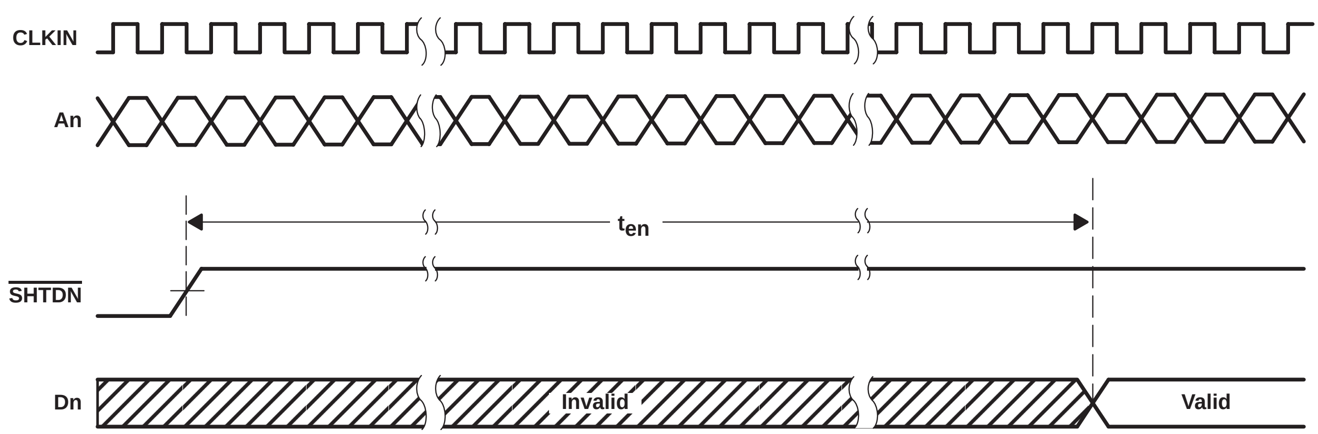


Figure 9. Enable Time Waveforms

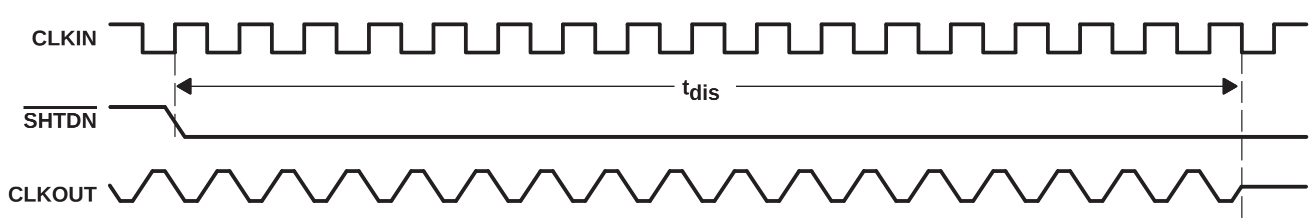


Figure 10. Disable Time Waveforms

TYPICAL CHARACTERISTICS

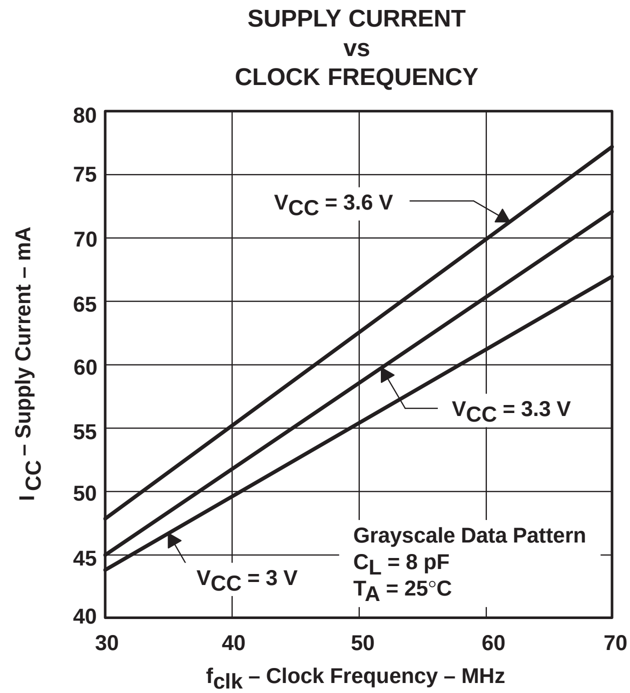


Figure 11. RMS Grayscale I_{CC} vs Clock Frequency

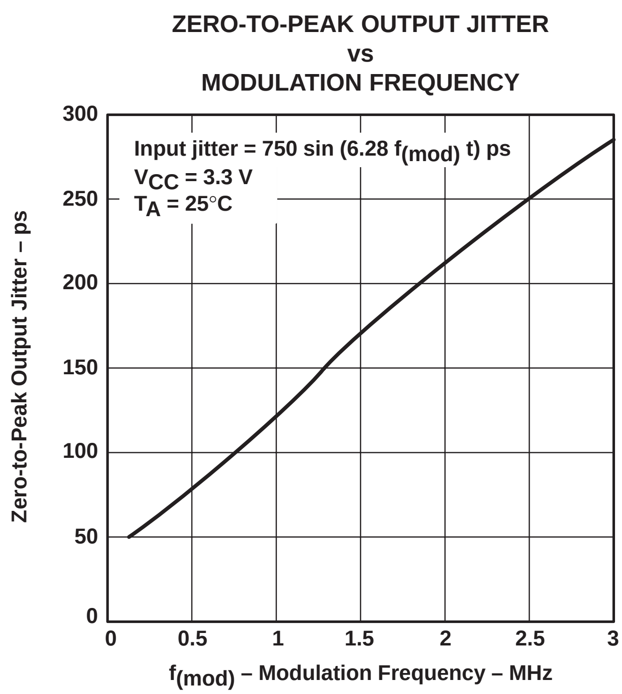
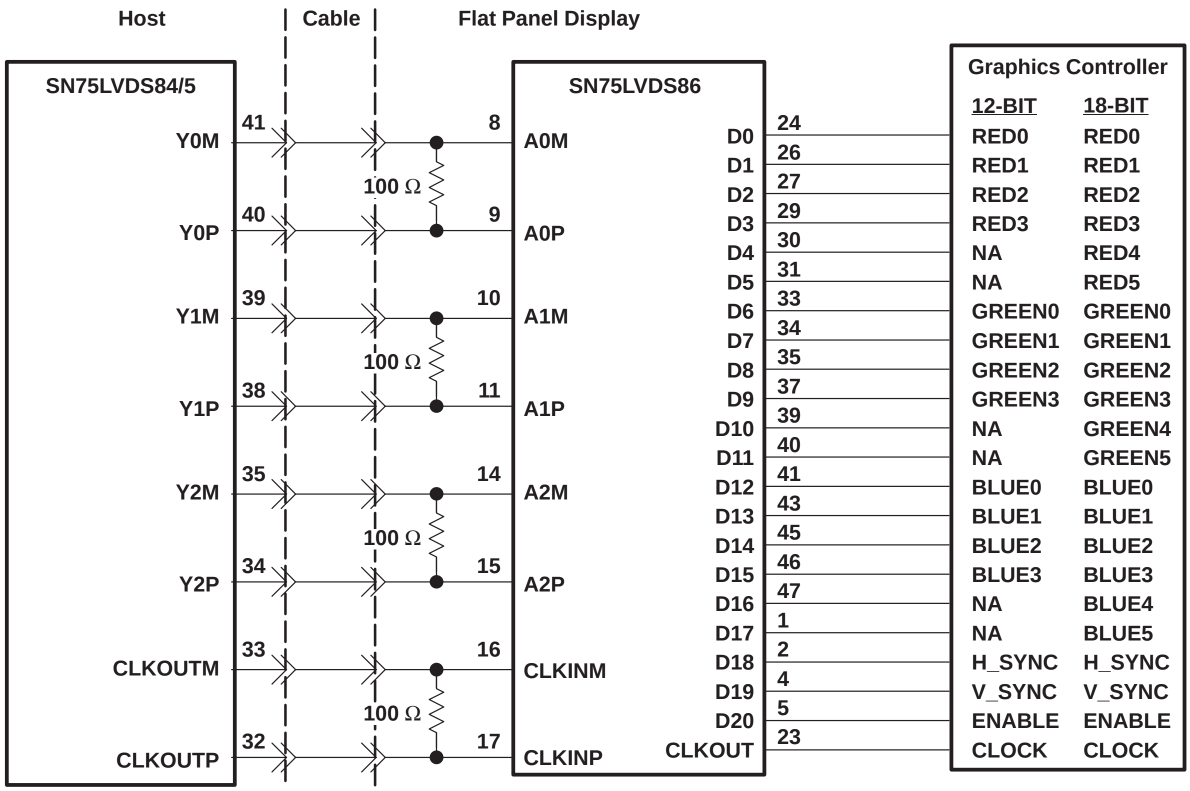


Figure 12. Typical FlatLink PLL Characteristics

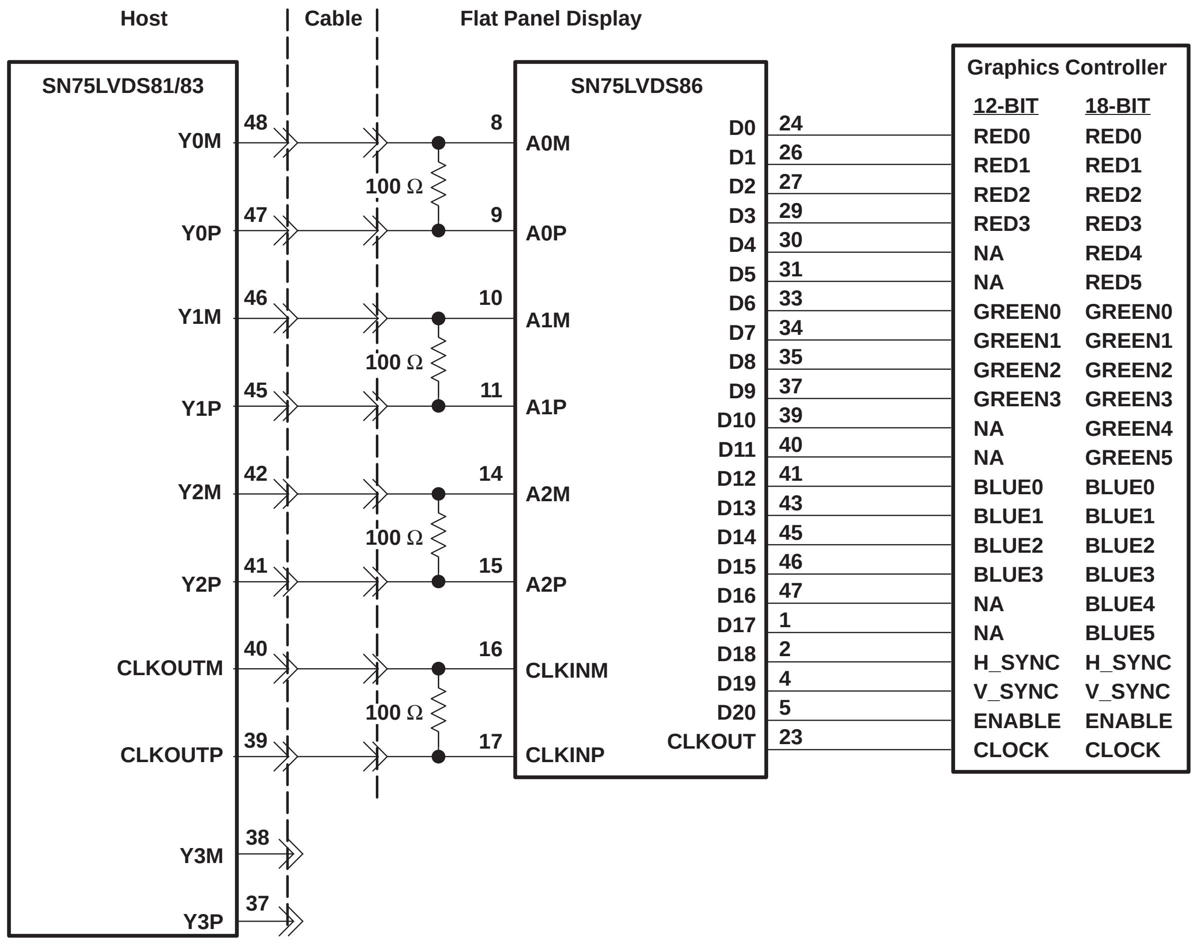
APPLICATION INFORMATION



NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
B. NA – not applicable, these unused inputs should be left open.

Figure 13. 18-Bit Color Host to Flat Panel Display Application

APPLICATION INFORMATION



NOTES: A. The four 100-Ω terminating resistors are recommended to be 0603 types.
B. NA – not applicable, these unused inputs should be left open.

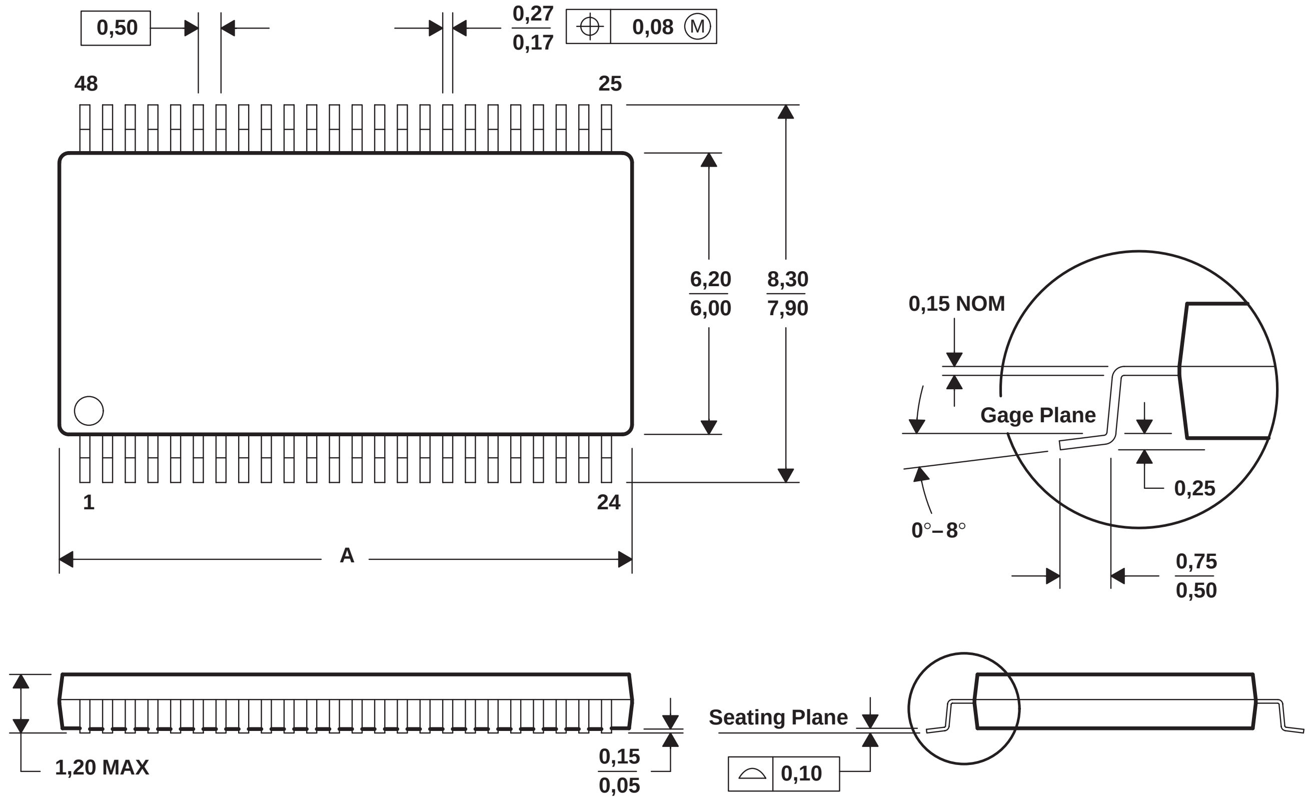
Figure 14. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application†

† See the *FlatLink Designer's Guide* (SLLA012) for more application information.

MECHANICAL INFORMATION

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153