



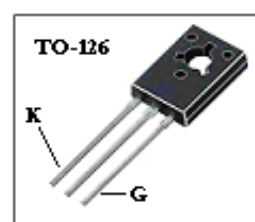
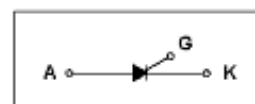
Sensitive Gate Silicon Controlled Rectifier

General Description

Glassivated PNP devices designed for high volume consumer applications such as temperature, light, and speed control; process and remote control, and warning systems where reliability of operation is important.

Features

- Glassivated Surface for Reliability and Uniformity
- Power Rated at Economical Prices
- Practical Level Triggering and Holding Characteristics
- Flat, Rugged, Thermopad Construction for Low Thermal Resistance
- Sensitive Gate Triggering



Maximum Ratings ($T_j=25^\circ\text{C}$ unless otherwise specified)

T_{stg}	Storage Temperature	-40~150
T_j	Operating Junction Temperature	-40~110
V_{DRM}	Peak Repetitive Off-State Voltage(Forward)	400V
V_{RRM}	Peak Repetitive Off-State Voltage(Reverse)	400V
$I_T(\text{RMS})$	On-State R.M.S Current (180° Conduction Angles, $T_C = 80^\circ\text{C}$)	4A
$I_{T(AV)}$	On-State Average Current (180° Conduction Angles, $T_C = 80^\circ\text{C}$)	2.55A
I_{TSM}	Surge On-State Current (1/2 Cycle, 60Hz, Sine Wave, Non-repetitive, $T_j = 110^\circ\text{C}$)	20A
I^2t	Circuit Fusing Considerations($t = 8.3\text{ms}$)	1.65A ² s
P_{GM}	Forward Peak Gate Power Dissipation (Pulse Width $\leq 1.0\text{ }\mu\text{sec}$, $T_c=80^\circ\text{C}$)	0.5W
$P_{G(AV)}$	Forward Average Gate Power Dissipation (Pulse Width $\leq 1.0\text{ }\mu\text{sec}$, $T_c=80^\circ\text{C}$)	0.1W
I_{GM}	Forward Peak Gate Current (Pulse Width $\leq 1.0\text{ }\mu\text{sec}$, $T_c=80^\circ\text{C}$)	0.2A

**Electrical Characteristics** ($T_C=25$ unless otherwise specified)

Symbol	Items	Min.	Typ.	Max.	Unit	Conditions
I_{DRM} OR I_{RRM}	Peak Repetitive Forward or Reverse Blocking Current.			10 100	μA	$V_{AK}=\text{Rated } V_{DRM} \text{ or } V_{RRM}$ $R_{KG}=1000 \text{ ohms}$ $T_j=25$ $T_j=110$
V_{TM}	Peak Forward On-State Voltage (1)			2.2	V	$I_{FM}=1A$
I_{GT}	Gate Trigger Current (2)		15 35	200 500	μA	$V_{AK}=6V(DC)$, $R_L=100 \text{ ohms}$ $T_j=25$ $T_j=-40$
V_{GT}	Gate Trigger Voltage (2)	0.4 0.5	0.6 0.75	0.8 1.0	V	$V_{AK}=6V(DC)$, $R_L=100 \text{ ohms}$ $T_j=25$ $T_j=-40$
V_{GRM}	Peak Reverse Gate Voltage			6.0	V	$I_{GR}=10 \mu A$
V_{GD}	Gate Non-Trigger Voltage	0.2			V	$V_{AK}=12V$, $R_L=100 \text{ ohms}$ $T_j=110$
I_H	Holding Current		0.19 0.33 0.07	3.0 6.0 2.0	mA	Initiating current=20mA, Gate open, $V_D=12V(DC)$ $T_j=25$ $T_j=-40$ $T_j=110$
I_L	Latching Current		0.2 0.35	5.0	mA	$V_{AK}=12V$, $I_G=20mA$ $T_j=25$ $T_j=-40$
$R_{th(j-c)}$	Thermal Resistance			3.0	/W	Junction to Case
$R_{th(j-a)}$	Thermal Resistance			75	/W	Junction to Ambient
TL	Maximum Lead Temperature for Soldering Purpose 1/8'',from case for 10 Seconds			260		
dv/dt	Critical Rate-of-Rise Off-state Voltage		8.0		V/ μs	$V_{AK}=\text{Rated } V_{DRM}$, Exponential waveform , $R_{GK}=1000 \text{ ohms}$ Gate open $T_j=110$

(1) Pulse Test : Pulse Width $\leq 2.0ms$, Duty Cycle $\leq 2\%$ (2) R_{GK} is not included in measurement



Performance Curves

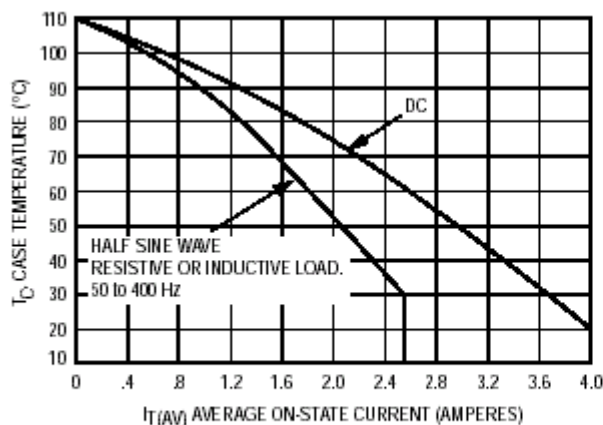


Figure 1. Average Current Derating

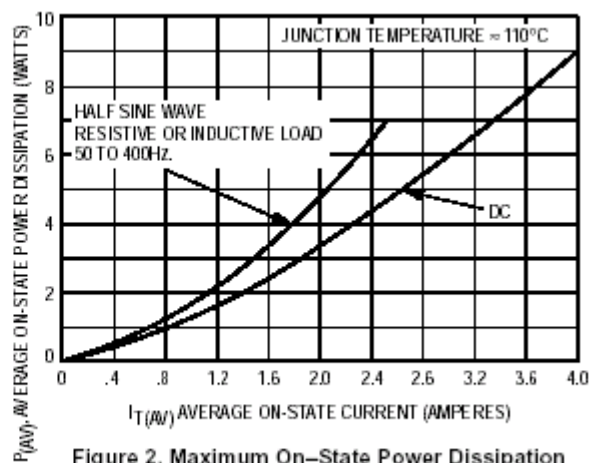


Figure 2. Maximum On-State Power Dissipation

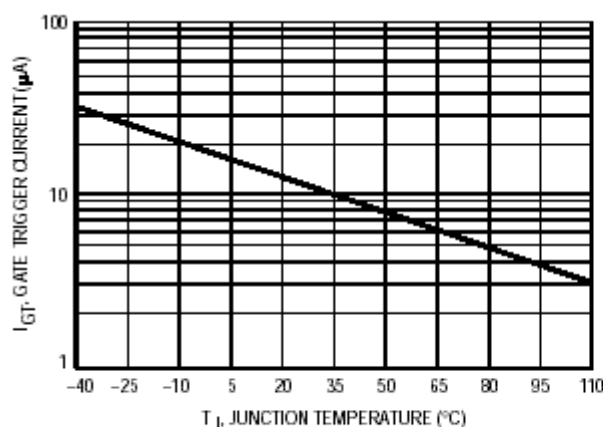


Figure 3. Typical Gate Trigger Current versus Junction Temperature

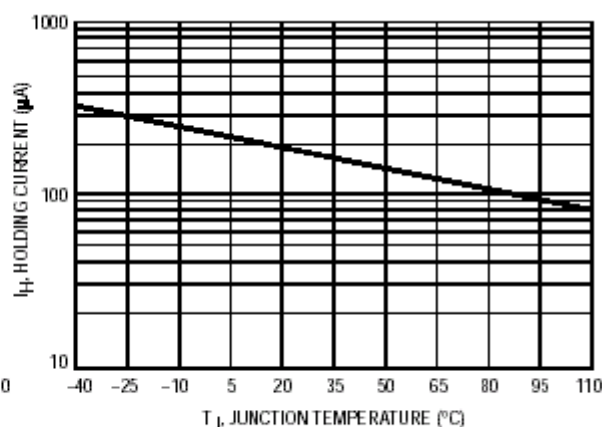


Figure 4. Typical Holding Current versus Junction Temperature

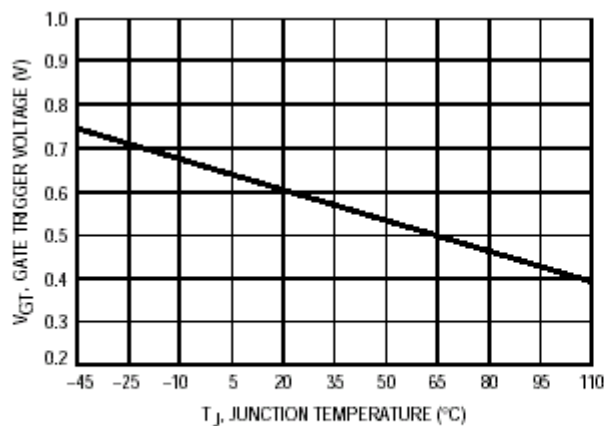


Figure 5. Typical Gate Trigger Voltage versus Junction Temperature

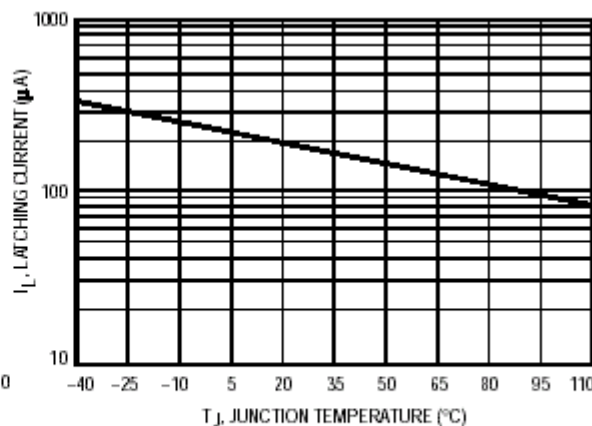


Figure 6. Typical Latching Current versus Junction Temperature