TJA1145A

High-speed CAN transceiver for partial networking

Rev. 2 — 23 September 2020 Product data sheet

1. General description

The TJA1145A is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1145A features very low power consumption in Standby and Sleep modes and supports ISO 11898-2:2016 compliant CAN Partial Networking by means of a selective wake-up function.

A dedicated implementation of the partial networking function has been embedded into the FD variants TJA1145AT/FD and TJA1145ATK/FD (see Section 7.3.2 for further details on CAN FD). This function is called ‘FD-passive’ and is the ability to ignore CAN FD frames while waiting for a valid wake-up frame in Sleep/Standby mode. This additional feature of partial networking is the perfect fit for networks that support both CAN FD and standard CAN 2.0 communications. It allows normal CAN controllers that do not need to communicate CAN FD messages to remain in partial networking Sleep/Standby mode during CAN FD communication without generating bus errors.

Advanced power management regulates the supply throughout the node and supports local and remote wake-up functionality. I/O levels are automatically adjusted to the I/O levels of the controller, allowing the TJA1145A to interface directly with 3.3 V to 5 V microcontrollers. An SPI interface is provided for transceiver control and for retrieving status information. Bus connections are truly floating when power is off.

The TJA1145A implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

These features make the TJA1145A the ideal choice for high-speed CAN networks containing nodes that are always connected to the battery supply line but, in order to minimize current consumption, are only active when required by the application.

2. Features and benefits

2.1 General

- ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant
- Timing guaranteed for data rates up to 5 Mbit/s in the CAN FD fast phase
- Autonomous bus biasing
- Optimized for in-vehicle high-speed CAN communication
- No ‘false’ wake-ups due to CAN FD in TJA1145Ax/FD variants

- Hardware and software compatible with the TJA1145, with improved EMC performance

2.2 Designed for automotive applications

- ±8 kV ElectroStatic Discharge (ESD) protection, according to the Human Body Model (HBM) on the CAN bus pins
- ±6 kV ESD protection, according to IEC TS 62228 on pins BAT and WAKE and on the CAN bus pins
- CAN bus pins short-circuit proof to ±58 V
- Battery and CAN bus pins protected against transients according to ISO 7637-3, test pulses 1, 2a, 3a and 3b.
- Suitable for use in 12 V and 24 V systems
- Available in SO14 and leadless HVSON14 package (3 mm × 4.5 mm) with improved Automated Optical Inspection (AOI) capability
- AEC-Q100 qualified
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.3 Advanced ECU power management system

- Very low-current Standby and Sleep modes, with full wake-up capability
- Entire node can be powered down via the inhibit output
- Remote wake-up capability via standard CAN wake-up pattern or via ISO 11898-2:2016 compliant selective wake-up frame detection
- Local wake-up via the WAKE pin
- Wake-up source recognition
- Bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s and 1 Mbit/s supported during selective wake-up'
- Local wake-up can be disabled to reduce current consumption
- Transceiver disengages from the bus when the battery supply is removed
- VIO input allows for direct interfacing with 3.3 V to 5 V microcontrollers

2.4 Protection and diagnosis

- 16-, 24- or 32-bit SPI for configuration, control and diagnosis
- Transmit Data (TXD) dominant time-out function with diagnosis
- Overtemperature warning and shut-down
- Undervoltage detection and recovery on pins VCC, VIO and BAT
- Cold start diagnosis (via bits PO and NMS)
- Advanced system and transceiver interrupt handling

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage		4.5	-	28	V
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IO}	supply voltage on pin V_{IO}		2.85	-	5.5	V
$V_{th(det)poff}$	power-off detection threshold voltage	V_{BAT} falling	2.8	-	3	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin VCC		4.5	-	4.75	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO	V_{BAT} > 4.5 V	2.7	-	2.85	V
I_{BAT}	battery supply current	Normal mode	-	1	1.5	mA
		Sleep mode; CAN Offline mode; –40 °C < T_{vj} < 85 °C; V_{BAT} = 7 V to 18 V	-	48	64	µA
		Standby mode; CAN Offline mode; –40 °C < T_{vj} < 85 °C; V_{BAT} = 7 V to 18 V	-	56	73	µA
I_{CC}	supply current	CAN Active mode; CAN recessive; V_{TXD} = V_{IO}	-	3	6	mA
		CAN Active mode; CAN dominant; V_{TXD} = 0 V	-	45	65	mA
		Standby/Normal mode; CAN inactive; –40 °C < T_{vj} < 85 °C	-	4.7	8.5	µA
		Sleep mode; CAN inactive; –40 °C < T_{vj} < 85 °C	-	3.8	7	µA
I_{IO}	supply current on pin V_{IO}	Standby/Normal mode; –40 °C < T_{vj} < 85 °C	-	7.1	11	µA
		Sleep mode; –40 °C < T_{vj} < 85 °C	-	5	8	µA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins CANH, CANL	–6	-	+6	kV
V_{CANH}	voltage on pin CANH		–58	-	+58	V
V_{CANL}	voltage on pin CANL		–58	-	+58	V
T_{vj}	virtual junction temperature		–40	-	+150	°C

All information provided in this document is subject to legal disclaimers.

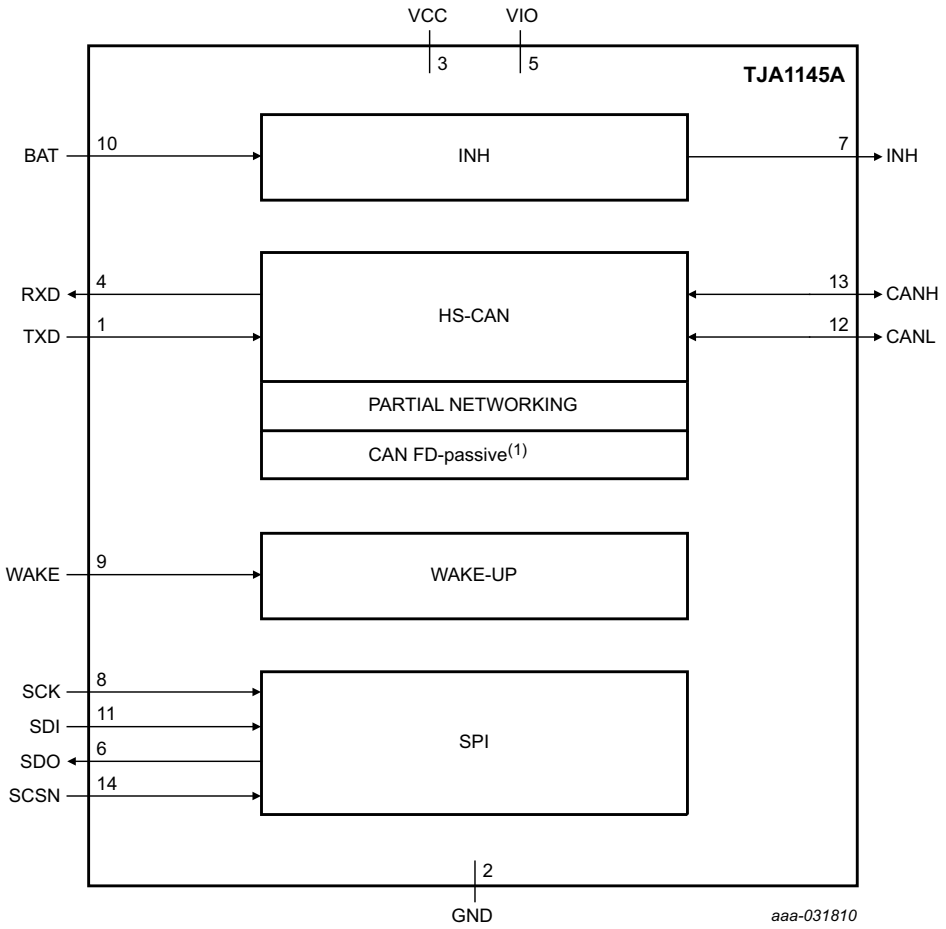
© NXP Semiconductors N.V. 2020. All rights reserved.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1145AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1145AT/FD	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1145ATK	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2
TJA1145ATK/FD	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

5. Block diagram



(1) TJA1145AT/FD and TJA1145ATK/FD only.

Fig 1. Block diagram

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

6. Pinning information

6.1 Pinning

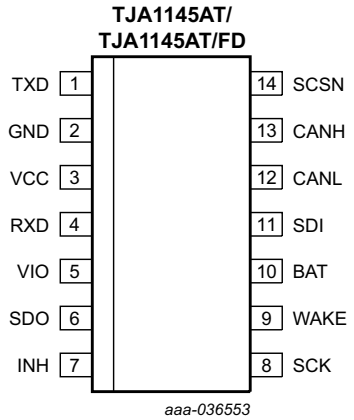


Fig 2. Pin configuration diagram: SO14

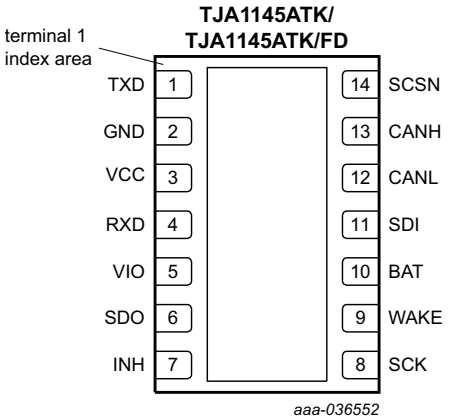


Fig 3. Pin configuration diagram: HVSON14 Transparent top view

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2[1]	ground
VCC	3	5 V CAN transceiver supply voltage
RXD	4	receive data output; reads out data from the bus lines
VIO	5	supply voltage for I/O level adaptor
SDO	6	SPI data output
INH	7	inhibit output for switching external voltage regulators
SCK	8	SPI clock input
WAKE	9	local wake-up input
BAT	10	battery supply voltage
SDI	11	SPI data input
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
SCSN	14	SPI chip select input

[1] HVSON14 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

7. Functional description

The TJA1145A is a stand-alone high-speed CAN transceiver containing a variety of fail-safe and diagnostic features that offer enhanced system reliability and advanced power management. The transceiver combines the functionality of the TJA1043 with ISO 11898-2:2016 compliant CAN partial networking and autonomous bus biasing.

7.1 System controller

The system controller manages register configuration and controls the internal functions of the TJA1145A. Detailed device status information is collected and made available to the microcontroller.

7.1.1 Operating modes

The system controller contains a state machine that supports five operating modes: Normal, Standby, Sleep, Overtemp and Off. The state transitions are illustrated in Figure 4.

7.1.1.1 Normal mode

Normal mode is the active operating mode. In this mode, the TJA1145A is fully operational. All device hardware is available and can be activated (see Table 4).

Normal mode can be selected from Standby or Sleep mode via an SPI command (MC = 111).

7.1.1.2 Standby mode

Standby mode is the first-level power-saving mode of the TJA1145A, featuring low current consumption. The transceiver is unable to transmit or receive data in Standby mode, but the INH pin remains active so voltage regulators controlled by this pin will be active.

If remote CAN wake-up is enabled (CWE = 1; see Table 22), the receiver monitors bus activity for a wake-up request. The bus pins are biased to GND (via $R_{i(cm)}$) when the bus is inactive and at approximately 2.5 V when there is activity on the bus (autonomous biasing). CAN wake-up can occur via a standard wake-up pattern or via a selective wake-up frame (selective wake-up is enabled when CPNC = PNCOK = 1; otherwise standard wake-up is enabled).

Pin RXD is forced LOW when any enabled wake-up or interrupt event is detected (see Section 7.6).

The TJA1145A switches to Standby mode:

- from Off mode if the battery voltage rises above the power-on detection threshold, $V_{th(det)pon}$.
- from Overtemp mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$.
- from Sleep mode on the occurrence of a wake-up or interrupt event (see Section 7.6)
- from Normal or Sleep mode via an SPI command (MC = 100)
- from Normal mode if Sleep mode is selected via an SPI command (MC = 001) while a wake-up event is pending or all wake-up sources are disabled

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

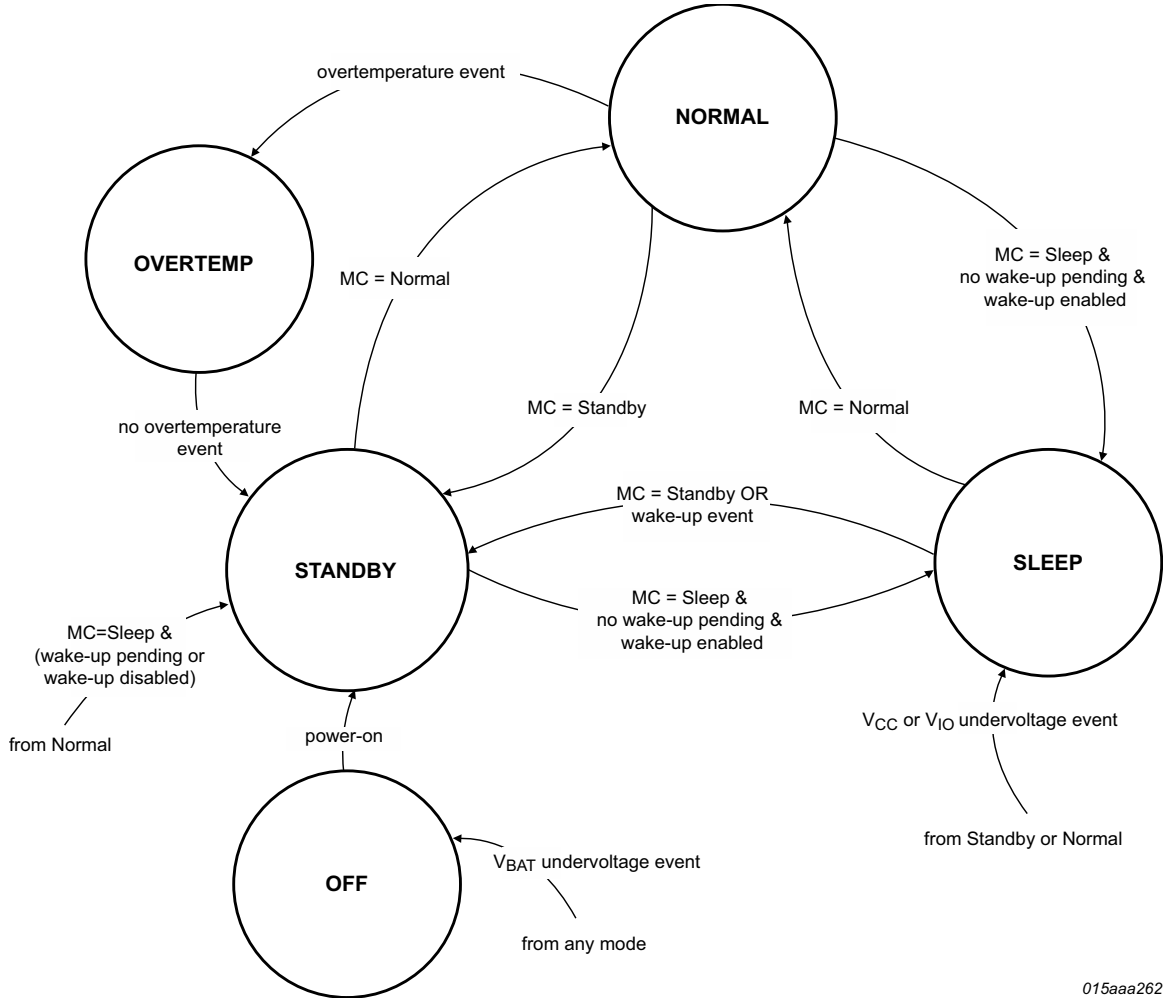


Fig 4. TJA1145A system controller state diagram

7.1.1.3 Sleep mode

Sleep mode is the second-level power saving mode of the TJA1145A. In Sleep mode, the transceiver behaves as in Standby Mode with the exception that pin INH is set to a high-ohmic state. Voltage regulators controlled by this pin will be switched off, and the current into pin BAT will be reduced to a minimum.

Any enabled wake-up or interrupt event (except SPIF), or an SPI command (provided a valid V_{IO} voltage is connected), will wake up the transceiver from Sleep mode.

Sleep mode can be selected from Normal or Standby mode via an SPI command (MC = 001). The TJA1145A will switch to Sleep mode on receipt of this command, provided there are no pending wake-up events and at least one regular wake-up source (CAN bus or WAKE pin; see Section 7.6) is enabled. Any attempt to enter Sleep mode while one of these conditions has not been met will cause the TJA1145A to switch to Standby mode.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

The TJA1145A will also be forced to switch to Sleep mode after $t_{d(uvd\text{-}sleep)}$ if a V_{CC} of V_{IO} undervoltage event is detected ($V_{CC}/V_{IO} < V_{uvd(VCC)}/V_{uvd(VIO)}$ for longer than $t_{d(uvd)}$). In this event, all pending wake-up events will be cleared. CAN wake-up (CWE = 1) and local wake-up via the WAKE pin (WPFE = WPRE = 1) are enabled in order to avoid a system deadlock (see Section 7.11) and selective wake-up is disabled (CPNC = 0).

Status bit FSMS in the Main status register (Table 6) indicates whether a transition to Sleep mode was selected via an SPI command (FSMS = 0) or was forced by an undervoltage event on VCC or VIO (FSMS = 1). This bit can be read after the TJA1145A wakes up from Sleep mode to allow the settings of CWE, WPFE, WPRE and CPNC to be re-adjusted if an undervoltage event forced the transition to Sleep mode (FSMS = 1).

7.1.1.4 Off mode

The TJA1145A will be in Off mode when the battery voltage is too low to supply the IC. This is the default mode when the battery is first connected. The TJA1145A will switch to Off mode from any mode if the battery voltage drops below the power-off threshold ($V_{th(det)poff}$). In Off mode, the CAN pins and pin INH are in a high-ohmic state.

When the battery supply voltage rises above the power-on threshold ($V_{th(det)pon}$), the TJA1145A starts to boot up, triggering an initialization procedure. The TJA1145A will switch to Standby mode after $t_{startup}$.

7.1.1.5 Overtemp mode

Overtemp mode is provided to prevent TJA1145A being damaged by excessive temperatures. The TJA1145A switches immediately to Overtemp mode from Normal mode when the global chip temperature rises above the overtemperature protection activation threshold, $T_{th(act)otp}$.

To help prevent the loss of data due to overheating, the TJA1145A issues a warning when the IC temperature rises above the overtemperature warning threshold ($T_{th(warn)otp}$). When this happens, status bit OTWS is set and an overtemperature interrupt is generated (OTW = 1), if enabled (OTWE = 1).

In Overtemp mode, the CAN transmitter and receiver are disabled and the CAN pins are in a high-ohmic state. Wake-up events will not be detected, but a pending wake-up will still be signalled by a LOW level on pin RXD, which will persist after the overtemperature event has been cleared.

The TJA1145A exits Overtemp mode:

- and switches to Standby mode if the chip temperature falls below the overtemperature protection release threshold, $T_{th(rel)otp}$
- if the device is forced to switch to Off mode ($V_{BAT} < V_{th(det)poff}$)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

7.1.1.6 Hardware characterization for the TJA1145A operating modes

Table 4. Hardware characterization by functional block

Block	Operating mode				
	Off	**Standby**	**Normal**	**Sleep**	**Overtemp**
SPI	disabled	active	active	active if V_{IO} supplied[1]	disabled
INH	high-ohmic	V_{BAT} level	V_{BAT} level	high-ohmic	V_{BAT} level
CAN	off	Offline	Active/ Offline/ Listen-only (determined by bits CMC; see Table 7)	Offline	off
RXD	V_{IO} level	V_{IO} level/LOW if wake-up event detected	CAN bit stream if CMC = 01/10/11; otherwise same as Standby/Sleep	V_{IO} level/LOW if wake-up event detected	V_{IO} level/LOW if wake-up pending

[1] SPI speed is limited in Sleep mode (see Table 35).

7.1.2 System control registers

The operating mode is selected via bits MC in the Mode control register. The Mode control register is accessed via SPI address 0x01 (see Section 7.12).

Table 5. Mode control register (address 01h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	MC	R/W		mode control:
			001	Sleep mode
			100	Standby mode
			111	Normal mode

The Main status register can be accessed to monitor the status of the overtemperature warning flag and to determine whether the TJA1145A has entered Normal mode after initial power-up. Bit FSMS indicates whether the most recent transition to Sleep mode was triggered by an undervoltage event or by an SPI command.

Table 6. Main status register (address 03h)

Bit	Symbol	Access	Value	Description
7	FSMS	R		Sleep mode transition status:
			0	transition to Sleep mode triggered by an SPI command
			1	an undervoltage on VCC and/or VIO forced a transition to Sleep mode
6	OTWS	R		overtemperature warning status:
			0	IC temperature below overtemperature warning threshold
			1	IC temperature above overtemperature warning threshold
5	NMS	R		Normal mode status:
			0	TJA1145A has entered Normal mode (after power-up)
			1	TJA1145A has powered up but has not yet switched to Normal mode
4:0	reserved	R	-	

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

7.2 High-speed CAN transceiver

The integrated high-speed CAN transceiver is designed for active communication at bit rates up to 1 Mbit/s, providing differential transmit and receive capability to a CAN protocol controller. The transceiver is ISO 11898-2:2016 compliant (defining high-speed CAN with selective wake-up functionality and autonomous bus biasing). The CAN transmitter is supplied via pin VCC while the CAN receiver is supplied via pin BAT. The TJA1145A includes additional timing parameters on loop delay symmetry to ensure reliable communication in fast phase at data rates up to 5 Mbit/s, as used in CAN FD networks.

The CAN transceiver supports autonomous CAN biasing, which helps to minimize RF emissions. CANH and CANL are always biased to 2.5 V when the transceiver is in Active or Listen-only modes (CMC = 01/10/11).

Autonomous biasing is active in CAN Offline mode - to 2.5 V if there is activity on the bus (CAN Offline Bias mode) and to GND if there is no activity on the bus for $t > t_{to(silence)}$ (CAN Offline mode).

This is useful when the node is disabled due to a malfunction in the microcontroller or when CAN partial networking is enabled. The TJA1145A ensures that the CAN bus is correctly biased to avoid disturbing ongoing communication between other nodes. The autonomous CAN bias voltage is derived directly from V_{BAT}.

7.2.1 CAN operating modes

The integrated CAN transceiver supports four operating modes: Active, Listen-only, Offline and Offline Bias (see Figure 5). The CAN transceiver operating mode depends on the TJA1145A operating mode and on the setting of bits CMC in the CAN control register (Table 7).

When the TJA1145A is in Normal mode, the CAN transceiver operating mode (Offline, Active or Listen-only) can be selected via bits CMC in the CAN control register (Table 7). When the TJA1145A is in Standby or Sleep modes, the transceiver is forced to Offline or Offline Bias mode (depending on bus activity).

7.2.1.1 CAN Active mode

In CAN Active mode, the transceiver can transmit and receive data via CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data, which is output on pin RXD. The transmitter converts digital data generated by the CAN controller (input on pin TXD) into analog signals suitable for transmission over the CANH and CANL bus lines.

CAN Active mode is selected when CMC = 01 or 10. When CMC = 01, V_{CC} undervoltage detection is enabled and the transceiver switches to CAN Offline or CAN Offline Bias mode when the voltage on V_{CC} drops below $V_{uvd(VCC)}$. When CMC = 10, V_{CC} undervoltage detection is disabled. The transmitter will remain active until the TJA1145A is forced into Sleep mode by the V_{CC} undervoltage event; the transceiver will then switch to CAN Offline or CAN Offline Bias mode.

The CAN transceiver is in Active mode when:

- the TJA1145A is in Normal mode (MC = 111) and the CAN transceiver has been enabled by setting bits CMC in the CAN control register to 01 or 10 (see Table 7) and:

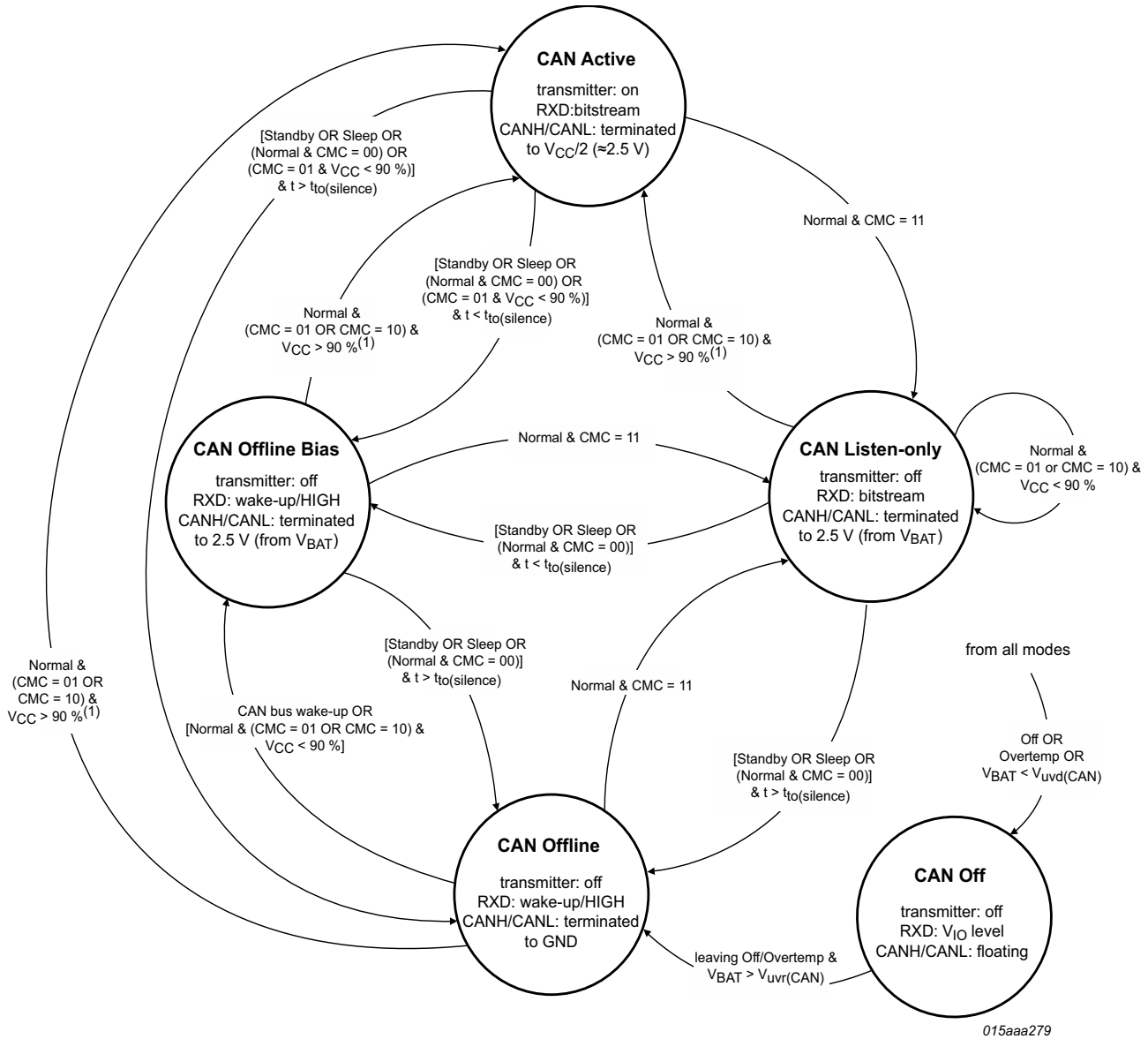
All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

– if CMC = 01, the voltage on pin VCC is above the V_{CC} undervoltage detection threshold ($V_{uvd(VCC)}$)

If pin TXD is held LOW (e.g. by a short-circuit to GND) when CAN Active mode is selected via bits CMC, the transceiver will not enter CAN Active mode but will switch to or remain in CAN Listen-only mode. It will remain in Listen-only mode until pin TXD goes HIGH in order to prevent a hardware and/or software application failure from driving the bus lines to an unwanted dominant state.

In CAN Active mode, the CAN bias voltage is derived from V_{CC}.



(1) To prevent the bus lines being driven to a permanent dominant state, the transceiver will not switch to CAN Active mode or CAN Listen-only mode if pin TXD is held LOW (e.g. by a short-circuit to GND)

Fig 5. CAN transceiver state machine

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

The application can determine whether the CAN transceiver is ready to transmit/receive data or is disabled by reading the CAN Transceiver Status (CTS) bit in the Transceiver Status Register (Table 8).

7.2.1.2 CAN Listen-only mode

CAN Listen-only mode allows the TJA1145A to monitor bus activity while the transceiver is inactive, without influencing bus levels. This facility could be used by development tools that need to listen to the bus but do not need to transmit or receive data or for software-driven selective wake-up. Dedicated microcontrollers could be used for selective wake-up, providing an embedded low-power CAN engine designed to monitor the bus for potential wake-up events.

In Listen-only mode the CAN transmitter is disabled, reducing current consumption. The CAN receiver and CAN biasing remain active. This enables the host microcontroller to switch to a low-power mode in which an embedded CAN protocol controller remains active, waiting for a signal to wake up the microcontroller.

The CAN transceiver is in Listen-only mode when:

- the TJA1145A is in Normal mode and CMC = 11

The CAN transceiver will not leave Listen-only mode while TXD is LOW or CAN Active mode is selected with CMC = 01 or 10 while the voltage on VCC is below the undervoltage threshold, $V_{uvd(VCC)}$.

7.2.1.3 CAN Offline and Offline Bias modes

In CAN Offline mode, the transceiver monitors the CAN bus for a wake-up event, provided CAN wake-up detection is enabled (CWE = 1). CANH and CANL are biased to GND.

CAN Offline Bias mode is the same as CAN Offline mode, with the exception that the CAN bus is biased to 2.5 V. This mode is activated automatically when activity is detected on the CAN bus while the transceiver is in CAN Offline mode. The transceiver will return to CAN Offline mode if the CAN bus is silent (no CAN bus edges) for longer than $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline mode from CAN Active mode or CAN Listen-only mode if:

- the TJA1145A switches to Standby or Sleep mode OR
- the TJA1145A is in Normal mode and CMC = 00

provided the CAN-bus has been inactive for at least $t_{to(silence)}$. If the CAN-bus has been inactive for less than $t_{to(silence)}$, the CAN transceiver switches first to CAN Offline Bias mode and then to CAN Offline mode once the bus has been silent for $t_{to(silence)}$.

The CAN transceiver switches to CAN Offline/Offline Bias mode from CAN Active mode if CMC = 01 and the voltage on VCC drops below the undervoltage threshold or if CMC = 10 and the TJA1145A switches to Sleep mode in response to a V_{CC} undervoltage event.

The CAN transceiver switches to CAN Offline mode:

- from CAN Offline Bias mode if no activity is detected on the bus (no CAN edges) for $t > t_{to(silence)}$ OR

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

- when the TJA1145A switches from Off or Overtemp mode to Standby mode

The CAN transceiver switches from CAN Offline mode to CAN Offline Bias mode if:

- a standard wake-up pattern is detected on the CAN bus OR
- the CAN transceiver is in Normal mode, CMC = 01 or 10 and V_{CC} < 90 %

7.2.1.4 CAN Off mode

The CAN transceiver is switched off completely with the bus lines floating when:

- the TJA1145A switches to Off or Overtemp mode OR
- V_{BAT} falls below the CAN receiver undervoltage detection threshold, $V_{uvd(CAN)}$

It will be switched on again on entering CAN Offline mode when V_{BAT} rises above the undervoltage recovery threshold ($V_{uvr(CAN)}$) and the CAN transceiver is no longer in Off/Overtemp mode. CAN Off mode prevents reverse currents flowing from the bus when the battery supply to the CAN transceiver is lost.

7.2.2 CAN standard wake-up (partial networking not enabled)

If the CAN transceiver is in Offline mode and CAN wake-up is enabled (CWE = 1), but CAN selective wake-up is disabled (CPNC = 0 or PNCOK = 0), the TJA1145A will monitor the bus for a standard wake-up pattern.

A filter at the receiver input prevents unwanted wake-up events occurring due to automotive transients or EMI. This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus.

The TJA1145A wakes up from Standby or Sleep mode when a dedicated wake-up pattern (specified in ISO 11898-2:2016) is detected on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

Dominant or recessive bits between the above mentioned phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 6). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.

When a valid CAN wake-up pattern is detected on the bus, wake-up bit CW in the Transceiver event status register is set (see Table 19) and pin RXD is driven LOW. If the TJA1145A was in Sleep mode when the wake-up pattern was detected, it will switch pin INH to V_{BAT} to activate external voltage regulators (e.g. for supplying V_{CC} and V_{IO}) and enter Standby mode.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

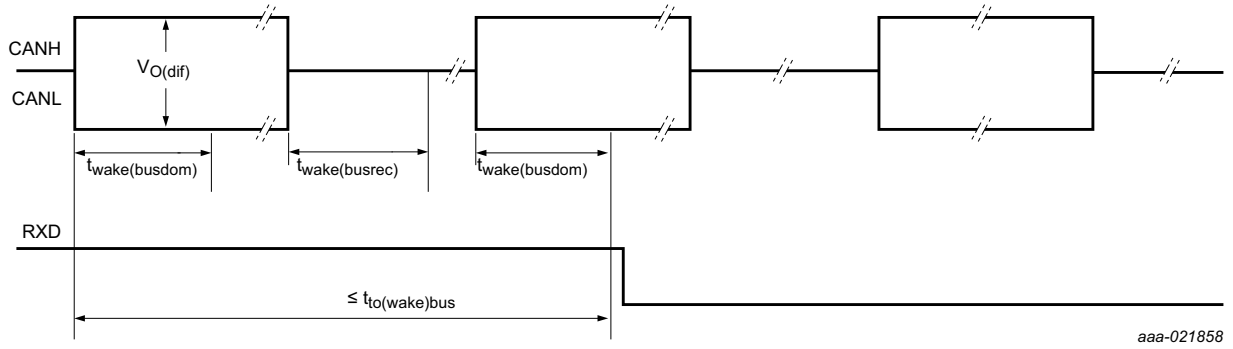


Fig 6. CAN wake-up timing

7.2.3 CAN control and Transceiver status registers

Table 7. CAN control register (address 20h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	
6	CFDC	R/W		CAN FD tolerance (TJA1145Ax/FD variants only; otherwise ignored)
			0	CAN FD tolerance disabled
			1	CAN FD tolerance enabled
5	PNCOK	R/W		CAN partial networking configuration:
			0	partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	partial networking registers configured successfully
4	CPNC	R/W		CAN selective wake-up; when enabled, node is part of a partial network:
			0	disable CAN selective wake-up
			1	enable CAN selective wake-up
3:2	reserved	R	-	
1:0	CMC	R/W		CAN transceiver operating mode selection:
			00	Offline mode
			01	Active mode (while TJA1145A is in Normal mode); V_{CC} undervoltage detection active; transition to Active mode, and remaining in Active mode, requires V_{CC} above undervoltage threshold
			10	Active mode (while TJA1145A is in Normal mode); V_{CC} undervoltage detection inactive; transition to Active mode requires V_{CC} above undervoltage threshold
			11	Listen-only mode

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 8. Transceiver status register (address 22h)

Bit	Symbol	Access	Value	Description
7	CTS	R		CAN transceiver status:
			0	CAN transceiver not in Active mode
			1	CAN transceiver in Active mode
6	CPNERR	R		CAN partial networking error status:
			0	no CAN partial networking error detected (PNFDE = 0 AND PNCOK = 1)
			1	CAN partial networking error detected (PNFDE = 1 OR PNCOK = 0); wake-up via standard wake-up pattern only
5	CPNS	R		CAN partial networking status:
			0	CAN partial networking configuration error detected (PNCOK = 0)
			1	CAN partial networking configuration OK (PNCOK = 1)
4	COSCS	R		CAN oscillator status:
			0	CAN partial networking oscillator not running at target frequency
			1	CAN partial networking oscillator running at target frequency
3	CBSS	R		CAN bus silence status:
			0	CAN bus active (communication detected on bus)
			1	CAN bus inactive (for longer than $t_{to(silence)}$
2	reserved	R	-	
1	VCS[1]	R		V_{CC} supply voltage status:
			0	V_{CC} is above the undervoltage detection threshold ($V_{uvd(VCC)}$)
			1	V_{CC} is below the undervoltage detection threshold ($V_{uvd(VCC)}$)
0	CFS	R		CAN failure status:
			0	no TXD dominant time-out event detected
			1	CAN transmitter disabled due to a TXD dominant time-out event

[1] Only active when CMC = 01.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

7.3 CAN partial networking

Partial networking allows nodes in a CAN network to be selectively activated in response to dedicated wake-up frames (WUF). Only nodes that are functionally required are active on the bus while the other nodes remain in a low-power mode until needed.

If both CAN wake-up (CWE = 1) and CAN selective wake-up (CPNC = 1) are enabled, and the partial networking registers are configured correctly (PNCOK = 1), the transceiver monitors the bus for dedicated CAN wake-up frames.

7.3.1 Wake-up frame (WUF)

A wake-up frame is a CAN frame according to ISO 11898-1:2015, consisting of an identifier field (ID), a Data Length Code (DLC), a data field and a Cyclic Redundancy Check (CRC) code including the CRC delimiter.

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the Frame control register (Table 12).

A valid WUF identifier is defined and stored in the ID registers (Table 10). An ID mask can be defined to allow a group of identifiers to be recognized as valid by an individual node. The identifier mask is defined in the mask registers (Table 11), where a 1 means ‘don’t care’.

In the example illustrated in Figure 7, based on the standard frame format, the 11-bit identifier is defined as 0x1A0. The identifier is stored in ID registers 2 (0x29) and 3 (0x2A). The three least significant bits of the ID mask, bits 2 to 4 of Mask register 2 (0x2D) are set to 1, which means that the corresponding identifier bits are ‘don’t care’. This means that any of eight different identifiers will be recognized as valid in the received WUF (from 0x1A0 to 0x1A7).

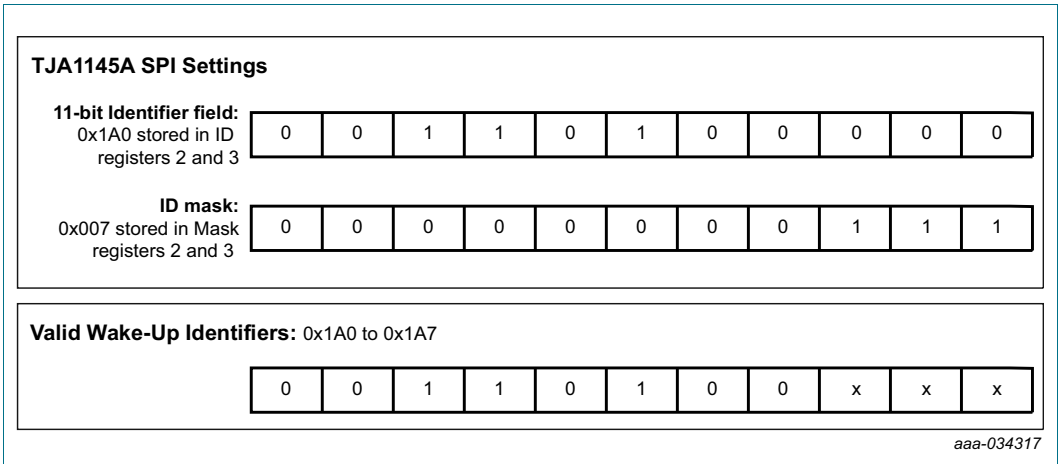


Fig 7. Evaluating the ID field in a selective wake-up frame

The data field indicates which nodes are to be woken up. Within the data field, groups of nodes can be pre-defined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

The data length code (bits DLC in the Frame control register; Table 12) determines the number of data bytes (between 0 and 8) expected in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC ≠ 0000), at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see Table 13) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 byes long, up to 64 groups of nodes can be defined).

If DLC = 0000, a node will wake up if the WUF contains a valid identifier and the received data length code is 0000, regardless of the values stored in the data mask. If DLC ≠ 0000 and all data mask bits are set to 0, the device cannot be woken up via the CAN bus (note that all data mask bits are set to 1 by default; see Table 31). If a WUF contains a valid ID but the DLCs (in the Frame control register and in the WUF) don't match, the data field is ignored and no nodes are woken up.

In the example illustrated in Figure 8, the data field consists of a single byte (DLC = 1). This means that the data field in the incoming wake-up frame is evaluated against data mask 7 (stored at address 6Fh; see Table 13 and Figure 9). Data mask 7 is defined as 10101000 in the example. This means that up to three groups of nodes could be woken up (group 1, 3 and 5) if the respective bits in the data frame are also set to 1.

The received message shown in Figure 8 could, potentially, wake up four groups of nodes: groups 2, 3, 4 and 5. Two matches are found (groups 3 and 5) when the message data bits are compared with the configured data mask (DM7).

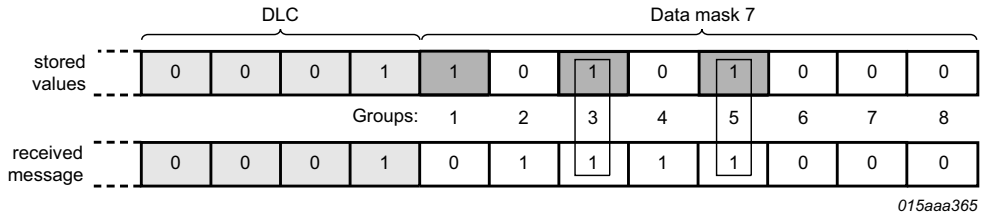


Fig 8. Evaluating the Data field in a selective wake-up frame

Optionally, the data length code and the data field can be excluded from the evaluation of the wake-up frame. If bit PNDM = 0, only the identifier field is evaluated to determine if the frame contains a valid wake-up message. If PNDM = 1 (the default value), the data field is included in the wake-up filtering.

When PNDM = 0, a valid wake-up message is detected and a wake-up event is captured (and CW is set to 1) when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

When PNDM = 1, a valid wake-up message is detected when:

- the identifier field in the received wake-up frame matches the pattern in the ID registers after filtering AND
- the frame is not a Remote frame AND

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

- the data length code in the received message matches the configured data length code (bits DLC) AND
- if the data length code is greater than 0, at least one bit in the data field of the received frame is set and the corresponding bit in the associated data mask register is also set AND
- the CRC field in the received frame (including a recessive CRC delimiter) was received without error

If the TJA1145A receives a CAN message containing errors (e.g. a 'stuffing' error) transmitted in advance of the ACK field, an internal error counter is incremented. If a CAN message is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the partial networking module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDE = 1) and the device wakes up; the counter is reset to zero when the bias is switched off and partial networking is re-enabled.

Partial networking is assumed to be configured correctly when PNCOK is set to 1 by the application software. The TJA1145A clears PNCOK after a write access to any of the CAN partial networking configuration registers (see Section 7.3.3).

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured correctly (PNCOK = 0), and the CAN transceiver is in Offline mode with wake-up enabled (CWE = 1), then any valid wake-up pattern (according to ISO 11898-2:2016) will trigger a wake-up event.

If the CAN transceiver is not in Offline mode (CMC $\neq$ 00) or CAN wake-up is disabled (CWE = 0), all wake-up patterns on the bus will be ignored.

CAN bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s and 1 Mbit/s are supported during selective wake-up. The bit rate is selected via bits CDR (see Table 9).

7.3.2 CAN FD frames

CAN FD stands for 'CAN with Flexible Data-Rate'. It is based on the CAN protocol as specified in ISO 11898-1:2015.

CAN FD is being gradually introduced into the automotive market. In time, all CAN controllers will be required to comply with the new standard (enabling 'FD-active' nodes) or at least to tolerate CAN FD communication (enabling 'FD-passive' nodes). The TJA1145Ax/FD variants support FD-passive features by means of a dedicated implementation of the partial networking protocol.

These variants can be configured to recognize CAN FD frames as valid frames. When CFDC = 1, the error counter is decremented every time the control field of a CAN FD frame is received. The TJA1145Ax/FD remains in low-power mode (CAN FD-passive) with partial networking enabled. CAN FD frames are never recognized as valid wake-up frames, even if PNDM = 0 and the frame contains a valid ID. After receiving the control field of a CAN FD frame, the TJA1145Ax/FD ignores further bus signals until idle is again detected.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

CAN FD passive is supported up to a ratio of one-to-eight between arbitration and data bit rates, without unwanted wake-ups. The CAN FD filter parameter defined in ISO 11898-2:2016 and SAE J2284 is supported up to a ratio of one-to-four, with a maximum supported bit data bit rate of 2 Mbit/s and a maximum arbitration speed of 500 kbit/s.

CAN FD frames are interpreted as frames with errors by the partial networking module in the TJA1145AT and TJA1145ATK, and in the TJA1145Ax/FD variants when CFDC = 0. So the error counter is incremented when a CAN FD frame is received. If the ratio of CAN FD frames to valid CAN frames exceeds the threshold that triggers error counter overflow, bit PNFDE is set to 1 and the device wakes up.

7.3.3 CAN partial networking configuration registers

Dedicated registers are provided for configuring CAN partial networking.

Table 9. Data rate register (address 26h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2:0	CDR	R/W		CAN data rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100	reserved (intended for future use; currently selects 500 kbit/s)
			101	500 kbit/s
			110	reserved (intended for future use; currently selects 500 kbit/s)
			111	1000 kbit/s

Table 10. ID registers 0 to 3 (addresses 27h to 2Ah)

Addr.	Bit	Symbol	Access	Value	Description
27h	7:0	ID7:ID0	R/W	-	bits ID7 to ID0 of the extended frame format
28h	7:0	ID15:ID08	R/W	-	bits ID15 to ID8 of the extended frame format
29h	7:2	ID23:ID18	R/W	-	bits ID23 to ID18 of the extended frame format bits ID5 to ID0 of the standard frame format
	1:0	ID17:ID16	R/W	-	bits ID17 to ID16 of the extended frame format
2Ah	7:5	reserved	R	-	
	4:0	ID28:ID24	R/W	-	bits ID28 to ID24 of the extended frame format bits ID10 to ID6 of the standard frame format

Table 11. ID mask registers 0 to 3 (addresses 2Bh to 2Eh)

Addr.	Bit	Symbol	Access	Value	Description
2Bh	7:0	M7:M0	R/W	-	ID mask bits 7 to 0 of extended frame format
2Ch	7:0	M15:M8	R/W	-	ID mask bits 15 to 8 of extended frame format

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 11. ID mask registers 0 to 3 (addresses 2Bh to 2Eh) *…continued*

Addr.	Bit	Symbol	Access	Value	Description
2Dh	7:2	M23:M18	R/W	-	ID mask bits 23 to 18 of extended frame format ID mask bits 5 to 0 of standard frame format
	1:0	M17:M16	R/W	-	ID mask bits 17 to 16 of extended frame format
2Eh	7:5	reserved	R	-	
	4:0	M28:M24	R/W	-	ID mask bits 28 to 24 of extended frame format ID mask. bits 10 to 6 of standard frame format

Table 12. Frame control register (address 2Fh)

Bit	Symbol	Access	Value	Description
7	IDE	R/W	-	identifier format:
			0	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W	-	partial networking data mask:
			0	data length code and data field are ‘don’t care’ for wake-up
			1	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	
3:0	DLC	R/W		number of data bytes expected in a CAN frame:
			0000	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	tolerated, 8 bytes expected

Table 13. Data mask registers (addresses 68h to 6Fh)

Addr.	Bit	Symbol	Access	Value	Description
68h	7:0	DM0	R/W	-	data mask 0 configuration
69h	7:0	DM1	R/W	-	data mask 1 configuration
6Ah	7:0	DM2	R/W	-	data mask 2 configuration
6Bh	7:0	DM3	R/W	-	data mask 3 configuration
6Ch	7:0	DM4	R/W	-	data mask 4 configuration
6Dh	7:0	DM5	R/W	-	data mask 5 configuration
6Eh	7:0	DM6	R/W	-	data mask 6 configuration
6Fh	7:0	DM7	R/W	-	data mask 7 configuration

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

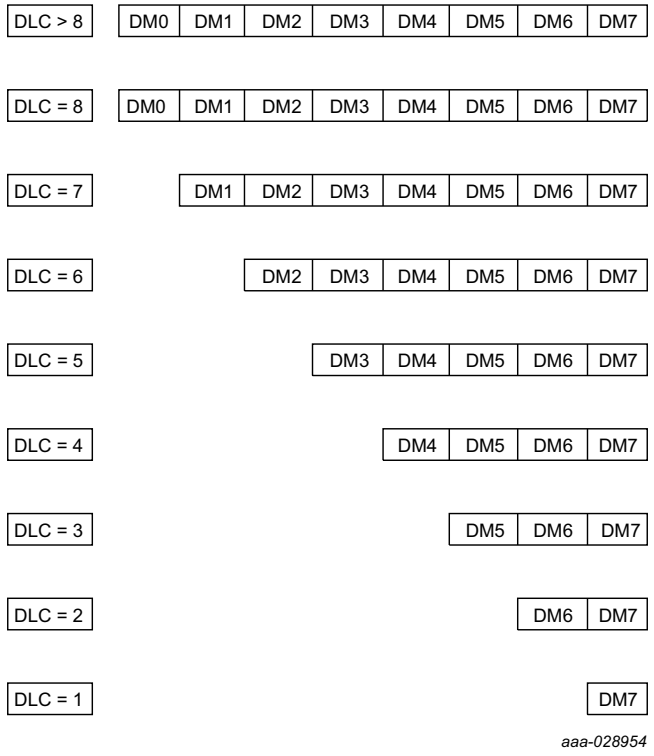


Fig 9. Data mask register usage for different values of DLC

7.4 Fail-safe features

7.4.1 TXD dominant time-out

A TXD dominant time-out timer is started when pin TXD is forced LOW while the transceiver is in Active Mode. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 15 kbit/s.

When the TXD dominant time-out time is exceeded, a CAN failure interrupt is generated (CF = 1; see Table 19), if enabled (CFE = 1; see Table 22). In addition, the status of the TXD dominant time-out can be read via the CFS bit in the Transceiver status register (Table 8) and bit CTS is set to 0.

7.4.2 Pull-up on TXD pin

Pin TXD has an internal pull-up towards V_{IO} to ensure a safe defined recessive driver state in case the pin is left floating.

7.4.3 V_{CC} undervoltage event

When CMC = 01 and the supply to the CAN transceiver (V_{CC}) falls below $V_{uvd(VCC)}$, a CAN failure event is captured (CF = 1), assuming CAN failure detection is enabled (CFE = 1), and status bit VCS is set to 1.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

7.4.4 Loss of power at pin BAT

A loss of power at pin BAT has no influence on the bus lines or on the microcontroller. No reverse currents will flow from the bus.

7.5 Local wake-up via WAKE pin

Local wake-up is enabled via bits WPRE and WPFE in the WAKE pin event capture enable register (see Table 23). A wake-up event is triggered by a LOW-to-HIGH (if WPRE = 1) and/or a HIGH-to-LOW (if WPFE = 1) transition on the WAKE pin. This arrangement allows for maximum flexibility when designing a local wake-up circuit. In applications that don't make use of the local wake-up facility, local wake-up should be disabled and the WAKE pin connected to GND to ensure optimal EMI performance.

Table 14. WAKE status register (address 4Bh)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPVS	R		WAKE pin status:
			0	voltage on WAKE pin below switching threshold ($V_{th(sw)}$)
			1	voltage on WAKE pin above switching threshold ($V_{th(sw)}$)
0	reserved	R	-	

While the TJA1145A is in Normal mode, the status of the voltage on pin WAKE can always be read via bit WPVS. Otherwise, WPVS is only valid if local wake-up is enabled (WPRE = 1 and/or WPFE = 1).

7.6 Wake-up and interrupt event diagnosis via pin RXD

Wake-up and interrupt event diagnosis in the TJA1145A is intended to provide the microcontroller with information on the status of a range of features and functions. This information is stored in the event status registers (Table 18 to Table 20) and is signaled on pin RXD pin, if enabled.

A distinction is made between regular wake-up events and interrupt events (at least one regular wake-up source must be enabled to allow the TJA1145A to switch to Sleep mode; see Section 7.1.1.3).

Table 15. Regular wake-up events

Symbol	Event	Power-on	Description
CW	CAN wake-up	disabled	a CAN wake-up event was detected while the transceiver was in CAN Offline mode.
WPR	rising edge on WAKE pin	disabled	a rising-edge wake-up was detected on pin WAKE
WPF	falling edge on WAKE pin	disabled	a falling-edge wake-up was detected on pin WAKE

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 16. Interrupt events

Symbol	Event	Power-on	Description
PO	power-on	always enabled	the TJA1145A has exited Off mode (after battery power has been restored/connected)
OTW	overtemperature warning	disabled	the IC temperature has exceeded the overtemperature warning threshold (only detected in Normal mode)
SPIF	SPI failure	disabled	SPI clock count error (only 16-, 24- and 32-bit commands are valid), illegal MC code or attempted write access to locked register (an SPI failure event will not wake-up the TJA1145A from Sleep mode)
PNFDE	PN frame detection error	always enabled	partial networking frame detection error
CBS	CAN bus silence	disabled	no activity on CAN bus for $t_{to(silence)}$ (detected only when CBSE = 1 while bus active)
CF	CAN failure	disabled	one of the following CAN failure events detected (not is Sleep mode): - CAN transceiver deactivated due to a dominant clamped TXD - CAN transceiver deactivated due to a V_{CC} undervoltage event (if CMC = 01)

PO and PNFDE interrupts are always captured. Wake-up and interrupt detection can be enabled/disabled for the remaining events individually via the event capture enable registers (Table 21 to Table 23).

If an event occurs while the associated event capture function is enabled, the relevant event status bit is set. If the transceiver is in CAN Offline mode, pin RXD is forced LOW to indicate that a wake-up or interrupt event has been detected. If the TJA1145A is in Sleep mode when an event (other than a SPIF interrupt) occurs, pin INH is forced HIGH and the TJA1145A switches to Standby mode. If the TJA1145A is in Standby mode when the event occurs, pin RXD is forced LOW to flag an interrupt/wake-up event. The detection of any enabled wake-up or interrupt event will trigger a wake-up in Standby mode. The detection of any enabled wake-up or interrupt event other than a SPIF interrupt will trigger a wake-up in Sleep mode.

The microcontroller can monitor events via the event status registers. An extra status register, the Global event status register (Table 17), is provided to help speed up software polling routines. By polling the Global event status register, the microcontroller can quickly determine the type of event captured (system, transceiver or WAKE) and then query the relevant table (Table 18, Table 19 or Table 20 respectively).

After the event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant bit (writing 0 will have no effect). A number of status bits can be cleared in a single write operation by writing 1 to all relevant bits.

It is strongly recommended to clear only the status bits that were set to 1 when the status registers were last read. This precaution ensures that events triggered just before the write access are not lost.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

7.6.1 Interrupt/wake-up delay

If interrupt or wake-up events occur very frequently while the transceiver is in CAN Offline mode, they can have a significant impact on the software processing time (because pin RXD is repeatedly driven LOW, requiring a response from the microcontroller each time an interrupt/wake-up is generated). The TJA1145A incorporates an interrupt/wake-up delay timer to limit the disturbance to the software.

When one of the event capture status bits is cleared, pin RXD is released (HIGH) and a timer is started. If further events occur while the timer is running, the relevant status bits are set. If one or more events are pending when the timer expires after $t_{d(event)}$, pin RXD goes LOW again to alert the microcontroller.

In this way, the microcontroller is interrupted once to process a number of events rather than several times to process individual events. If all active event capture bits have been cleared (by the microcontroller) when the timer expires after $t_{d(event)}$, pin RXD remains HIGH (since there are no pending events). The event capture registers can be read at any time.

7.6.2 Sleep mode protection

It is very important that event detection is configured correctly when the TJA1145A switches to Sleep mode to ensure it will respond to a wake-up event. For this reason, and to avoid potential system deadlocks, at least one regular wake-up event must be enabled and all event status bits must be cleared before the TJA1145A switches to Sleep mode. Otherwise the TJA1145A will switch to Standby mode in response to a go-to-sleep command (MC = 001).

7.6.3 Event status and event capture registers

After an event source has been identified, the status flag should be cleared (set to 0) by writing 1 to the relevant status bit (writing 0 will have no effect).

Table 17. Global event status register (address 60h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	
3	WPE	R		WAKE pin event:
			0	no pending WAKE pin event
			1	WAKE pin event pending at address 0x64
2	TRXE	R		transceiver event:
			0	no pending transceiver event
			1	transceiver event pending at address 0x63
1	reserved	R	-	
0	SYSE	R		system event:
			0	no pending system event
			1	system event pending at address 0x61

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 18. System event status register (address 61h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	PO[1]	R/W		power-on:
			0	no recent battery power-on
			1	the TJA1145A has left Off mode after battery power-on
3	reserved	R	-	
2	OTW	R/W		overtemperature warning:
			0	overtemperature not detected
			1	the global chip temperature has exceeded the overtemperature warning threshold ($T_{th(warn)otp}$)
1	SPIF	R/W		SPI failure:
			0	no SPI failure detected
			1	SPI failure detected
0	reserved	R	-	

[1] PO is cleared when the TJA1145A is forced to Sleep mode due to an undervoltage event. The information stored in PO could be lost if the transition to Sleep mode was forced by an undervoltage event. Bit NMS, which is set to 0 when the TJA1145A switches to Normal mode after power-on, compensates for this.

Table 19. Transceiver event status register (address 63h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	
5	PNFDE	R/W		partial networking frame detection error:
			0	no partial networking frame detection error detected
			1	partial networking frame detection error detected
4	CBS	R/W		CAN-bus status:
			0	CAN-bus active
			1	no activity on CAN-bus for $t_{to(silence)}$
3:2	reserved	R	-	
1	CF[1]	R/W		CAN failure:
			0	no CAN failure detected
			1	CAN failure event detected
0	CW	R/W		CAN wake-up:
			0	no CAN wake-up event detected
			1	CAN wake-up event detected

[1] CF is only enabled in Normal mode while the transceiver is in CAN Active mode and is triggered if TXD is clamped dominant OR a V_{CC} undervoltage is detected (when CMC = 01).

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 20. WAKE pin event status register (address 64h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPR	R/W		WAKE pin rising edge:
			0	no rising edge detected on WAKE pin
			1	rising edge detected on WAKE pin
0	WPF	R/W		WAKE pin falling edge:
			0	no falling edge detected on WAKE pin
			1	falling edge detected on WAKE pin

Table 21. System event capture enable register (address 04h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	
2	OTWE	R/W		overtemperature warning enable:
			0	overtemperature warning disabled
			1	overtemperature warning enabled
1	SPIFE	R/W		SPI failure enable:
			0	SPI failure detection disabled
			1	SPI failure detection enabled
0	reserved	R	-	

Table 22. Transceiver event capture enable register (address 23h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	
4	CBSE	R/W		CAN-bus silence enable:
			0	CAN-bus silence detection disabled
			1	CAN-bus silence detection enabled
3:2	reserved	R	-	
1	CFE	R/W		CAN failure enable:
			0	CAN failure detection disabled
			1	CAN failure detection enabled
0	CWE	R/W		CAN wake-up enable:
			0	CAN wake-up detection disabled
			1	CAN wake-up detection enabled

Table 23. WAKE pin event capture enable register (address 4Ch)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	
1	WPRE	R/W		WAKE pin rising-edge enable:
			0	rising-edge detection on WAKE pin disabled
			1	rising-edge detection on WAKE pin enabled

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 23. WAKE pin event capture enable register (address 4Ch) *…continued*

Bit	Symbol	Access	Value	Description
0	WPFE	R/W		WAKE pin falling-edge enable:
			0	falling-edge detection on WAKE pin disabled
			1	falling-edge detection on WAKE pin enabled

7.7 Device ID

A byte is reserved at address 0x7E for a TJA1145A identification code.

Table 24. Identification register (address 7Eh)

Bit	Symbol	Access	Value	Description
7:0	IDS[7:0]	R		device identification code
			70h	TJA1145AT, TJA1145ATK
			74h	TJA1145AT/FD, TJA1145ATK/FD

7.8 Lock control register

Sections of the register address area can be write-protected to protect against unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the TJA1145A updating status registers etc.

Table 25. Lock control register (address 0Ah)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	cleared for future use
6	LK6C	R/W		lock control 6: address area 0x68 to 0x6F - partial networking data byte registers
			0	SPI write-access enabled
			1	SPI write-access disabled
5	LK5C	R/W		lock control 5: address area 0x50 to 0x5F
			0	SPI write-access enabled
			1	SPI write-access disabled
4	LK4C	R/W		lock control 4: address area 0x40 to 0x4F - WAKE pin configuration
			0	SPI write-access enabled
			1	SPI write-access disabled
3	LK3C	R/W		lock control 3: address area 0x30 to 0x3F
			0	SPI write-access enabled
			1	SPI write-access disabled
2	LK2C	R/W		lock control 2: address area 0x20 to 0x2F - transceiver control and partial networking
			0	SPI write-access enabled
			1	SPI write-access disabled
1	LK1C	R/W		lock control 1: address area 0x10 to 0x1F
			0	SPI write-access enabled
			1	SPI write-access disabled

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 25. Lock control register (address 0Ah) *…continued*

Bit	Symbol	Access	Value	Description
0	LK0C	R/W		lock control 0: address area 0x06 to 0x09 - general purpose memory
			0	SPI write-access enabled
			1	SPI write-access disabled

7.9 General-purpose memory

TJA1145A allocates 4 bytes of memory for general-purpose registers used to store user information. The general purpose registers can be accessed via the SPI at address 0x06 to 0x09 (see Table 26).

7.10 VIO supply pin

Pin VIO should be connected to the microcontroller supply voltage. This will cause the signal levels of the TXD, RXD and the SPI interface pins to be adjusted to the I/O levels of the microcontroller, enabling direct interfacing without the need for glue logic.

7.11 V_{CC}/V_{IO} undervoltage protection

If an undervoltage is detected on pins VCC or VIO, and it remains valid for longer than the undervoltage detection delay time, $t_{d(uvd)}$, the TJA1145A is forced to Sleep mode (see Figure 4). A number of preventative measures are taken when the TJA1145A is forced to Sleep mode to avoid deadlock and unpredictable states:

- All previously captured events (address range 0x61 to 0x64) are cleared before the TJA1145A switches to Sleep Mode to avoid repeated attempts to wake up while an undervoltage is present.
- Both CAN wake-up (CWE = 1) and local wake-up via the WAKE pin (WPFE = WPRE = 1) are enabled in order to avoid a deadlock situation where the TJA1145A cannot be woken up after entering Sleep mode.
- Partial Networking is disabled (CPNC = 0) to ensure immediate wake-up in response to bus traffic after the TJA1145A has recovered from an undervoltage event.
- The Partial Networking Configuration bit is cleared (CPNOK = 0) to indicate that partial networking might not have been configured correctly when the TJA1145A switched to Sleep mode.

Status bit FSMS is set to 1 when a transition to Sleep mode is forced by an undervoltage event (see Table 6). This bit can be sampled after the TJA1145A wakes up from Sleep mode to allow the settings of CWE, WPFE, WPRE and CPNC to be re-adjusted if an undervoltage event forced the transition to Sleep mode (FSMS = 1).

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

7.12 SPI

7.12.1 Introduction

The Serial Peripheral Interface (SPI) provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select; active LOW; default level is HIGH (pull-up)
- SCK: SPI clock; default level is LOW due to internal pull-down
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH (may need external pull-up or pull-down if not available in the host controller)

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in Figure 10.

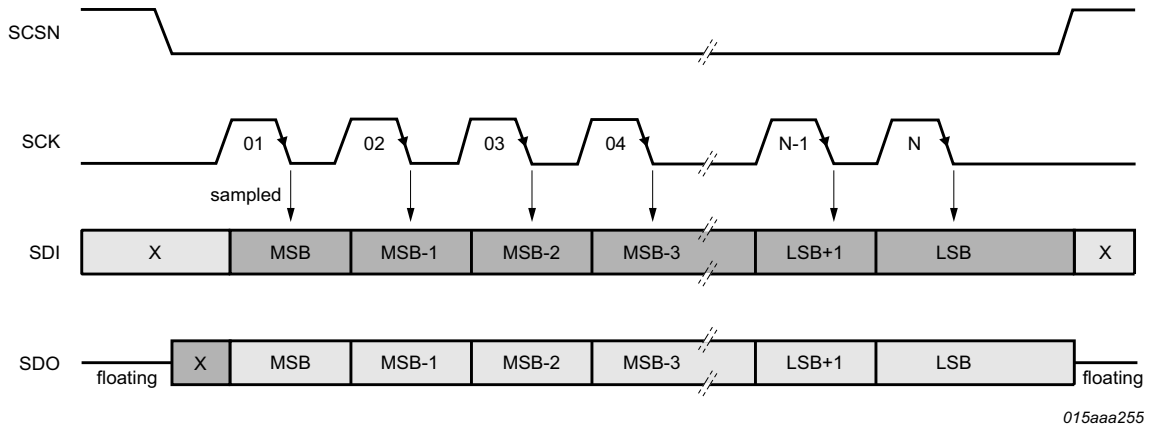


Fig 10. SPI timing protocol

The SPI data in the TJA1145A is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 7-bit address. Two bytes (16 bits) must be transmitted to the TJA1145A for a single register read or write operation. The first byte contains the 7-bit address along with a ‘read-only’ bit (the LSB). The read-only bit must be 0 to indicate a write operation (if this bit is 1, a read operation is assumed and any data on the SDI pin is ignored). The second byte contains the data to be written to the register.

24- and 32-bit read and write operations are also supported. The register address is automatically incremented, once for a 24-bit operation and twice for a 32-bit operation, as illustrated in Figure 11.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

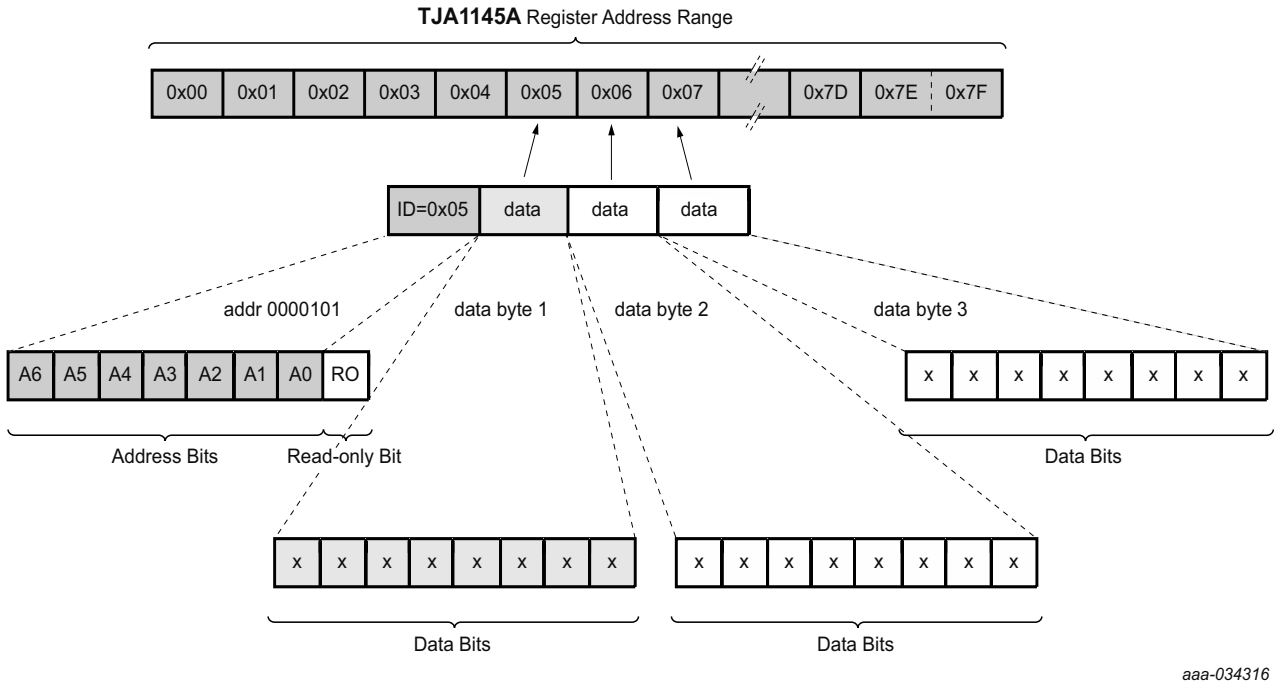


Fig 11. SPI data structure for a write operation (16-, 24- or 32-bit)

During an SPI data read or write operation, the contents of the addressed register(s) is returned via pin SDO.

The TJA1145A tolerates attempts to write to registers that don't exist. If the available address space is exceeded during a write operation, the data above the valid address range is ignored (without generating an SPI failure event).

During a write operation, the TJA1145A monitors the number of SPI bits transmitted. If the number recorded is not 16, 24 or 32, then the write operation is aborted and an SPI failure event is captured (SPIF = 1).

If more than 32 bits are clocked in on pin SDI during a read operation, the data stream on SDI is reflected on SDO from bit 33 onwards.

7.12.2 Register map

The addressable register space contains 128 registers with addresses from 0x00 to 0x7F. An overview of the register mapping is provided in Table 26 to Table 30. The functionality of the individual bits is discussed in more detail in relevant sections of the data sheet.

Table 26. Overview of primary control registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x01	Mode control	reserved					MC		
0x03	Main status	FSMS	OTWS	NMS	reserved				
0x04	System event enable	reserved					OTWE	SPIFE	reserved
0x06	Memory 0	GPM[7:0]							

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 26. Overview of primary control registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x07	Memory 1	GPM[15:8]							
0x08	Memory 2	GPM[23:16]							
0x09	Memory 3	GPM[31:24]							
0x0A	Lock control	reserved	LK6C	LK5C	LK4C	LK3C	LK2C	LK1C	LK0C

Table 27. Overview of transceiver control and partial networking registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x20	CAN control	reserved	CFDC	PNCOK	CPNC	reserved		CMC	
0x22	Transceiver status	CTS	CPNERR	CPNS	COSCS	CBSS	reserved	VCS	CFS
0x23	Transceiver event enable	reserved			CBSE	reserved		CFE	CWE
0x26	Data rate	reserved					CDR		
0x27	Identifier 0	ID[7:0]							
0x28	Identifier 1	ID[15:8]							
0x29	Identifier 2	ID[23:16]							
0x2A	Identifier 3	reserved			ID[28:24]				
0x2B	Mask 0	M[7:0]							
0x2C	Mask 1	M[15:8]							
0x2D	Mask 2	M[23:16]							
0x2E	Mask 3	reserved			M[28:24]				
0x2F	Frame control	IDE	PNDM	reserved		DLC			
0x68	Data mask 0	DM0[7:0]							
0x69	Data mask 1	DM1[7:0]							
0x6A	Data mask 2	DM2[7:0]							
0x6B	Data mask 3	DM3[7:0]							
0x6C	Data mask 4	DM4[7:0]							
0x6D	Data mask 5	DM5[7:0]							
0x6E	Data mask 6	DM6[7:0]							
0x6F	Data mask 7	DM7[7:0]							

Table 28. Overview of WAKE pin control and status registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x4B	WAKE pin status	reserved						WPVS	reserved
0x4C	WAKE pin enable	reserved						WPRE	WPFE

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 29. Overview of Event Capture registers

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x60	Event capture status	reserved				WPE	TRXE	reserved	SYSE
0x61	System event status	reserved			PO	reserved	OTW	SPIF	reserved
0x63	Transceiver event status	reserved		PNFDE	CBS	reserved		CF	CW
0x64	WAKE pin event status	reserved						WPR	WPF

Table 30. Overview of Identification register

Address	Register Name	Bit:							
		7	6	5	4	3	2	1	0
0x7E	Identification	IDS[7:0]							

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

7.12.3 Register configuration in TJA1145A operating modes

A number of register bits may change state automatically when the TJA1145A switches from one operating mode to another. This is particularly evident when the TJA1145A switches to Off mode or when an undervoltage event forces a transition to Sleep mode. These changes are summarized in Table 31. If an SPI transmission is in progress when the TJA1145A changes state, the transmission is ignored (automatic state changes have priority).

Table 31. Register bit settings in TJA1145A operating modes

Symbol	Off (reset values)	Standby	Normal	Sleep	Overtemp	Forced Sleep (uv)
CBS	0	no change	no change	no change	no change	0
CBSE	0	no change	no change	no change	no change	no change
CBSS	1	actual state	actual state	actual state	actual state	actual state
CDR	101	no change	no change	no change	no change	no change
CF	0	no change	no change	no change	no change	0
CFDC	0	no change	no change	no change	no change	no change
CFE	0	no change	no change	no change	no change	no change
CFS	0	actual state	actual state	actual state	actual state	actual state
CMC	01	no change	no change	no change	no change	no change
COSCS	0	actual state	actual state	actual state	actual state	actual state
CPNC	0	no change	no change	no change	no change	0
CPNERR	1	actual state	actual state	actual state	actual state	actual state
CPNS	0	actual state	actual state	actual state	actual state	actual state
CTS	0	0	actual state	0	0	0
CW	0	no change	no change	no change	no change	0
CWE	0	no change	no change	no change	no change	1
DMn	11111111	no change	no change	no change	no change	no change
DLC	0000	no change	no change	no change	no change	no change
FSMS	0	no change	no change	0	no change	1
GPMn	00000000	no change	no change	no change	no change	no change
IDn	00000000	no change	no change	no change	no change	no change
IDE	0	no change	no change	no change	no change	no change
IDS	01110000 (AT, ATK) 01110100 (AT/FD, ATK/FD)	no change	no change	no change	no change	no change
LKnC	0	no change	no change	no change	no change	no change
Mn	00000000	no change	no change	no change	no change	no change
MC	100	100	111	001	don’t care	001
NMS	1	no change	0	no change	no change	no change
OTW	0	no change	no change	no change	no change	0
OTWE	0	no change	no change	no change	no change	no change
OTWS	0	actual state	actual state	actual state	actual state	actual state
PNCOK	0	no change	no change	no change	no change	0
PNDM	1	no change	no change	no change	no change	no change
PNFDE	0	no change	no change	no change	no change	0

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 31. Register bit settings in TJA1145A operating modes *…continued*

Symbol	Off (reset values)	Standby	Normal	Sleep	Overtemp	Forced Sleep (uv)
PO	1	no change	no change	no change	no change	0
SPIF	0	no change	no change	no change	no change	0
SPIFE	0	no change	no change	no change	no change	no change
SYSE	1	no change	no change	no change	no change	0
TRXE	0	no change	no change	no change	no change	0
VCS	0	actual state	actual state	actual state	actual state	actual state
WPE	0	no change	no change	no change	no change	0
WPF	0	no change	no change	no change	no change	0
WPFE	0	no change	no change	no change	no change	1
WPR	0	no change	no change	no change	no change	0
WPRE	0	no change	no change	no change	no change	1
WPVS	0	no change	no change	no change	no change	no change

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

8. Limiting values

Table 32. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	pins VCC, VIO [2]	−0.2	+6	V
		pins TXD, RXD, SDI, SDO, SCK, SCSN [3]	−0.2	V_{IO} + 0.2	V
		pins WAKE, INH	−18	+40	V
		pin BAT	−0.2	+40	V
		pins CANH and CANL with respect to any other pin	−58	+58	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		−40	+40	V
V_{trt}	transient voltage	on pins CANL, CANH, WAKE, BAT [4]			
		pulse 1	−100	-	V
		pulse 2a	-	75	V
		pulse 3a	−150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω) discharge circuit [5]			
		on pins CANH and CANL; pin BAT with capacitor; pin WAKE with 10 nF capacitor and 10 kΩ resistor	−6	+6	kV
		Human Body Model (HBM)			
		on any pin [6]	−2	+2	kV
		on pins BAT, WAKE [7]	−4	+4	kV
		on pins CANH, CANL [8]	−8	+8	kV
		Machine Model (MM) [9]			
		on any pin	−100	+100	V
		Charged Device Model (CDM) [10]			
		on corner pins	−750	+750	V
		on any other pin	−500	+500	V
T_{vj}	virtual junction temperature	[11]	−40	+150	°C
T_{stg}	storage temperature		−55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] When the device is not powered up, $I_{VCC(max)}$ = 25 mA.

[3] Maximum voltage should never exceed 6 V.

[4] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2.

[5] Verified by an external test house according to IEC TS 62228, Section 4.3.

[6] According to AEC-Q100-002.

[7] Pins stressed to reference group containing all grounds, emulating the application circuit (Figure 15). HBM pulse as specified in AEC-Q100-002 used.

[8] Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 15). HBM pulse as specified in AEC-Q100-002 used.

[9] According to AEC-Q100-003.

[10] According to AEC-Q100-011.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

[11] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9. Thermal characteristics

Table 33. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(vj-a)}$	thermal resistance from virtual junction to ambient	SO14 [1]	106	K/W
		HVSON14	60	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

10. Static characteristics

Table 34. Static characteristics

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; V_{CC} = 4.5 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin BAT						
$V_{th(det)pon}$	power-on detection threshold voltage	V_{BAT} rising	4.2	-	4.55	V
$V_{th(det)poff}$	power-off detection threshold voltage	V_{BAT} falling	2.8	-	3	V
$V_{uvr(CAN)}$	CAN undervoltage recovery voltage	V_{BAT} rising	4.5	-	5	V
$V_{uvd(CAN)}$	CAN undervoltage detection voltage	V_{BAT} falling	4.2	-	4.55	V
I_{BAT}	battery supply current	Normal mode; MC = 111	-	1	1.5	mA
		Sleep mode; MC = 001; CWE = 1; CAN Offline mode; −40 °C < T_{vj} < 85 °C; V_{BAT} = 7 V to 18 V	-	48	64	µA
		Standby mode; MC = 100; CWE = 1; CAN Offline mode; −40 °C < T_{vj} < 85 °C; V_{BAT} = 7 V to 18 V	-	56	73	µA
		additional current in CAN Offline Bias mode; −40 °C < T_{vj} < 85 °C	-	46	63	µA
		additional current in CAN Offline Bias mode with active partial networking decoder; Standby or Sleep mode; −40 °C < T_{vj} < 85 °C [2]		0.4	0.65	mA
		additional current from WAKE input; WPRE = WPFE = 1; −40 °C < T_{vj} < 85 °C		2	3	µA
Supply; pin VCC						
$V_{uvd(VCC)}$	undervoltage detection voltage on pin VCC		4.5	-	4.75	V
I_{CC}	supply current	CAN Active mode; CAN recessive; V_{TXD} = V_{IO}	-	3	6	mA
		CAN Active mode; CAN dominant; V_{TXD} = 0 V	-	45	65	mA
		Standby/Normal mode; CAN inactive; −40 °C < T_{vj} < 85 °C	-	4.7	8.5	µA
		Sleep mode; CAN inactive; −40 °C < T_{vj} < 85 °C	-	3.8	7	µA
		short circuit on bus lines; CAN dominant; V_{TXD} = 0 V; −3 V < (V_{CANH} = V_{CANL}) < +18 V	-	55	65	mA

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 34. Static characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; V_{CC} = 4.5 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin VIO						
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO	V_{BAT} > 4.5 V	2.7	-	2.85	V
I_{IO}	supply current on pin V_{IO}	Standby/Normal mode; −40 °C < T_{vj} < 85 °C	-	7.1	11	µA
		Sleep mode; −40 °C < T_{vj} < 85 °C	-	5	8	µA
Serial peripheral interface inputs; pins SDI, SCK and SCSN						
$V_{th(sw)}$	switching threshold voltage	V_{IO} = 2.97 V to 5.5 V	0.25V_{IO}	-	0.75V_{IO}	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis	V_{IO} = 2.97 V to 5.5 V	0.05V_{IO}	-	-	V
$R_{pd(SCK)}$	pull-down resistance on pin SCK		40	60	80	kΩ
$R_{pu(SCSN)}$	pull-up resistance on pin SCSN		40	60	80	kΩ
$R_{pd(SDI)}$	pull-down resistance on pin SDI	V_{SDI} < $V_{th(sw)}$	40	60	80	kΩ
$R_{pu(SDI)}$	pull-up resistance on pin SDI	V_{SDI} > $V_{th(sw)}$	40	60	80	kΩ
Serial peripheral interface data output; pin SDO						
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	V_{IO} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
$I_{LO(off)}$	off-state output leakage current	V_{SCSN} = V_{IO}; V_O = 0 V to V_{IO}	−5	-	+5	µA
Inhibit output: pin INH						
V_O	output voltage	I_{INH} = −180 µA	V_{BAT} − 0.8	-	V_{BAT}	V
R_{pd}	pull-down resistance	Sleep mode	3	4	5	MΩ
CAN transmit data input; pin TXD						
$V_{th(sw)}$	switching threshold voltage	V_{IO} = 2.97 V to 5.5 V	0.25V_{IO}	-	0.75V_{IO}	V
$V_{th(sw)hys}$	switching threshold voltage hysteresis	V_{IO} = 2.97 V to 5.5 V	0.05V_{IO}	-	-	V
R_{pu}	pull-up resistance		40	60	80	kΩ
CAN receive data output; pin RXD						
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	V_{IO} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
R_{pu}	pull-up resistance	CAN Offline mode	40	60	80	kΩ
Local wake input; pin WAKE						
$V_{th(sw)r}$	rising switching threshold voltage		2.8	-	4.1	V
$V_{th(sw)f}$	falling switching threshold voltage		2.4	-	3.75	V
$V_{hys(i)}$	input hysteresis voltage		250	-	800	mV
I_i	input current	T_{vj} = −40 °C to +85 °C	-	-	1.5	µA

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 34. Static characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; V_{CC} = 4.5 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High-speed CAN bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	CAN Active mode; V_{TXD} = 0 V; $t < t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{CC} − V_{CANH} − V_{CANL}; V_{CC} = 5 V	−400	-	+400	mV
V_{TXsym}	transmitter voltage symmetry	V_{TXsym} = V_{CANH} + V_{CANL}; [2] f_{TXD} = 250 kHz, 1 MHz or 2.5 MHz; [3] V_{CC} = 4.75 V to 5.25 V; C_{SPLIT} = 4.7 nF	0.9V_{CC}	-	1.1V_{CC}	V
$V_{O(dif)}$	differential output voltage	CAN Active mode (dominant); V_{TXD} = 0 V; V_{CC} = 4.75 V to 5.5 V; $t < t_{to(dom)TXD}$				
		R_L = 45 Ω to 70 Ω	1.5	-	3	V
		R_L = 2240 Ω	1.5	-	5	V
		recessive; R_L = no load				
		CAN Active/Listen-only/Offline Bias mode; V_{TXD} = V_{IO}	−50	-	+50	mV
		CAN Offline mode	−0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	CAN Active mode; V_{TXD} = V_{IO}; R_L = no load	2	0.5V_{CC}	3	V
		CAN Offline mode; R_L = no load	−0.1	-	+0.1	V
		CAN Offline Bias/Listen-only modes; R_L = no load; V_{CC} = 0 V	2	2.5	3	V
$I_{O(sc)dom}$	dominant short-circuit output current	CAN Active mode; V_{TXD} = 0 V; V_{CC} = 5 V				
		pin CANH; V_{CANH} = −15 V to +27 V	−55	-	-	mA
		pin CANL; V_{CANL} = −15 V to +27 V	-	-	+55	mA
$I_{O(sc)rec}$	recessive short-circuit output current	V_{CANL} = V_{CANH} = −27 V to +32 V; V_{TXD} = V_{IO}	−3	-	+3	mA
$V_{th(RX)dif}$	differential receiver threshold voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		CAN Active/Listen-only modes	0.5	0.7	0.9	V
		CAN Offline mode	0.4	0.7	1.15	V
$V_{rec(RX)}$	receiver recessive voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		CAN Active/Listen-only modes	−4[2]	-	0.5	V
		CAN Offline mode	−4[2]	-	0.4	V

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 34. Static characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; V_{CC} = 4.5 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{dom(RX)}$	receiver dominant voltage	−12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V				
		CAN Active/Listen-only modes	0.9	-	9.0[2]	V
		CAN Offline mode	1.15	-	9.0[2]	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	CAN Active/Listen-only modes; −12 V ≤ V_{CANL} ≤ +12 V; −12 V ≤ V_{CANH} ≤ +12 V	1	30	60	mV
R_i	input resistance	−2 V ≤ V_{CANL} ≤ +7 V; −2 V ≤ V_{CANH} ≤ +7 V	9	15	28	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V	−1	-	+1	%
$R_{i(dif)}$	differential input resistance	−2 V ≤ V_{CANL} ≤ +7 V; −2 V ≤ V_{CANH} ≤ +7 V	19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	[2]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[2]	-	-	10	pF
I_L	leakage current	V_{BAT} = V_{CC} = 0 V or V_{BAT} = V_{CC} = shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} = 5 V	−5	-	+5	µA
Temperature protection						
$T_{th(act)otp}$	overtemperature protection activation threshold temperature		167	177	187	°C
$T_{th(rel)otp}$	overtemperature protection release threshold temperature		127	137	147	°C
$T_{th(warn)otp}$	overtemperature protection warning threshold temperature		127	137	147	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Not tested in production; guaranteed by design.

[3] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 17.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

11. Dynamic characteristics

Table 35. Dynamic characteristics

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; V_{CC} = 4.5 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage sources; pins BAT, VCC and VIO						
$t_{startup}$	start-up time	from V_{BAT} exceeding the power-on detection threshold until INH active	-	2.8	4.7	ms
$t_{d(uvd)}$	undervoltage detection delay time		6	-	54	µs
$t_{d(uvd-sleep)}$	delay time from undervoltage detection to sleep mode	from undervoltage detection on VCC and/or VIO until TJA1145A forced to Sleep mode	180	-	440	ms
Serial peripheral interface timing; pins SCSN, SCK, SDI and SDO; see Figure 14						
$t_{cy(clk)}$	clock cycle time	Normal/Standby modes	250	-	-	ns
		Sleep mode	1	-	-	µs
$t_{SPILEAD}$	SPI enable lead time	Normal/Standby modes	50	-	-	ns
		Sleep mode	200	-	-	ns
t_{SPILAG}	SPI enable lag time	Normal/Standby modes	50	-	-	ns
		Sleep mode	200	-	-	ns
$t_{clk(H)}$	clock HIGH time	Normal/Standby modes	100	-	-	ns
		Sleep mode	475	-	-	ns
$t_{clk(L)}$	clock LOW time	Normal/Standby modes	100	-	-	ns
		Sleep mode	475	-	-	ns
$t_{su(D)}$	data input set-up time	Normal/Standby modes	50	-	-	ns
		Sleep mode	200	-	-	ns
$t_{h(D)}$	data input hold time	Normal/Standby modes	50	-	-	ns
		Sleep mode	200	-	-	ns
$t_{v(Q)}$	data output valid time	pin SDO; C_L = 20 pF; Normal/Standby modes	-	-	50	ns
		pin SDO; C_L = 20 pF; Sleep mode	-	-	200	ns
$t_{d(SDI-SDO)}$	SDI to SDO delay time	SPI address bits and read-only bit; C_L = 20 pF	-	-	50	ns
$t_{WH(S)}$	chip select pulse width HIGH	pin SCSN; Normal/Standby modes	250	-	-	ns
		pin SCSN; Sleep mode	1	-	-	µs
$t_{d(SCKL-SCSNL)}$	delay time from SCK LOW to SCSN LOW		50	-	-	ns
CAN transceiver timing; pins CANH, CANL, TXD and RXD						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	[2]	-	80	-	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	[2]	-	80	-	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	[2]	-	105	-	ns

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 35. Dynamic characteristics *…continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; V_{CC} = 4.5 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	[2]	-	120	-	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	$t_{bit(TXD)}$ = 200 ns [3]	-	-	255	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	$t_{bit(TXD)}$ = 200 ns [3]	-	-	255	ns
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns [3]	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns [3]	155	-	210	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns [3]	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns [3]	120	-	220	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	−65	-	+40	ns
		$t_{bit(TXD)}$ = 200 ns	−45	-	+15	ns
$t_{wake(busdom)}$	bus dominant wake-up time	first pulse (after first recessive) for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	1.8	µs
		second pulse for wake-up on pins CANH and CANL	0.5	-	1.8	µs
$t_{wake(busrec)}$	bus recessive wake-up time	first pulse for wake-up on pins CANH and CANL; CAN Offline mode	0.5	-	1.8	µs
		second pulse (after first dominant) for wake-up on pins CANH and CANL	0.5	-	1.8	µs
$t_{to(wake)bus}$	bus wake-up time-out time	between first and second dominant pulses; CAN Offline mode	0.8	-	10	ms
$t_{to(dom)TXD}$	TXD dominant time-out time	CAN Active mode; V_{TXD} = 0 V	2.7	-	3.3	ms
$t_{to(silence)}$	bus silence time-out time	recessive time measurement started in all CAN modes	0.95	-	1.17	s
$t_{d(busact-bias)}$	delay time from bus active to bias		-	-	200	µs
$t_{startup(CAN)}$	CAN start-up time	when switching to Active mode (CTS = 1)	-	-	220	µs
CAN partial networking						
$N_{bit(idle)}$	number of idle bits	before a new SOF is accepted; CFDC = 1 [4]	6	-	10	-
$t_{fltr(bit)dom}$	dominant bit filter time	arbitration data rate ≤ 500 kbit/s; CFDC = 1 [4] [5]	5	-	17.5	%
Pin RXD: interrupt/wake-up event timing (valid in CAN Offline mode only)						
$t_{d(event)}$	event capture delay time	CAN Offline mode	0.9	-	1.1	ms
t_{blank}	blanking time	when switching from Offline to Active/Listen-only mode	-	-	25	µs

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 35. Dynamic characteristics *...continued*

T_{vj} = −40 °C to +150 °C; V_{BAT} = 4.5 V to 28 V; V_{IO} = 2.85 V to 5.5 V; V_{CC} = 4.5 V to 5.5 V; R_L = $R_{(CANH-CANL)}$ = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; typical values are given at V_{BAT} = 13 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin WAKE						
t_{wake}	wake-up time		50	-	-	µs
Pin INH						
$t_{d(buswake-INHH)}$	delay time from bus wake-up to INH HIGH		-	-	100	µs

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] See Figure 12 and Figure 16.

[3] See Figure 13 and Figure 16.

[4] Not tested in production; guaranteed by design.

[5] Up to 2 Mbit/s data speed.

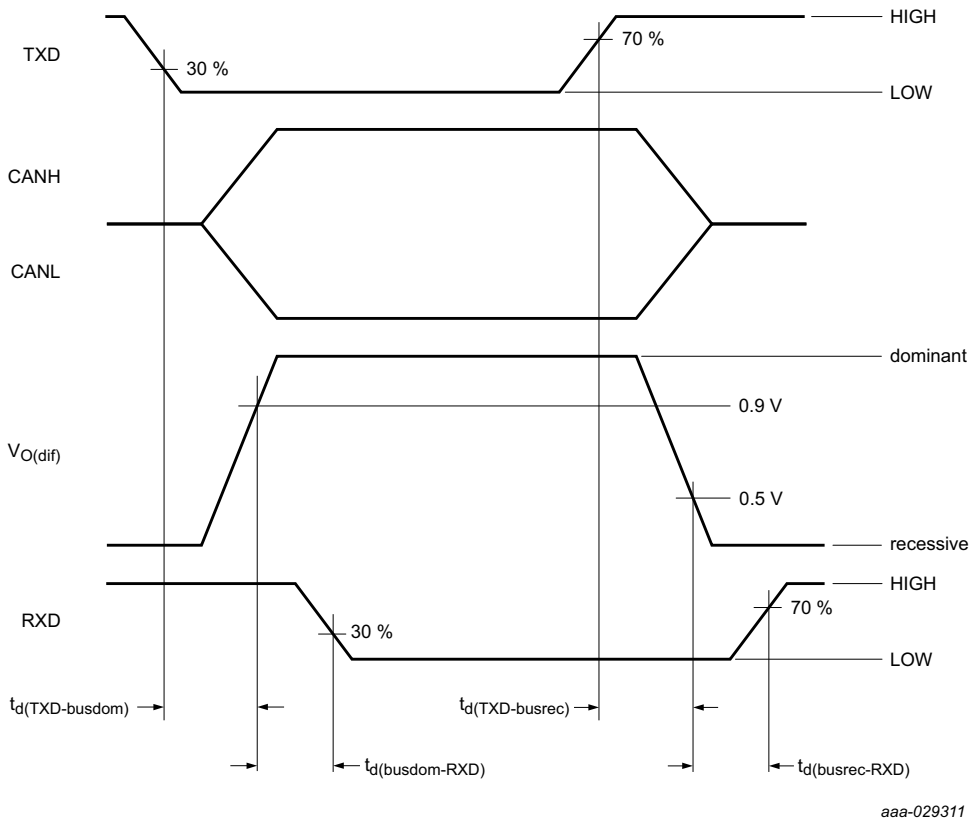


Fig 12. CAN transceiver timing diagram

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

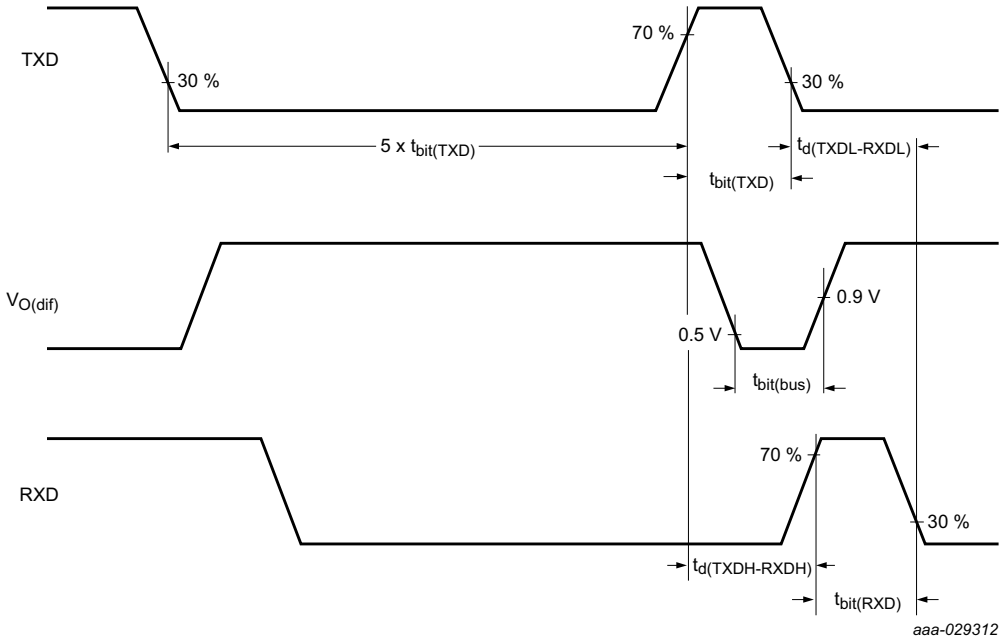
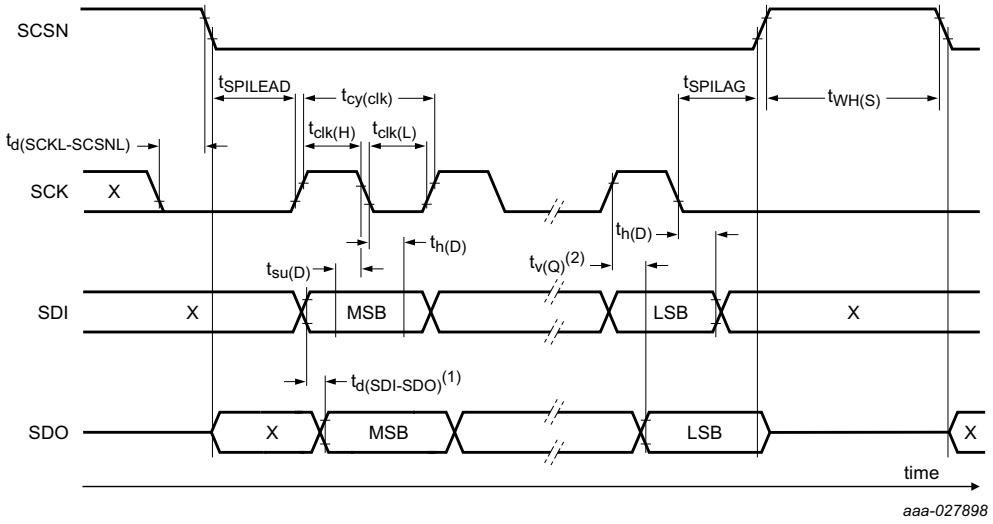


Fig 13. CAN FD timing definitions according to ISO 11898-2:2016



(1) The SDI to SDO delay time is valid for SPI address bits and the read-only bit.

(2) The data output valid time is valid for the SPI data bits.

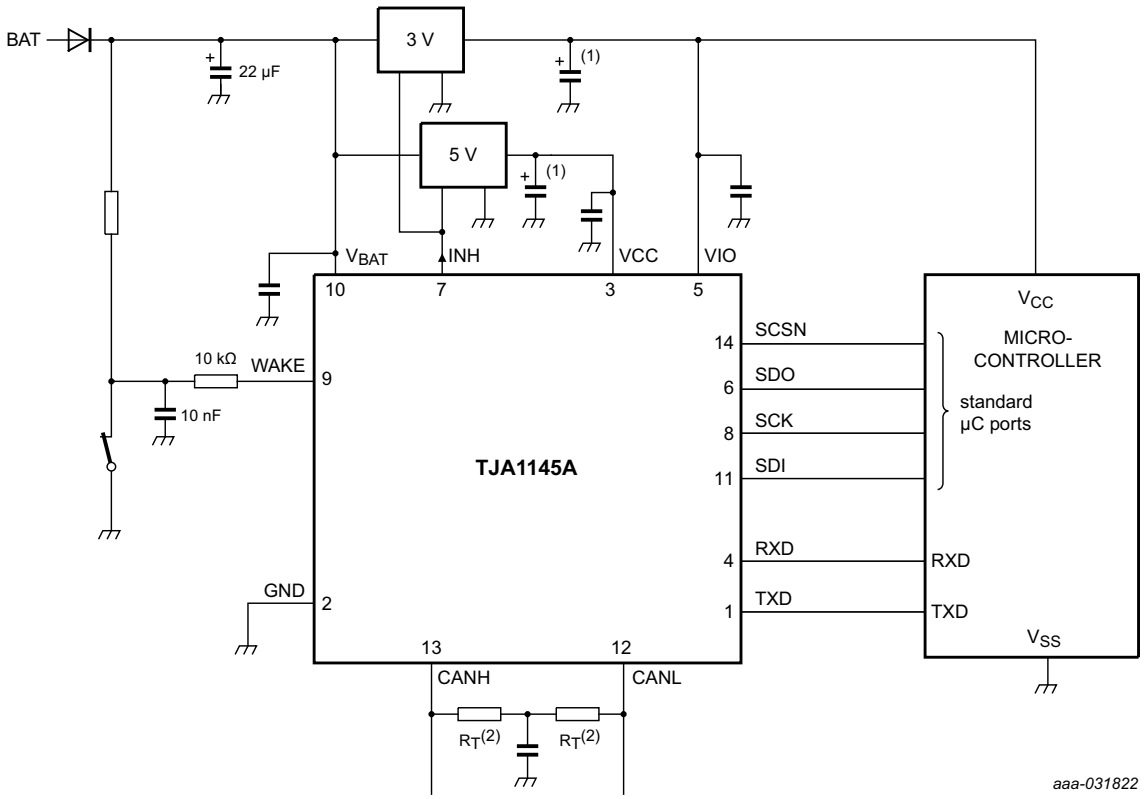
Fig 14. SPI timing diagram

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

12. Application information

12.1 Application diagram



(1) Optional, depends on regulator.

(2) For bus line end nodes, R_T = 60 Ω in order to support the 'split termination concept'. For sub-nodes, an optional 'weak' termination of e.g. R_T = 1.3 kΩ can be used, if required by the OEM.

Fig 15. Typical application using the TJA1145A

12.2 Application hints

Further information on the application of the TJA1145A can be found in the NXP application hints document *AH1903 Application Hints - High speed CAN transceiver for partial networking TJA1145A.*

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

13. Test information

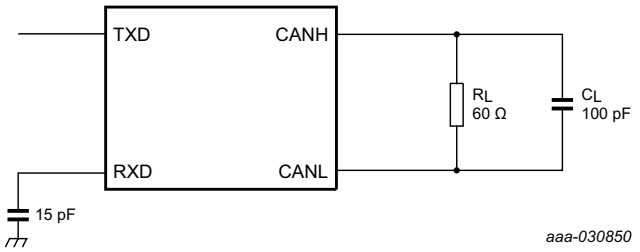


Fig 16. Timing test circuit for CAN transceiver

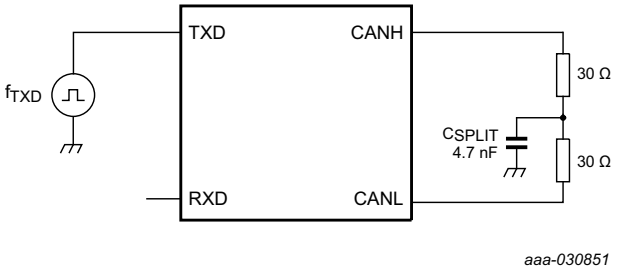


Fig 17. Test circuit for measuring transceiver driver symmetry

13.1 Quality information

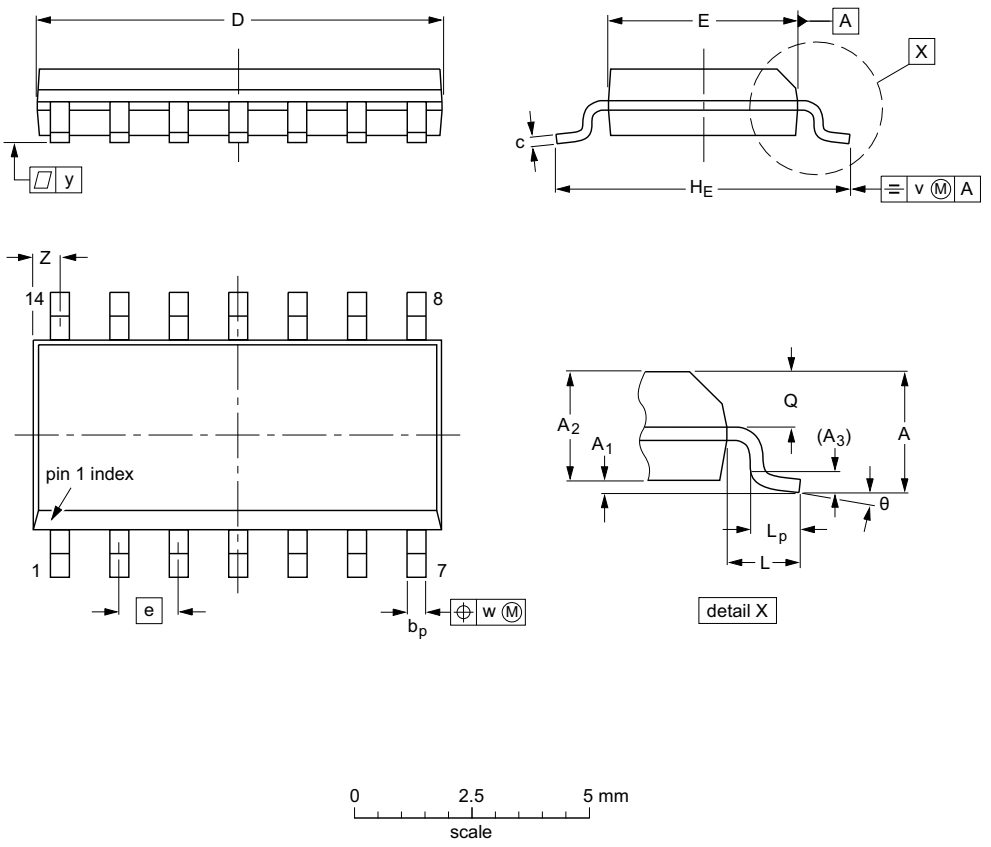
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

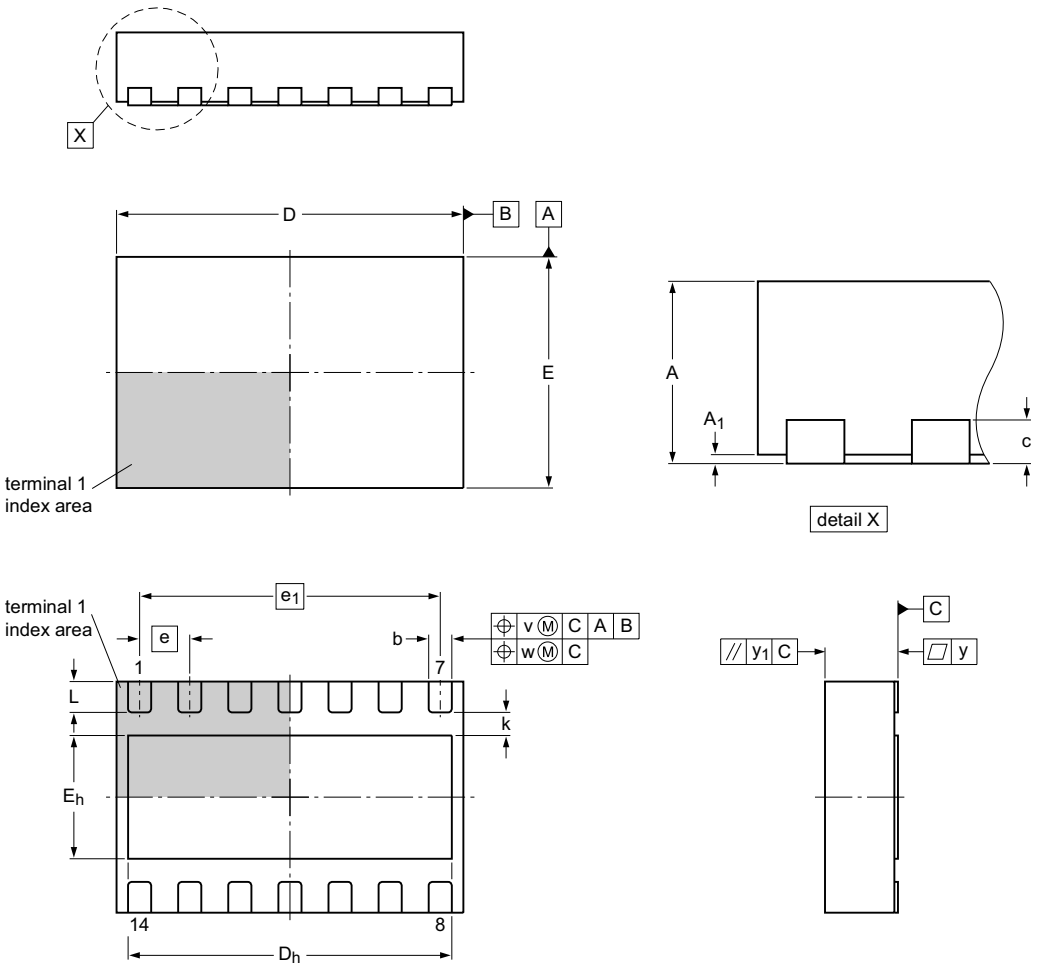
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 18. Package outline SOT108-1 (SO14)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit	A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
mm nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Fig 19. Package outline SOT1086-2 (HVSON14)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 36 and 37

Table 36. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 37. Lead-free process (from J-STD-020D)

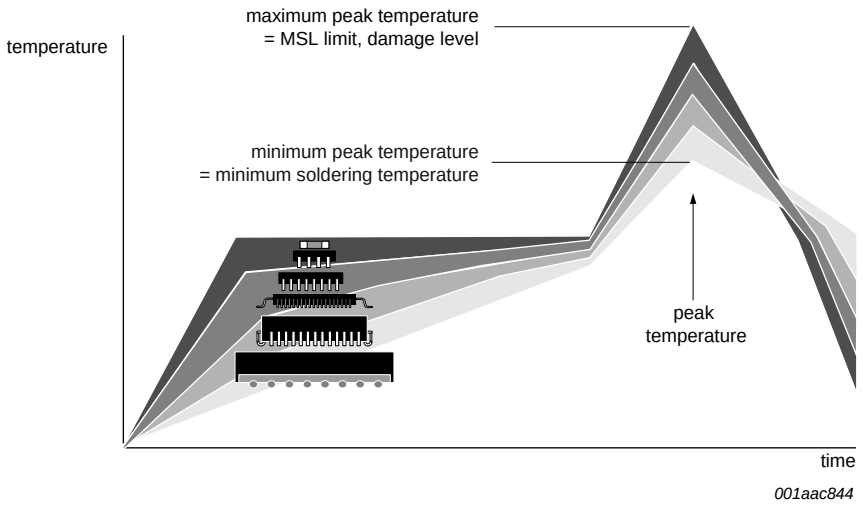
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.



MSL: Moisture Sensitivity Level

Fig 20. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Soldering of HVSON packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can found in the following application notes:

- *AN10365 'Surface mount reflow soldering description"*
- *AN10366 "HVQFN application information"*

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

18. Appendix: ISO 11898-2:2016 parameter cross-reference list

Table 38. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{SYM}	V_{TXsym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)dom}$	dominant short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
Optional HS-PMA transmit dominant timeout			
Transmit dominant timeout, long	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant timeout, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_i	input resistance
Matching of internal resistance	MR	ΔR_i	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}	receiver timing symmetry

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

Table 38. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating VCAN_H and VCAN_L			
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
Number of recessive bits before next SOF			
Number of recessive bits before a new SOF shall be accepted	N_{Bits_idle}	$N_{bit(idle)}$	number of idle bits
Bitfiter in CAN FD data phase			
CAN FD data phase bitfilter (option 1)	$pBitfilter_{option1}$	$t_{fltr(bit)dom}$	dominant bit filter time
HS-PMA bus biasing control timings			
CAN activity filter time, long	t_{Filter}	$t_{wake(busdom)}$[1]	bus dominant wake-up time
CAN activity filter time, short		$t_{wake(busrec)}$[1]	bus recessive wake-up time
Wake-up timeout, short	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up timeout, long			
Timeout for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus Bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	delay time from bus active to bias

[1] $t_{fltr(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

19. Revision history

Table 39. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1145A v.2	20200923	Product data sheet	-	TJA1145A v.1
Modifications:	• Added variants TJA1145AT and TJA1145AT/FD in an SO14 package. • Table 31: error corrected (CMC reset value changed to 01)			
TJA1145A v.1	20190823	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

21. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2020. All rights reserved.

22. Contents

1 General description 1
2 Features and benefits 1
2.1 General 1
2.2 Designed for automotive applications 2
2.3 Advanced ECU power management system . . 2
2.4 Protection and diagnosis 2
3 Quick reference data 3
4 Ordering information 4
5 Block diagram 4
6 Pinning information 5
6.1 Pinning 5
6.2 Pin description 5
7 Functional description 6
7.1 System controller 6
7.1.1 Operating modes 6
7.1.1.1 Normal mode 6
7.1.1.2 Standby mode 6
7.1.1.3 Sleep mode 7
7.1.1.4 Off mode 8
7.1.1.5 Overtemp mode 8
7.1.1.6 Hardware characterization for the TJA1145A operating modes 9
7.1.2 System control registers 9
7.2 High-speed CAN transceiver 10
7.2.1 CAN operating modes 10
7.2.1.1 CAN Active mode 10
7.2.1.2 CAN Listen-only mode 12
7.2.1.3 CAN Offline and Offline Bias modes 12
7.2.1.4 CAN Off mode 13
7.2.2 CAN standard wake-up (partial networking not enabled) 13
7.2.3 CAN control and Transceiver status registers 14
7.3 CAN partial networking 16
7.3.1 Wake-up frame (WUF) 16
7.3.2 CAN FD frames 18
7.3.3 CAN partial networking configuration registers 19
7.4 Fail-safe features 21
7.4.1 TXD dominant time-out 21
7.4.2 Pull-up on TXD pin 21
7.4.3 V_{CC} undervoltage event 21
7.4.4 Loss of power at pin BAT 22
7.5 Local wake-up via WAKE pin 22
7.6 Wake-up and interrupt event diagnosis via pin RXD 22
7.6.1 Interrupt/wake-up delay 24
7.6.2 Sleep mode protection 24
7.6.3 Event status and event capture registers 24
7.7 Device ID 27
7.8 Lock control register 27
7.9 General-purpose memory 28
7.10 VIO supply pin 28
7.11 V_{CC}/V_{IO} undervoltage protection 28
7.12 SPI 29
7.12.1 Introduction 29
7.12.2 Register map 30
7.12.3 Register configuration in TJA1145A operating modes 33
8 Limiting values 35
9 Thermal characteristics 36
10 Static characteristics 37
11 Dynamic characteristics 41
12 Application information 45
12.1 Application diagram 45
12.2 Application hints 45
13 Test information 46
13.1 Quality information 46
14 Package outline 47
15 Handling information 49
16 Soldering of SMD packages 49
16.1 Introduction to soldering 49
16.2 Wave and reflow soldering 49
16.3 Wave soldering 49
16.4 Reflow soldering 50
17 Soldering of HVSON packages 51
18 Appendix: ISO 11898-2:2016 parameter cross-reference list 52
19 Revision history 54
20 Legal information 55
20.1 Data sheet status 55
20.2 Definitions 55
20.3 Disclaimers 55
20.4 Trademarks 56
21 Contact information 56
22 Contents 57

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2020. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 23 September 2020
Document identifier: TJA1145A