



## TPD8E003 8-Channel ESD Protection Diode for Keypad and GPIO

### 1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - $\pm 12$ -kV Contact Discharge
  - $\pm 15$ -kV Air-Gap Discharge
- IEC 61000-4-5 Surge Protection
  - 3.5-A (8/20  $\mu$ s)
- IO Capacitance: 9 pF (Typical)
- DC Breakdown Voltage: 6 V (Minimum)
- Low Leakage Current: 100 nA (Maximum)
- Industrial Temperature Range:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Space-Saving, Ultra-Thin, WSON Package

### 2 Applications

- End Equipment
  - Laptops and Desktops
  - IP Phones
- Interfaces
  - Keypads
  - GPIO Headers
  - Touchscreens
  - Low-Speed Memory Interfaces

### 3 Description

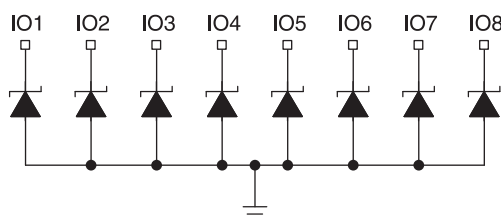
The TPD8E003 device is a unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode array. The TPD8E003 is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device provides 8 channels of ESD protection in a space-saving WSON package. Typical applications for the TPD8E003 include Keypad, GPIO, resistive touchscreen, and low-speed memory interfaces. Also, see the TPD2E2U06 and TPD4E05U06 for 2- and 4-channel ESD protection solutions, respectively.

#### Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE  | BODY SIZE (NOM)          |
|-------------|----------|--------------------------|
| TPD8E003    | WSON (8) | 1.70 mm $\times$ 1.35 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Circuit Schematic



## Table of Contents

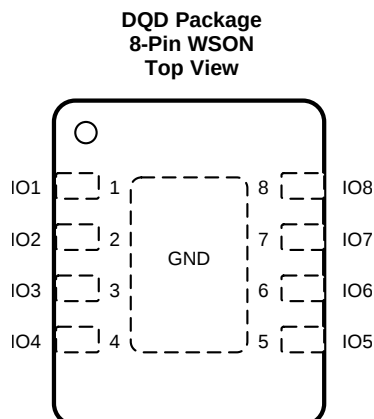
|                                                |          |                                                                  |           |
|------------------------------------------------|----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                        | <b>1</b> | 7.3 Feature Description .....                                    | <b>6</b>  |
| <b>2 Applications</b> .....                    | <b>1</b> | 7.4 Device Functional Modes .....                                | <b>6</b>  |
| <b>3 Description</b> .....                     | <b>1</b> | <b>8 Application and Implementation</b> .....                    | <b>7</b>  |
| <b>4 Revision History</b> .....                | <b>2</b> | 8.1 Application Information .....                                | <b>7</b>  |
| <b>5 Pin Configuration and Functions</b> ..... | <b>3</b> | 8.2 Typical Application .....                                    | <b>7</b>  |
| <b>6 Specifications</b> .....                  | <b>4</b> | <b>9 Power Supply Recommendations</b> .....                      | <b>9</b>  |
| 6.1 Absolute Maximum Ratings .....             | <b>4</b> | <b>10 Layout</b> .....                                           | <b>9</b>  |
| 6.2 ESD Ratings .....                          | <b>4</b> | 10.1 Layout Guidelines .....                                     | <b>9</b>  |
| 6.3 ESD Ratings – Surge Protection .....       | <b>4</b> | 10.2 Layout Example .....                                        | <b>9</b>  |
| 6.4 Recommended Operating Conditions .....     | <b>4</b> | <b>11 Device and Documentation Support</b> .....                 | <b>11</b> |
| 6.5 Thermal Information .....                  | <b>4</b> | 11.1 Community Resources .....                                   | <b>11</b> |
| 6.6 Electrical Characteristics .....           | <b>5</b> | 11.2 Trademarks .....                                            | <b>11</b> |
| 6.7 Typical Characteristics .....              | <b>5</b> | 11.3 Electrostatic Discharge Caution .....                       | <b>11</b> |
| <b>7 Detailed Description</b> .....            | <b>6</b> | 11.4 Glossary .....                                              | <b>11</b> |
| 7.1 Overview .....                             | <b>6</b> | <b>12 Mechanical, Packaging, and Orderable Information</b> ..... | <b>11</b> |
| 7.2 Functional Block Diagram .....             | <b>6</b> |                                                                  |           |

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (September 2010) to Revision B                                                                                                                                                                                                                                                                                                | Page     |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| • Added <i>ESD Ratings</i> tables, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | <b>1</b> |
| • Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet .....                                                                                                                                                                                                                                                               | <b>1</b> |

## 5 Pin Configuration and Functions



**Pin Functions**

| PIN |      | TYPE <sup>(1)</sup> | DESCRIPTION           |
|-----|------|---------------------|-----------------------|
| NO. | NAME |                     |                       |
| 1   | IO1  | I/O                 | ESD protected channel |
| 2   | IO2  | I/O                 | ESD protected channel |
| 3   | IO3  | I/O                 | ESD protected channel |
| 4   | IO4  | I/O                 | ESD protected channel |
| 5   | IO5  | I/O                 | ESD protected channel |
| 6   | IO6  | I/O                 | ESD protected channel |
| 7   | IO7  | I/O                 | ESD protected channel |
| 8   | IO8  | I/O                 | ESD protected channel |
| GND | GND  | G                   | Connect to ground     |

(1) G = Ground, I = Input, O = Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                               | MIN | MAX | UNIT |
|-----------------------------------------------|-----|-----|------|
| IO voltage tolerance (IO pins)                |     | 6   | V    |
| Peak pulse power (tp = 8/20 $\mu$ s)          |     | 55  | W    |
| Peak pulse current (tp = 8/20 $\mu$ s)        |     | 3.5 | A    |
| T <sub>A</sub> Operating free-air temperature | –40 | 85  | °C   |
| T <sub>stg</sub> Storage temperature          | –55 | 155 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                                            |                                                                                | VALUE | UNIT |
|--------------------------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                            | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 ESD Ratings – Surge Protection

|                                            |                                 | VALUE  | UNIT |
|--------------------------------------------|---------------------------------|--------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | IEC 61000-4-2 contact discharge | ±12000 | V    |
|                                            | IEC 61000-4-2 air-gap discharge | ±15000 |      |

### 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                               | MIN | NOM | MAX | UNIT |
|-----------------------------------------------|-----|-----|-----|------|
| V <sub>IO</sub> Input pin voltage             | 0   |     | 5.5 | V    |
| T <sub>A</sub> Operating free-air temperature | –40 |     | 85  | °C   |

### 6.5 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPD8E003  | UNIT |
|-------------------------------|----------------------------------------------|-----------|------|
|                               |                                              | DQD (WSN) |      |
|                               |                                              | 8 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 98.3      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 110.3     | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 42.5      | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 9.2       | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 42.2      | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 22.0      | °C/W |

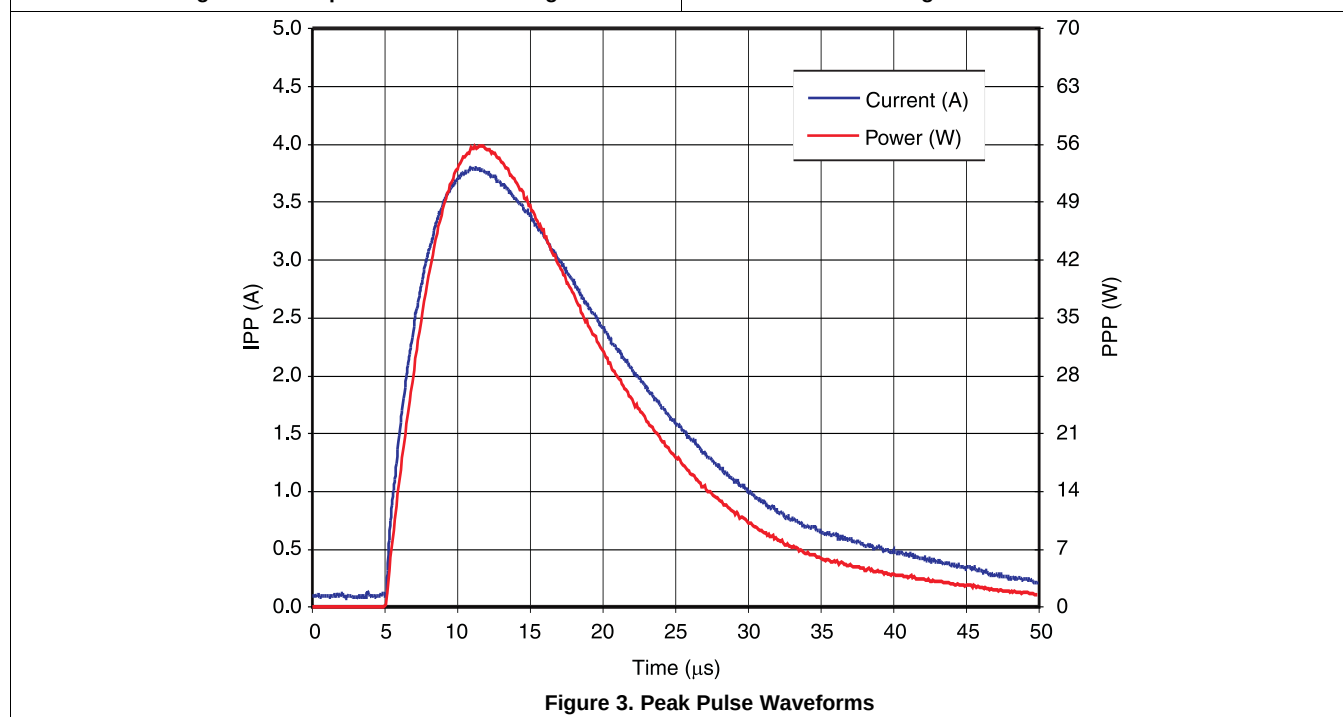
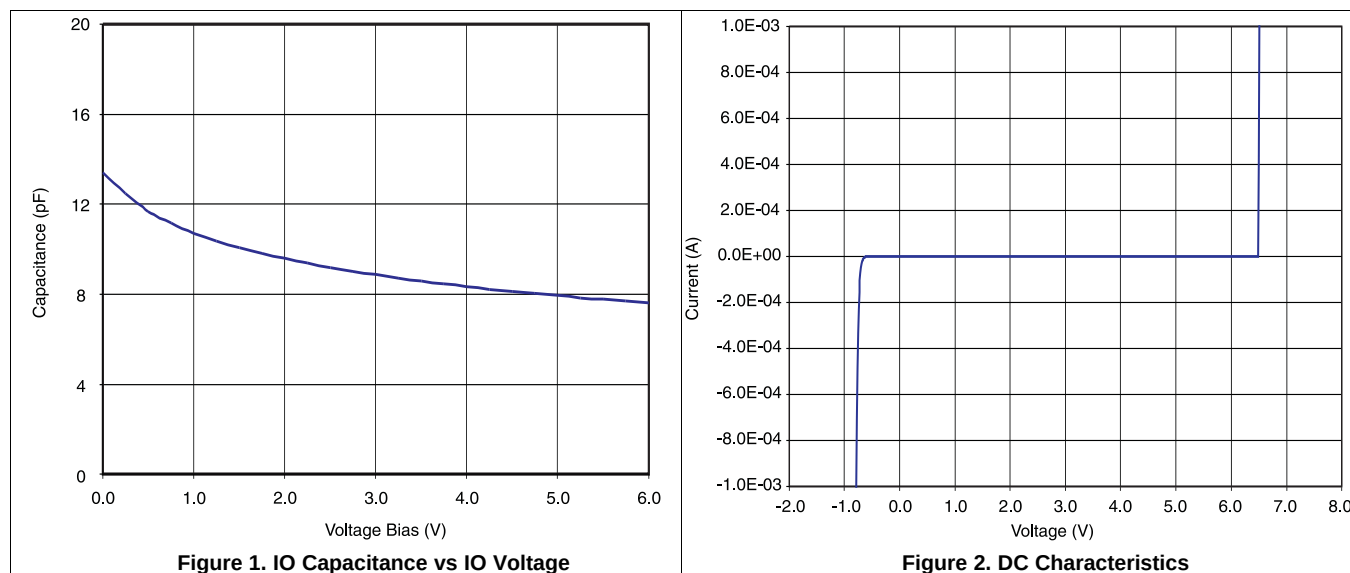
- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER              | TEST CONDITION                | MIN | TYP | MAX | UNIT          |
|------------------------|-------------------------------|-----|-----|-----|---------------|
| $V_{\text{clamp}}$     | Clamp voltage                 |     |     | 10  | V             |
| $I_{\text{I}}$         | Leakage current               |     |     | 0.1 | $\mu\text{A}$ |
| $C_{\text{IO}}$        | IO capacitance                | 7   | 9   | 12  | pF            |
| $\Delta C_{\text{IO}}$ | Differential line capacitance |     | 0.1 |     | pF            |
| $V_{\text{BR}}$        | Break-down voltage            | 6   |     |     | V             |
| $R_{\text{dyn}}$       | Dynamic resistance            |     | 1   |     | $\Omega$      |

## 6.7 Typical Characteristics

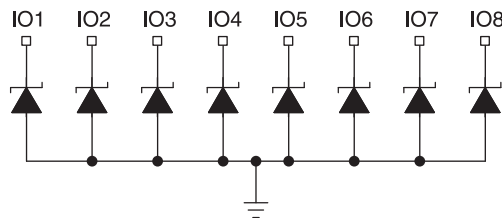


## 7 Detailed Description

### 7.1 Overview

The TPD8E003 is a unidirectional TVS-based, ESD protection diode array. The TPD8E003 is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (Level 4). This device provides 8 channels of ESD protection in a space-saving WSON package.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to  $\pm 12$ -kV contact and  $\pm 15$ -kV air gap. An ESD/surge clamp diverts the current to ground.

#### 7.3.2 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 3.5 A and 55 W (8/20  $\mu$ s waveform). An ESD/surge clamp diverts this current to ground.

#### 7.3.3 IO Capacitance

The capacitance between each I/O pin-to-ground is 9 pF (typical) and 12 pF (maximum).

#### 7.3.4 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5 V.

#### 7.3.5 Low Leakage Current

The I/O pins feature a low leakage current of 100 nA (maximum) with a bias of 2.5 V.

#### 7.3.6 Industrial Temperature Range

This device features an industrial operating range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

#### 7.3.7 Space-Saving Package

This device features a space-saving WSON package that puts many channels of ESD in a small form factor.

### 7.4 Device Functional Modes

TPD8E003 is a passive integrated circuit that triggers when voltages are above  $V_{BR}$  or below the lower diodes  $V_f$  ( $-0.6$  V). During ESD events, voltages as high as  $\pm 15$  kV (air) can be directed to ground through the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD8E003 (usually within 10s of nano-seconds) the device reverts to passive.

## 8 Application and Implementation

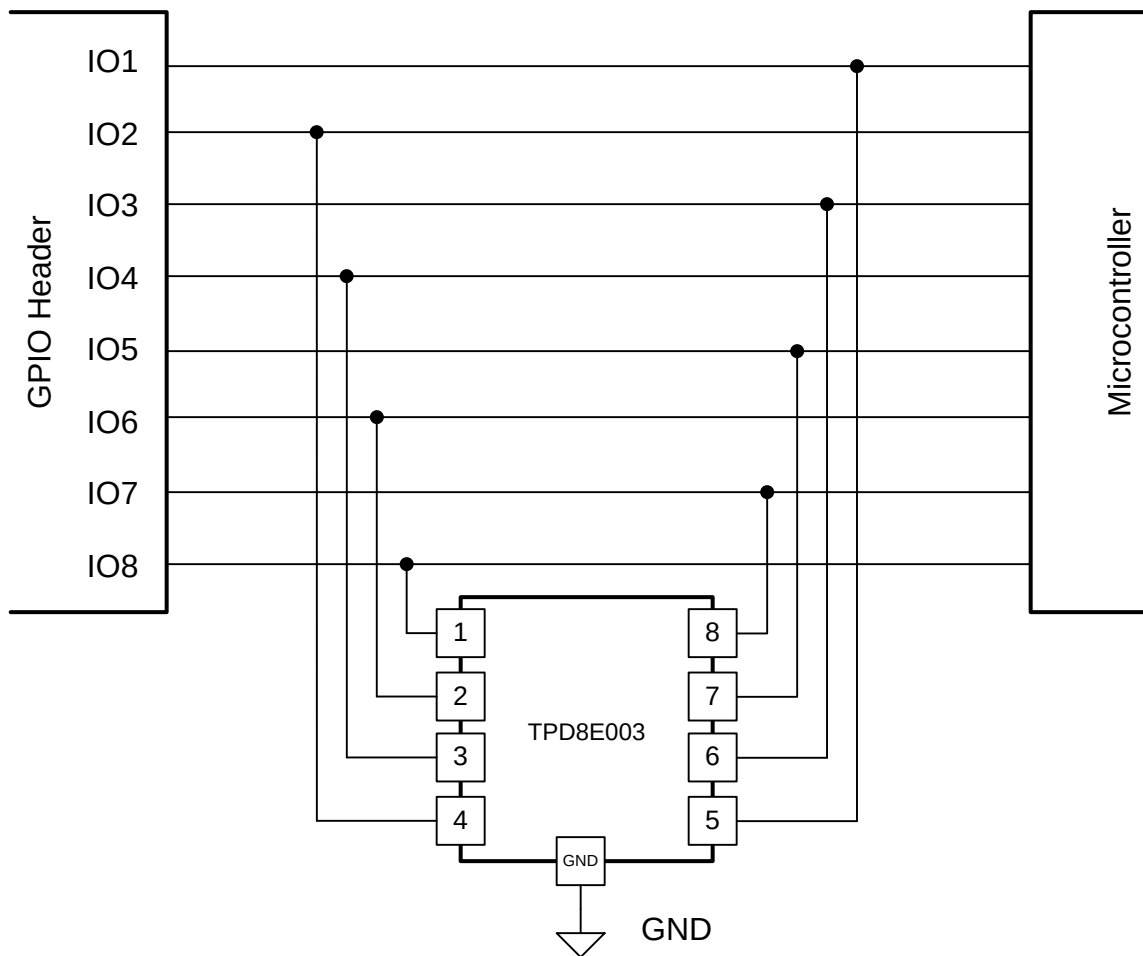
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPD8E003 offers eight ESD clamp circuits in a space-saving DQD package. When placed near the connector, the TPD8E003 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD8E003 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike.

### 8.2 Typical Application



**Figure 4. GPIO Header Application**

#### 8.2.1 Design Requirements

For this design example, one TPD8E003 is used to protect an 8-pin GPIO header.

Given the example application, the parameters listed in [Table 1](#) are known.

**Table 1. Design Parameters**

| PARAMETER                            | VALUE                       |
|--------------------------------------|-----------------------------|
| Signal Range on Protected Lines      | 0 V to 5 V                  |
| Required Level of IEC ESD Protection | ±8kV Contact, ±15kV Air Gap |

## 8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer must know the following:

- Voltage range of the signal on all protected lines
- Required ESD protection needed

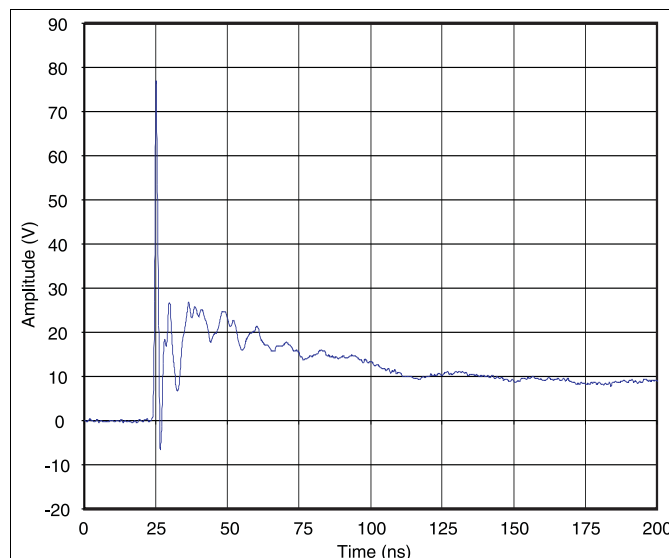
### 8.2.2.1 Signal Range

The TPD8E003 supports signal ranges between 0 V and 5.5 V, which supports the GPIO application.

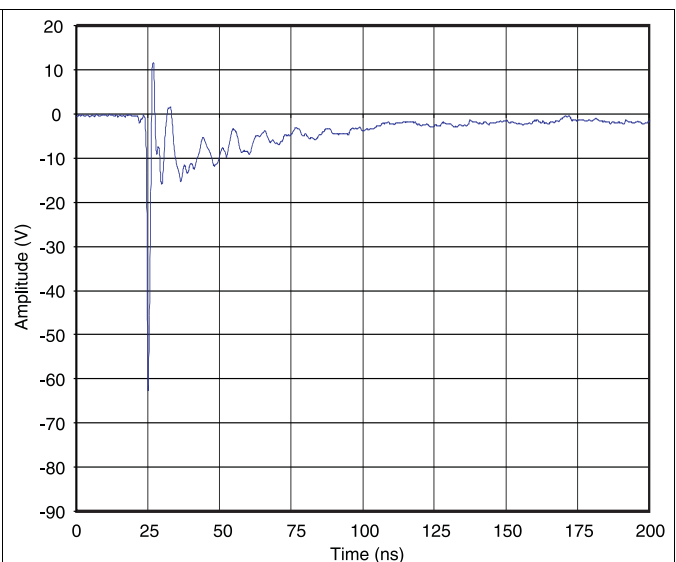
### 8.2.2.2 Required ESD Protection

The TPD8E003 is rated to withstand up to ±12-kV contact and ±15-kV air gap IEC ESD. This meets the IEC ESD design target with room to spare.

## 8.2.3 Application Curves



**Figure 5. IEC ESD Clamping Waveforms  
8-kV Contact**



**Figure 6. IEC ESD Clamping Waveforms  
-8-kV Contact**



## 9 Power Supply Recommendations

This device is a passive ESD protection device and there is no need to power it. Take care making sure that the maximum voltage specifications for each line are not violated.

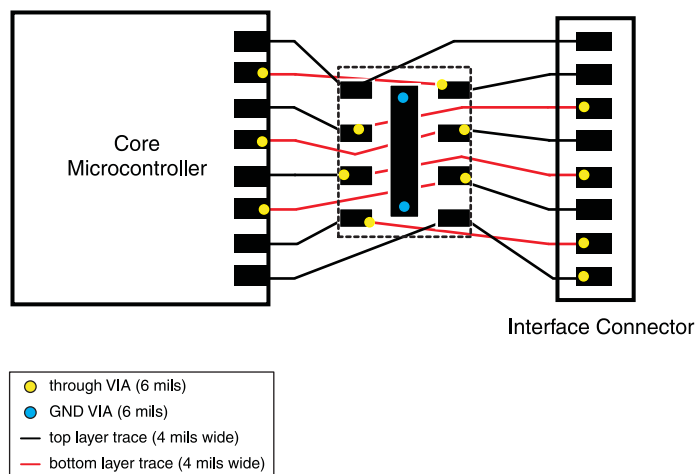
## 10 Layout

### 10.1 Layout Guidelines

For proper operation of the ESD clamps, both during normal function and ESD events, the following layout and design guidelines must be followed:

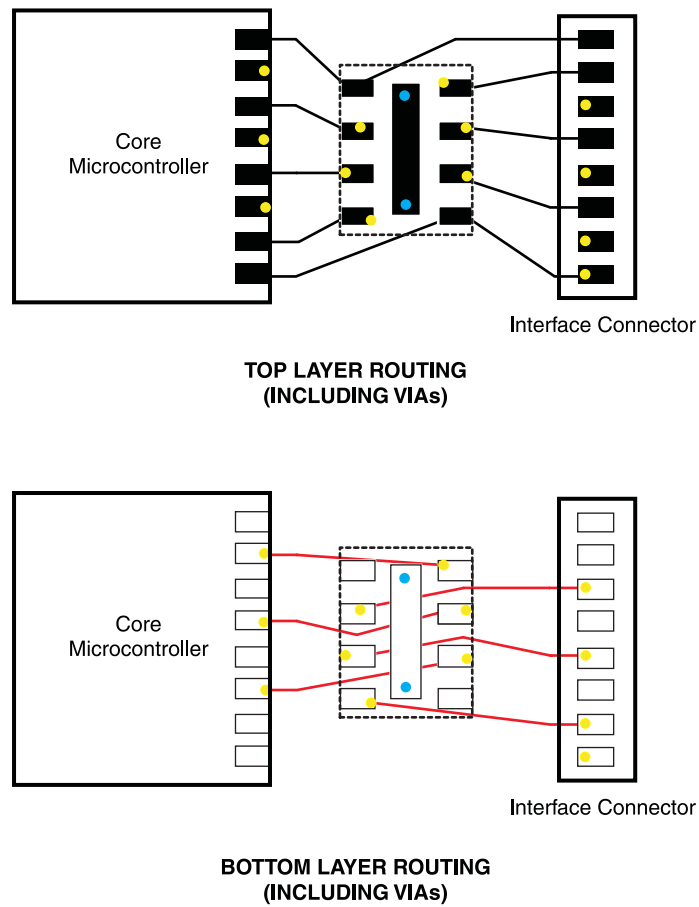
- Place the TPD8E003 solution close to the connector. This allows the TPD8E003 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
- TI recommends employing two signal layers in the printed-circuit board (PCB) to route through the eight ESD clamp terminals of the TPD8E003.
- Ensure that there is proper metallization for the GND vertical interconnect access (VIA). During an ESD event, the in-rush current flows to the system GND plane through the GND VIA. Having a low-impedance path allows the current to flow quickly to GND, effectively building a robust, system-level ESD immunity.
- Place the VIA under the DQD pad in locations that offer maximum flexibility in board routing.
- One common set of guidelines (not restricted to all cases):
  - Trace width: 4 mm
  - VIA diameter: 6 mm
  - DQD package pad dimensions: 8 mm × 12 mm

### 10.2 Layout Example



**Figure 7. Board Layout With the TPD8E003DQDR**

## Layout Example (continued)



**Figure 8. Top and Bottom Layer Board Layout With the TPD8E003DQDR**

## 11 Device and Documentation Support

### 11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.2 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPD8E003DQDR     | ACTIVE        | WSO          | DQD                | 8    | 3000           | RoHS & Green    | NIPDAUAG                             | Level-1-260C-UNLIM   | -40 to 85    | (65S, 65U)              | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

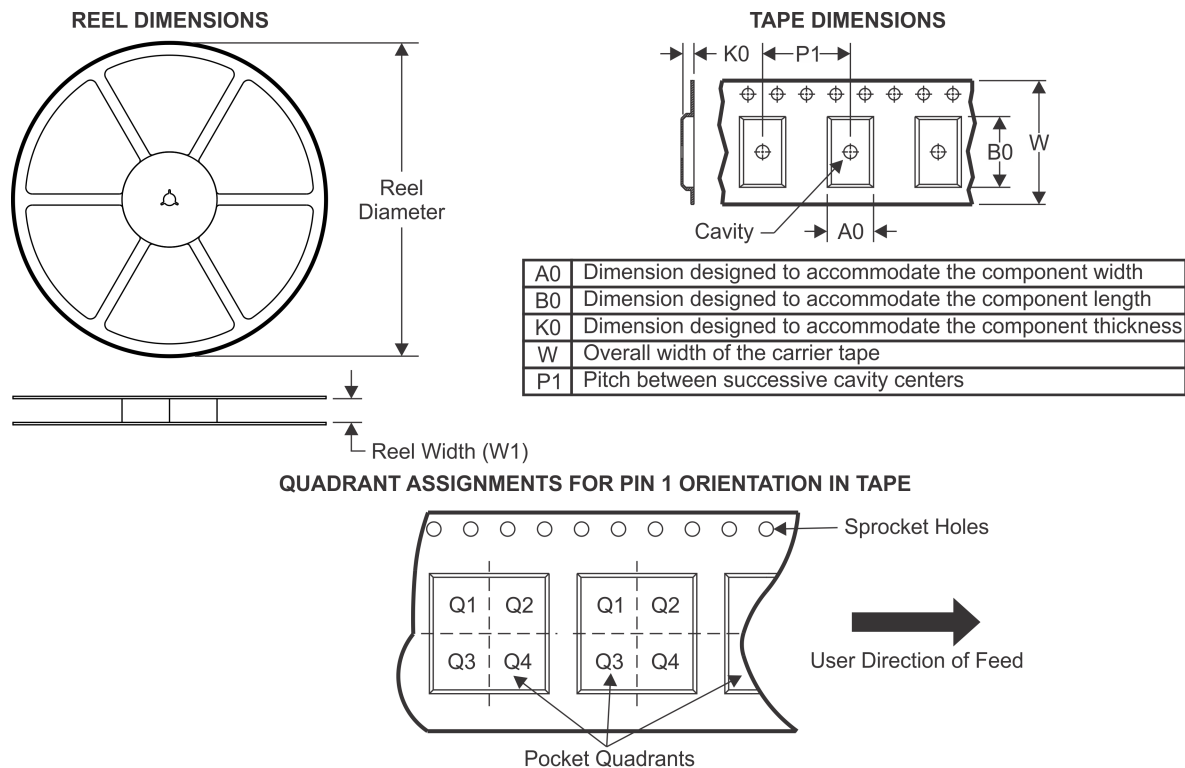
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

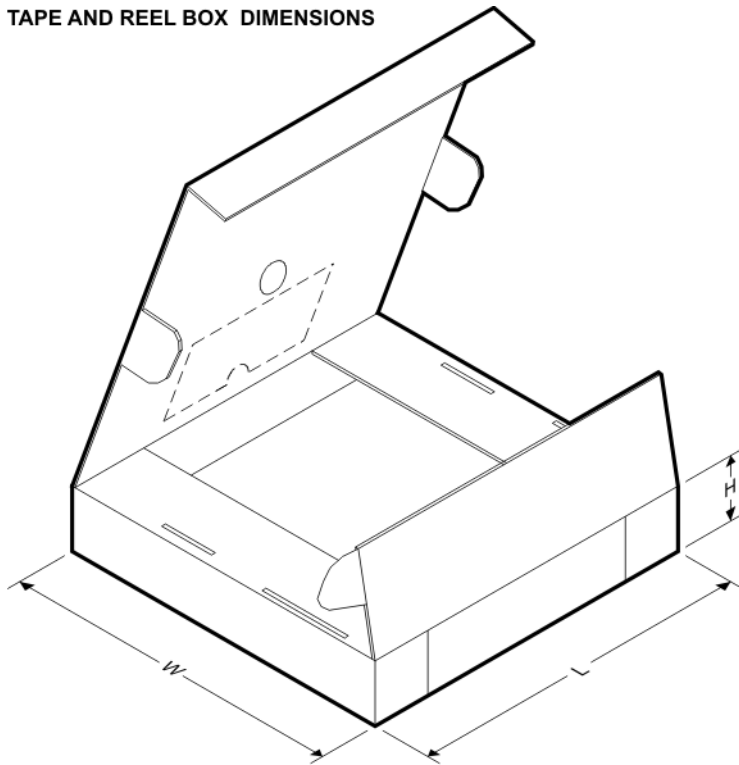
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

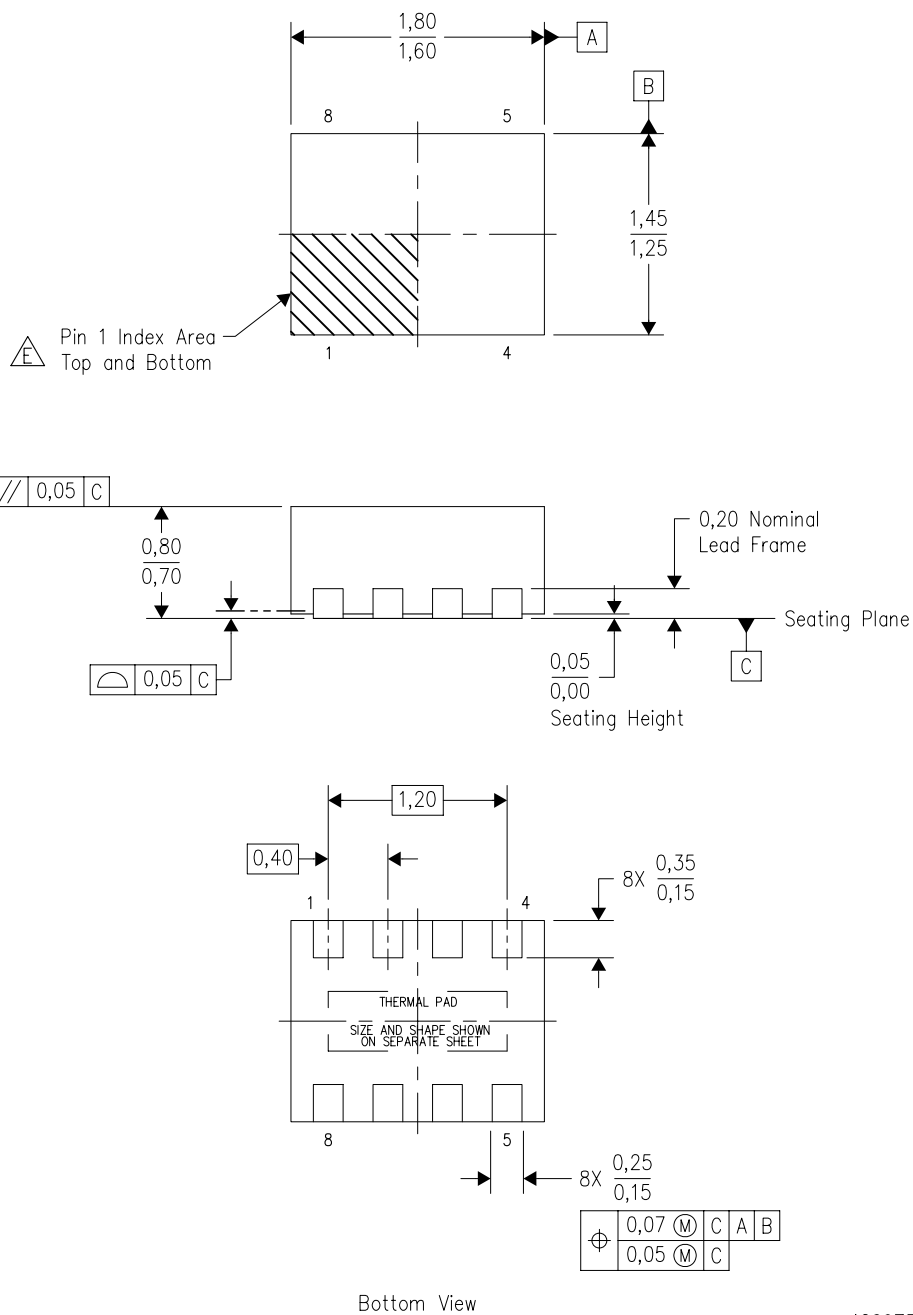
| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPD8E003DQDR | WSO          | DQD             | 8    | 3000 | 180.0              | 8.4                | 1.65    | 2.0     | 0.95    | 4.0     | 8.0    | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPD8E003DQDR | WSO8         | DQD             | 8    | 3000 | 183.0       | 183.0      | 20.0        |



4209732-2/C 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F.  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

DQD (R-PWSON-N8)

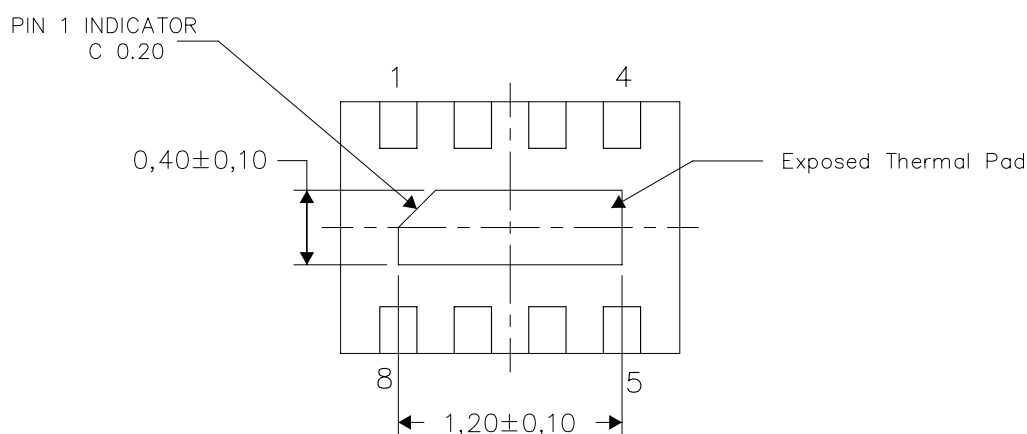
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4209733-2/C 12/11

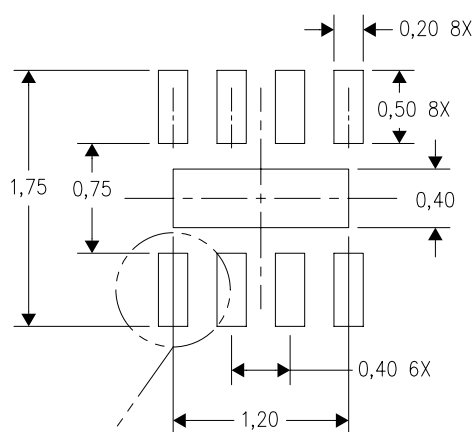
NOTE: All linear dimensions are in millimeters



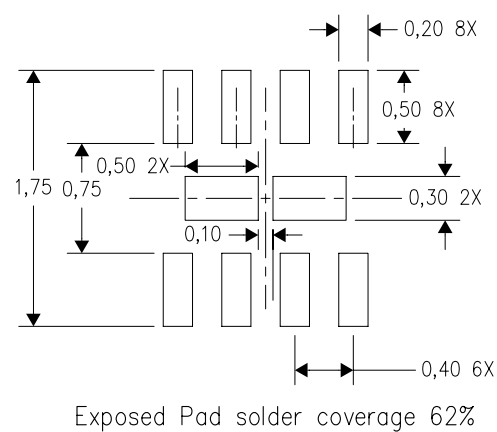
DQD (R-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

Land Pattern



Stencil Pattern



4211174-2/B 01/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2021, Texas Instruments Incorporated