



STK4030V

AF Power Amplifier (Split Power Supply)
(35 W min, THD = 0.08%)

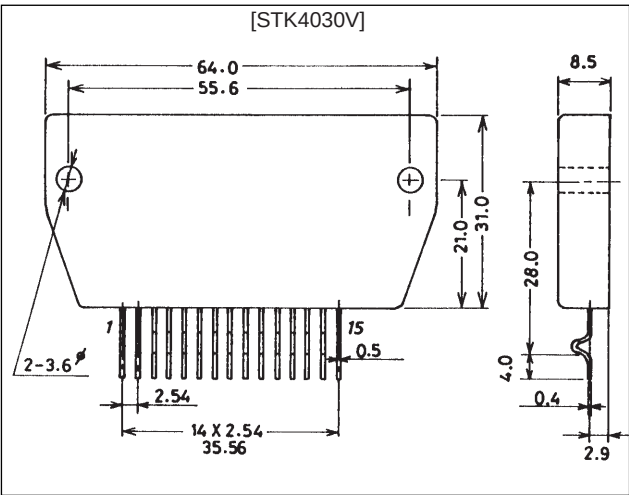
Features

- Compact packaging supports slimmer set designs (up to 70 W)
- Series designed for 20 up to 100 W (200 W) and pin-compatibility (120 to 200 W have 18 pins)
- Simpler heat sink design facilitates thermal design of slim stereo sets
- Current mirror circuit application reduces distortion to 0.08%
- Supports addition of electronic circuits for thermal shutdown and load-short protection circuit as well as pop noise muting which occurs when the power supply switch is turned on and off

Package Dimensions

unit: mm

4062



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		±45	V
Thermal resistance	θj-c		2.1	°C/W
Junction temperature	Tj		150	°C
Operating substrate temperature	Tc		125	°C
Storage temperature	Tstg		-30 to +125	°C
Available time for load shorted	t _s *	V _{CC} = ±30 V, R _L = 8 Ω, f = 50 Hz, P _O = 35 W	2	s

Note: Use a constant-voltage power supply as the test power supply unless otherwise specified.
* Use the transformer power supply shown on the next page when measuring the available time for load shorted and the output noise voltage.

Recommended Operating Conditions at Ta = 25°C

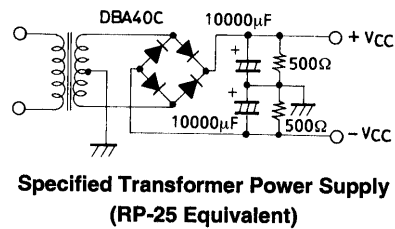
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V _{CC}		±30	V
Load resistance	R _L		8	Ω

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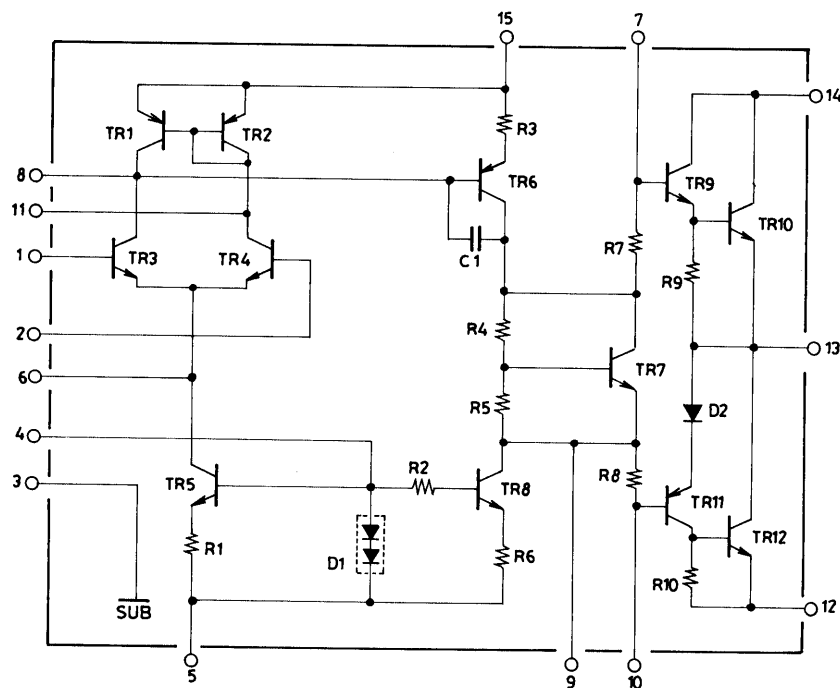
Operating Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = \pm 30\text{ V}$, $R_L = 8\ \Omega$, $V_G = 40\text{ dB}$, $R_g = 600\ \Omega$, 100 k LPF on , R_L (non-inductive)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	$V_{CC} = \pm 36\text{ V}$	15		120	mA
Output power	$P_O(1)$	THD = 0.08%, $f = 20\text{ Hz to } 20\text{ kHz}$	35			W
	$P_O(2)$	$V_{CC} = \pm 27\text{ V}$, THD = 0.2%, $R_L = 4\ \Omega$, $f = 1\text{ kHz}$	40			
Total harmonic distortion	THD	$P_O = 1.0\text{ W}$, $f = 1\text{ kHz}$			0.08	%
Frequency response	f_L, f_H	$P_O = 1.0\text{ W}$, -3 dB		20 to 50 k		Hz
Input resistance	r_i	$P_O = 1.0\text{ W}$, $f = 1\text{ kHz}$		55		k Ω
Output noise voltage	V_{NO}^*	$V_{CC} = \pm 36\text{ V}$, $R_g = 10\text{ k}\Omega$		1.2		mVrms
Neutral voltage	V_N	$V_{CC} = \pm 36\text{ V}$	-70	0	+70	mV

Equivalent Circuit

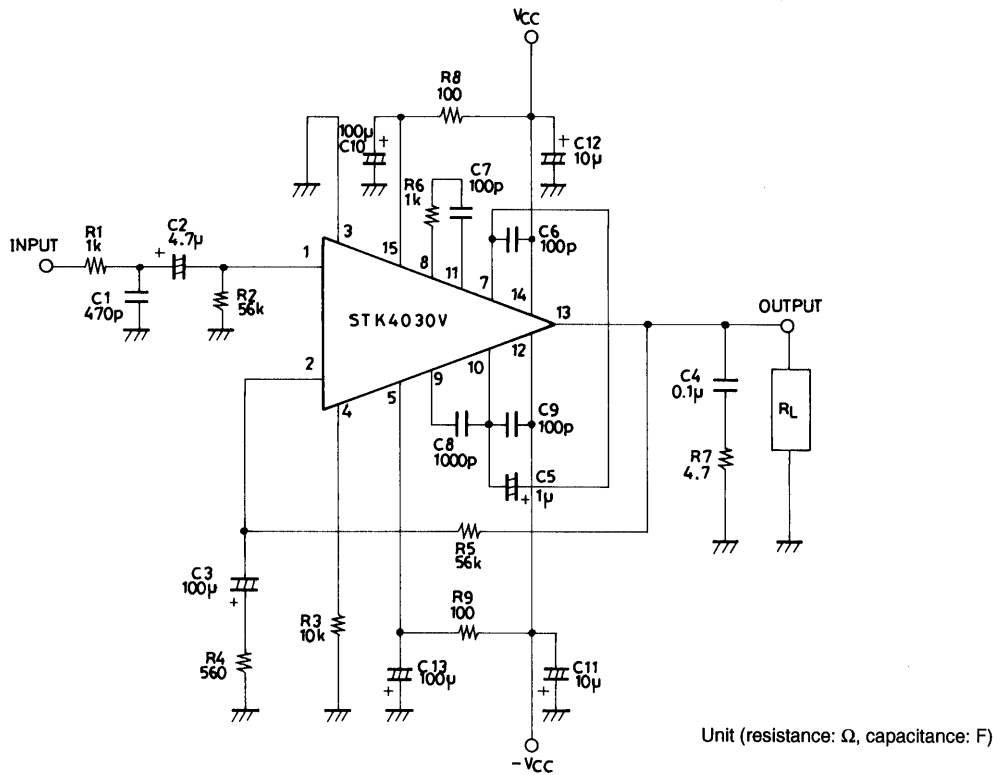


Equivalent Circuit

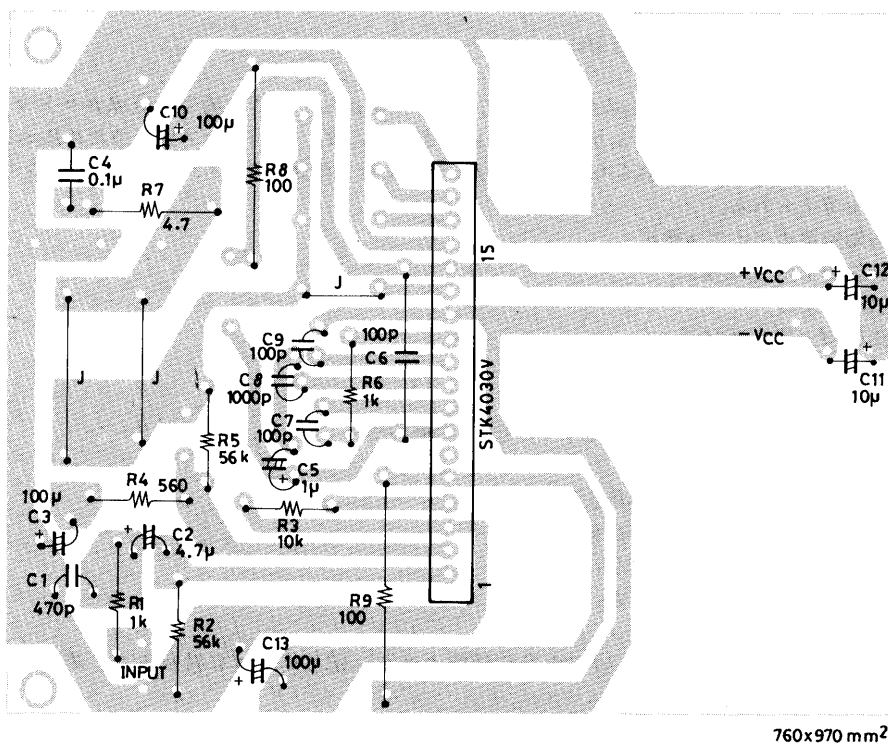


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Application Circuit: 35W min Single Channel AF Power Amplifier



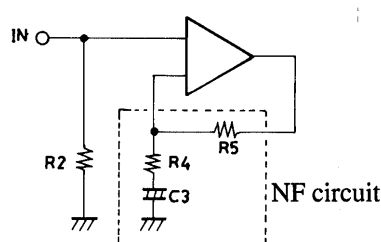
Sample Printed Circuit Pattern for Application Circuit (Copper-foiled side)



Unit (resistance: Ω , capacitance: F)

Description of External Parts

- R_1, C_1 : Input filter circuit
- Reduces high-frequency noise.
- C_2 : Input coupling capacitor
- DC current suppression. A reduction in reactance is effective because of increases in capacitor reactance at low frequencies and 1/f noise dependence on signal source resistance which result in output noise worsening.
- R_2 : Input bias resistor
- Biases the input pin to zero.
 - Effects V_N stability (refer to NF circuit).
 - Due to differential input, input resistance is more or less determined by this resistance value.
- R_4, R_5 : NFB circuit (AC NF circuit). Use of resistor with 1% error is suggested.
- $C_3 (R_2)$



- C_3 : AC NF capacitor
- R_4, R_5 : Used for VG setting.

- VG settings are obtained using R_4 and R_5 according to the following equation:

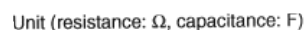
$$\log_{20} \cdot \frac{R_5}{R_4} \quad 40 \text{ dB is recommended.}$$

- Low-frequency cutoff frequency settings are obtained using R_4 and C_3 according to the following equation:

$$f_L = \frac{1}{2\pi \cdot R_4 \cdot C_3} \quad [\text{Hz}]$$

When changing the VG setting, you should change R_4 which requires a recheck of the low cutoff frequency setting. When the VG setting is changed using R_5 , the setting should ensure R_2 equals R_5 so that V_N balance stability is maintained. If the resistor value is increased more than the existing value, V_N balance may be disturbed and result in deterioration of V_N temperature characteristics.

- R_3 : Differential constant-current bias resistor
- R_6, R_7 : For oscillation suppression and phase compensation applications
(For use with differential stage applications)
- R_7, C_4 : For oscillation suppression and phase compensation applications
(A Mylar capacitor is recommended for C_4 for use with output stage applications)
- C_6, C_9 : For oscillation suppression and phase compensation applications
Power stage (Must be connected near the pin) C_6 : Positive (+) power C_9 : Negative (−) power
- C_8 : For oscillation suppression and phase compensation applications
(Oscillation suppression before power step clip)
- C_5 : For oscillation suppression and distortion improvement applications
- R_8, C_{10} : Ripple filter circuit on positive (+) side.
- R_9, C_{13} : Ripple filter circuit on negative (−) side.
- C_{11}, C_{12} : For oscillation suppression applications
- Used for reducing power supply impedance to stable IC operation and should be connected near the IC pin. We recommend that you use an electrolytic capacitor.



- This catalog provides information as of October, 1996. Specifications and information herein are subject to change without notice.