54LS174,54LS175,DM54LS174,DM54LS175, DM74LS174,DM74LS175

54LS174 DM54LS174 DM74LS174 54LS175 DM54LS175 DM74LS175 Hex/Quad D Flip-Flops with Clear

Literature Number: SNOS290A

National Semiconductor

June 1989

54LS174/DM54LS174/DM74LS174, 54LS175/DM54LS175/DM74LS175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

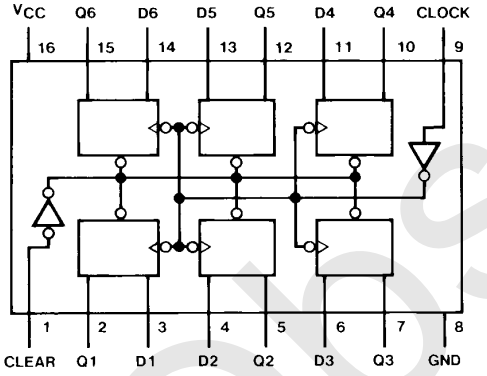
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- LS174 contains six flip-flops with single-rail outputs
- LS175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 14 mW
- Alternate Military/Aerospace device (54LS174, 54LS175) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

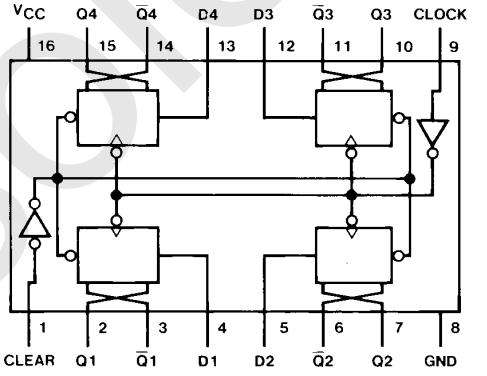
Dual-In-Line Package



TL/F/6404–1

Order Number 54LS174DMQB, 54LS174FMQB, 54LS174LMQB, DM54LS174J, DM54LS174W, DM74LS174M or DM74LS174N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package



TL/F/6404–2

Order Number 54LS175DMQB, 54LS175FMQB, 54LS175LMQB, DM54LS175J DM54LS175W, DM74LS175M or DM74LS175N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = LS175 only

Obsolete

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RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS174			DM74LS174			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
t_W	Pulse Width (Note 6)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 6)		20			20			ns
t_H	Data Hold Time (Note 6)		0			0			ns
t_{REL}	Clear Release Time (Note 6)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'LS174 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock			−0.4	mA
			Clear			−0.4	
			Data			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			16	26	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock.

Note 6: T_A = 25°C and V_{CC} = 5V.

Obsolete

'LS174 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		30		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		35		42	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS175			DM74LS175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
t_W	Pulse Width (Note 3)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 3)		20			20			ns
t_H	Data Hold Time (Note 3)		0			0			ns
t_{REL}	Clear Release Time (Note 3)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Obsolete

'LS175 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock			−0.4	mA
			Clear			−0.4	
			Data			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			11	18	mA

'LS175 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		35		42	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

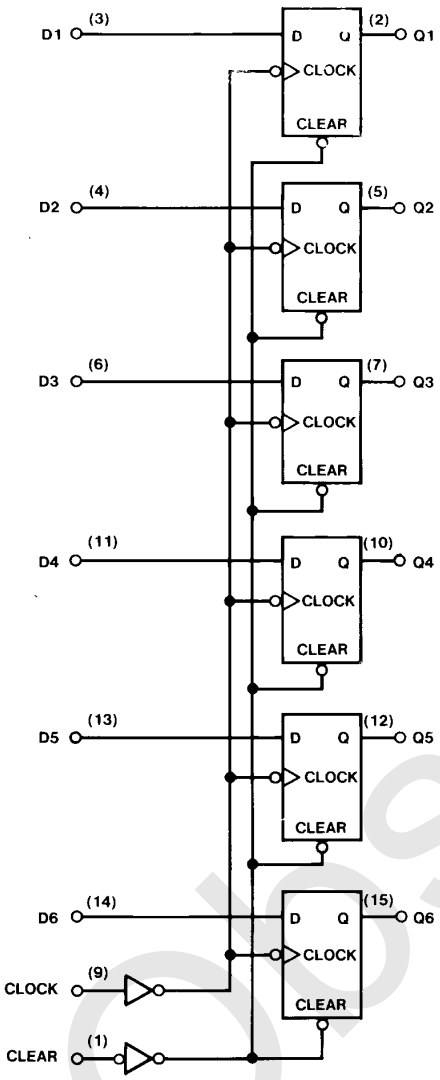
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock input.

Obsolete

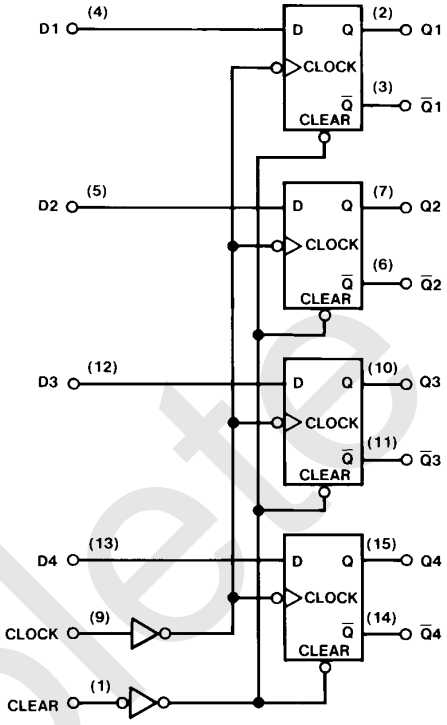
Logic Diagrams

LS174



TL/F/6404–3

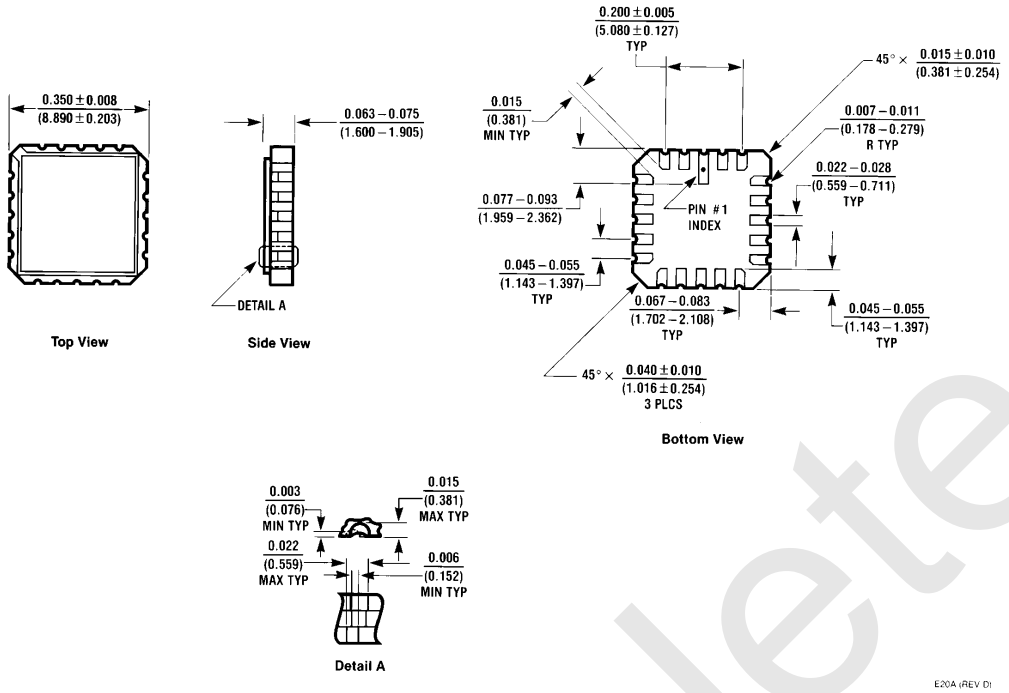
LS175



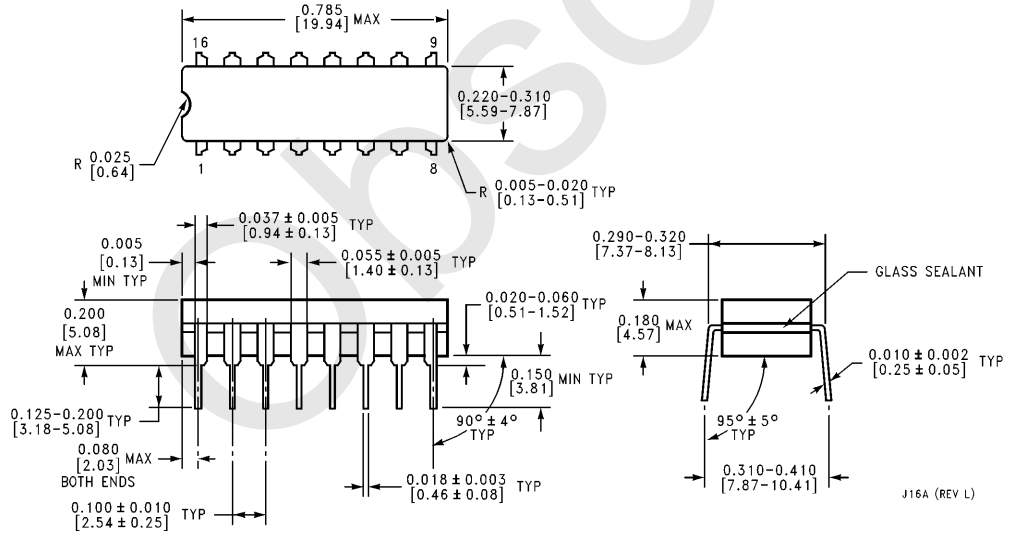
TL/F/6404–4

Obsolete

Physical Dimensions inches (millimeters)



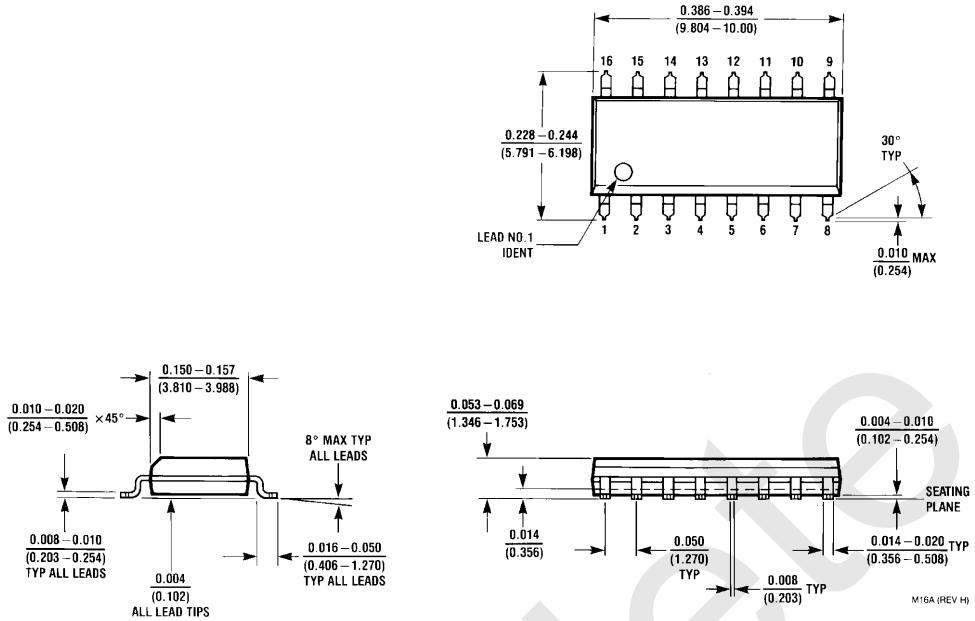
Ceramic Leadless Chip Carrier (E)
Order Number 54LS174LMQB or 54LS175LMQB
NS Package Number E20A



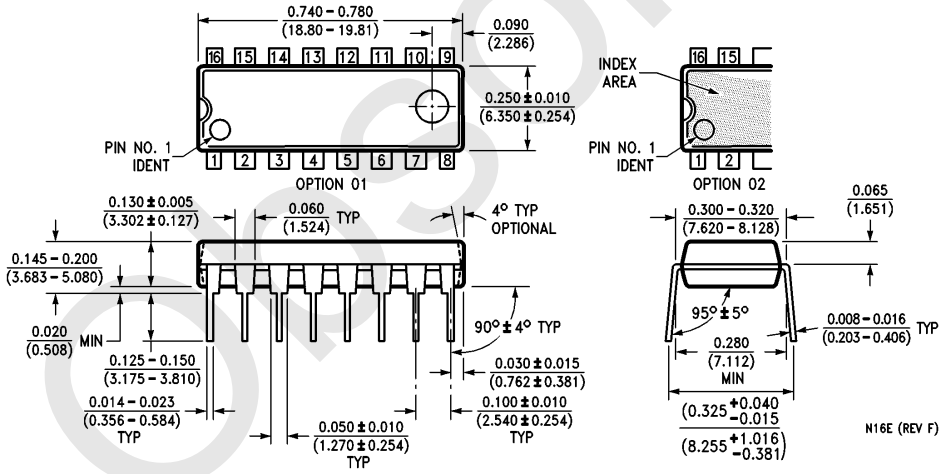
16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS174DMQB, 54LS175DMQB, DM54LS174J or DM54LS175J
NS Package Number J16A

Obsolete

Physical Dimensions inches (millimeters) (Continued)



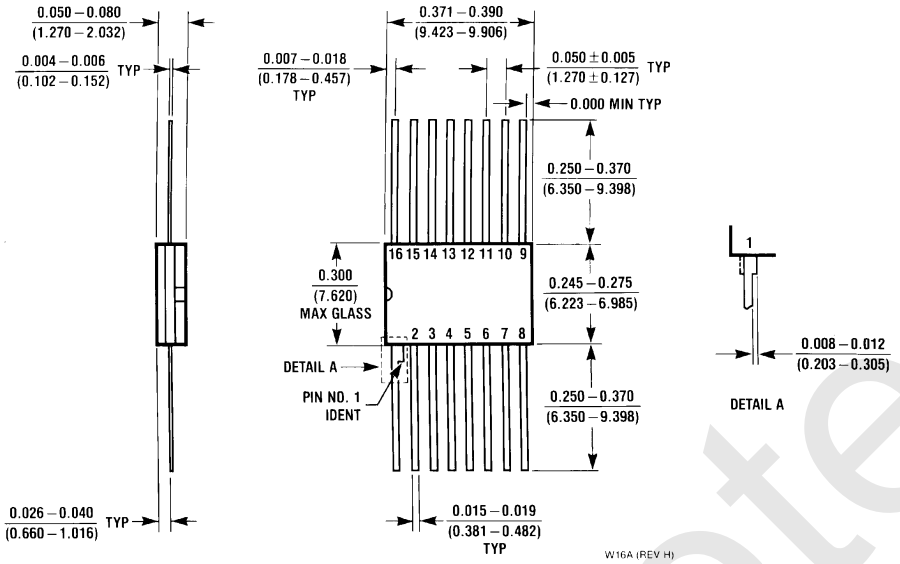
16-Lead Small Outline Molded Package (M)
Order Number DM74LS174M or DM74LS175M
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS174N or DM74LS175N
NS Package Number N16E

Obsolete

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS174FMQB, 54LS175FMQB, DM54LS174W or DM54LS175W
NS Package Number W16A

Obsolete

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