SONY

CXA3556N

IF Down Converter for Digital Broadcast

Description

The CXA3556N is a one-chip integrated IC that processes IF signals of a digital broadcast tuner and includes an AGC amplifier circuit, a mixer circuit, a local oscillator circuit and an output amplifier circuit.

The package utilizes a 24-pin SSOP suitable for surface mounting.

Features

- AGC control width that has a 56dB variable range
- Low noise characteristics
- Low distortion characteristics (in particular, during AGC gain reduction)
- Includes switching function between down converter mode and linear amplifier mode
- Variable output amplifier gain by changing external resistance
- Includes RF AGC output pin
- Variable RF AGC settings
- AGC control curve characteristics with excellent linearity

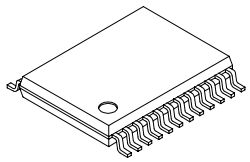
Applications

Digital broadcast tuners

Structure

Bipolar silicon monolithic IC

24 pin SSOP (Plastic)



Absolute Maximum Rating (Ta = 25°C)

• Supply voltage	Vcc	–0.3 to +12	V
• Operating temperature	Topr	–55 to +150	°C

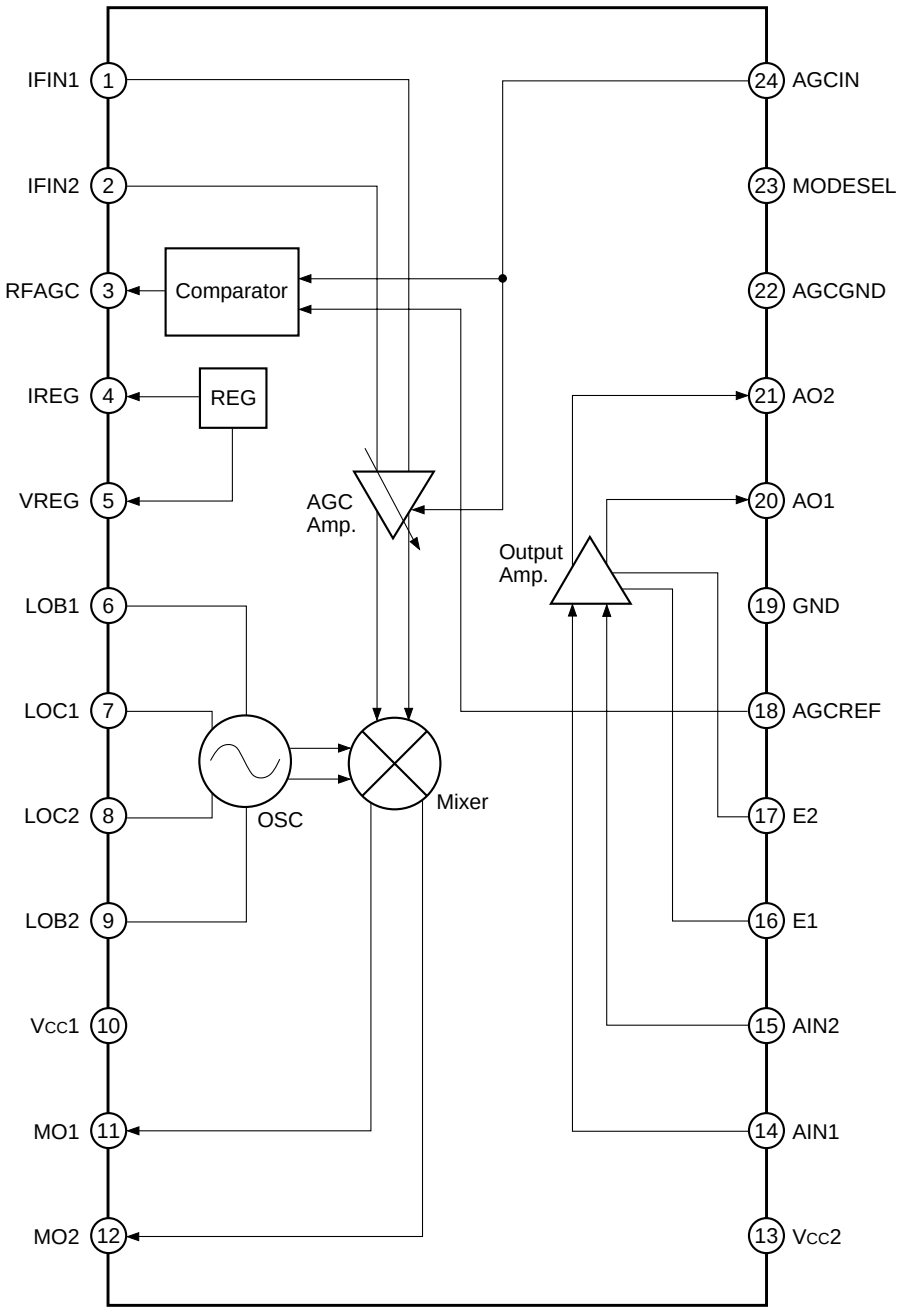
Operating Conditions

• Supply voltage	Vcc	4.75 to 5.25	V
• Operating temperature	Topr	–25 to +75	°C

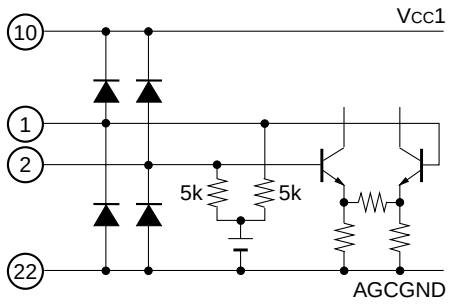
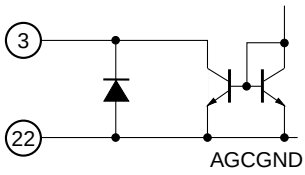
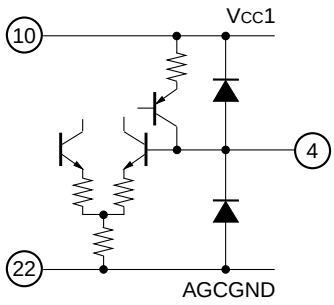
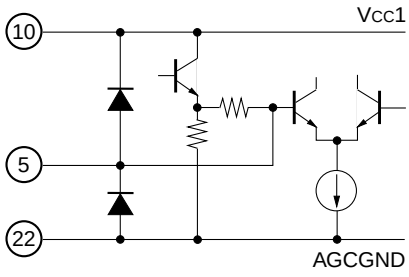
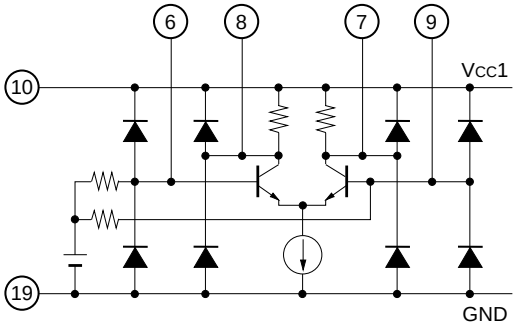
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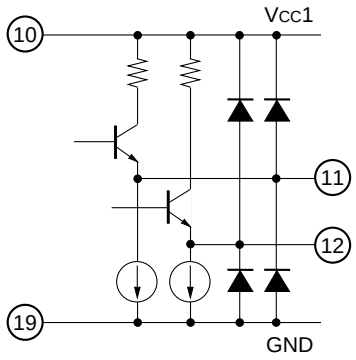
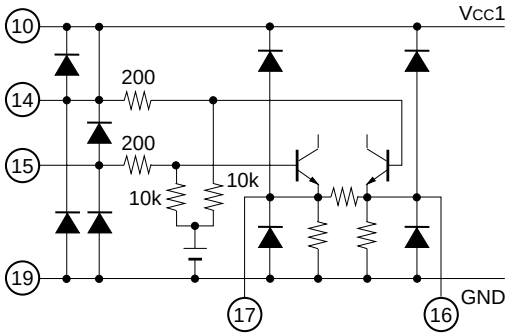
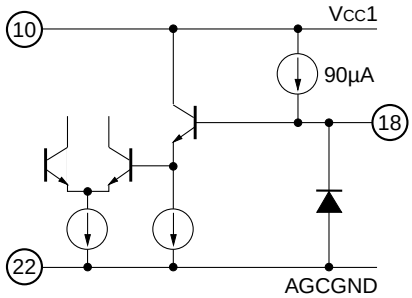
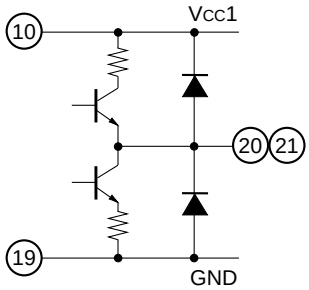
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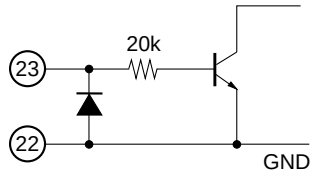
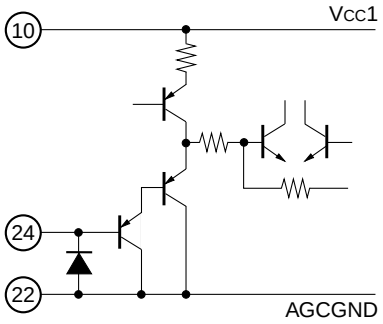
Block Diagram and Pin Configuration



Pin Description and Equivalent Circuit

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin description
1	IFIN1	1.4V		IF inputs.
2	IFIN2	1.4V		
3	RFAGC	—		RF AGC voltage output. Comparator output. Low level: 0.4V or less High level: 8V or more
4	IREG	2.6V		Connects external resistance 27kΩ.
5	VREG	3.3V		Connects external capacitance 1µF.
6	LOB1	2.9V		Connects external capacitance and crystal oscillator.
7	LOC1	3.7V		
8	LOC2	3.7V		
9	LOB2	2.9V		

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin description
10	$V_{CC}1$	5V		Power supply.
11	MO1	2.3V		Mixer output pin.
12	MO2	2.3V		
13	$V_{CC}2$	5V		Power supply.
14	AIN1	1.3V		Output amplifier circuit inputs. Gain of output amplifier circuit can be changed by connecting external resistance between Pins 16 and 17.
15	AIN2	1.3V		
16	E1	0.6V		
17	E2	0.6V		
18	AGCREF	—		RF AGC setting voltage adjustment pin. Connect external resistance between Pin 18 and GND and change the value to change RF AGC output voltage.
19	GND	0V		GND
20	AO1	2.7V		Output amplifier output.
21	AO2	2.7V		

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin description
22	AGCGND	0V		AGC circuit GND.
23	MODESEL	—		Selects either IF down converter mode or linear amplifier mode. When the voltage applied to this pin is 0.3V or less, the mode is down converter mode. When the voltage is 4.75 to 5.25V, the mode is linear amplifier mode.
24	AGCIN	—		AGC control. Input voltage range is 0 to 2.2V.

Electrical Characteristics (V_{CC} = 5V, Ta = 25°C)

(1) IF down converter mode (fvco = 49.38MHz)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption A	$I_{CC}A$	Input signal = no signal AGC_IN voltage = 0V	44	63	77	mA
Gain 1	G1	Input signal = 1 wave (43.5MHz), AGC_IN voltage = 2.2V Output signal = 1Vp-p	65	68.5	73	dB
Gain 2	G2	Input signal = 1 wave (43.5MHz), AGC_IN voltage = 0V Output signal = 1Vp-p	10	12.2	15	dB
Gain width	G3	G3 = G1 – G2	54	56	58	dB
IM3_1	DIS1	Input signal = 2 waves (43.5MHz, 43.6MHz)/–26dBm Output signal = 1Vp-p	–44	–51	—	dBc
IM3_2	DIS2	Input signal = 2 waves (43.5MHz, 43.6MHz)/–21dBm Output signal = 1Vp-p	–42	–51	—	dBc
Output noise 1	NF1	Input signal = –60dBm (43.5MHz) Output signal = 1Vp-p	—	–100	–96	dBc/Hz
Output noise 2	NF2	Input signal = –20dBm (43.5MHz) Output signal = 1Vp-p	—	–120	–111	dBc/Hz

(2) Linear amplifier mode

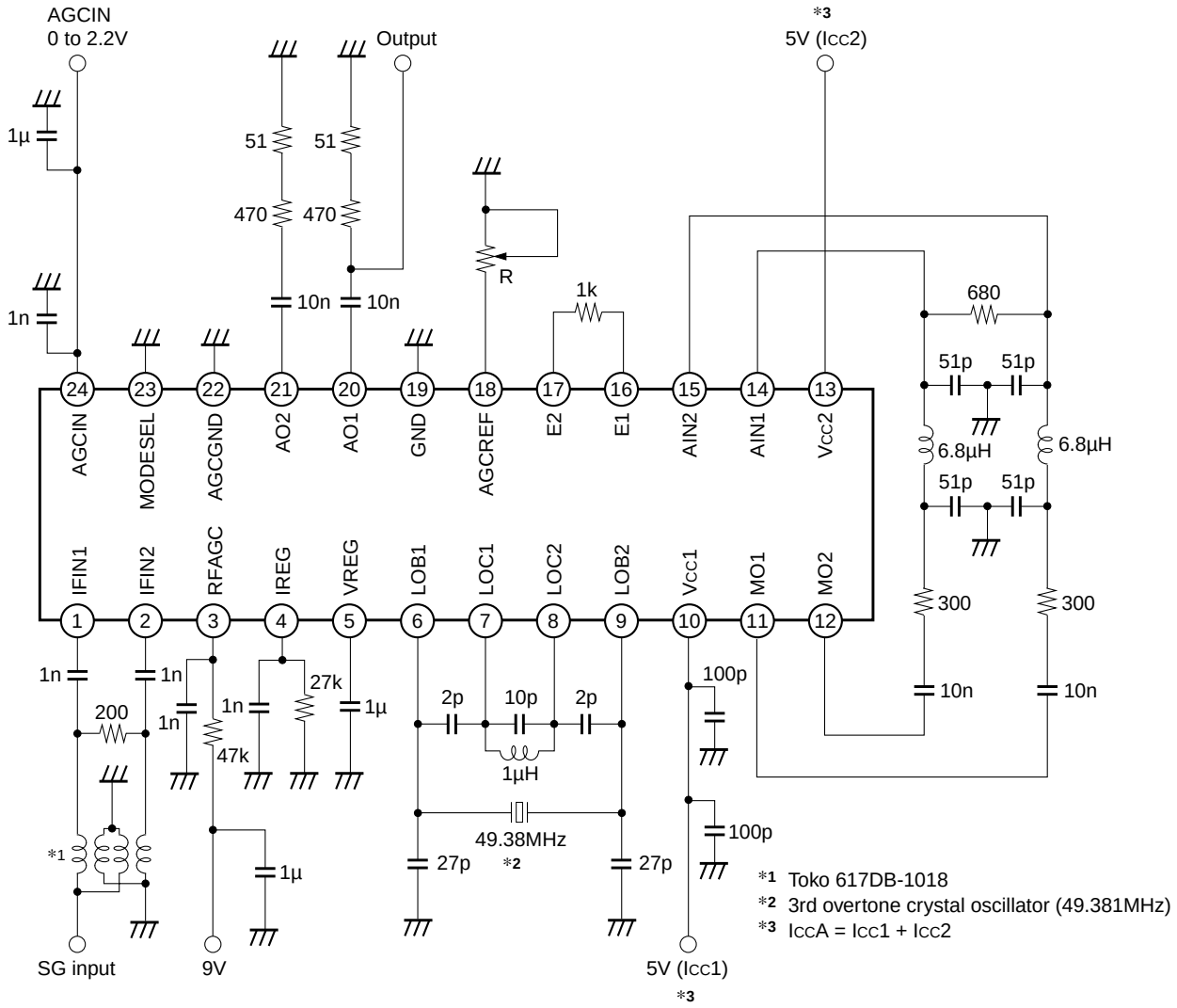
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Current consumption B	$I_{CC}B$	Input signal = no signal AGC_IN voltage = 0V	44	63	77	mA
Gain 4	G4	Input signal = 1 wave (43.5MHz), AGC_IN voltage = 2.2V Output signal = 1Vp-p	65	68.5	73	dB
Gain 5	G5	Input signal = 1 wave (43.5MHz), AGC_IN voltage = 0V Output signal = 1Vp-p	10	12.7	15	dB
Gain width	G6	G6 = G4 – G5	54	56	58	dB
IM3_3	DIS3	Input signal = 2 waves (43.5MHz, 43.6MHz)/–26dBm Output signal = 1Vp-p	–44	–51	—	dBc
IM3_4	DIS4	Input signal = 2 waves (43.5MHz, 43.6MHz)/–21dBm Output signal = 1Vp-p	–42	–51	—	dBc
Output noise 3	NF3	Input signal = –60dBm (43.5MHz) Output signal = 1Vp-p	—	–100	–96	dBc/Hz
Output noise 4	NF4	Input signal = –20dBm (43.5MHz) Output signal = 1Vp-p	—	–120	–111	dBc/Hz

(3) Output amplifier characteristics

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
F characteristics	F	Input signal = 60MHz Short between Pins 16 and 17	–3	–1.5	0	dB

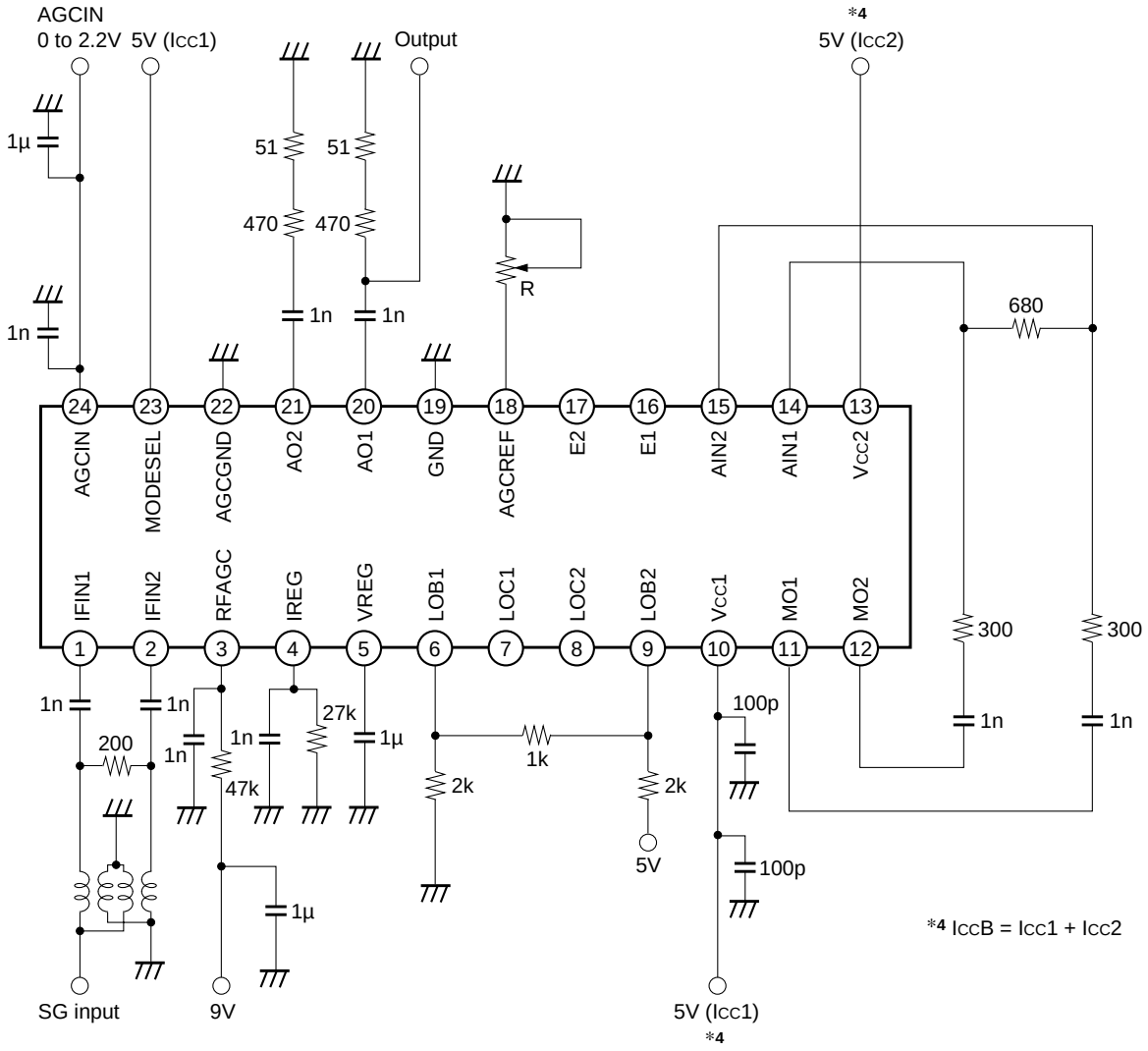
Measurement circuit 1

IF down converter mode



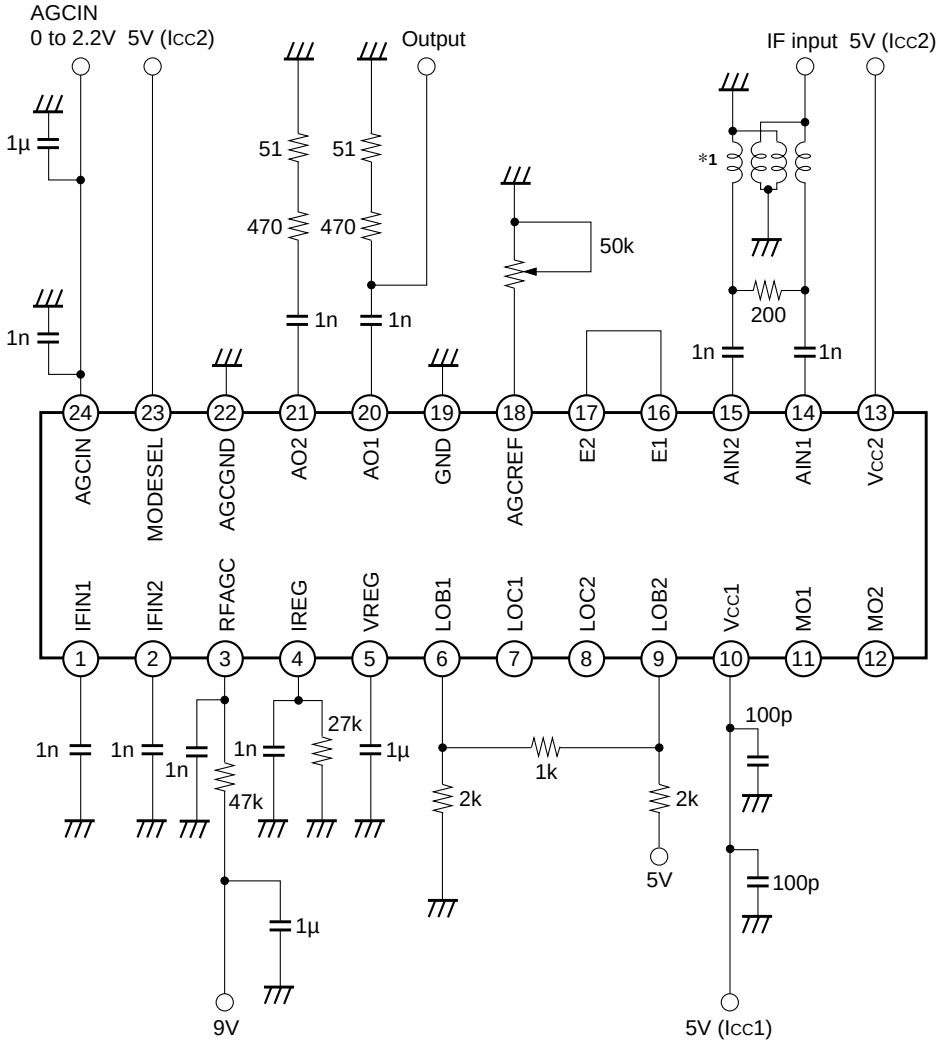
Measurement circuit 2

Linear mode



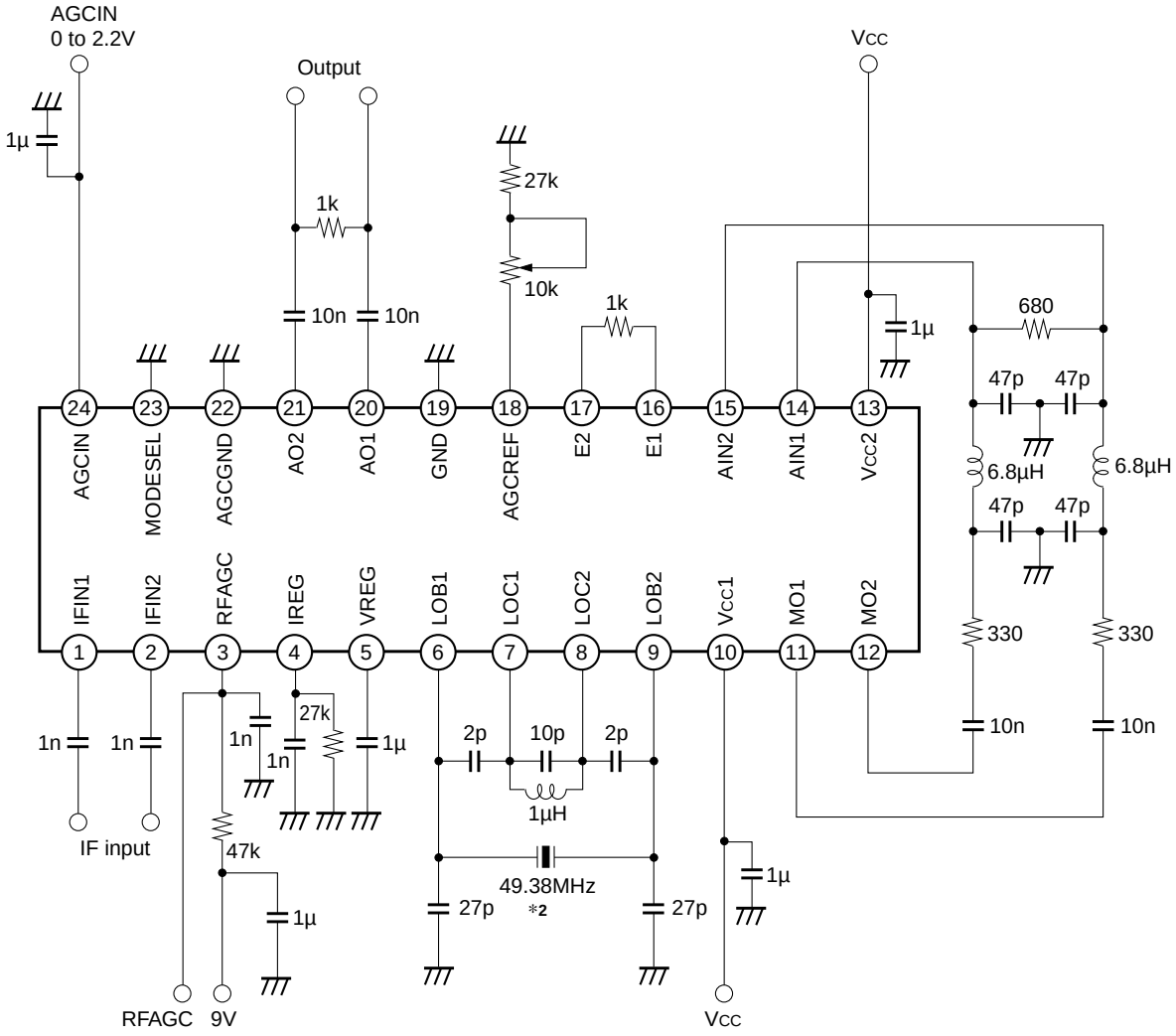
Measurement circuit 3

Output amplifier F characteristics



Application circuit

IF down converter mode



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Functions

The CXA3556N is an IF down converter IC for digital broadcasts. This IC contains a mixer circuit, a local oscillator circuit and an AGC circuit that standardizes IF signals in response to levels of input signals.
It can also operate in a mode other than down converter (linear amplifier mode) and making possible use in a wide variety of digital broadcast tuners. (Control using Pin 23 bias voltage.)

1. AGC Circuit

This is a variable gain amplifier circuit that standardizes output in response to levels of input signals. This circuit has especially excellent low distortion and noise characteristics even when the input level is large. It also has a variable width of 56dB as the gain control range with excellent linearity of the gain control curve.

2. Local Oscillator Circuit

This circuit has a structure that uses a crystal oscillator and oscillates at 3rd overtone frequency. The circuit sets the parallel frequency of the parallel LC resonator between Pins 7 and 8 close to a tertiary overtone frequency (F_{VCO}). This oscillator circuit can also use an LC resonance circuit in place of the crystal oscillator to form an oscillator circuit.

3. Output Amplifier Circuit

Adding a resistor between Pins 16 and 17 allows the gain to be changed in proportion to that resistance. (Refer to characteristic graph Fig. 5 Gain vs. resistance between E1 and E2.)
The output stage of this amplifier is also designed to be 500Ω load/1Vp-p.

4. Mixer Circuit

This circuit outputs the frequency difference between the signal input to IF IN and the local oscillator signal.

5. RF AGC Circuit

This circuit has high image quality in both strong and weak electric fields. In particular, it controls the RF IC gain existing in the first stage of the CXA3556N to delay the characteristics related to S/N to the maximum limits. The circuit controls the RF IC gain using RF AGC voltage (Pin 3) in order that signals input to IF IN (Pins 1, 2) grow larger in weak electric fields. The RF AGC voltage at Pin 3 is obtained from results of a comparison between the AGC control voltage (Pin 24 input voltage) that detects output signals and the voltage at Pin 18 that can be freely set using the resistance value. When the control voltage is low, the RF IC gain decreases and when the control voltage is high, the RF IC gain increases.

IF down converter mode characteristics

Fig. 1. Gain vs. AGCIN voltage

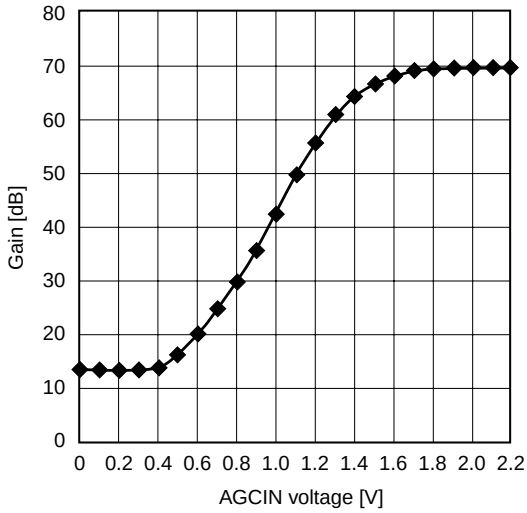


Fig. 2. Output noise vs. input level

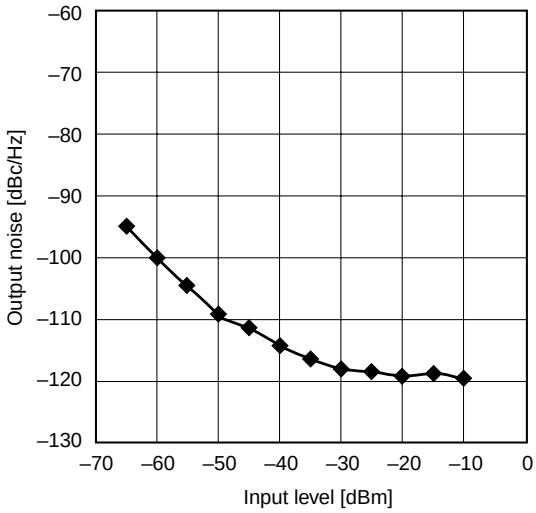


Fig. 3. IM3 vs. input level

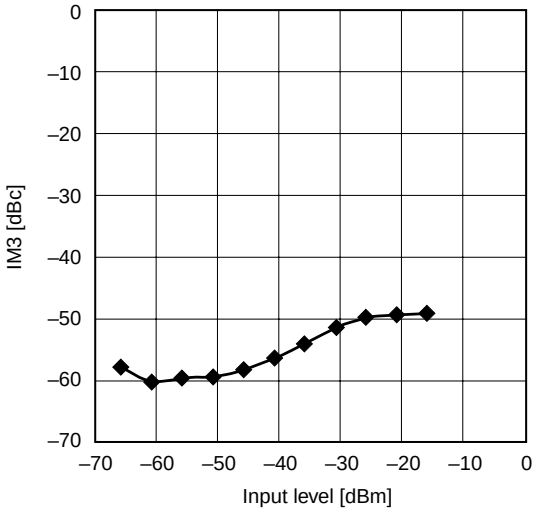


Fig. 4. REFAGC voltage vs. AGCIN voltage

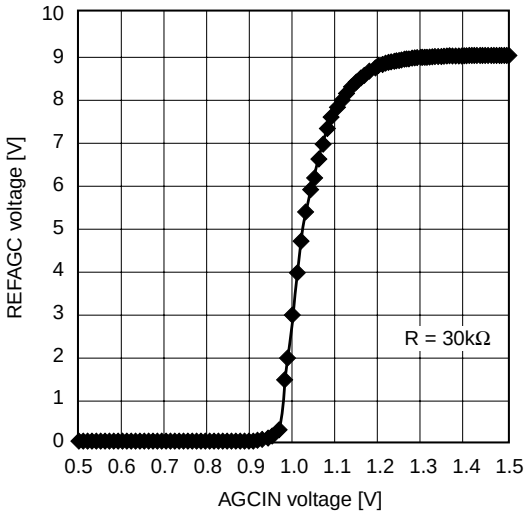
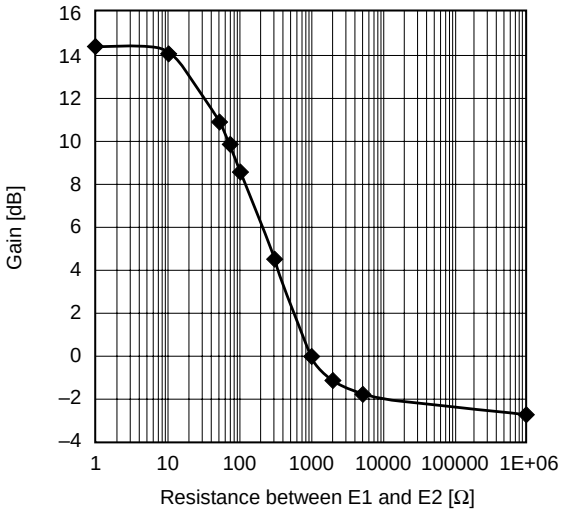
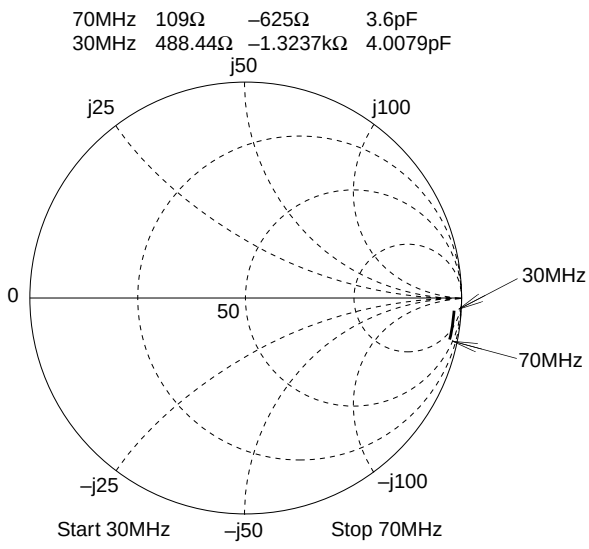


Fig. 5. Gain vs. resistance between E1 and E2



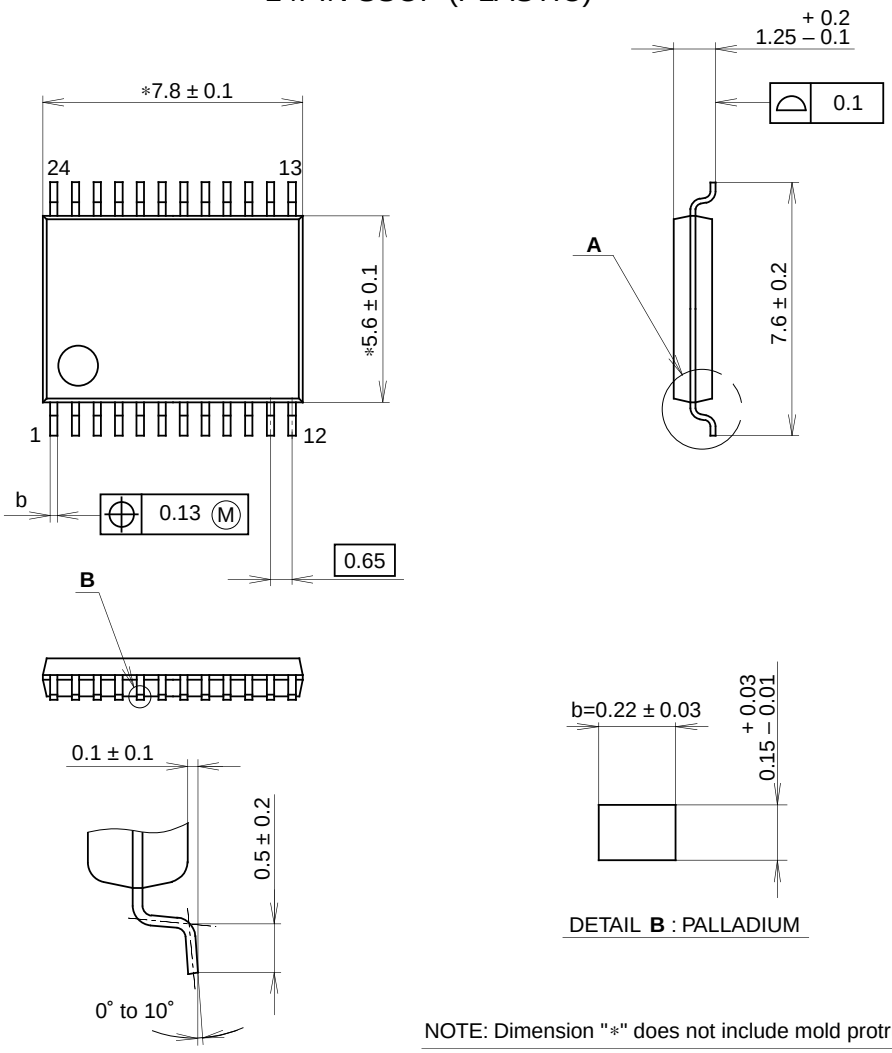
* Gain when 1kΩ is connected between E1 and E2 is 0dB.

Fig. 6. Input characteristics



Package Outline Unit: mm

24PIN SSOP (PLASTIC)



DETAIL **A**

DETAIL **B** : PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	SSOP-24P-L01
EIAJ CODE	P-SSOP24-7.8x5.6-0.65
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g