
MSM7660

Digital Video Decoder (NTSC/PAL Compatible)

GENERAL DESCRIPTION

The MSM7660 is a decoder which converts digitally sampled NTSC or PAL video signals to the format based on ITU-RBT601.

The MSM7660 can accept composite video and S video signals.

For composite signals, the MSM7660 converts signals to YUV data via a 2-dimensional Y/C separation circuit. For S video signals, the MSM7660 converts signals to YUV data by passing the 2-dimensional Y/C separation circuit.

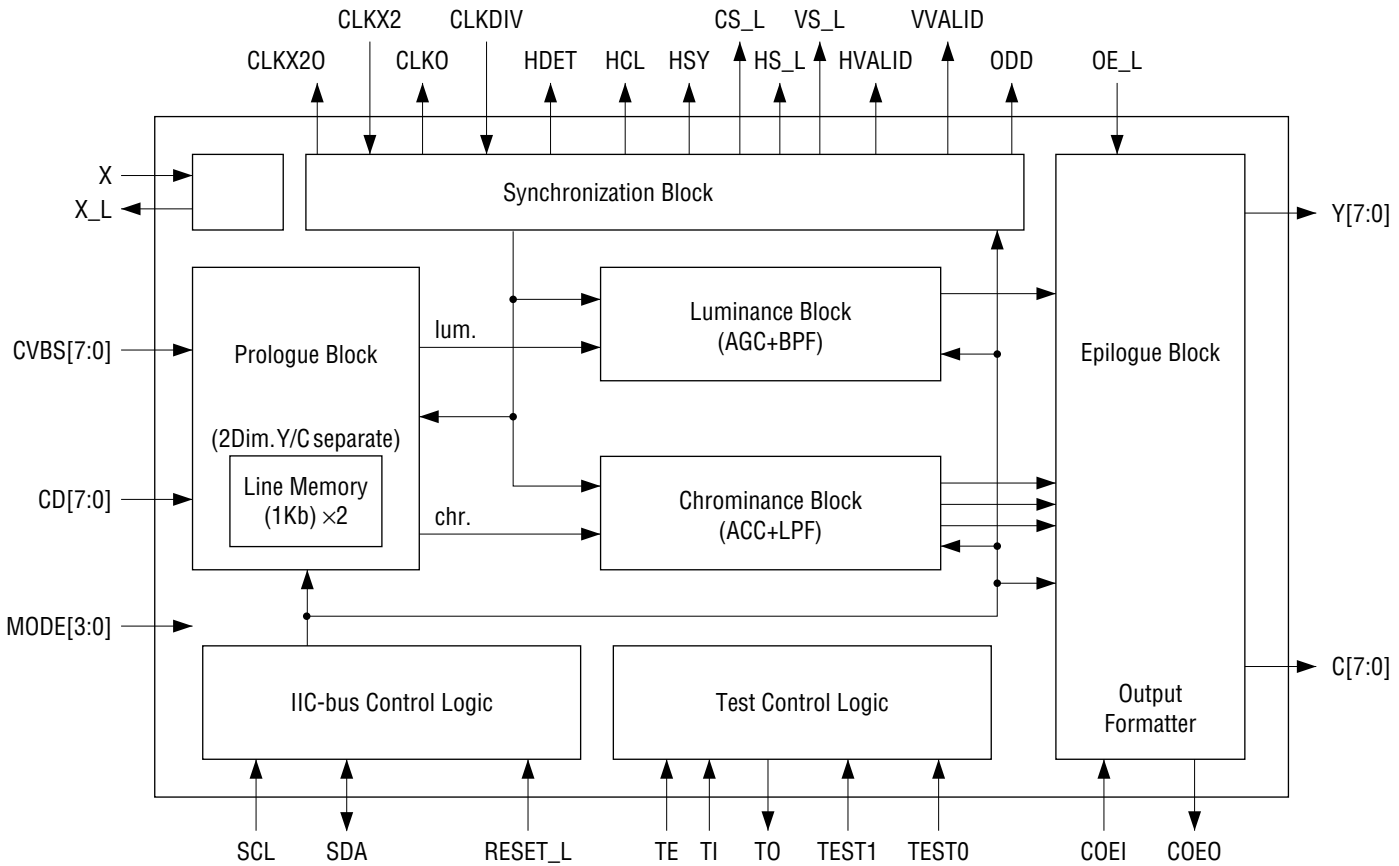
An internal AGC/ACC circuit makes decoding of images relatively easy.

Video signals are internally synchronized, so a relatively wide range of video signals can be decoded without using an external VCO circuit.

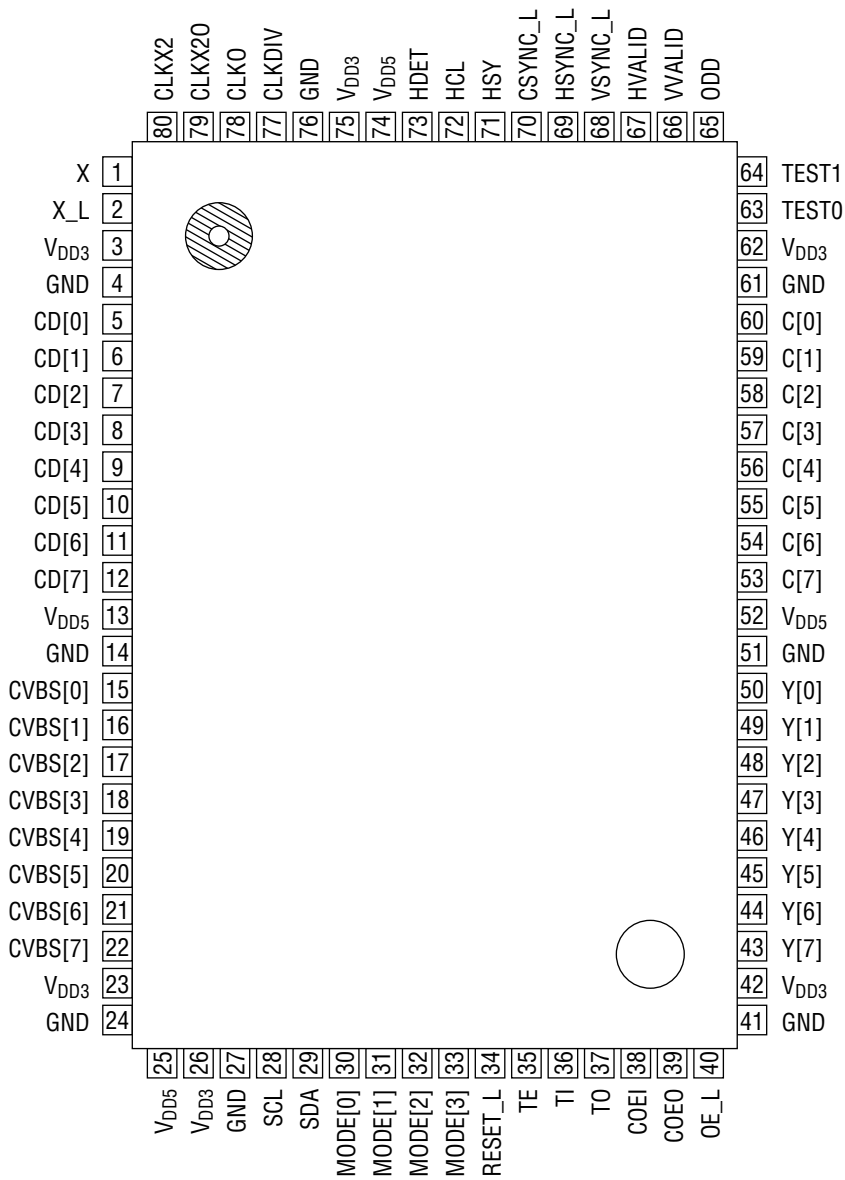
FEATURES

- Accepts composite video and S video signals
- Compatible with NTSC/PAL
- 2-dimensional Y/C separation using adaptive comb filter (this filter is bypassed for S video signal input)
 - NTSC: 3 lines/2 lines
 - PAL: 2 lines
- Sampling frequency
 - 14.75 MHz (PAL Square Pixel)
 - 14.31818 MHz (NTSC 4Fsc)
 - 12.27 MHz (NTSC Square Pixel)
 - 13.5 MHz (ITU-RS601)
- Internal AGC/ACC circuit
- 8-bit Y/C (CbCr) output (conforms to ITU-RBT601)
 - YCbCr: 4:2:2
 - YCbCr: 4:1:1
- High impedance output possible, priority cascade control function
- I²C-BUS interface
- External terminal mode (default) or internal register mode can be selected for operation mode setting.
- A frequency one or two times the sampling clock is supplied to LSI
- Power consumption: 500 mW (Typ. 13.5 MHz)
- Package:
 - 80-pin plastic QFP (QFP80-P-1420-0.80-BK) (Product name: MSM7660GS-BK)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic QFP

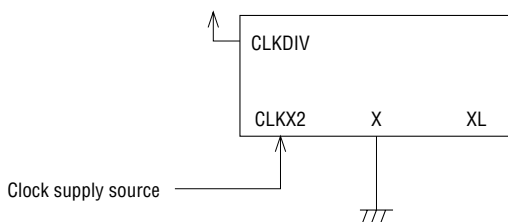
PIN DESCRIPTIONS

| Pin | Symbol | I/O | Description |
|----------|------------------|-----|--|
| 1 | X | I | Test pin. Normally, to "L" level. |
| 2 | X_L | O | Unused pin. |
| 3 | V _{DD3} | | Internal logic power supply (3.3 V typ.) |
| 4 | GND | | |
| 5 to 12 | CD[0 to 7] | I | Chrominance signal input pin (valid only for S video input) Set to "L" level at composite signal input |
| 13 | V _{DD5} | | Peripheral I/O power supply (5 V typ.) |
| 14 | GND | | |
| 15 to 22 | CVBS[0 to 7] | I | Composite digital data input pin Luminance signal is input for S video input. |
| 23 | V _{DD3} | | Internal logic power supply (3.3 V typ.) |
| 24 | GND | | |
| 25 | V _{DD5} | | Peripheral I/O power supply (5 V typ.) |
| 26 | V _{DD3} | | Internal logic power supply (3.3 V typ.) |
| 27 | GND | | |
| 28 | SCL | I | I ² C-bus clock pin |
| 29 | SDA | I/O | I ² C-bus data pin |
| 30 to 33 | MODE[0 to 3] | I | Mode input pins. Dip switches can be used because these pins are internally pulled-up. MODE[3] 0: composite 1: S video MODE[2:0] 000: NTSC ITU-RS601 13.5MHz 001: NTSC Square Pixel 12.27 MHz 010: NTSC 4Fsc 14.32 MHz 100: PAL ITU-RS601 13.5 MHz 101: PAL Square Pixel 14.75 MH others: Undefined |
| 34 | RESET_L | I | System reset input pin (active at "L") |
| 35 | TE | I | Test pin. Normally, set to "L" level |
| 36 | TI | I | Test pin. Normally, set to "L" level |
| 37 | TO | O | Test pin |
| 38 | COEI | I | Cascade priority control input pin Connected to COEO of decoder with higher priority. |
| 39 | COEO | O | Cascade priority control output pin Outputs "L" when COEI is "L" or when this LSI is in output enable status. |
| 40 | OE_L | I | Y/C/HSYNC-L/VSYNC-L output enable input pin (active at "L") OR condition with register setting |
| 41 | GND | | |
| 42 | V _{DD3} | | Internal logic power supply (3.3 V typ.) |

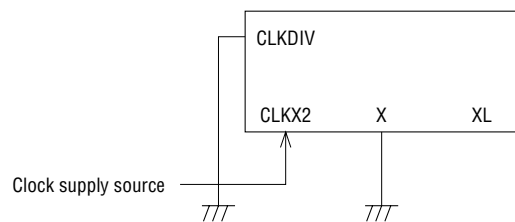
| Pin | Symbol | I/O | Description |
|----------|----------------------|-----|---|
| 43 to 50 | Y[7 to 0] | 0 | Luminance signal output pin |
| 51 | GND | | |
| 52 | V _{DD5} | | Peripheral I/O power supply (5.0 V typ.) |
| 53 to 60 | C[7 to 0] | 0 | Chrominance signal output pin |
| 61 | GND | | |
| 62 | V _{DD3} | | Internal logic power supply (3.3 V typ.) |
| 63 | TEST0 | I | Input pin for testing. Normally use this pin at open state or "H" level. |
| 64 | TEST1 | I | Input pin for testing. Normally use this pin at open state or "H" level. |
| 65 | ODD | 0 | Field display output pin Outputs "H" for odd field. |
| 66 | VVALID | 0 | Vertical valid line timing output pin |
| 67 | HVALID | 0 | Horizontal valid pixel timing output pin |
| 68 | VS _{YNC} _L | 0 | V sync output pin |
| 69 | HS _{YNC} _L | 0 | H sync output pin |
| 70 | CS _{YNC} _L | 0 | Composite sync output pin |
| 71 | HSY | 0 | Sync chip timing output pin for AD converter |
| 72 | HCL | 0 | Clamp timing output pin for AD converter |
| 73 | HDET | 0 | HLOCK synchronization detection display output pin (Outputs "H" when H synchronization is established.) |
| 74 | V _{DD5} | | Peripheral I/O power supply (5.0 V typ.) |
| 75 | V _{DD3} | | Internal logic power supply (3.3 V typ.) |
| 76 | GND | | |
| 77 | CLKDIV | I | Clock select input pin Inputs "H" when a half CLKX2 is used as the internal clock. |
| 78 | CLKO | 0 | Clock output pin Outputs internal clock. |
| 79 | CLKX20 | 0 | Clock output pin Bypasses clock input and outputs clock input. |
| 80 | CLKX2 | I | Clock input pin (a clock one or two times the sampling clock is input) |

[Clock supply method and handling]

1. Supplying double pixel clock from external supply source



2. Supplying pixel clock from external supply source



ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|----------------------|-----------|--------------------------|-------------------------|--------------------|
| Power Supply Voltage | V_{DD5} | $T_a=25^{\circ}\text{C}$ | -0.3 to +7 | V |
| | V_{DD3} | $T_a=25^{\circ}\text{C}$ | -0.3 to +4.5 | |
| Input Voltage | V_I | $T_a=25^{\circ}\text{C}$ | -0.3 to $V_{DD5} + 0.3$ | V |
| Power Consumption | P_W | — | 800 | mW |
| Storage Temperature | T_{STG} | — | -55 to +150 | $^{\circ}\text{C}$ |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-----------------------------|----------------|--------------------------|--------------|------|-----------|--------------------|
| Power Supply Voltage | V_{DD5} | $T_a=25^{\circ}\text{C}$ | 4.5 | 5.0 | 5.5 | V |
| | V_{DD3} | $T_a=25^{\circ}\text{C}$ | 3.0 | 3.3 | 3.6 | |
| Power Supply Voltage | GND | $T_a=25^{\circ}\text{C}$ | — | 0.0 | — | V |
| High Level Input Voltage | V_{IH1} | — | 2.2 | — | V_{DD5} | V |
| High Level Input Voltage | $V_{IH2} (*1)$ | — | $0.8V_{DD5}$ | — | V_{DD5} | V |
| Low Level Input Voltage | V_{IL} | — | 0.0 | — | 0.8 | V |
| Operating Temperature Range | T_a | — | 0 | — | 70 | $^{\circ}\text{C}$ |

*1: CCKX2, CLKDIV, SDA

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta=0 to 70°C, VDD3=3.3V±0.3V, VDD5=5V±10%)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | |
|----------------------------------|------------------------------|---|---------------------|------|------------------|------|----|
| High Level Output Voltage | V _{OH} | I _{OH} =-2mA (*1) | 0.8V _{DD5} | — | V _{DD5} | V | |
| | | I _{OH} =-4mA (*2) | | | | | |
| | | I _{OH} =-8mA (*3) | | | | | |
| Low Level Output Voltage | V _{OL} | I _{OL} =2mA (*1) | 0 | — | 0.8 | V | |
| | | I _{OL} =4mA (*2) | | | | | |
| | | I _{OL} =8mA (*3) | | | | | |
| Input Leak Current | I _I | V _I =GND to V _{DD5} | -10 | — | 10 | μA | |
| | | V _I =GND to V _{DD5} PULL-UP=50k (*4) | -250 | — | -20 | | |
| Output Leak Current | I _O | V _I =GND to V _{DD5} | -10 | — | 10 | μA | |
| Power Supply Current (operating) | I _{DD} | CLK=15MHz | 3V system | — | 110 | 150 | mA |
| | | | 5V system | — | 20 | 30 | mA |
| Power Supply Current (standby) | I _{DDs} | 3V system | — | 1 | 3 | mA | |
| | | 5V system | — | 50 | 200 | μA | |
| SDA Output Voltage | SDA _{V_L} | — | 0 | — | 0.4 | V | |
| SDA Output Current | SDA _{I_O} | — | 3 | — | | mA | |

*1: TO

*2: HSYNC_L, VSYNC_L, HDET, COEO

*3: Y[7:0], C[7:0], HCL, HSY, HSY, CSYNC_L, HVALID, VVALID, ODD, CLKX2O, CLKO

*4: MODE[3:0], COEI, TEST0, TEST1

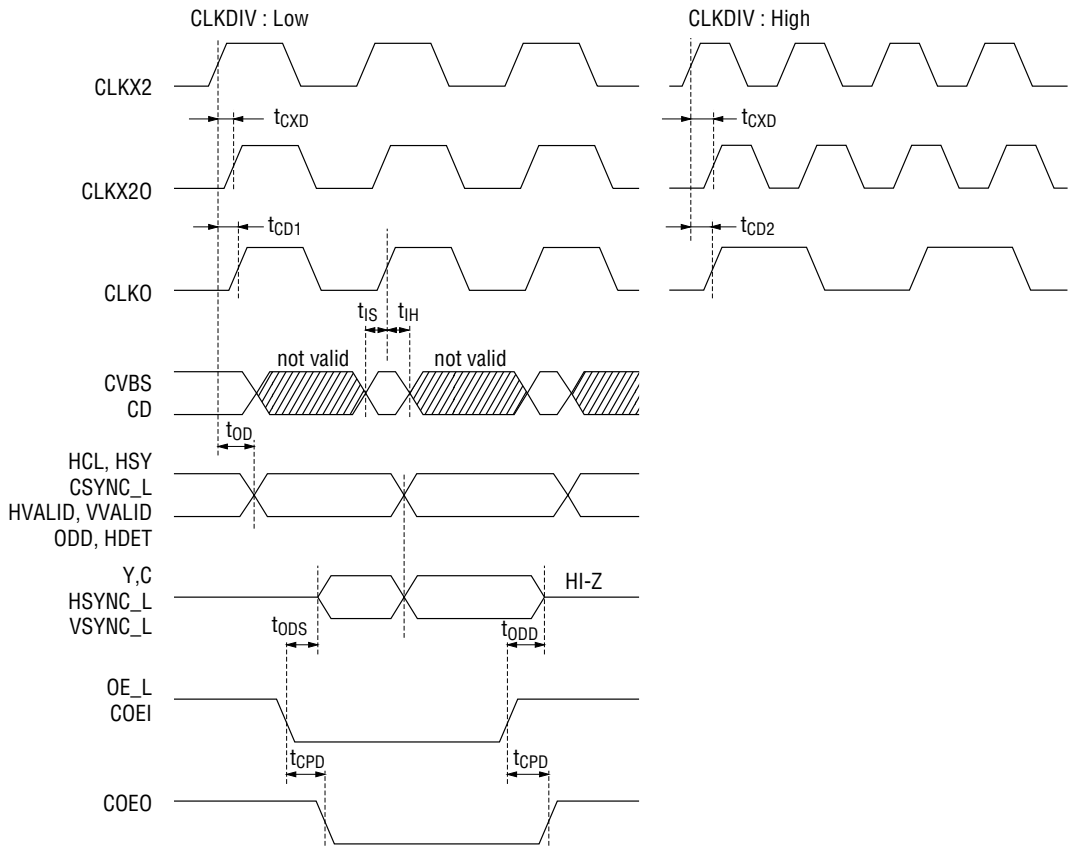
AC Characteristics

(Ta=0 to 70°C, V_{DD3}=3.3V±0.3V, V_{DD5}=5V±0.5V)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--|------------------------------------|-------------------|------|-------|------|------|
| CLKX2 cycle time | t _{CLKX2} | PAL Square Pixel | — | 33.9 | — | ns |
| | | NTSC 4Fsc | — | 34.9 | — | ns |
| | | NTSC Square Pixel | — | 40.75 | — | ns |
| | | ITU-RS601 | — | 37.05 | — | ns |
| Input Data Setup Time | t _{IS} | — | 20 | — | — | ns |
| Input Data Hold Time | t _{IH} | — | 0 | — | — | ns |
| Output Data Delay Time* | t _{OD} | — | 5 | — | 30 | ns |
| Output Data Set Time* | t _{ODS} | — | 2 | — | 12 | ns |
| Output Data Disable Time* | t _{ODD} | — | 2 | — | 13 | ns |
| Cascade Priority Signal Delay Time* | t _{CPD} | — | 2 | — | 14 | ns |
| Output Clock Delay Time* | t _{CXD} | — | 5 | — | 14 | ns |
| Output Clock Delay Time* (CLKDIV: Low) (Internal clock) | t _{CD1} | — | 6 | — | 20 | ns |
| | (CLKDIV: High) t _{CD2} | — | 8 | — | 22 | ns |
| Clock Cycle Time | t _{C_SCL} | Rpull_up=4.7kΩ | 200 | — | — | MHz |
| Clock Duty Cycle | t _{D_SCL} | — | — | 50 | — | % |
| Low level Cycle | t _{L_SCL} | Rpull_up=4.7kΩ | 100 | — | — | ns |

(*output load 15pF)

Input and Output Timing



BLOCK DESCRIPTION

1. Prologue Block

The prologue Block performs Y/C separation using a 2-dimensional adaptive comb filter when composite signals (CVBS) are input.

The following operation modes can be changed via the I²C-bus. The * mark indicates a default. The default is a state that is selected when reset.

- 1) Video input mode select
 - Composite video input *
 - S video input
- 2) Video input mode select
 - NTSC system*
 - PAL system
- 3) Operation mode select

| | |
|--------------------------------|-----------|
| NTSC ITU recommendation BT.601 | 13.5MHz* |
| MTSC Square Pixel | 12.27MHz |
| NTSC 4Fsc | 14.32 MHz |
| PAL ITU recommendation BT.601 | 13.5MHz |
| PAL Square Pixel | 14.75 MHz |
- 4) Y/C separation mode select
 - Adaptive comb filter is used. *
 - Unadaptive comb filter is used.
 - Comb filter is not used.

The adaptive comb filter detects the correlation up to 3 lines between continuous lines. The Y/C is separated by the comb filter according to the way of correlation if these lines are correlated. The Y/C is separated by the trap filter if these lines are not correlated not correlated (only 2 lines in the case of PAL).

In the unadaptive comb filter, the Y/C is always separated by removing the luminance component based on the average of preceding and following lines (when there is the correlation between 3 lines).

If the comb filter is not used, the Y/C is separated by the trap filter.

The Y/C separation circuit is bypassed by S video signal input.

In addition, the functions of this block work only when lines are valid as image information.

The processing of CVBS signals is not made during V-blanking.

2. Luminance Block

The luminance block removes synchronous signals from the signals containing luminance components after Y/C separation. The signals are corrected and output as luminance signals. This block can select the following operation modes.

- 1) Use of prefilter and sharp filter
 - Used*
 - Not used

These filters are used for enhancing the edges of luminance component signals.

- | | |
|---|----------------------|
| 2) AGC loop filter time constant select | |
| slow | Factor value 1/1024n |
| medium | 1/64n* |
| fast | 1/n |
| fixed | 0 |

3) Parameter for AGC reference level fine adjustment

4) Parameter for sync separation level fine adjustment

The luminance signals are synchronized by AGC correction values obtained by the above processings

- 5) Selection of aperture bandpass filter coefficient
- middle range*
 - high range

- 6) Coring range select off*
- ±4LBS
 - ±5LBS
 - ±7LBS

- 7) Aperture weighting factor select
- 0*
 - 0.25
 - 0.75
 - 1.5

The profile of these signals can be corrected by coring and aperture correction.

- 8) Use of pixel position correction circuit
- Used*
 - Not used

3. Chrominance Block

This is a chroma signal processing block.
The following modes can be selected.

- 1) Use of color bandpass filter
- Used*
 - Not used
- 2) AGC loop filter time constant select
- | | |
|--------|----------------------|
| slow | Factor value 1/1024n |
| medium | 1/64n* |
| fast | 1/n |
| fixed | 0 |
- 3) Parameter for burst level fine adjustment

- 4) The threshold level for valid chroma amplitude is selected base on a color burst ratio.
 - 0.5
 - 0.25*
 - 0.125
- 5) Color killer mode select
 - Auto color killer mode*
 - Forcible color killer

6) Parameter for color subcarrier phase fine adjustment

In this block, chroma signals pass through the chroma bandpass filter to cut an unnecessary band. To maintain a constant chroma level, UV demodulation is performed on these signals via the ACC correction circuit. (this filter can be bypassed.)

If the demodulation result does not reach a specified level, color killer signals are generated to fix the ACC gain. This functions as an auto color killer control circuit.

The UV demodulation result is output as chrominance signals via a low pass filter.

4. Synchronization Block

This is a synchronizing signal processing block.

Chip output synchronizing signals and synchronizing signals for internal use are generated by this block. Various signals are output in this block and the following operation modes can be selected.

- 1-1) Fine adjustment of HSY signal (start side)
- 1-2) Fine adjustment of HSY signal (stop side)
- 2-1) Fine adjustment of HCL signal (start side)
- 2-2) Fine adjustment of HCL signal (stop side)
- 3) HSY, HCL signal enable select
 - High Level*
 - Active

These signal are used to sink chip and clamp timing to the A/D converter
- 4) Fine adjustment of HSYNC_L signal
- 5-1) Fine adjustment of HVALID signal (start side)
- 5-2) Fine adjustment of HVALID signal (stop side)
- 6-1) Fine adjustment of VVALID signal (start side)
- 6-2) Fine adjustment of VVALID signal (stop side)

The data signals are transmitted or received at the rising edge of the HVALID signal.

- 7) TV, VTR mode select
 - TV mode
 - VTR mode*

The TV mode or VTR mode in synchronizing mode is selected.

The TV mode outputs a fixed pixel number per one line.

The VTR mode outputs the results of decoding in accordance with the HSYNC signal regardless

of whether a jitter exists or not. Some VTR may disturb synchronization.

5. Epilogue Block

The Epilogue Block outputs UV signals from the chrominance block and Y signals from the luminance block in the format based on the signal obtained by setting of the control register.

In this block, the following modes can be selected.

- 1) Display of blue back when synchronization fails.

OFF

ON*

- 2) Output signal Y/CbCr format select

YCbCr 4 : 1 : 1

YCbCr 4 : 2 : 2*

The chrominance signal (U, V component) outputs Cb and Cr data to the C pin in an output format described later.

- 3) Selection of 8-bit chroma signal output format

Offset binary*

2's Complement

- 4) Output pin enable select

High impedance

Output enable*

The Epilogue Block has a high impedance priority cascade control function to enable the bus connection of output signals. The target tristate buses are Y, C, HSYNC_L and VSYNC_L, and this block makes an output enable instruction for these signals

- 5) Luminance signal phase adjustment

normal*

forward 1 clock

backward 1 clock

- 6) Chrominance signal phase adjustment

normal*

forward 1 clock

backward 1 clock

6. I²C Control Block

This is the serial interface block based on the I²C standard of Phillips Corporation.

This block functions only as a Slave-Receiver.

The external control can set the internal registers (MRA, MRB, HSYT, etc.).

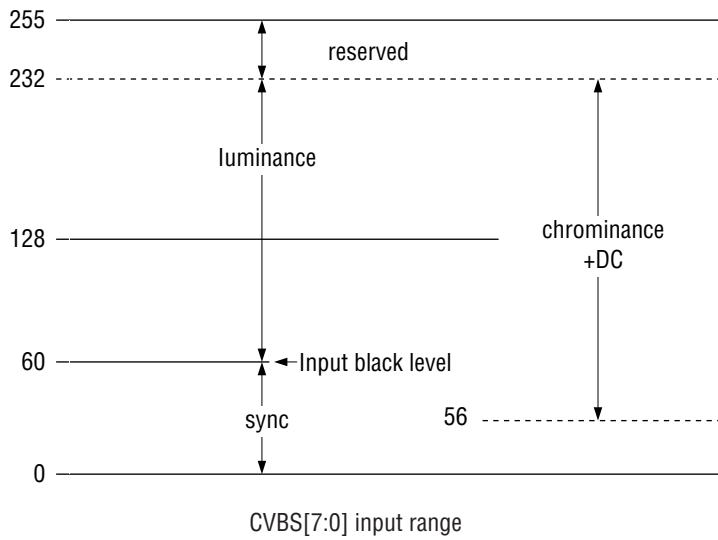
7. Test Control Block

This block is used to test this LSI. Normally it is not used.

FUNCTIONAL DESCRIPTION

Input Signal Level

Input signal is 8-bit in a straight binary format.
The recommended input range is shown below.



Output format

The YCbCr 4:2:2 format and 4:1:1 format are shown below.
 The output format can be changed by register settings.

| OUTPUT | PIXEL BYTE SEQUENCE | | | | | |
|---------|---------------------|-----|-----|-----|-----|-----|
| Y7(MSB) | Y7 | Y7 | Y7 | Y7 | Y7 | Y7 |
| Y6 | Y6 | Y6 | Y6 | Y6 | Y6 | Y6 |
| Y5 | Y5 | Y5 | Y5 | Y5 | Y5 | Y5 |
| Y4 | Y4 | Y4 | Y4 | Y4 | Y4 | Y4 |
| Y3 | Y3 | Y3 | Y3 | Y3 | Y3 | Y3 |
| Y2 | Y2 | Y2 | Y2 | Y2 | Y2 | Y2 |
| Y1 | Y1 | Y1 | Y1 | Y1 | Y1 | Y1 |
| Y0(LSB) | Y0 | Y0 | Y0 | Y0 | Y0 | Y0 |
| C7(MSB) | Cb7 | Cr7 | Cb7 | Cr7 | Cb7 | Cr7 |
| C6 | Cb6 | Cr6 | Cb6 | Cr6 | Cb6 | Cr6 |
| C5 | Cb5 | Cr5 | Cb5 | Cr5 | Cb5 | Cr5 |
| C4 | Cb4 | Cr4 | Cb4 | Cr4 | Cb4 | Cr4 |
| C3 | Cb3 | Cr3 | Cb3 | Cr3 | Cb3 | Cr3 |
| C2 | Cb2 | Cr2 | Cb2 | Cr2 | Cb2 | Cr2 |
| C1 | Cb1 | Cr1 | Cb1 | Cr1 | Cb1 | Cr1 |
| C0(LSB) | Cb0 | Cr0 | Cb0 | Cr0 | Cb0 | Cr0 |
| Y point | 0 | 1 | 2 | 3 | 4 | 5 |
| C point | 0 | | 2 | | 4 | |

YCbCr 4:2:2 format

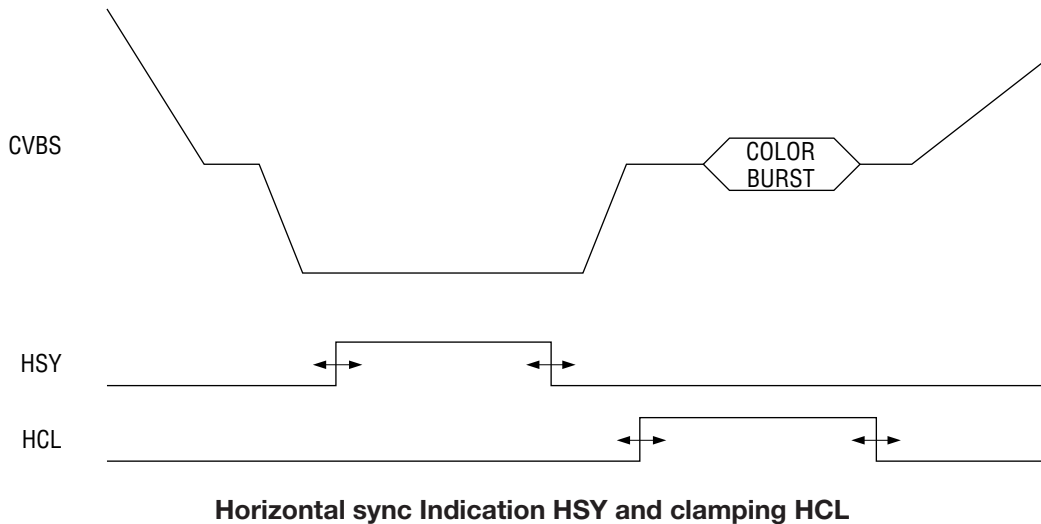
| OUTPUT | PIXEL BYTE SEQUENCE | | | | | | | |
|---------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Y7(MSB) | Y7 | Y7 | Y7 | Y7 | Y7 | Y7 | Y7 | Y7 |
| Y6 | Y6 | Y6 | Y6 | Y6 | Y6 | Y6 | Y6 | Y6 |
| Y5 | Y5 | Y5 | Y5 | Y5 | Y5 | Y5 | Y5 | Y5 |
| Y4 | Y4 | Y4 | Y4 | Y4 | Y4 | Y4 | Y4 | Y4 |
| Y3 | Y3 | Y3 | Y3 | Y3 | Y3 | Y3 | Y3 | Y3 |
| Y2 | Y2 | Y2 | Y2 | Y2 | Y2 | Y2 | Y2 | Y2 |
| Y1 | Y1 | Y1 | Y1 | Y1 | Y1 | Y1 | Y1 | Y1 |
| Y0(LSB) | Y0 | Y0 | Y0 | Y0 | Y0 | Y0 | Y0 | Y0 |
| C7(MSB) | Cb7 | Cb5 | Cb3 | Cb1 | Cb7 | Cb5 | Cb3 | Cb1 |
| C6 | Cb6 | Cb4 | Cb2 | Cb0 | Cb6 | Cb4 | Cb2 | Cb0 |
| C5 | Cr7 | Cr5 | Cr3 | Cr1 | Cr7 | Cr5 | Cr3 | Cr1 |
| C4 | Cr6 | Cr4 | Cr2 | Cr0 | Cr6 | Cr4 | Cr2 | Cr0 |
| C3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| C2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| C1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| C0(LSB) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Y point | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| C point | 0 | | | | 4 | | | |

YCbCr 4:1:1 format

Timing Description

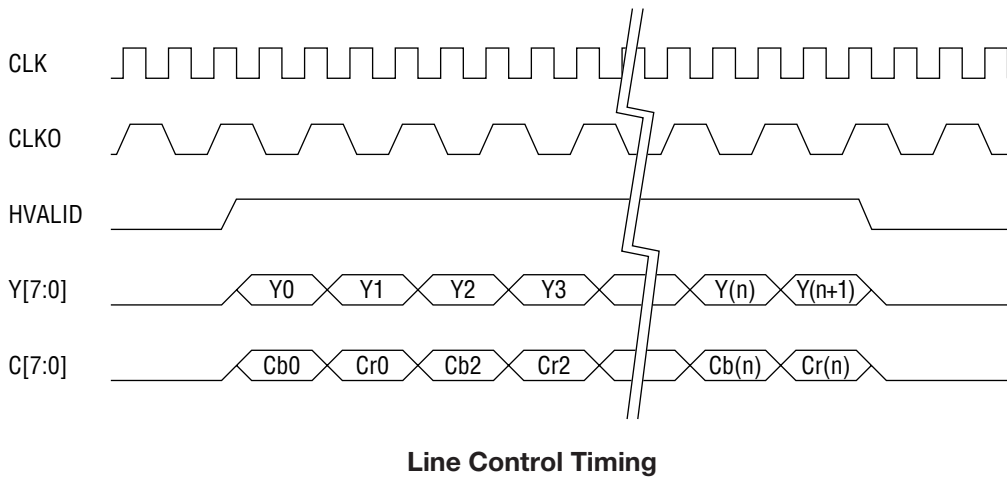
AD Converter Support Signal

The timing wave form of HSY/HCL signals, which measure the sync chip and clamp timing for the AD converter, is as follows.



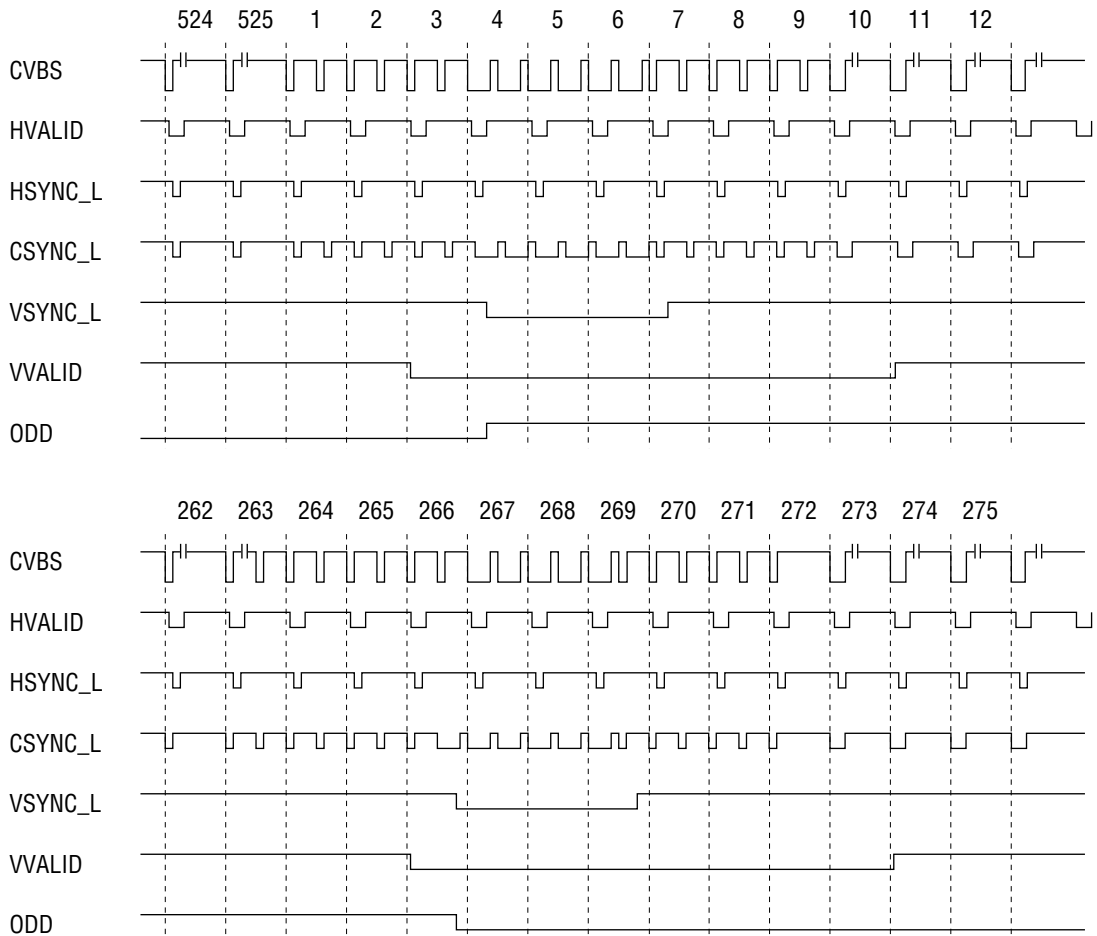
Line control signal

The line control signal timing is as follows.

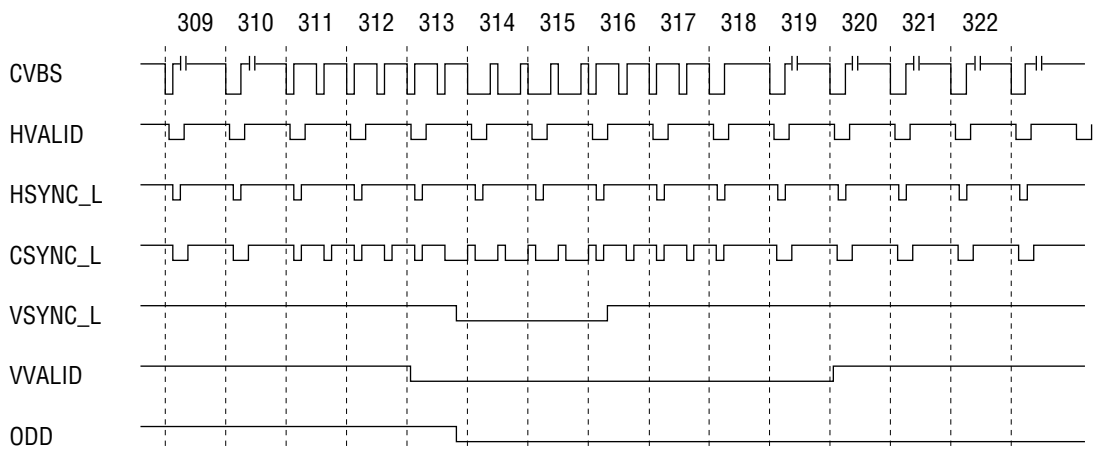
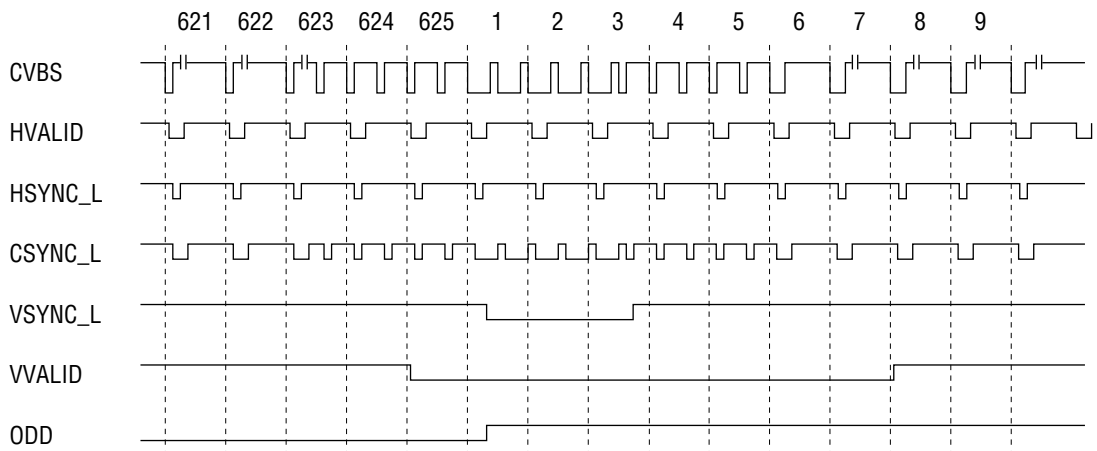


Vertical Synchronizing 4.3 Signal

The vertical synchronizing signal timing is as follows.



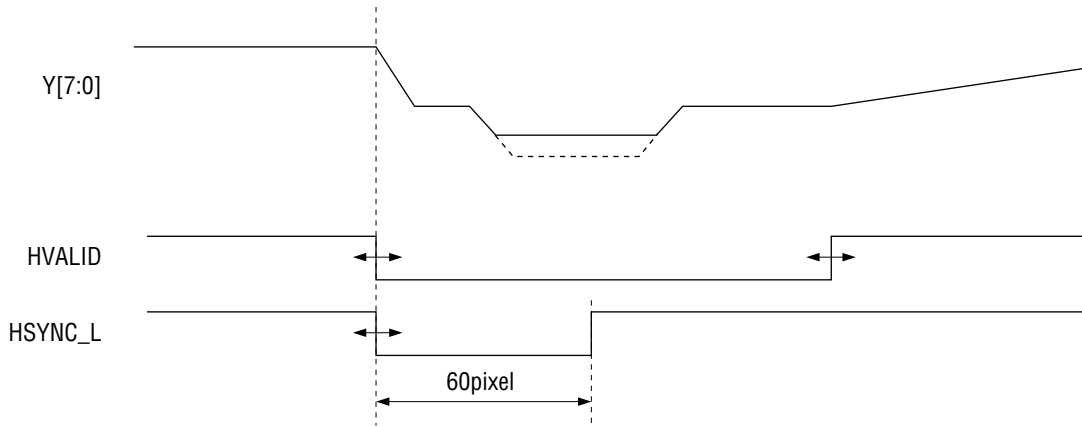
Vertical Timing (NTSC: 60Hz)



Vertical Timing (PAL: 50Hz)

Horizontal Synchronizing Signal

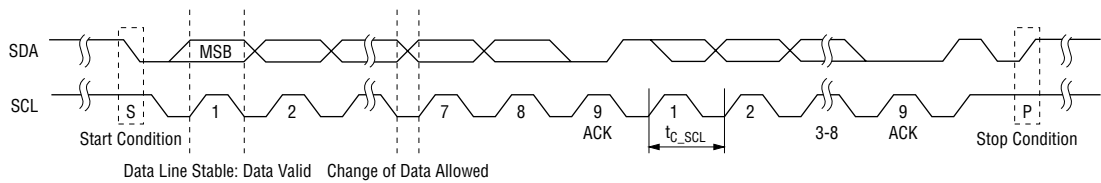
The horizontal synchronizing signal timing is as follows.



Horizontal Timing

I²C-bus Interface Input/Output Timing

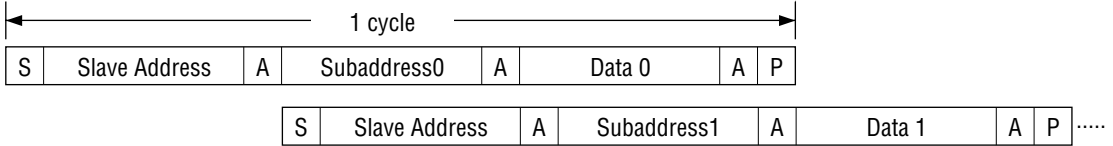
The basic input/output timing of the I²C-bus interface is as follows.



I²C-bus Basic Input/Output Timing

I²C BUS FORMAT

The I²C-bus interface input format is shown below.



| Symbol | Description |
|---------------|---|
| S | Start condition |
| Slave Address | Slave address 1000001, 8th bit is write signal. |
| A | Acknowledge. Generated by slave |
| Subaddress | Subaddress byte |
| Data n | Data to be written in address specified by subaddress |
| P | Stop condition |

It is required to input the above-mentioned format from the start condition to the stop condition each time of writing a subaddress

For example, when writing the subaddresses 0 to 2, the format should be input three times.

In case data of more than one byte are transferred,

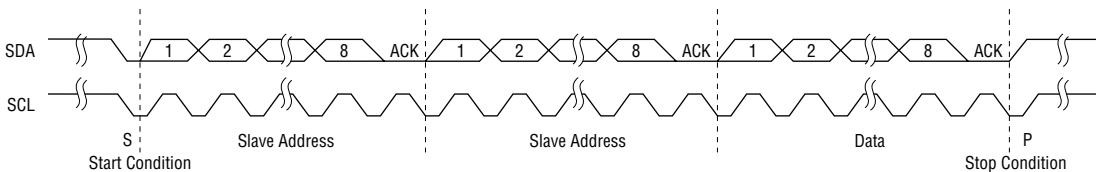


The 4th byte data and following data each are written over the same subaddress.

If one of the following matters occurs, the decoder will not return "A" (Acknowledge).

- The slave address does not match.
- A non-existent subaddress is specified.
- The write attribute of a register does not match "X" (write control bit).

The input timing is shown below.



OPERATION MODE SETTING

The video mode includes ;

1. Internal terminal mode to be directly set by a dedicated terminal
2. Register setting mode to be specified by setting the internal registers

These modes can be changed by the mode register MRA [4].

The reset state (default) is the external terminal mode.

The following registers can be set in the external terminal mode.

| | | | | |
|------------|-------------------|-------|-----------------------|----------|
| MRA[3] | input signal mode | *0: | Composite video input | |
| | | 1: | S-video input | |
| MRA[2 : 0] | input mode | *000: | NTSC ITU-R601 | 13.5MHz |
| | | 001: | NTSC Square Pixel | 12.27MHz |
| | | 010: | MTSC 4Fsc | 14.32MHz |
| | | 100: | PAL ITU-R601 | 13.5MHz |
| | | 101: | PAL Square Pixel | 14.75MHz |

INTERNAL REGISTERS

Register List

| Register List | Subaddress | Data byte | | | | | | | |
|---------------------------------|------------|-----------|--------|--------|--------|--------|--------|--------|--------|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Mode Register A (MRA) | 0 | MRA7 | MRA6 | MRA5 | MRA4 | MRA3 | MRA2 | MRA1 | MRA0 |
| Mode Register B (MRB) | 1 | MRB7 | MRB6 | MRB5 | MRB4 | MRB3 | MRB2 | MRB1 | MRB0 |
| Horizontal Sync Trimer (HSYT) | 2 | HSYT7 | HSYT6 | HSYT5 | HSYT4 | HSYT3 | HSYT2 | HSYT1 | HSYT0 |
| Horizontal Clamp Trimer (HCLT) | 3 | HCLT7 | HCLT6 | HCLT5 | HCLT4 | HCLT3 | HCLT2 | HCLT1 | HCLT0 |
| Horizontal Sync Delay (HSDL) | 4 | HSDL7 | HSDL6 | HSDL5 | HSDL4 | HSDL3 | HSDL2 | HSDL1 | HSDL0 |
| Horizontal Valid Trimer (HVALT) | 5 | HVALT7 | HVALT6 | HVALT5 | HVALT4 | HVALT3 | HVALT2 | HVALT1 | HVALT0 |
| Vertical Valid Trimer (VVALT) | 6 | VVALT7 | VVALT6 | VVALT5 | VVALT4 | VVALT3 | VVALT2 | VVALT1 | VVALT0 |
| Luminance Control (LUMC) | 7 | LUMC7 | LUMC6 | LUMC5 | LUMC4 | LUMC3 | LUMC2 | LUMC1 | LUMC0 |
| AGC Loop filter Control (AGCLF) | 8 | AGCLF7 | AGCLF6 | AGCLF5 | AGCLF4 | AGCLF3 | AGCLF2 | AGCLF1 | AGCLF0 |
| Sync separation level (SSEPL) | 9 | | SSEPL6 | SSEPL5 | SSEPL4 | SSEPL3 | SSEPL2 | SSEPL1 | SSEPL0 |
| Chrominance Control (CHRC) | A | CHRC7 | CHRC6 | CHRC5 | CHRC4 | CHRC3 | CHRC2 | CHRC1 | CHRC0 |
| ACC Loop filter Control (ACCLF) | B | ACCLF7 | ACCLF6 | ACCLF5 | ACCLF4 | ACCLF3 | ACCLF2 | ACCLF1 | ACCLF0 |
| Hue Control (HUE) | C | HUE7 | HUE6 | HUE5 | HUE4 | HUE3 | HUE2 | HUE1 | HUE0 |
| Output enable Control (OEC) | D | OEC7 | OEC6 | OEC5 | OEC4 | OEC3 | OEC2 | OEC1 | OEC0 |
| Output Phase Control for Data Y | E | OPCY7 | OPCY6 | OPCY5 | OPCY4 | OPCY3 | OPCY2 | OPCY1 | OPCY0 |
| Output Phase Control for Data C | F | OPCC7 | OPCC6 | OPCC5 | OPCC4 | OPCC3 | OPCC2 | OPCC1 | OPCC0 |

Register Description

Registers controlled by I²C bus are shown below.
 A register setting value with an "*" indicates the default.

Mode Register A (MRA) <default: 0x40>

| | | | | |
|----------|----------------------|-------|------------------------|----------|
| MRA[7] | Undefined | | | |
| MRA[6] | Synchronization mode | 0: | TV mode | |
| | | *1: | VTR mode | |
| MRA[5] | Chroma format | *0: | Offset binary | |
| | | 1: | 2's Complement | |
| MRA[4] | Override | *0: | external terminal mode | |
| | | 1: | register mode | |
| MRA[3] | Video Input mode | *0: | composite video input | |
| | | 1: | S video input | |
| MRA[2:0] | Video Input mode | *000: | NTSC CCIR601 | 13.5MHz |
| | | 001: | NTSC Square Pixel | 12.27MHz |
| | | 010: | NTSC 4Fsc | 14.32MHz |
| | | 100: | PAL CCIR601 | 13.5MHz |
| | | 101: | PAL Square Pixel | 14.75MHz |

Mode Register B (MRB) <default: 0x14>

| | | | | |
|--------|----------------------|-----|---|------------|
| MRB[7] | Sub Pixel Alignment | *0: | Sub Pixel Alignment is used. | |
| | | 1: | Sub Pixel Alignment is not used. | |
| MRB[6] | Color killer mode | *0: | Auto color killer (Chrominance signal level becomes "0" when color burst level is below specified value.) | |
| | | *1: | Forced color killer ON (Chrominance signal level is forced to be "0".) | |
| MRB[5] | Pixel Sampling Ratio | *0: | (4:2:2) | 1: (4:1:1) |
| MRB[4] | Blue Back | 0: | OFF (Video signal is demodulated and output regardless detection of synchronization.) | |
| | | *1: | AUTO (Blue Back is output when synchronization is not detected.) | |

| | | |
|----------|-----------------------------|---|
| MRB[3] | Sync enable, clamping pulse | *0: HCL, HSY outputs "HIGH" level 1: HCL, HSY outputs active |
| MRB[2] | Black level control | 0: Black level 7.5IRE *1: Black level 0IRE (Valid only for NTSC input.) |
| MRB[1:0] | Y/C separation mode | *00: adaptive comb filter (Operation mode is selected monitoring the correlation of 3 lines.) 01: nonadaptive comb filter (Operation mode is always fixed.) 10: Comb filter is not used. 11: undefined |

Horizontal Sync Trimer (HSYT) <default: 0x00>

| | | | |
|-----------|----------------------------|---------------|-----------------|
| HSYT[7:4] | HSY begin trimer (8/pixel) | 0xC: -4 (-32) | ~0xB: +11 (+88) |
| HSYT[3:0] | HSY stop trimer (8/pixel) | 0xC: -4 (-32) | ~0xB: +11 (+88) |

Horizontal Clamp Trimer (HCLT) <default: 0x00>

| | | | |
|-----------|----------------------------|---------------|----------------|
| HCLT[7:4] | HCL begin trimer (8/pixel) | 0x8: -8 (-64) | ~0x7: +7 (+56) |
| HCLT[3:0] | HCL stop trimer (8/pixel) | 0x8: -8 (-64) | ~0x7: +7 (+56) |

Horizontal Sync Delay (HSDL) <default: 0x00>

| | | | |
|-----------|--------------------------------|-------------------|-------------------|
| HSDL[7:4] | HSYNC_L delay trimer (4/pixel) | 0x80: -128 (-512) | ~0x7F: +127 (508) |
|-----------|--------------------------------|-------------------|-------------------|

Horizontal Valid Trimer (HVALT) <default: 0x00>

| | | | |
|------------|-------------------------------|---------------|---------------|
| HVALT[7:4] | HVALID begin trimer (1/pixel) | 0x4: -8 (-64) | ~0x3: +7 (56) |
| HVALT[3:0] | HVALID stop trimer (1/pixel) | 0x4: -8 (-64) | ~0x3: +7 (56) |

Vertical Valid Trimer (VVALT) <default: 0x00>

| | | | |
|------------|-----------------------------|---------|----------|
| VVALT[7:4] | VVALID begin trimer (/line) | 0x8: -8 | ~0x7: +7 |
| VVALT[3:0] | VVALID stop trimer (/line) | 0x8: -8 | ~0x7: +7 |

Luminance Control (LUMC) <default: 0x40>

| | | | | |
|-----------|----------------------------------|------|------|------------------------|
| LUMC[7] | Undefined | | | |
| LUMC[6] | Use of Pre-filter | 0: | 0: | Prefilter is not used. |
| | | *1: | *1: | Prefilter is used. |
| LUMC[5:4] | Aperture bandpass select | *00: | *00: | middle range |
| | | 01: | 01: | |
| | | 10: | 10: | |
| | | 11: | 11: | high range |
| LUMC[3:2] | Coring range select | *00: | *00: | coring off |
| | | 01: | 01: | +/-3LSB |
| | | 10: | 10: | +/-4LSB |
| | | 11: | 11: | +/-6LSB |
| LUMC[1:0] | Aperture filter weighting factor | *00: | *00: | 0 |
| | | 01: | 01: | 0.25 |
| | | 10: | 10: | 0.5 |
| | | 11: | 11: | 1 |

AGC Loop filter control (AGCLF) <default: 0x40>

| | | | | |
|------------|-------------------------------|--------|--------|--------|
| AGCLF[7:6] | AGC loop filter time constant | 00: | 00: | slow |
| | | *01: | *01: | medium |
| | | 10: | 10: | fast |
| | | 11: | 11: | fixed |
| AGCLF[5:0] | AGC reference level | 0x20: | 0x20: | -32 |
| | | ~0xIF: | ~0xIF: | +31 |

Sync separation level (SSEPL) <default: 0x00>

| | | | | |
|------------|-----------------------|--------|--------|-----|
| SSEPL[6:0] | Sync separation level | 0x40: | 0x40: | -64 |
| | | ~0x3F: | ~0x3F: | +63 |

Chrominance Control (CHRC) <default: 0x1>

| | | | | | |
|-----------|-----------------------------|------|-------------------------|-----|----|
| CHRC[7:3] | Undefined | | | | |
| CHRC[2] | Chroma bandpass filter | 0: | OFF | *1: | ON |
| CHRC[1:0] | Color kill threshold factor | 00: | 0.5*color burst level | | |
| | | *01: | 0.25*color burst level | | |
| | | 10: | 0.125*color burst level | | |
| | | 11: | Undefined | | |

ACC Loop filter control (ACCLF) <default: 0x20>

| | | | | | |
|------------|-------------------------------|-------|--------|--------|-----|
| ACCLF[7] | Undefined | | | | |
| ACCLF[6:5] | ACC loop filter time constant | 00: | slow | | |
| | | *01: | medium | | |
| | | 10: | fast | | |
| | | 11: | fixed | | |
| ACCLF[4:0] | ACC reference level | 0x10: | -16 | ~0x0F: | +15 |

Hue control (HUE) <default: 0x00>

| | | | | | |
|----------|-------------|-------|--------------|--------|---------------|
| HUE[7:0] | Hue control | 0x80: | -180 degrees | ~0x7F: | 178.6 degrees |
|----------|-------------|-------|--------------|--------|---------------|

Output enable control (OEC) <default: 0xF>

| | | | | | |
|----------|---------------------------|-----|--------------|--|--|
| OEC[7:4] | Undefined | | | | |
| OEC[3] | Output enable for data C | 0: | Hi-impedance | | |
| | | *1: | active | | |
| OEC[2] | Output enable for HSYNC_L | 0: | Hi-impedance | | |
| | | *1: | active | | |
| OEC[1] | Output enable for VSYNC_L | 0: | Hi-impedance | | |
| | | *1: | active | | |
| OEC[0] | Output enable for data Y | 0: | Hi-impedance | | |
| | | *1: | active | | |

Output phase control for data Y (OPCY) <default: 0x00>

OPCY[7:2] Undefined

OPCY[1:0] Output phase control for data Y *0: normal
1: forward 1 clock
2: Undefined
3: backward 1 clock

Output phase control for data C (OPCC) <default: 0x00>

OPCCY[7:2] Undefined

OPCC[1:0] Output phase control for data C *0: normal
1: forward 1 clock
2: Undefined
3: backward 1 clock

Relationship between Register Setting Value and Adjusted Value

Horizontal Sync Timer

Position adjustment of sync chip clamp timing signal

HSYT [7:4] :Adjusting the starting position

| | | | | | | | | | | | | | | | | |
|-----------------------------|-----|-----|-----|----|---|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Register Setting Value (0x) | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B |
| Adjusted Value (Pixel) | -32 | -24 | -16 | -8 | 0 | +8 | +16 | +24 | +32 | +40 | +48 | +56 | +64 | +72 | +80 | +88 |

HSYT [3:0] :Adjusting the end position

| | | | | | | | | | | | | | | | | |
|-----------------------------|-----|-----|-----|----|---|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Register Setting Value (0x) | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B |
| Adjusted Value (Pixel) | -32 | -24 | -16 | -8 | 0 | +8 | +16 | +24 | +32 | +40 | +48 | +56 | +64 | +72 | +80 | +88 |

Horizontal Clamp Timer

Position adjustment of pedestal clamp timing signal

HCLT [7:4] :Adjusting the starting position

| | | | | | | | | | | | | | | | | |
|-----------------------------|-----|-----|-----|-----|-----|-----|-----|----|---|----|-----|-----|-----|-----|-----|-----|
| Register Setting Value (0x) | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Adjusted Value (Pixel) | -64 | -56 | -48 | -40 | -32 | -24 | -16 | -8 | 0 | +8 | +16 | +24 | +32 | +40 | +48 | +56 |

HCLT [3:0] :Adjusting the end position

| | | | | | | | | | | | | | | | | |
|-----------------------------|-----|-----|-----|-----|-----|-----|-----|----|---|----|-----|-----|-----|-----|-----|-----|
| Register Setting Value (0x) | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Adjusted Value (Pixel) | -64 | -56 | -48 | -40 | -32 | -24 | -16 | -8 | 0 | +8 | +16 | +24 | +32 | +40 | +48 | +56 |

Horizontal Sync Delay

Adjustment of the starting position of horizontal sync signal

HSDL [7:0]

| | | MSB[7 : 4] | | | | | | | | | | | | | | | |
|----------------|---|------------|------|------|------|------|------|------|-----|-----|------|------|------|------|------|------|------|
| | | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| LSB [3 : 0] | 0 | -512 | -448 | -384 | -320 | -256 | -192 | -128 | -64 | 0 | +64 | +128 | +192 | +256 | +320 | +384 | +448 |
| | 1 | -508 | -444 | -380 | -316 | -252 | -188 | -124 | -60 | +4 | +68 | +132 | +196 | +260 | +324 | +388 | +452 |
| | 2 | -504 | -440 | -376 | -312 | -248 | -184 | -120 | -56 | +8 | +72 | +136 | +200 | +264 | +328 | +392 | +456 |
| | 3 | -500 | -436 | -372 | -308 | -244 | -180 | -116 | -52 | +12 | +76 | +140 | +204 | +268 | +332 | +396 | +460 |
| | 4 | -496 | -432 | -368 | -304 | -240 | -176 | -112 | -48 | +16 | +80 | +144 | +208 | +272 | +336 | +400 | +464 |
| | 5 | -492 | -428 | -364 | -300 | -236 | -172 | -108 | -44 | +20 | +84 | +148 | +212 | +276 | +340 | +404 | +468 |
| | 6 | -488 | -424 | -360 | -296 | -232 | -168 | -104 | -40 | +24 | +88 | +152 | +216 | +280 | +344 | +408 | +472 |
| | 7 | -484 | -420 | -356 | -292 | -228 | -164 | -100 | -36 | +28 | +92 | +156 | +220 | +284 | +348 | +412 | +476 |
| | 8 | -480 | -416 | -352 | -288 | -224 | -160 | -96 | -32 | +32 | +96 | +160 | +224 | +288 | +352 | +416 | +480 |
| | 9 | -476 | -412 | -348 | -284 | -220 | -156 | -92 | -28 | +36 | +100 | +164 | +228 | +292 | +356 | +420 | +484 |
| | A | -472 | -408 | -344 | -280 | -216 | -152 | -88 | -24 | +40 | +104 | +168 | +232 | +296 | +360 | +424 | +488 |
| | B | -468 | -404 | -340 | -276 | -212 | -148 | -84 | -20 | +44 | +108 | +172 | +236 | +300 | +364 | +428 | +492 |
| | C | -464 | -400 | -336 | -272 | -208 | -144 | -80 | -16 | +48 | +112 | +176 | +240 | +304 | +368 | +432 | +496 |
| | D | -460 | -396 | -332 | -268 | -204 | -140 | -76 | -12 | +52 | +116 | +180 | +244 | +308 | +372 | +436 | +500 |
| | E | -456 | -392 | -328 | -264 | -200 | -136 | -72 | -8 | +56 | +120 | +184 | +248 | +312 | +376 | +440 | +504 |
| | F | -452 | -388 | -324 | -260 | -196 | -132 | -68 | -4 | +60 | +124 | +188 | +252 | +316 | +380 | +444 | +508 |

Horizontal Valid Timer

Position adjustment of horizontal valid pixel timing signal

HVALT [7:4] :Adjusting the starting position

| | | | | | | | | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| Register Setting Value (0x) | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Adjusted Value (Pixel) | -8 | -7 | -6 | -5 | -4 | -3 | -2 | -1 | 0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |

HVALT [3:0] :Adjusting the end position

| | | | | | | | | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| Register Setting Value (0x) | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Adjusted Value (Pixel) | -8 | -7 | -6 | -5 | -4 | -3 | -2 | -1 | 0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |

Vertical Valid Timer

Position adjustment of vertical valid line timing signal

VVALT [7:4] :Adjusting the starting position

| | | | | | | | | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| Register Setting Value (0x) | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Adjusted Value (Line) | -8 | -7 | -6 | -5 | -4 | -3 | -2 | -1 | 0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |

VVALT [3:0] :Adjusting the end position

| | | | | | | | | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|----|----|---|----|----|----|----|----|----|----|
| Register Setting Value (0x) | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Adjusted Value (Line) | -8 | -7 | -6 | -5 | -4 | -3 | -2 | -1 | 0 | +1 | +2 | +3 | +4 | +5 | +6 | +7 |

AGC Loop filter control

AGCLF [5:0] :Adjusting sync level

| Register Setting Value (0x) | MSB [5 : 4] | | | | |
|-----------------------------|-------------|-----|-----|-----|-----|
| | 2 | 3 | 0 | 1 | |
| LSB [3 : 0] | 0 | -32 | -16 | 0 | +16 |
| | 1 | -31 | -15 | +1 | +17 |
| | 2 | -30 | -14 | +2 | +18 |
| | 3 | -29 | -13 | +3 | +19 |
| | 4 | -28 | -12 | +4 | +20 |
| | 5 | -27 | -11 | +5 | +21 |
| | 6 | -26 | -10 | +6 | +22 |
| | 7 | -25 | -9 | +7 | +23 |
| | 8 | -24 | -8 | +8 | +24 |
| | 9 | -23 | -7 | +9 | +25 |
| | A | -22 | -6 | +10 | +26 |
| | B | -21 | -5 | +11 | +27 |
| | C | -20 | -4 | +12 | +28 |
| | D | -19 | -3 | +13 | +29 |
| | E | -18 | -2 | +14 | +30 |
| | F | -17 | -1 | +15 | +31 |

Sync separation level

SSEPL [6:0] :Adjusting the blanking level

| Register Setting Value (0x) | | MSB [6 : 4] | | | | | | | |
|-----------------------------|---|-------------|-----|-----|-----|-----|-----|-----|-----|
| | | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| LSB [3 : 0] | 0 | -64 | -48 | -32 | -16 | 0 | +16 | +32 | +48 |
| | 1 | -63 | -47 | -31 | -15 | +1 | +17 | +33 | +49 |
| | 2 | -62 | -46 | -30 | -14 | +2 | +18 | +34 | +50 |
| | 3 | -61 | -45 | -29 | -13 | +3 | +19 | +35 | +51 |
| | 4 | -60 | -44 | -28 | -12 | +4 | +20 | +36 | +52 |
| | 5 | -59 | -43 | -27 | -11 | +5 | +21 | +37 | +53 |
| | 6 | -58 | -42 | -26 | -10 | +6 | +22 | +38 | +54 |
| | 7 | -57 | -41 | -25 | -9 | +7 | +23 | +39 | +55 |
| | 8 | -56 | -40 | -24 | -8 | +8 | +24 | +40 | +56 |
| | 9 | -55 | -39 | -23 | -7 | +9 | +25 | +41 | +57 |
| | A | -54 | -38 | -22 | -6 | +10 | +26 | +42 | +58 |
| | B | -53 | -37 | -21 | -5 | +11 | +27 | +43 | +59 |
| | C | -52 | -36 | -20 | -4 | +12 | +28 | +44 | +60 |
| | D | -51 | -35 | -19 | -3 | +13 | +29 | +45 | +61 |
| | E | -50 | -34 | -18 | -2 | +14 | +30 | +46 | +62 |
| | F | -49 | -33 | -17 | -1 | +15 | +31 | +47 | +63 |

ACC Loop filter control

ACCLF [4:0] :Adjusting the color burst level

| Register Setting Value (0x) | | MSB [4] | |
|-----------------------------|---|---------|-----|
| | | 1 | 0 |
| LSB [3 : 0] | 0 | -16 | 0 |
| | 1 | -15 | +1 |
| | 2 | -14 | +2 |
| | 3 | -13 | +3 |
| | 4 | -12 | +4 |
| | 5 | -11 | +5 |
| | 6 | -10 | +6 |
| | 7 | -9 | +7 |
| | 8 | -8 | +8 |
| | 9 | -7 | +9 |
| | A | -6 | +10 |
| | B | -5 | +11 |
| | C | -4 | +12 |
| | D | -3 | +13 |
| | E | -2 | +14 |
| | F | -1 | +15 |

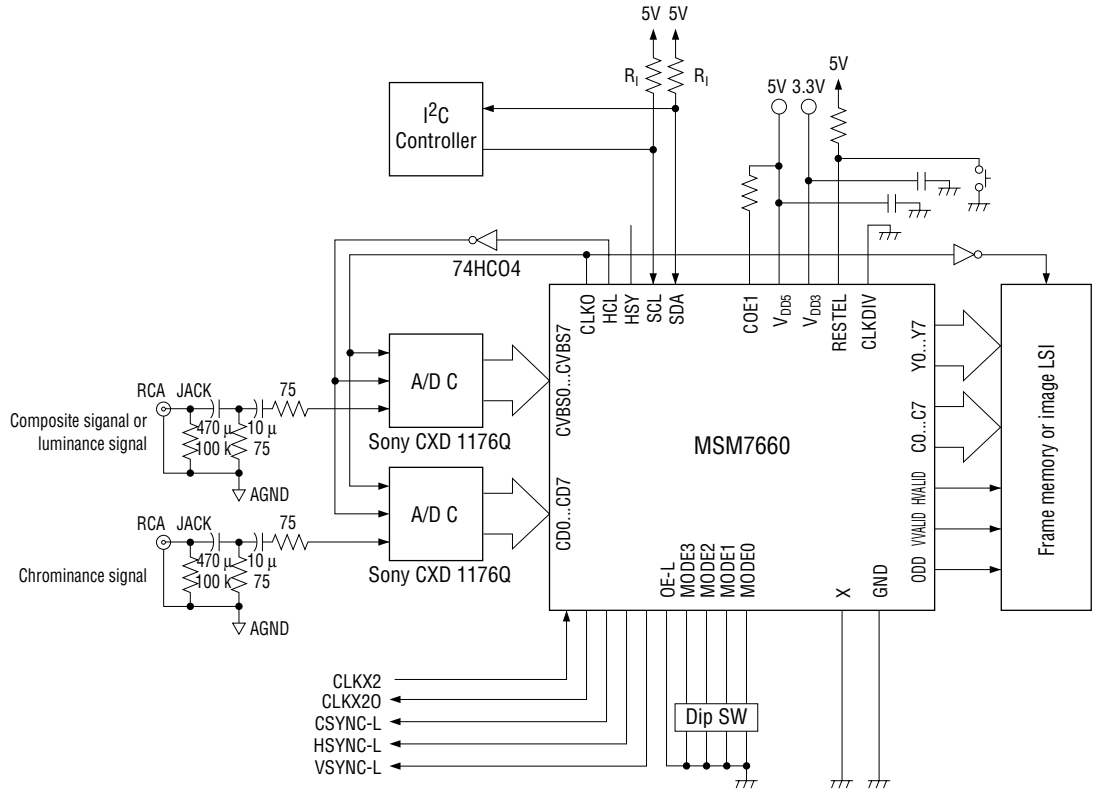
Hue control
Adjustment of color subcarrier phase

HUE [7:0]

| Register Setting Value (0x) | MSB [7 : 4] | | | | | | | | | | | | | | | | |
|-----------------------------|-------------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|
| | 8 | 9 | A | B | C | D | E | F | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | |
| LSB [3 : 0] | 0 | -180.0 | -157.5 | -135.0 | -112.5 | -90.0 | -67.5 | -45.0 | -22.5 | +0.0 | +22.5 | +45.0 | +67.5 | +90.0 | +112.5 | +135.0 | +157.5 |
| | 1 | -178.6 | -156.1 | -133.6 | -111.1 | -88.6 | -66.1 | -43.6 | -21.1 | +1.4 | +23.9 | +46.4 | +68.9 | +91.4 | +113.9 | +136.4 | +158.9 |
| | 2 | -177.2 | -154.7 | -132.2 | -109.7 | -87.2 | -64.7 | -42.2 | -19.7 | +2.8 | +25.3 | +47.8 | +70.3 | +92.8 | +115.3 | +137.8 | +160.3 |
| | 3 | -175.8 | -153.3 | -130.8 | -108.3 | -85.8 | -63.3 | -40.8 | -18.3 | +4.2 | +26.7 | +49.2 | +71.7 | +94.2 | +116.7 | +139.2 | +161.7 |
| | 4 | -174.4 | -151.9 | -129.4 | -106.9 | -84.4 | -61.9 | -39.4 | -16.9 | +5.6 | +28.1 | +50.6 | +73.1 | +95.6 | +118.1 | +140.6 | +163.1 |
| | 5 | -173.0 | -150.5 | -128.0 | -105.5 | -83.0 | -60.5 | -38.0 | -15.5 | +7.0 | +29.5 | +52.0 | +74.5 | +97.0 | +119.5 | +142.0 | +164.5 |
| | 6 | -171.6 | -149.1 | -126.6 | -104.1 | -81.6 | -59.1 | -36.6 | -14.1 | +8.4 | +30.9 | +53.4 | +75.9 | +98.4 | +120.9 | +143.4 | +165.9 |
| | 7 | -170.2 | -147.7 | -125.2 | -102.7 | -80.2 | -57.7 | -35.2 | -12.7 | +9.8 | +32.3 | +54.8 | +77.3 | +99.8 | +122.3 | +144.8 | +167.3 |
| | 8 | -168.8 | -146.3 | -123.8 | -101.3 | -78.8 | -56.3 | -33.8 | -11.3 | +11.3 | +33.8 | +56.3 | +78.8 | +101.3 | +123.8 | +146.3 | +168.8 |
| | 9 | -167.3 | -144.8 | -122.3 | -99.8 | -77.3 | -54.8 | -32.3 | -9.8 | +12.7 | +35.2 | +57.7 | +80.2 | +102.7 | +125.2 | +147.7 | +170.2 |
| | A | -165.9 | -143.4 | -120.9 | -98.4 | -75.9 | -53.4 | -30.9 | -8.4 | +14.1 | +36.6 | +59.1 | +81.6 | +104.1 | +126.6 | +149.1 | +171.6 |
| | B | -164.5 | -142.0 | -119.5 | -97.0 | -74.5 | -52.0 | -29.5 | -7.0 | +15.5 | +38.0 | +60.5 | +83.0 | +105.5 | +128.0 | +150.5 | +173.0 |
| | C | -163.1 | -140.6 | -118.1 | -95.6 | -73.1 | -50.6 | -28.1 | -5.6 | +16.9 | +39.4 | +61.9 | +84.4 | +106.9 | +129.4 | +151.9 | +174.4 |
| | D | -161.7 | -139.2 | -116.7 | -94.2 | -71.7 | -49.2 | -26.7 | -4.2 | +18.3 | +40.8 | +63.3 | +85.8 | +108.3 | +130.8 | +153.3 | +175.8 |
| | E | -160.3 | -137.8 | -115.3 | -92.8 | -70.3 | -47.8 | -25.3 | -2.8 | +19.7 | +42.2 | +64.7 | +87.2 | +109.7 | +132.2 | +154.7 | +177.2 |
| | F | -158.9 | -136.4 | -113.9 | -91.4 | -68.9 | -46.4 | -23.9 | -1.4 | +21.1 | +43.6 | +66.1 | +88.6 | +111.1 | +133.6 | +156.1 | +178.6 |

APPLICATION CIRCUIT EXAMPLE

Example of supplying the pixel clock from an external source



CASCADE PRIORITY CONTROL

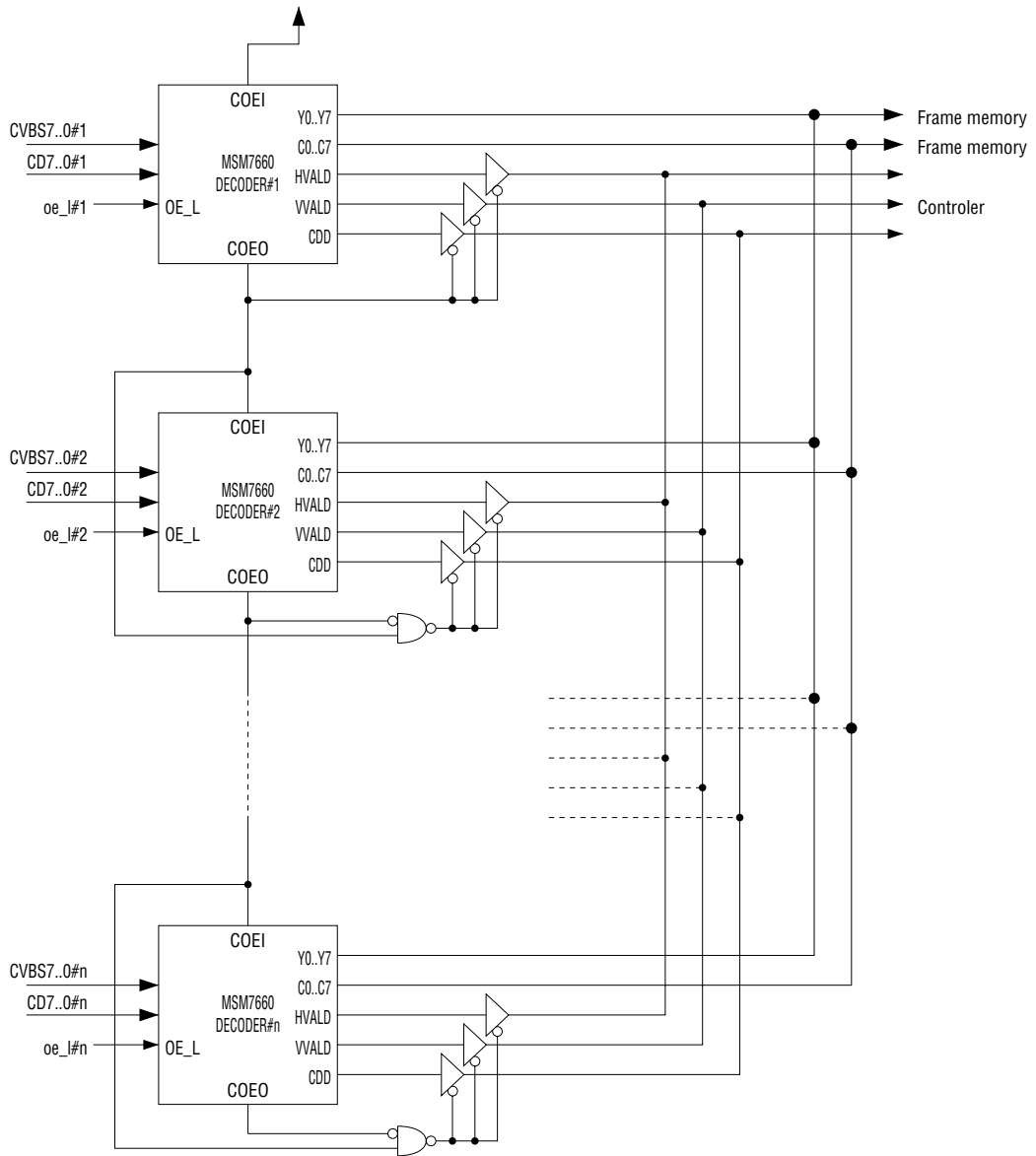
The MSM7660 can set Y/C signal output to high impedance, and can be wired with another bus that can be set to high impedance output.

Y/C output enable/disable is selected by the OE_L pin and register OEC. Cascade connection of COEI and COEO makes priority control possible. Priority is assigned to devices and when a device with higher priority is in enable status, devices with lower priority are automatically disabled. The priority control table is shown below.

| Register setting | | | | Input | | Output | | | | |
|------------------|--------|--------|--------|-------|------|--------|---------|---------|--------|------|
| OEC[0] | OEC[1] | OEC[2] | OEC[3] | coei | ce_l | Y0..Y7 | VSYNC_I | HSYNC_I | C0..C7 | COEO |
| X | X | X | X | 0 | X | Z | Z | Z | Z | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | Z | Z | Z | Z | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | enable | Z | Z | enable | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | enable | Z | Z | Z | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | Z | Z | Z | enable | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | Z | enable | enable | Z | 1 |
| X | X | X | X | 1 | 0 | enable | enable | enable | enable | 0 |

Z : High impedance

Cascade Priority Control Table



Cascade Priority Control Connection Example

PACKAGE OUTLINES AND DIMENSIONS

