MOSFETs Silicon P-Channel MOS (U-MOSⅥ)

SSM3J351R

1. Applications

- Power Management Switches

2. Features

(1) AEC-Q101 qualified (Please see the orderable part number list)

(2) 4 V drive

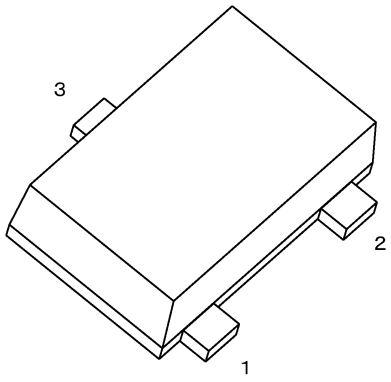
(3) Low drain-source on-resistance

: $R_{DS(ON)}$ = 107 mΩ (typ.) (V_{GS} = -10 V)

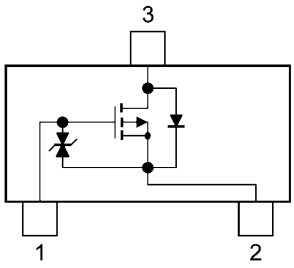
$R_{DS(ON)}$ = 122 mΩ (typ.) (V_{GS} = -4.5 V)

$R_{DS(ON)}$ = 129 mΩ (typ.) (V_{GS} = -4.0 V)

3. Packaging and Internal Circuit



SOT-23F



1: Gate
2: Source
3: Drain

4. Orderable part number

Orderable part number	AEC-Q101	Note
SSM3J351R,LF	—	General Use
SSM3J351R,LXGF	YES (Note 1)	Unintended Use (Note 1)
SSM3J351R,LXHF	YES	Automotive Use

Note 1: For more information, please contact our sales or use the inquiry form on our website.

Start of commercial production
2016-07

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5. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

Characteristics			Symbol	Rating	Unit
Drain-source voltage			V_{DSS}	-60	V
Gate-source voltage			V_{GSS}	-20/+10	
Drain current (DC)		(Note 1)	I_D	-3.5	A
Drain current (pulsed)		(Note 1), (Note 2)	I_{DP}	-14	
Power dissipation		(Note 3)	P_D	1	W
Power dissipation	(t ≤ 10 s)	(Note 3)	P_D	2	
Single-pulse avalanche energy		(Note 4)	E_{AS}	8.9	mJ
Avalanche current			I_{AR}	3.5	A
Channel temperature			T_{ch}	150	°C
Storage temperature			T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Pulse width (PW) ≤ 1 ms, duty ≤ 1 %

Note 3: Device mounted on a 25.4 mm × 25.4 mm × 1.6 mm FR4 glass epoxy board (Cu pad: 645 mm^2)

Note 4: V_{DD} = 25 V, T_{ch} = 25 °C (Initial state), L = 1 mH, R_G = 25 Ω

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance, $R_{th(ch-a)}$, and the drain power dissipation, P_D, vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

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6. Electrical Characteristics

6.1. Static Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{DS} = 0 V, V_{GS} = -16 V/+10 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = -60 V, V_{GS} = 0 V	—	—	-10	
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = -1 mA, V_{GS} = 0 V	-60	—	—	V
Drain-source breakdown voltage	(Note 1)	$V_{(BR)DSX}$	I_D = -1 mA, V_{GS} = 10 V	-50	—	—	
Gate threshold voltage		V_{th}	V_{DS} = -10 V, I_D = -1 mA	-0.8	—	-2.0	
Drain-source on-resistance	(Note 2)	$R_{DS(ON)}$	I_D = -1.0 A, V_{GS} = -4.0 V	—	129	184	mΩ
			I_D = -1.0 A, V_{GS} = -4.5 V	—	122	164	
			I_D = -1.0 A, V_{GS} = -10 V	—	107	134	
Forward transfer admittance	(Note 2)	$\|Y_{fs}\|$	V_{DS} = -10 V, I_D = -1.0 A	—	6.4	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Pulse measurement.

6.2. Dynamic Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	—	660	—	pF
Reverse transfer capacitance	C_{rss}		—	50	—	
Output capacitance	C_{oss}		—	70	—	
Switching time (turn-on time)	t_{on}	V_{DD} = -30 V, I_D = -1.0 A, V_{GS} = 0 to -4.5 V, R_G = 10 Ω, Duty ≤ 1 %, V_{IN}: t_r, t_f < 5 ns, Common source, See Chapter 5.3.	—	32	—	ns
Switching time (turn-off time)	t_{off}		—	100	—	

6.3. Switching Time Test Circuit

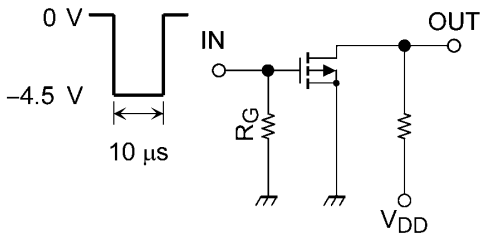


Fig. 6.3.1 Switching Time Test Circuit

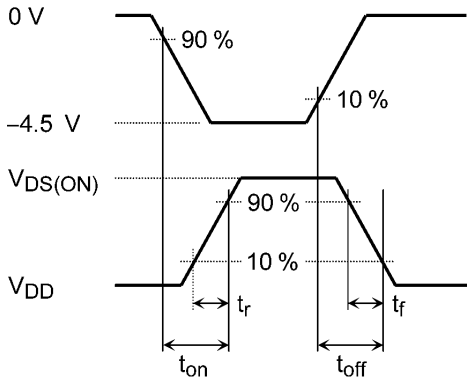


Fig. 6.3.2 Input Waveform/Output Waveform

6.4. Gate Charge Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} = -48 V, I_D = -3.5 A, V_{GS} = -10 V	—	15.1	—	nC
Gate-source charge 1	Q_{gs1}		—	0.6	—	
Gate-drain charge	Q_{gd}		—	3	—	

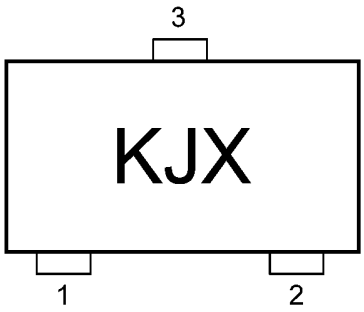
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6.5. Source-Drain Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	(Note 1)	V_{DSF}	I_D = 3.5 A, V_{GS} = 0 V	—	0.85	1.2	V

Note 1: Pulse measurement.

7. Marking



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8. Characteristics Curves (Note)

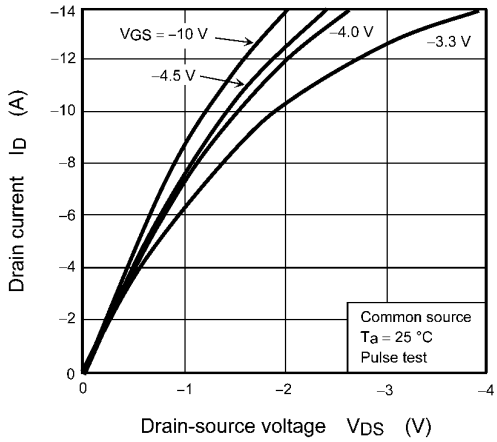


Fig. 8.1 I_D - V_{DS}

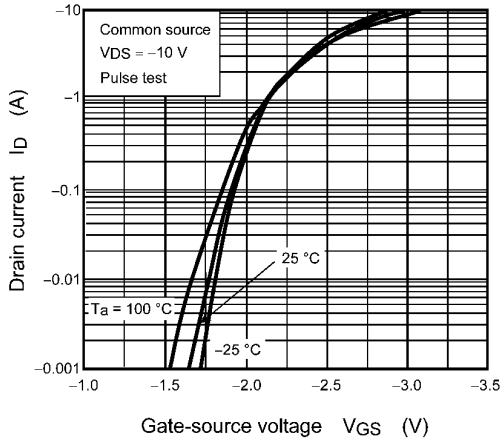


Fig. 8.2 I_D - V_{GS}

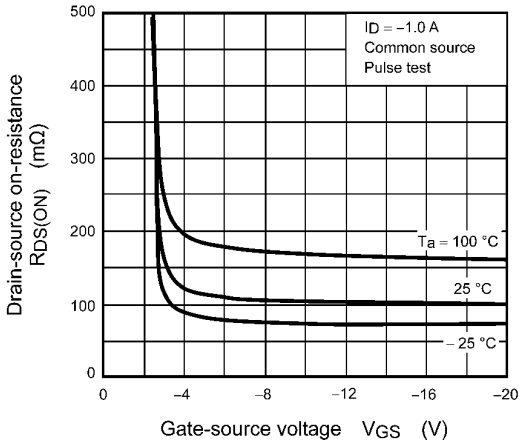


Fig. 8.3 $R_{DS(ON)}$ - V_{GS}

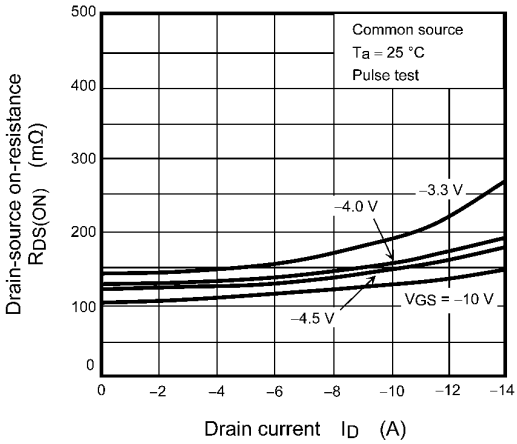


Fig. 8.4 $R_{DS(ON)}$ - I_D

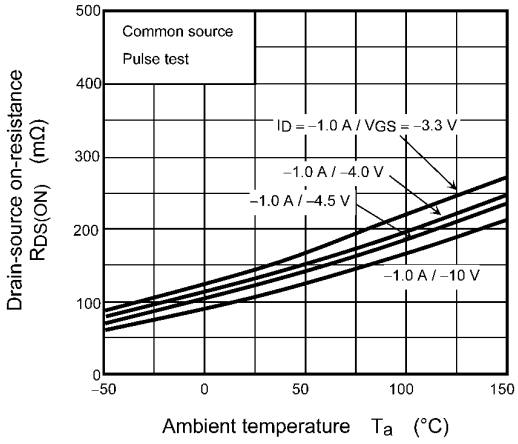


Fig. 8.5 $R_{DS(ON)}$ - T_a

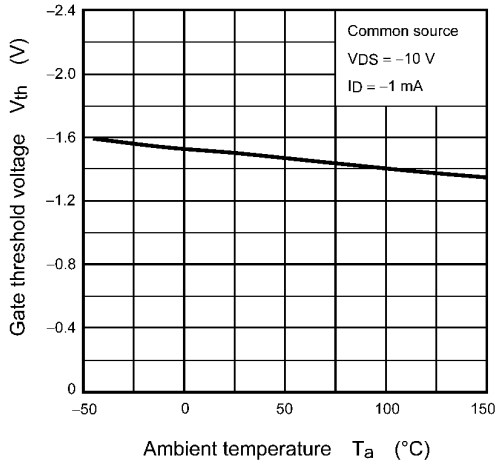


Fig. 8.6 V_{th} - T_a

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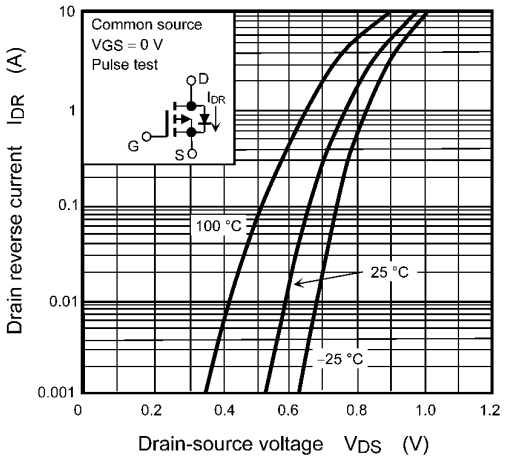


Fig. 8.7 I_{DR} - V_{DS}

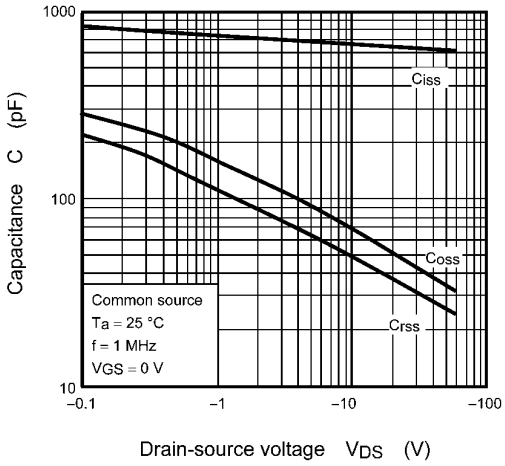


Fig. 8.8 C - V_{DS}

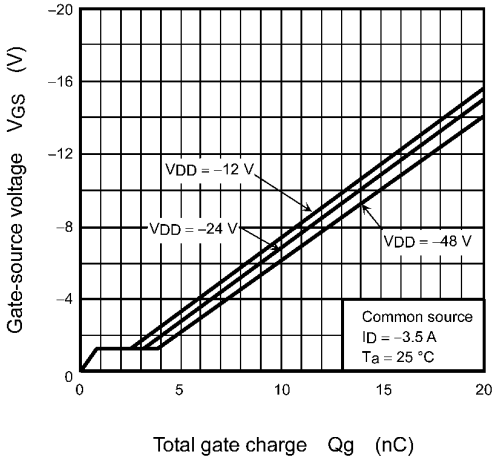


Fig. 8.9 Dynamic Input Characteristics

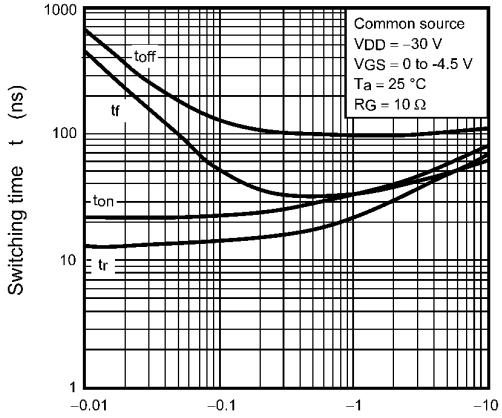


Fig. 8.10 t - I_D

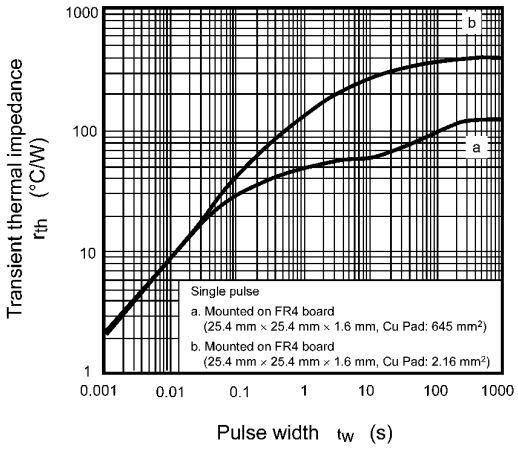


Fig. 8.11 r_{th} - t_w

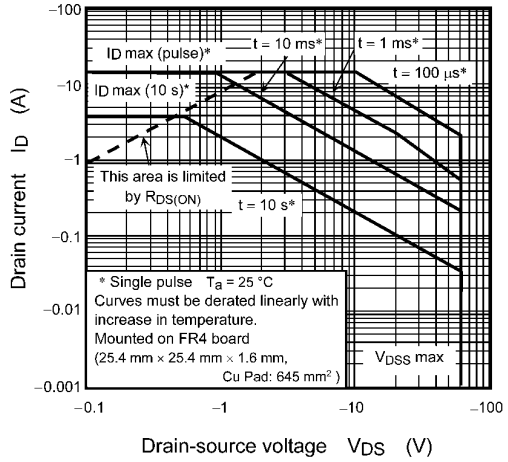


Fig. 8.12 Safe Operating Area

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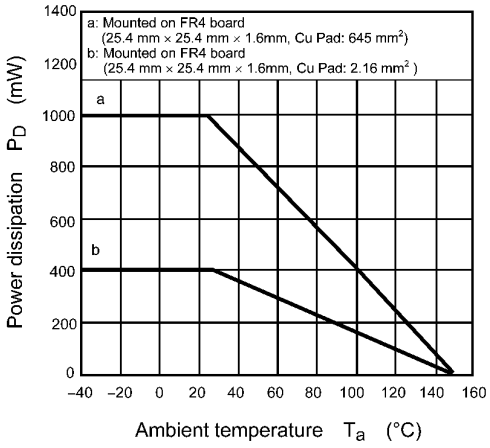


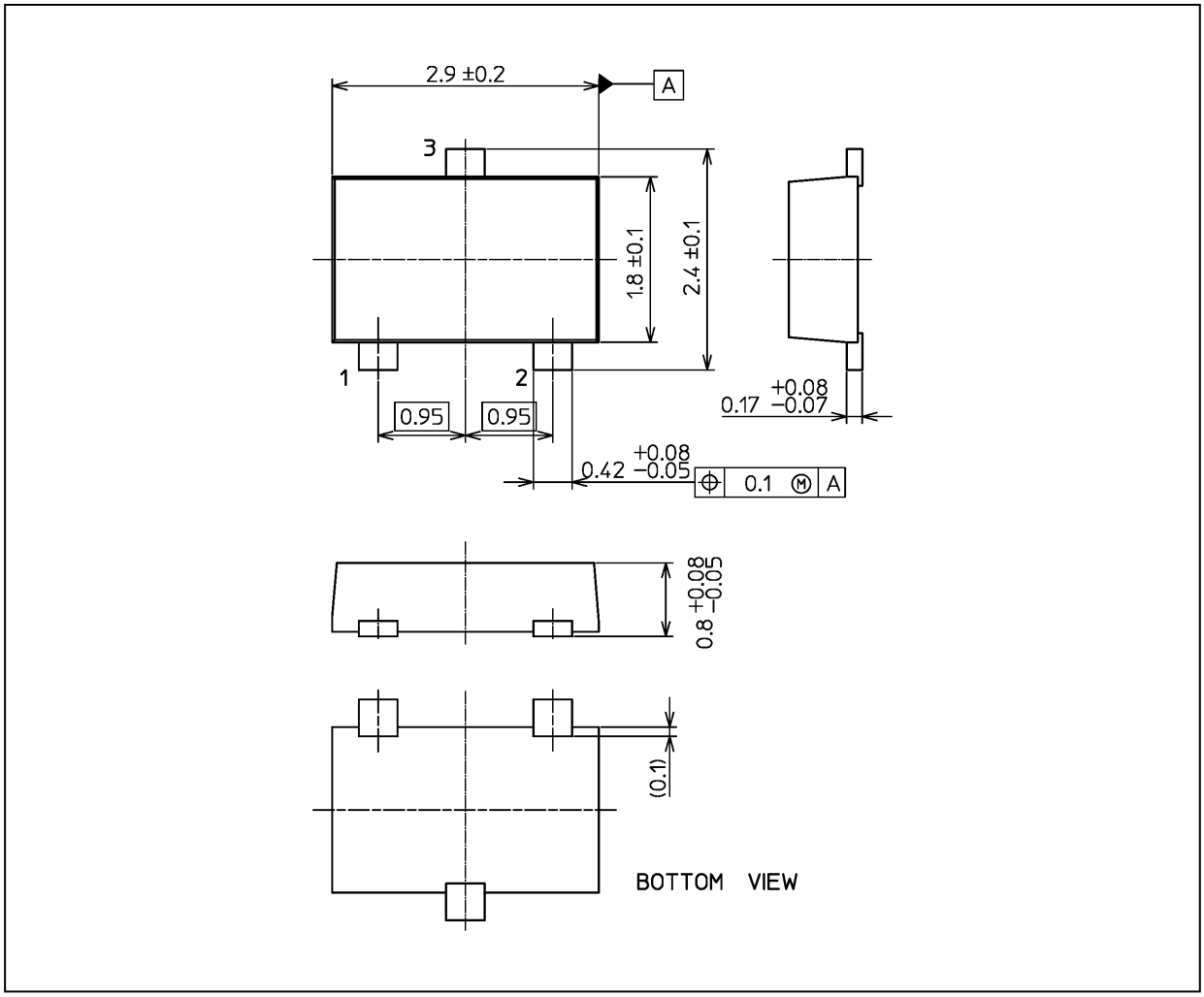
Fig. 8.13 P_D - T_a

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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Package Dimensions

Unit: mm



Weight: 0.011 g (typ.)

Package Name(s)
Nickname: SOT-23F

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