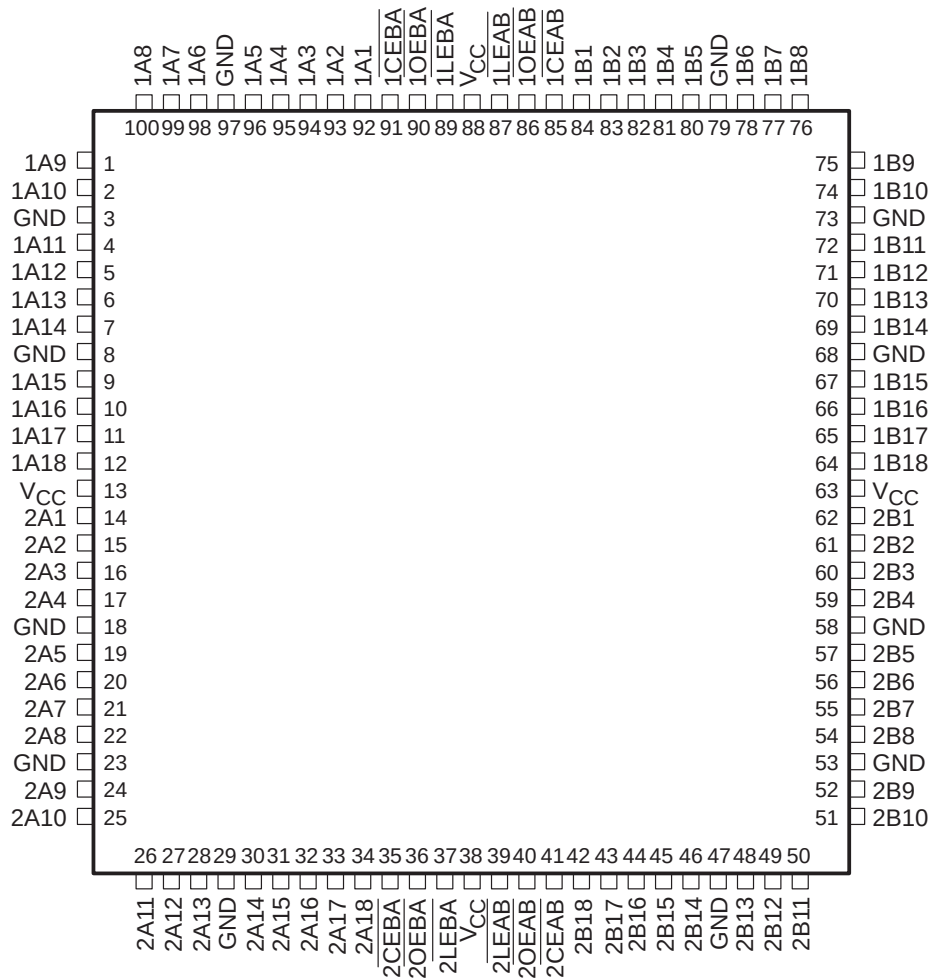


SN54ABTH32543, SN74ABTH32543 36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments *Widebus+™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Released as DSCC SMD 5962-9557801NXD
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include 100-Pin Plastic Thin Quad Flat (PZ) Package With $14 \times 14\text{-mm}$ Body Using 0.5-mm Lead Pitch and Space-Saving 100-Pin Ceramic Quad Flat (HS) Package†

'ABTH32543 . . . PZ PACKAGE
(TOP VIEW)



† The HS package is not production released.



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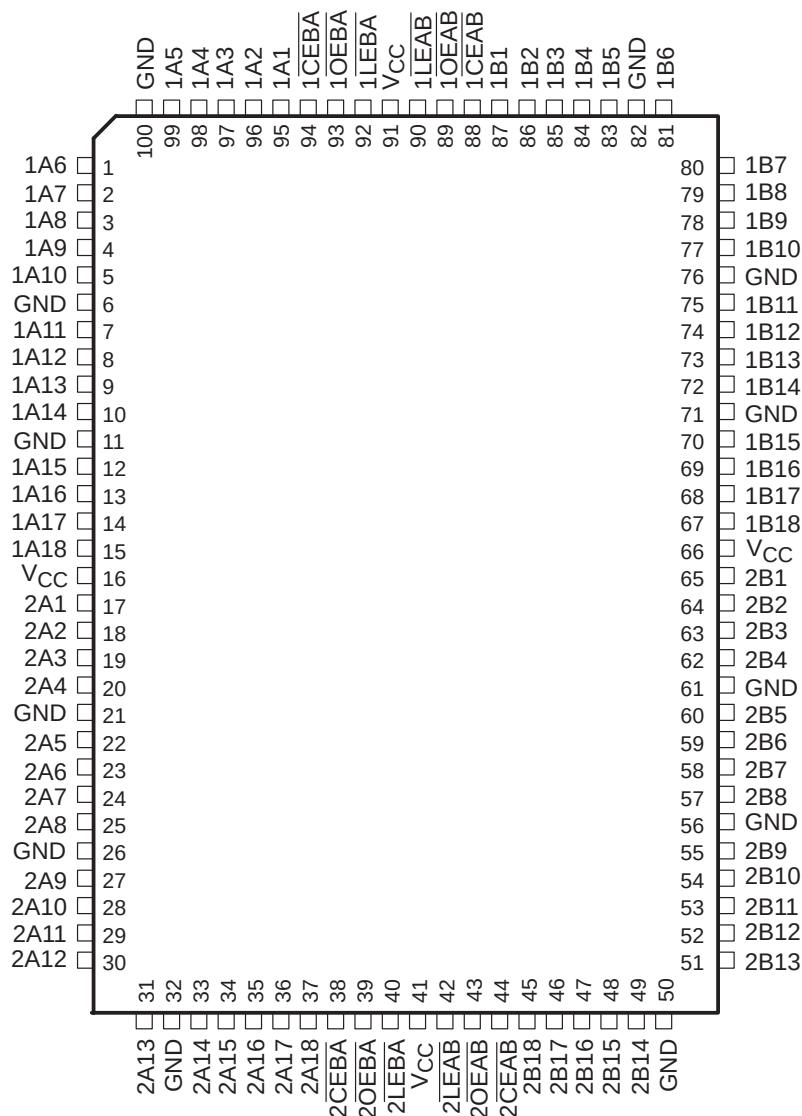
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SN54ABTH32543 . . . HS PACKAGE†
(TOP VIEW)



† For HS package availability, please contact the factory or your local TI Field Sales Office.

description

The 'ABTH32543 are 36-bit registered transceivers that contain two sets of D-type latches for temporary storage of data flowing in either direction. These devices can be used as two 18-bit transceivers or one 36-bit transceiver. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.



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description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH32543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABTH32543 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE[†]
(each 18-bit section)

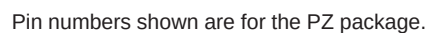
INPUTS				OUTPUT B
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	$B_0^{\ddagger}$
L	L	L	L	L
L	L	L	H	H

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

[‡] Output level before the indicated steady-state input conditions were established

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The diagram illustrates the logic for one of 17 channels. It features four 3-input AND gates at the top, each with two active-low inputs (labeled 1OEBA, 1CEBA, 1LEBA) and one active-high input (labeled 1A1). The outputs of these AND gates are connected to a network of inverters, OR gates, and two 1D flip-flops (labeled C1). The final output is labeled 1B1. A bracket at the bottom indicates that this logic is repeated for 17 other channels.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABTH32543	96 mA
SN74ABTH32543	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): PZ package	50°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABTH32543		SN74ABTH32543		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ABTH32543			SN74ABTH32543			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5			V
		$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3			
		$V_{CC} = 4.5\text{ V}$	2			2			
V_{OL}		$V_{CC} = 4.5\text{ V}$			0.55			0.55	V
								0.55	
V_{hys}				100			100		mV
I_I	Control inputs	$V_{CC} = 0\text{ to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$						±1	μA
	A or B ports	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$						±20	
	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$			±1				
	A or B ports				±20				
$I_I(\text{hold})$	A or B ports	$V_{CC} = 4.5\text{ V}$			$V_I = 0.8\text{ V}$			100	μA
					$V_I = 2\text{ V}$			-100	
$I_{OZPU}^{\ddagger}$		$V_{CC} = 0\text{ to }2.1\text{ V}$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $\overline{OE} = X$			±50			±50	μA
$I_{OZPD}^{\ddagger}$		$V_{CC} = 2.1\text{ V to }0$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $\overline{OE} = X$			±50			±50	μA
I_{off}		$V_{CC} = 0$, $V_I\text{ or }V_O \leq 4.5\text{ V}$						±100	μA
I_{CEX}		$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$			50			50	μA
$I_O^{\S}$		$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-100	-180	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$			3			3	mA
					20			20	
					2			2	
$\Delta I_{CC}^{\parallel}$		$V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$			1			1	mA
C_i	Control inputs	$V_I = 2.5\text{ V or }0.5\text{ V}$			3.5			3.5	pF
C_{io}	A or B ports	$V_O = 2.5\text{ V or }0.5\text{ V}$			9.5			9.5	pF

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This parameter is specified by characterization.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

∥ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}^{\#}$	SN54ABTH32543		SN74ABTH32543		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		3.3		3.3		ns
t_{su}	Setup time	Data before $\overline{LEAB}\uparrow$ or $\overline{LEBA}\uparrow$	2.1		2.6		ns
		Data before $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$	1.7		2		
t_h	Hold time	Data after $\overline{LEAB}\uparrow$ or $\overline{LEBA}\uparrow$	0.6		1.1		ns
		Data after $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$	0.9		1.2		

These limits apply only to the SN74ABTH32543.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}^\dagger$			SN54ABTH32543		SN74ABTH32543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	3.5	5.2	0.5	6.3	1	5.9	ns
t_{PHL}			1	3.5	5.1	0.5	5.9	1	5.7	
t_{PLH}	$\overline{LE}$	A or B	1.9	4.6	6.3	0.8	7.9	1.9	7.5	ns
t_{PHL}			1.9	4.3	5.9	0.8	6.9	1.9	6.6	
t_{PZH}	$\overline{CE}$	A or B	1.7	4.3	6.7	0.8	8.3	1.7	8	ns
t_{PZL}			2.6	5.2	8	1	8.8	2.6	8.8	
t_{PHZ}	$\overline{CE}$	A or B	1.6	3.8	6.6	0.5	7.4	1.6	7.1	ns
t_{PLZ}			2.4	4.6	7	1	7.9	2.4	7.5	
t_{PZH}	$\overline{OE}$	A or B	1.4	3.8	6.1	0.5	7.6	1.4	7.3	ns
t_{PZL}			2.3	4.7	7.4	1	8.2	2.3	8.1	
t_{PHZ}	$\overline{OE}$	A or B	1.3	3.4	6.1	0.5	6.7	1.3	6.5	ns
t_{PLZ}			2	4.2	6.6	0.8	7.2	2	6.9	

[†] These limits apply only to the SN74ABTH32543.

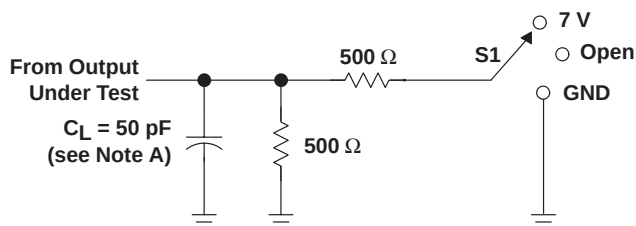
SN54ABTH32543, SN74ABTH32543

36-BIT REGISTERED BUS TRANSCEIVERS

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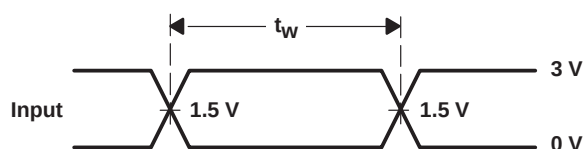
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PARAMETER MEASUREMENT INFORMATION

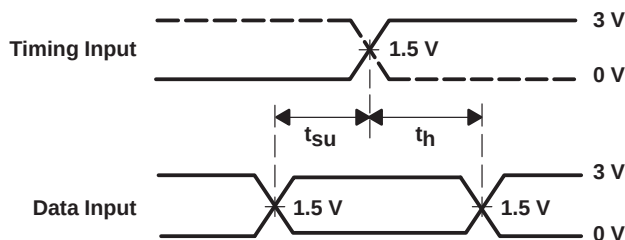


LOAD CIRCUIT

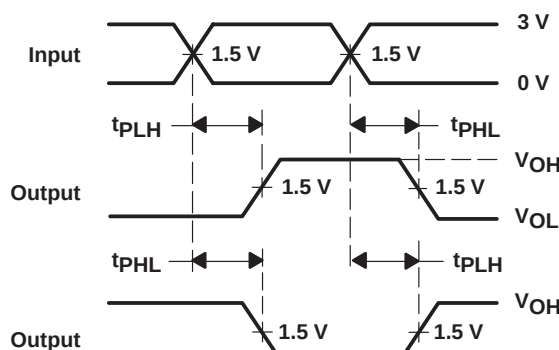
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



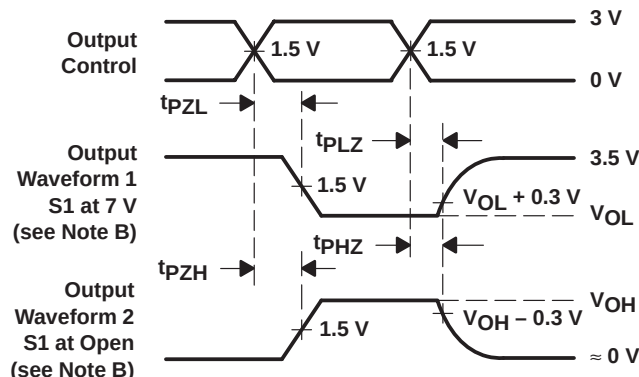
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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