

LM74701-Q1 "TVS Less" Low IQ Reverse Battery Protection Ideal Diode Controller

1 Features

- AEC-Q100 qualified with the following results
 - Device temperature grade 1: -40°C to $+125^{\circ}\text{C}$ ambient operating temperature range
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- 3.2-V to 65-V input range (3.9-V start up)
- -33-V reverse voltage rating
- Charge pump for external N-Channel MOSFET
- 20-mV ANODE to CATHODE forward voltage drop regulation
- 1- μA shutdown current (EN = Low)
- 80- μA operating quiescent current (EN = High)
- 2.3-A peak gate turnoff current
- Fast response to reverse current blocking: $< 0.75\ \mu\text{s}$
- Integrated battery voltage monitoring switch (SW)
- Meets automotive ISO7637 transient requirements without additional input TVS diode (**TVS Less**)
- 8-Pin SOT-23 package 2.90 mm $\times$ 1.60 mm

2 Applications

- Automotive ADAS systems - camera
- Automotive infotainment systems - head unit, telematics control unit
- Automotive USB hubs

3 Description

The LM74701-Q1 is an automotive AEC Q100 qualified ideal diode controller which operates in conjunction with an external N-channel MOSFET as an ideal diode for low loss reverse polarity protection with a 20-mV forward voltage drop. LM74701-Q1 is suitable for input protection of 12-V automotive systems. The 3.2-V input voltage support is particularly well suited for severe cold crank requirements in automotive systems.

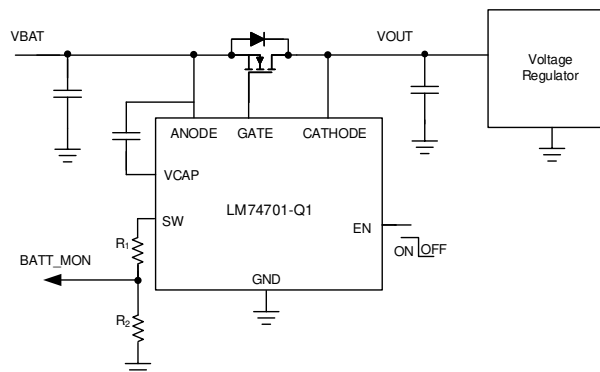
The device controls the GATE of the MOSFET to regulate the forward voltage drop at 20 mV. The regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. Fast response ($< 0.75\ \mu\text{s}$) to Reverse Current Blocking makes the device suitable for systems with output voltage holdup requirements during ISO7637 pulse testing as well as power fail and input micro-short conditions. The LM74701-Q1 has an unique integrated VDS clamp feature which enables users to achieve **"TVS Less"** input polarity protection solution and save on average a typical 60% of PCB space in constrained automotive systems.

The LM74701-Q1 controller provides a charge pump gate drive for an external N-channel MOSFET. With the enable pin low, the controller is off and draws approximately 1 μA of current.

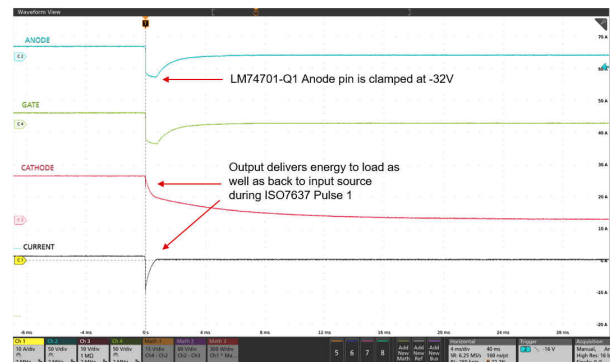
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM74701-Q1	SOT-23 (8)	2.90 mm $\times$ 1.60 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Schematic



"TVS Less" ISO7637-2 Pulse 1 Performance



Table of Contents

1 Features	1	9 Application and Implementation	14
2 Applications	1	9.1 Application Information.....	14
3 Description	1	9.2 Typical Application.....	14
4 Revision History	2	9.3 What to Do and What Not to Do.....	18
5 Pin Configuration and Functions	3	10 Power Supply Recommendations	19
6 Specifications	4	11 Layout	19
6.1 Absolute Maximum Ratings	4	11.1 Layout Guidelines.....	19
6.2 ESD Ratings	4	11.2 Layout Example.....	19
6.3 Recommended Operating Conditions	4	12 Device and Documentation Support	20
6.4 Thermal Information	5	12.1 Receiving Notification of Documentation Updates..	20
6.5 Electrical Characteristics	5	12.2 Support Resources.....	20
6.6 Switching Characteristics	6	12.3 Trademarks.....	20
7 Parameter Measurement Information	7	12.4 Electrostatic Discharge Caution.....	20
8 Detailed Description	8	12.5 Glossary.....	20
8.1 Overview.....	8	13 Mechanical, Packaging, and Orderable	
8.2 Functional Block Diagram.....	8	Information	20
8.3 Feature Description.....	9	13.1 Tape and Reel Information.....	21
8.4 Device Functional Modes.....	11		

4 Revision History

DATE	REVISION	NOTES
June 2021	*	Initial release.

5 Pin Configuration and Functions

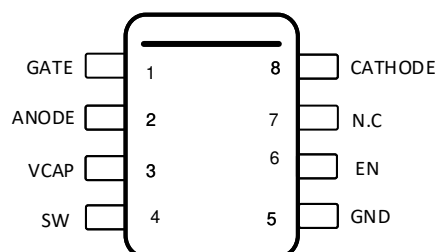


Figure 5-1. DDF Package 8-Pin SOT-23 Top View

Table 5-1. Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET.
2	ANODE	I	Anode of the ideal diode and input power. Connect to the source of the external N-channel MOSFET.
3	VCAP	O	Charge pump output. Connect to external charge pump capacitor.
4	SW	I	Voltage sensing disconnect switch terminal. ANODE and SW are internally connected through a switch when EN is high. A resistor ladder from this pin to GND can be used to monitor battery voltage. When EN is pulled low, the switch is OFF disconnecting the resistor ladder from the battery line thereby cutting off the leakage current.
5	GND	G	Ground pin.
6	EN	I	Enable pin. Can be connected to ANODE for always ON operation.
7	N.C	-	No connect. Keep this pin floating.
8	CATHODE	I	Cathode of the ideal diode. Connect to the drain of the external N-channel MOSFET.

(1) I = Input, O = Output, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input Pins	ANODE to GND	$-(V_{CLAMP}-1)$	65	V
	SW, EN to GND, $V_{(ANODE)} > 0$ V	-0.3	65	V
	EN to GND, $V_{(ANODE)} \leq 0$ V	$V_{(ANODE)}$	$(65 + V_{(ANODE)})$	V
	SW to GND, $V_{(ANODE)} \leq 0$ V	$V_{(ANODE)}$	$(0.3 + V_{(ANODE)})$	V
	I_{SW}	-1	10	mA
Output Pins	GATE to ANODE	-0.3	15	V
	VCAP to ANODE	-0.3	15	V
Output to Input Pins	CATHODE to ANODE	-5	V_{CLAMP}	V
Operating junction temperature ⁽²⁾		-40	150	°C
Storage temperature, T_{stg}		-40	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	
		Other pins	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
Input Pins	ANODE to GND	-60		60	V
	CATHODE to GND			60	
	EN to GND	-60		60	
Input to Output pins	ANODE to CATHODE	$-V_{CLAMP}$		5	V
External capacitance	ANODE	0.1		1	μF
	VCAP to ANODE	0.1			μF
External MOSFET max V_{GS} rating	GATE to ANODE	15			V
T_J	Operating junction temperature range ⁽²⁾	-40		150	°C

- (1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see [Electrical Characteristics](#).
- (2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM74701-Q1	UNIT
		DDF (SOT)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; typical values at $T_J = 25^{\circ}\text{C}$, $V_{(ANODE)} = 12\text{ V}$, $C_{(VCAP)} = 0.1\text{ }\mu\text{F}$, $V_{(EN)} = 3.3\text{ V}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ANODE} SUPPLY VOLTAGE						
V_{CLAMP}	V(CATHODE–ANODE) clamp voltage		34		43	V
$V_{(ANODE)}$	Operating input voltage		4		60	V
$V_{(ANODE\ POR)}$	VANODE POR Rising threshold				3.9	V
	VANODE POR Falling threshold		2.2	2.8	3.1	V
$V_{(ANODE\ POR(Hys))}$	VANODE POR Hysteresis		0.44		0.67	V
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)} = 0\text{ V}$		0.9	1.5	μA
$I_{(Q)}$	Operating Quiescent Current			80	130	μA
ENABLE INPUT						
$V_{(EN_IL)}$	Enable input low threshold		0.5	0.9	1.22	V
$V_{(EN_IH)}$	Enable input high threshold		1.06	2	2.6	V
$V_{(EN_Hys)}$	Enable Hysteresis		0.52		1.35	V
$I_{(EN)}$	Enable sink current	$V_{(EN)} = 12\text{ V}$		3	5	μA
V_{ANODE} to V_{CATHODE}						
$V_{(AK\ REG)}$	Regulated Forward $V_{(AK)}$ Threshold		13	20	29	mV
$V_{(AK)}$	$V_{(AK)}$ threshold for full conduction mode		34	54	59	mV
$V_{(AK\ REV)}$	$V_{(AK)}$ threshold for reverse current blocking		–17	–11	–2	mV
Gm	Regulation Error AMP Transconductance ⁽¹⁾		1200	1800	3100	$\mu\text{A/V}$
SWITCH						
$R_{(SW)}$	Battery sensing disconnect switch resistance	$4\text{ V} < V_{(ANODE)} \leq 60\text{ V}$	10	19.5	46	Ω
GATE DRIVE						
$I_{(GATE)}$	Peak source current	$V_{(ANODE)} - V_{(CATHODE)} = 100\text{ mV}$, $V_{(GATE)} - V_{(ANODE)} = 5\text{ V}$	3	11		mA
	Peak sink current	$V_{(ANODE)} - V_{(CATHODE)} = -20\text{ mV}$, $V_{(GATE)} - V_{(ANODE)} = 5\text{ V}$		2000		mA
	Regulation max sink current	$V_{(ANODE)} - V_{(CATHODE)} = 0\text{ V}$, $V_{(GATE)} - V_{(ANODE)} = 5\text{ V}$	6	26		μA
$R_{DS\ ON}$	discharge switch $R_{DS\ ON}$	$V_{(ANODE)} - V_{(CATHODE)} = -20\text{ mV}$, $V_{(GATE)} - V_{(ANODE)} = 100\text{ mV}$	0.4		2	Ω
CHARGE PUMP						

6.5 Electrical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; typical values at $T_J = 25^{\circ}\text{C}$, $V_{(\text{ANODE})} = 12\text{ V}$, $C_{(\text{VCAP})} = 0.1\text{ }\mu\text{F}$, $V_{(\text{EN})} = 3.3\text{ V}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(\text{VCAP})}$	Charge Pump source current (Charge pump on)	$V_{(\text{VCAP})} - V_{(\text{ANODE})} = 7\text{ V}$	162	300	600	μA
	Charge Pump sink current (Charge pump off)	$V_{(\text{VCAP})} - V_{(\text{ANODE})} = 14\text{ V}$		5	10	μA
$V_{(\text{VCAP})} - V_{(\text{ANODE})}$	Charge pump voltage at $V_{(\text{ANODE})} = 3.2\text{ V}$	$I_{(\text{VCAP})} \leq 30\text{ }\mu\text{A}$	8			V
	Charge pump turn on voltage		10.3	11.6	13	V
	Charge pump turn off voltage		11	12.4	13.9	V
	Charge Pump Enable comparator Hysteresis		0.4	0.8	1.2	V
$V_{(\text{VCAP UVLO})}$	$V_{(\text{VCAP})} - V_{(\text{ANODE})}$ UV release at rising edge	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$	5.7	6.5	7.5	V
	$V_{(\text{VCAP})} - V_{(\text{ANODE})}$ UV threshold at falling edge	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$	5.05	5.4	6.2	V
CATHODE						
$I_{(\text{CATHODE})}$	CATHODE sink current	$V_{(\text{ANODE})} = 12\text{ V}$, $V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV}$		1.7	2	μA
$I_{(\text{CATHODE})}$	CATHODE sink current	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV}$		1.2	2.5	μA
$I_{(\text{CATHODE})}$	CATHODE sink current	$V_{(\text{ANODE})} = -14\text{ V}$, $V_{(\text{DRAIN})} = 0\text{ V}$			2	μA
$I_{(\text{CATHODE})}$	CATHODE sink current	$V_{(\text{ANODE})} = -16\text{ V}$, $V_{(\text{CATHODE})} = 16\text{ V}$			24	μA

(1) Parameter guaranteed by design and characterization

6.6 Switching Characteristics

$T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$; typical values at $T_J = 25^{\circ}\text{C}$, $V_{(\text{ANODE})} = 12\text{ V}$, $C_{(\text{VCAP})} = 0.1\text{ }\mu\text{F}$, $V_{(\text{EN})} = 3.3\text{ V}$, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	Enable (low to high) to Gate Turn On delay	$V_{(\text{VCAP})} > V_{(\text{VCAP UVLO})}$		75	110	μs
$t_{\text{Reverse delay}}$	Reverse voltage detection to Gate Turn Off delay	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = 100\text{ mV}$ to -100 mV		0.45	0.75	μs
$t_{\text{Forward recovery}}$	Forward voltage detection to Gate Turn On delay	$V_{(\text{ANODE})} - V_{(\text{CATHODE})} = -100\text{ mV}$ to 700 mV		1.4	2.6	μs

7 Parameter Measurement Information

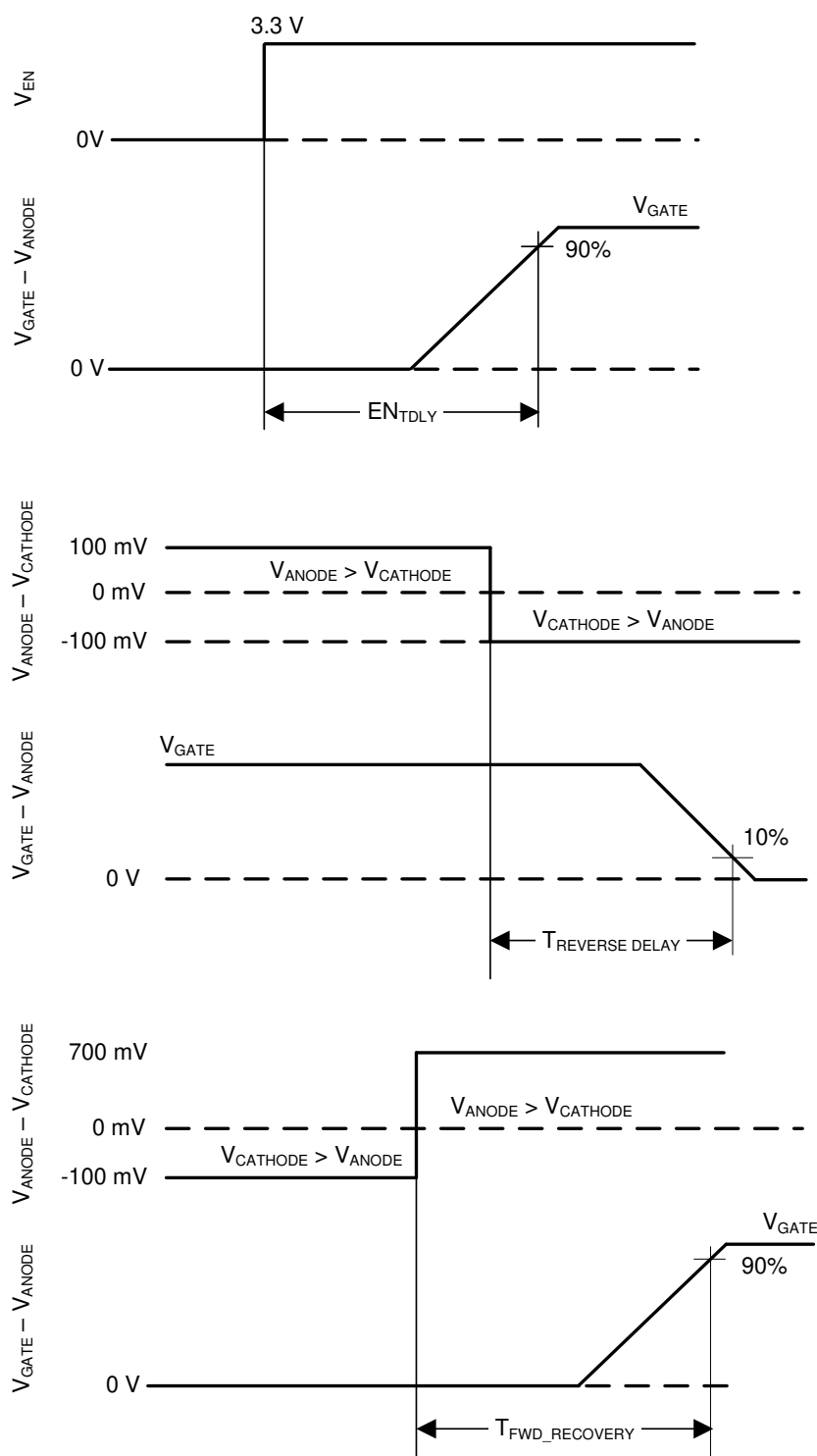


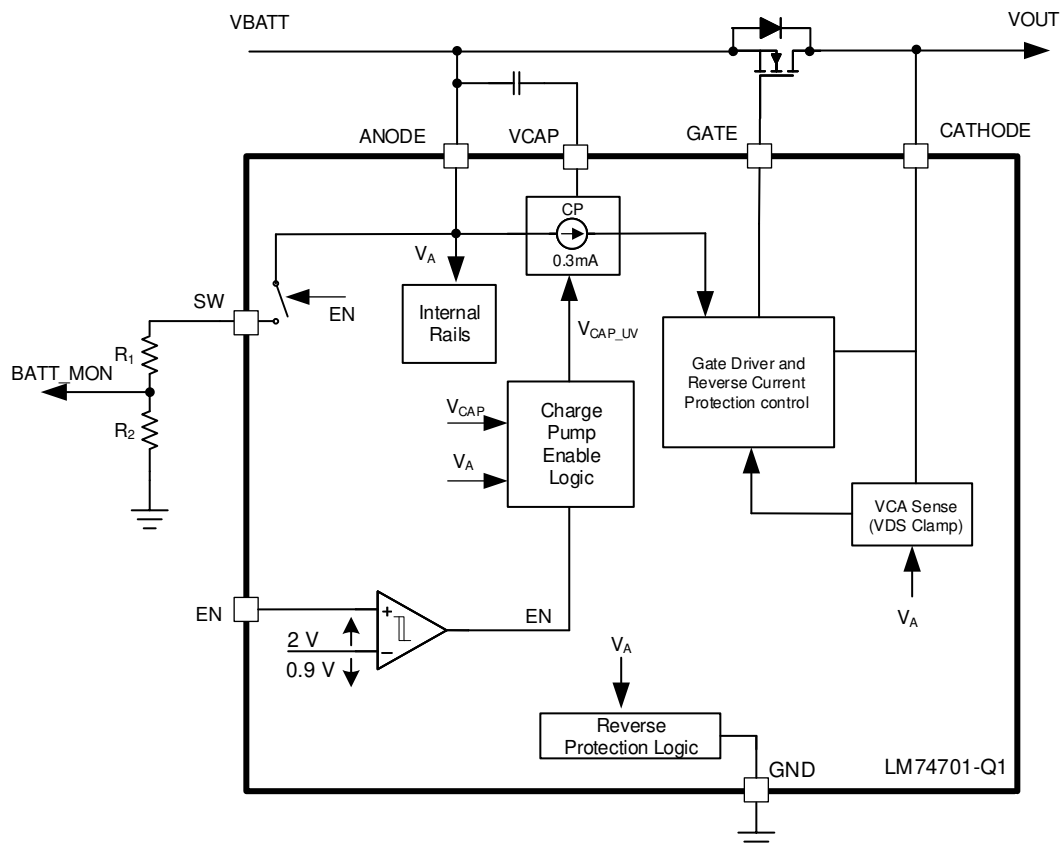
Figure 7-1. Timing Waveforms

8 Detailed Description

8.1 Overview

The LM74701-Q1 ideal diode controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit while minimizing the number of external components. This easy to use ideal diode controller is paired with an external N-channel MOSFET to replace other reverse polarity schemes such as a P-channel MOSFET or a Schottky diode. An internal charge pump is used to drive the external N-Channel MOSFET to a maximum gate drive voltage of approximately 12 V. The voltage drop across the MOSFET is continuously monitored between the ANODE and CATHODE pins, and the GATE to ANODE voltage is adjusted as needed to regulate the forward voltage drop at 20 mV. This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse drop event and ensures zero DC reverse current flow. A fast reverse current condition is detected when the voltage across ANODE and CATHODE pins reduces below –11 mV, resulting in the GATE pin being internally connected to the ANODE pin turning off the external N-channel MOSFET, and using the body diode to block any of the reverse current. An enable pin, EN is available to place the LM74701-Q1 in shutdown mode disabling the N-Channel MOSFET and minimizing the quiescent current. When device is enabled, an internal switch between SW and ANODE pin enables input voltage monitoring using an external resistor divider connected to SW pin. The device integrates **VDS clamp** feature which enables input "TVS Less" reverse polarity protection. For additional details on achieving input "TVS Less" reverse polarity protection solution, refer to device [Functional Modes](#) and [Application Information](#) section.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage

The ANODE pin is used to power the LM74701-Q1's internal circuitry, typically drawing 80 μA when enabled and 1 μA when disabled. If the ANODE pin voltage is greater than the POR rising threshold, then LM74701-Q1 operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from ANODE to GND is designed to vary from 65 V to –33 V, allowing the LM74701-Q1 to withstand negative voltage input.

8.3.2 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and ANODE pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor the EN pin voltage must be above the specified input high threshold, $V_{(EN_IH)}$. When enabled, the charge pump sources a charging current of 300- μA typical. If EN pins is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP to ANODE voltage must be above the undervoltage lockout threshold, typically 6.5 V, before the internal gate driver is enabled. Use [Equation 1](#) to calculate the initial gate driver enable delay.

$$T_{(DRV_EN)} = 75\mu\text{s} + C_{(VCAP)} \times \frac{V_{(VCAP_UVLOR)}}{300\mu\text{A}} \quad (1)$$

where

- $C_{(VCAP)}$ is the charge pump capacitance connected across ANODE and VCAP pins
- $V_{(VCAP_UVLOR)} = 6.5 \text{ V}$ (typical)

. To remove any chatter on the gate drive approximately 800 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to ANODE voltage reaches 12.4 V, typically, at which point the charge pump is disabled decreasing the current draw on the ANODE pin. The charge pump remains disabled until the VCAP to ANODE voltage is below to 11.6 V typically at which point the charge pump is enabled. The voltage between VCAP and ANODE continue to charge and discharge between 11.6 V and 12.4 V as shown in [Figure 8-1](#). By enabling and disabling the charge pump, the operating quiescent current of the LM74701-Q1 is reduced. When the charge pump is disabled it sinks 5 μA typically.

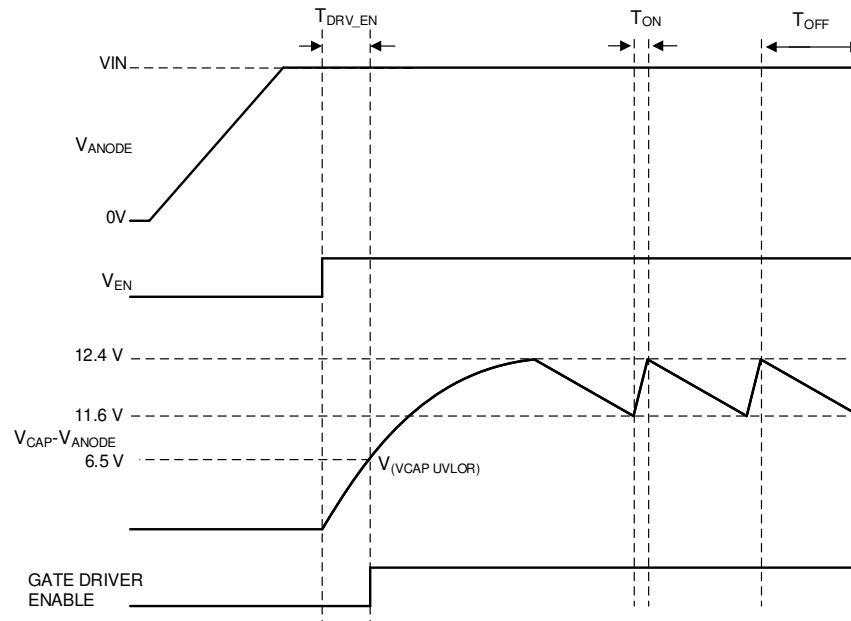


Figure 8-1. Charge Pump Operation

8.3.3 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the GATE to ANODE voltage to the corresponding mode of operation. There are four defined modes of operation that the gate driver operates under forward regulation, full conduction mode, reverse current protection and VDS clamp mode according to the ANODE to CATHODE voltage. These modes of operation are described in more detail in the [Regulated Conduction Mode](#), [Full Conduction Mode Reverse Current Protection Mode](#) and [VDS Clamp Mode](#) sections. [Figure 8-2](#) depicts how the modes of operation vary according to the ANODE to CATHODE voltage of the LM74701-Q1. The threshold between forward regulation mode and conduction mode is when the ANODE to CATHODE voltage is 50 mV. The threshold between forward regulation mode and reverse current protection mode is when the ANODE to CATHODE voltage is -11 mV. The threshold between reverse current protection mode and [VDS clamp mode](#) is when the ANODE to CATHODE voltage is -39-V typical.

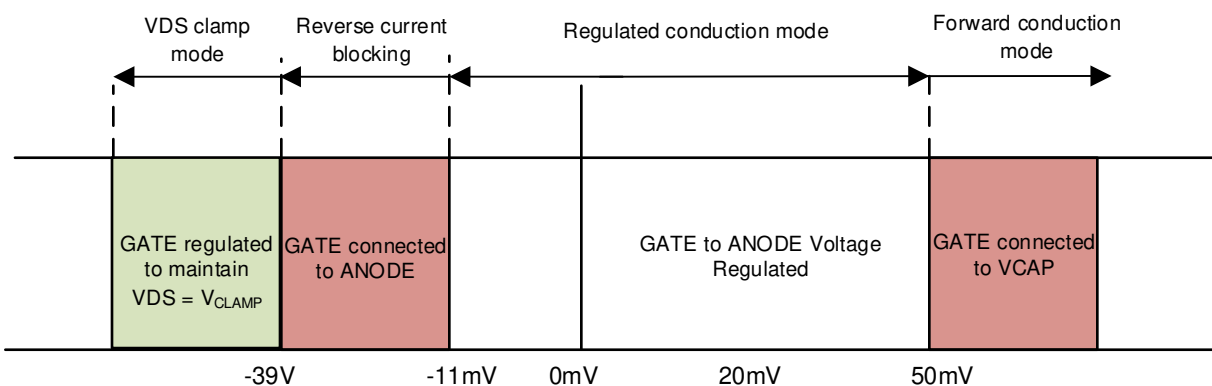


Figure 8-2. Gate Driver Mode Transitions

Before the gate driver is enabled following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP to ANODE voltage must be greater than the undervoltage lockout voltage.
- The ANODE voltage must be greater than VANODE POR Rising threshold.

If the above conditions are not achieved, then the GATE pin is internally connected to the ANODE pin, assuring that the external MOSFET is disabled. Once these conditions are achieved the gate driver operates in the correct mode depending on the ANODE to CATHODE voltage.

8.3.4 Enable

The LM74701-Q1 has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in [Gate Driver](#) and [Charge Pump](#) sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74701-Q1 in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as low as –33 V. This allows for the EN pin to be connected directly to the ANODE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 1 μ A pulls EN pin low and disables the device.

8.3.5 SW (Battery Voltage Monitoring)

The LM74701-Q1 has "SW" pin to enable battery voltage monitoring in automotive systems. When the device is enabled, an internal switch connects SW pin to ANODE. This enables monitoring battery voltage using an external resistor divider connected from SW pin to GND. When LM74701-Q1 is put in shutdown mode by pulling down the EN pin to ground, an internal switch between SW and ANODE pin is disconnected. This ensures there is no quiescent current drawn by the resistor ladder when system is put into low power shutdown mode. When not used, "SW" pin should be left floating.

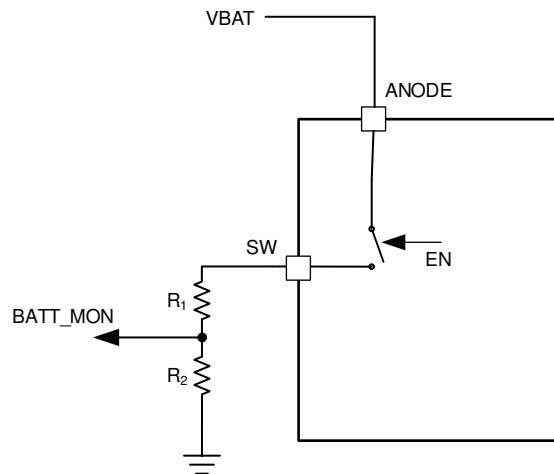


Figure 8-3. LM74701-Q1 SW Pin Functionality

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The LM74701-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold $V_{(EN_IL)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode, the LM74701-Q1 enters low I_Q operation with the ANODE pin only sinking 1 μ A. When the LM74701-Q1 is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the MOSFET's body diode.

8.4.2 Conduction Mode

Conduction mode occurs when the gate driver is enabled. There are three regions of operating during conduction mode based on the ANODE to CATHODE voltage of the LM74701-Q1. Each of the three modes is described in the [Regulated Conduction Mode](#), [Full Conduction Mode](#) and [VDS Clamp Mode](#) sections.

8.4.2.1 Regulated Conduction Mode

For the LM74701-Q1 to operate in regulated conduction mode, the gate driver must be enabled as described in the [Gate Driver](#) section and the current from source to drain of the external MOSFET must be within the range

to result in an ANODE to CATHODE voltage drop of -11 mV to 50 mV . During forward regulation mode the ANODE to CATHODE voltage is regulated to 20 mV by adjusting the GATE to ANODE voltage. This closed loop regulation scheme enables graceful turn off of the MOSFET at very light loads and ensures zero DC reverse current flow.

8.4.2.2 Full Conduction Mode

For the LM74701-Q1 to operate in full conduction mode the gate driver must be enabled as described in the [Gate Driver](#) section and the current from source to drain of the external MOSFET must be large enough to result in an ANODE to CATHODE voltage drop of greater than 50-mV typical. If these conditions are achieved the GATE pin is internally connected to the VCAP pin resulting in the GATE to ANODE voltage being approximately the same as the VCAP to ANODE voltage. By connecting VCAP to GATE the external MOSFET's $R_{DS(ON)}$ is minimized reducing the power loss of the external MOSFET when forward currents are large.

8.4.2.3 VDS Clamp Mode

The LM74701-Q1 features an integrated VDS clamp that operates the external MOSFET as an active clamp element to dissipate automotive EMC transients such as ISO7637-2 pulse 1 transient where there is no output voltage hold up requirement and system is allowed to turn off during such EMC transients. VDS clamp threshold is selected such that LM74701-Q1 does not engage into VDS clamp operation thereby ensuring the FET remains OFF during the RCB state for the system level EMC tests where output voltage hold up is required such as input short interruptions/micro cuts (LV124 E-10, ISO16750-2).

When the ISO7637 pulse 1 is applied at the input of LM74701-Q1:

1. Device GATE goes low and turns OFF the MOSFET once the voltage drop across ANODE to CATHODE reaches V(AK_REV) threshold.
2. Once the voltage across Drain and Source of the MOSFET reaches VCLAMP level (35-V min), GATE is turned ON back in the saturation region, operating external MOSFET as an active clamp and dissipates the ISO7637 pulse 1 energy. The typical circuit operation of LM74701-Q1 during ISO7637 pulse 1 is shown in [Figure 8-4](#).

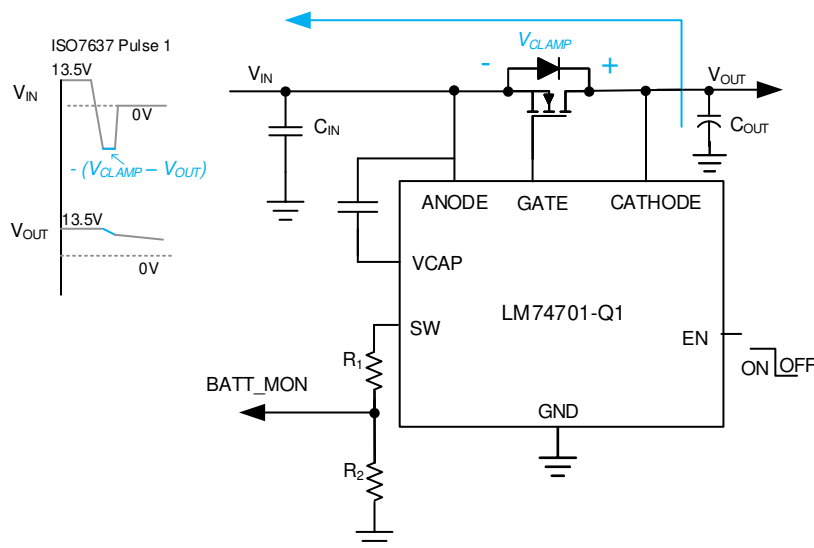


Figure 8-4. LM74701-Q1 Operation During VDS Clamp Mode

Note that the reverse current flows from VOUT back to input during the ISO7637 pulse 1 transient event, thus discharging VOUT capacitor. LM74701-Q1 CATHODE pin can handle negative voltage, however, if loads connected to the output of LM74701-Q1 can not handle negative voltage then the output filter should be designed to ensure that VOUT does not go negative during ISO7637 pulse 1 test. For all the other ISO7637 pulses (i.e pulse 2a, 2b, 3a, 3b), which are short duration transients, the input and output filter components

filtering effect suppresses these pulses. For additional details on system level EMC performance of LM74701-Q1, refer to [Application Information](#).

8.4.3 Reverse Current Protection Mode

For the LM74701-Q1 to operate in reverse current protection mode, the gate driver must be enabled as described in the [Gate Driver](#) section and the current of the external MOSFET must be flowing from the drain to the source. When the ANODE to CATHODE voltage is typically less than -11 mV reverse current protection mode is entered and the GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LM74701-Q1 is used with N-Channel MOSFET to achieve a typical reverse polarity protection solution. The schematic for the 12-V battery protection application is shown in Figure 9-1 where the LM74701-Q1 is used to drive N-Channel MOSFET Q1 in series with a battery. The VDS clamp feature integrated into LM74701-Q1 enables input TVS-less operation. The output capacitor C_{OUT} is recommended to protect the immediate output voltage collapse as a result of line disturbance and to make sure output remains positive during all system EMC transient tests.

9.2 Typical Application

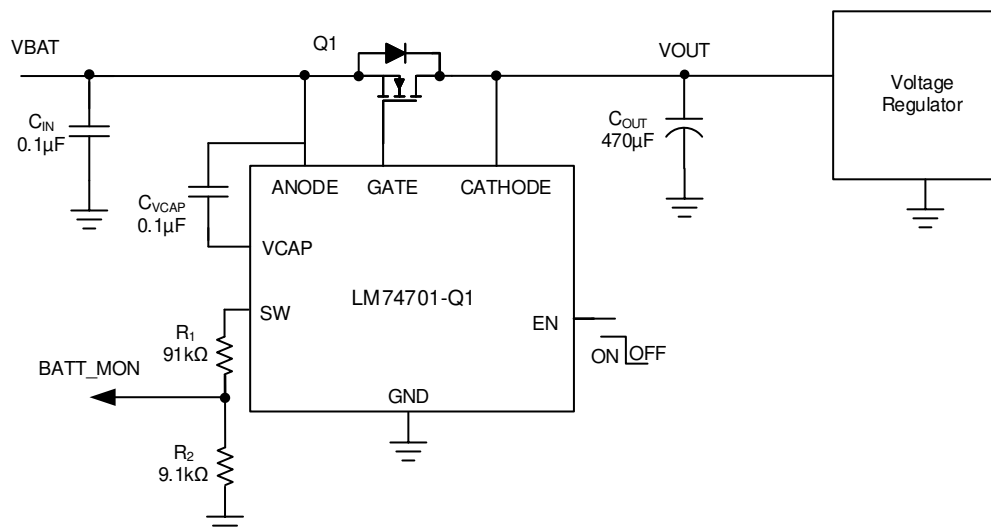


Figure 9-1. Typical Application Circuit

9.2.1 Design Requirements

A design example, with system design parameters listed in Table 9-1, is presented.

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12-V Battery, 13.5-V Nominal with 3.2-V Cold Crank and 35-V Load Dump
Output voltage	3.2 V during Cold Crank to 35-V Load Dump
Output current range	3-A Nominal, 5-A Maximum
Output capacitance	470-µF Typical Hold Up Capacitance
Key Automotive EMC Tests	ISO 7637-2 (–100 V, Pulse 1, Pulse 2a, Pulse 2b), ISO 16750-2 (Suppressed load dump 35 V), LV124, E-10 (Input Micro Short)

9.2.2 Detailed Design Procedure

9.2.2.1 Design Considerations

- Input operating voltage range, including cold crank and load dump conditions
- Nominal load current and maximum load current
- Robust EMC performance during key automotive EMC transient tests

9.2.2.2 MOSFET Selection

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current I_D , the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, Safe Operating Area (SOA), the maximum source current through body diode and the drain-to-source ON resistance $R_{DS(ON)}$.

The maximum continuous drain current (I_D) rating must exceed the maximum continuous load current.

To reduce the MOSFET conduction losses, MOSFET with the lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ may not be beneficial always. Higher $R_{DS(ON)}$ will provide increased voltage information to LM74701-Q1's reverse current comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with forward voltage drop of less than 50 mV at maximum current is a good starting point.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. With LM74701-Q1, the maximum differential voltage across the MOSFET is $V_{CLAMP(max)}$ of 43 V. A minimum of 60-V V_{DS} rated is recommended. This would include all the automotive transient events and any anticipated fault conditions.

During the ISO7637 Pulse 1, the maximum V_{DS} seen by the external MOSFET Q1 is $V_{DSCLAMP(max)}$ that is 43 V. The peak current during ISO7637-2 pulse 1 can be calculated by [Equation 2](#).

$$I_{ISO_PEAK} = (V_{ISO} + V_{OUT} - V_{DSCLAMP(max)}) / R_S \quad (2)$$

Where

- V_{ISO} is the negative peak of the ISO7637-2 pulse 1
- V_{OUT} is the initial level of the VBATT before ISO pulse is applied
- $V_{DSCLAMP}$ is maximum VCLAMP threshold of LM74701-Q1
- R_S is the ISO7637 pulse generator input impedance (10 Ω)

For ISO7637-2 pulse 1 with amplitude of –100 V, V_{OUT} nominal voltage of 13.5 V the peak current seen by MOSFET Q1 comes around 7 A.

The current profile tapers down from 7 A to 0 A from the peak of 7 A as shown in [Response to ISO 7637-2 Pulse 1](#). The resulting average current (I_{ISO_AVG}) can be approximated as one third of the peak current that is around 2.4 A. The V_{DS} clamp operation lasts for about 1 msec (max). Selecting a MOSFET with SOA characteristics covering the load line of 43 V which can support drain current greater than ($I_{ISO_PEAK}/2$) for 1 msec is a good starting point. For this particular design example, MOSFET which can support greater than 3.5 A of drain current at 43-V V_{DS} on SoA curve is suitable.

[Figure 9-2](#) shows typical SoA characteristics plot highlighting maximum drain current supported by the MOSFET for the duration of 1 msec. MOSFET data sheet SoA curves are typically plotted at ambient temperature, so consider sufficient margin over MOSFET parameters calculated values to ensure safe operation over desired operating temperature range.

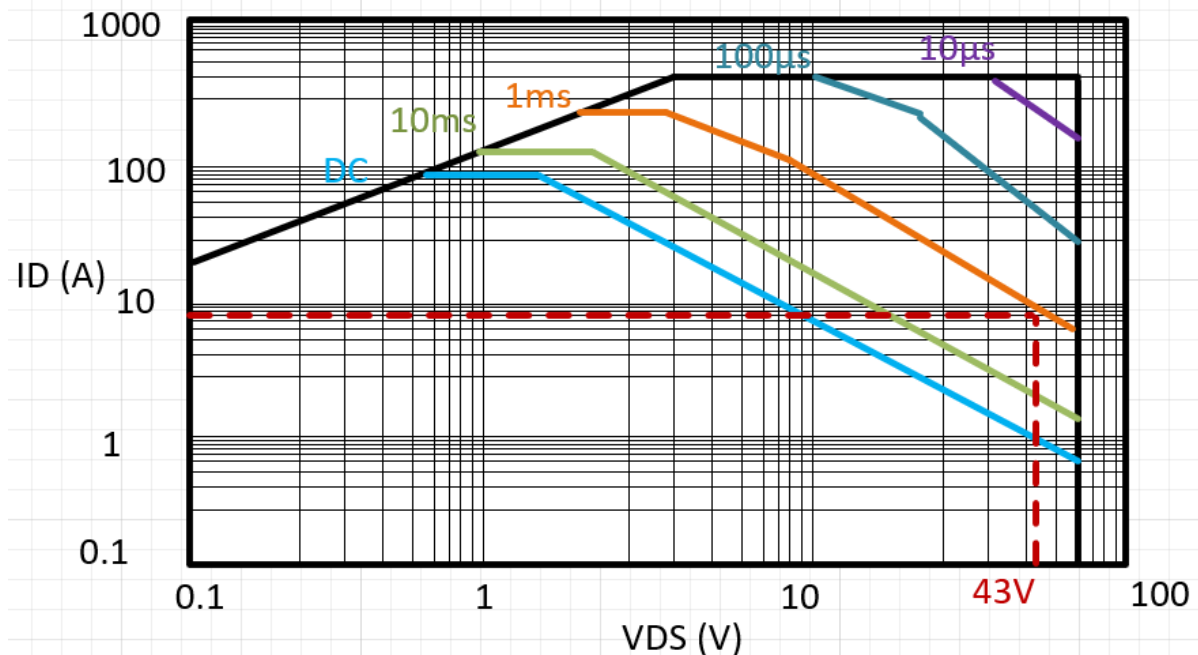


Figure 9-2. Typical MOSFET SoA Characteristics

As external MOSFET dissipates ISO7637-2 Pulse 1 energy, a special attention should be given while calculating maximum power dissipation and effective temperature rise. An average power dissipation across the MOSFET can be calculated by Equation 3.

$$P_{D_AVG} = V_{DS_CLAMP(max)} \times I_{ISO_AVG} \quad (3)$$

For given design example, average power dissipation comes around.

$$P_{D_AVG} = 43 \text{ V} \times 2.4 \text{ A} = 103.2 \text{ W} \quad (4)$$

Typical ISO7637-2 pulse 1 transient lasts for 2 ms with total time period of 200 ms between two consecutive pulses (Duty cycle of 1%). The effective temperature rise due to power dissipation across MOSFET during ISO7637-2 pulse 1 event can be calculated by looking at transient thermal impedance curve in a MOSFET data sheet. Figure 9-3 shows an example of how to estimate transient thermal impedance of a MOSFET for ISO7637-2 pulse 1 event.

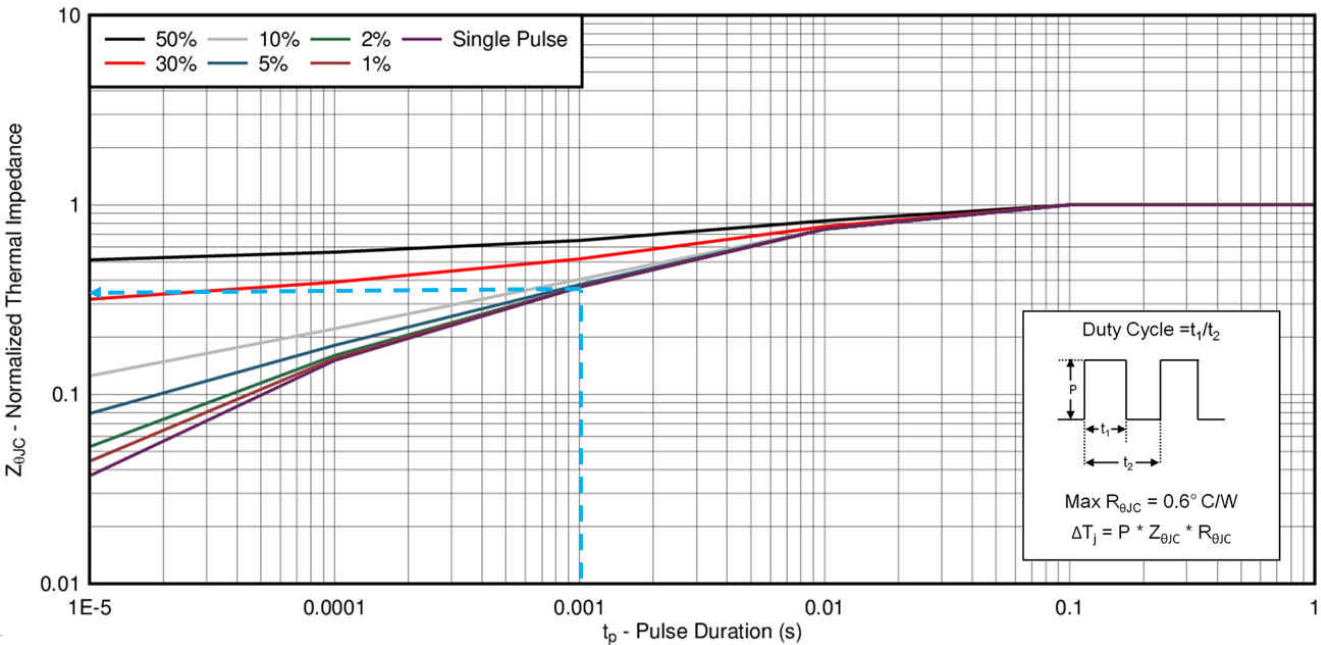


Figure 9-3. Typical MOSFET Transient Thermal Impedance

The maximum V_{GS} LM74701-Q1 can drive is 13.9 V, so a MOSFET with 15-V minimum V_{GS} rating should be selected.

Based on the design requirements and MOSFET selection criteria BUK7Y4R8-60E, SQJ460AEP, STL130N6F7 are some of the 60-V MOSFET options that can be selected.

9.2.2.3 Charge Pump VCAP (C_{VCAP}) and Input Capacitance (C_{IN})

Minimum required capacitance for charge pump VCAP and ANODE (input) is:

- VCAP: Minimum 0.1 μF is required; recommended value of VCAP (μF) $\geq 10 \times C_{ISS(\text{MOSFET})}(\mu\text{F})$
- C_{IN} : Minimum 0.1 μF of input capacitance placed closed to ANODE pin to GND

9.2.2.4 Output Capacitance (C_{OUT})

LM74701-Q1 CATHODE pin is capable of handling negative voltage. However, if loads connected to LM74701-Q1 output are not capable of handling negative voltage, then sufficient output capacitor is required to ensure output does not swing negative during ISO7637-2 pulse 1 operation.

The required output capacitor during ISO7637-2 pulse 1 to ensure output does not swing negative can be calculated using Equation 5.

$$C_{OUT} = (I_{LOAD} + I_{ISO_AVG}) \times 1\text{ms} / \Delta V_{OUT} \quad (5)$$

Where ΔV_{OUT} is difference between V_{OUT} at the start and the end of ISO7637-2 pulse 1.

9.2.3 Application Curves

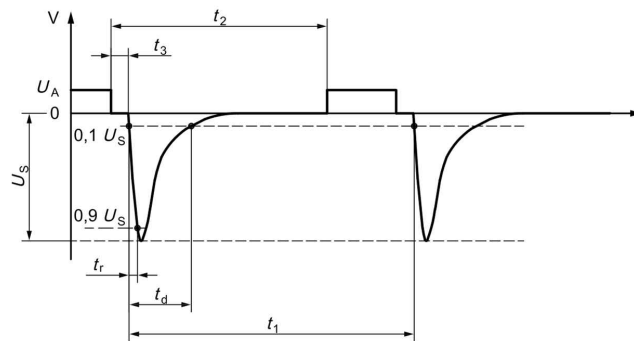
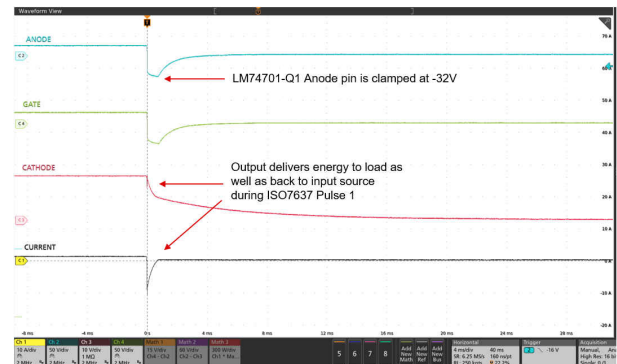
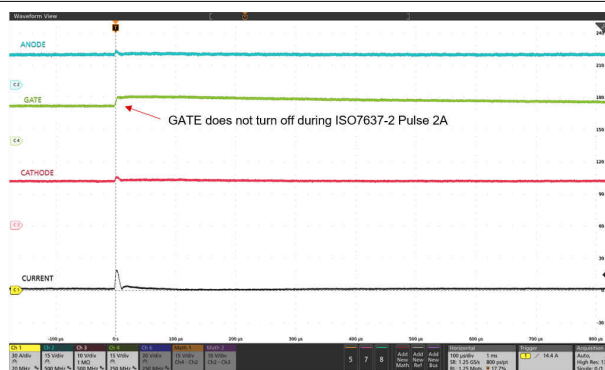


Figure 9-4. ISO 7637-2 Pulse 1



Time (4 ms/DIV)

Figure 9-5. Response to ISO 7637-2 Pulse 1



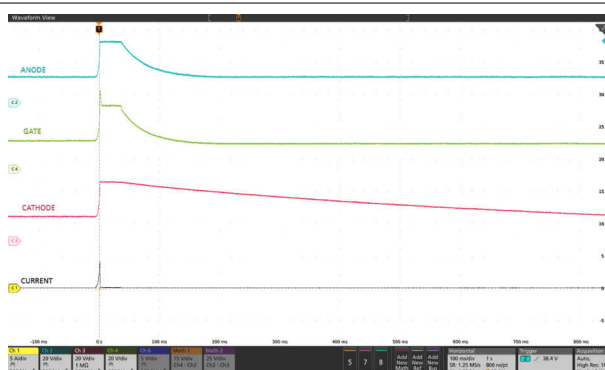
Time (100 μs/DIV)

Figure 9-6. Response to ISO 7637-2 Pulse 2A



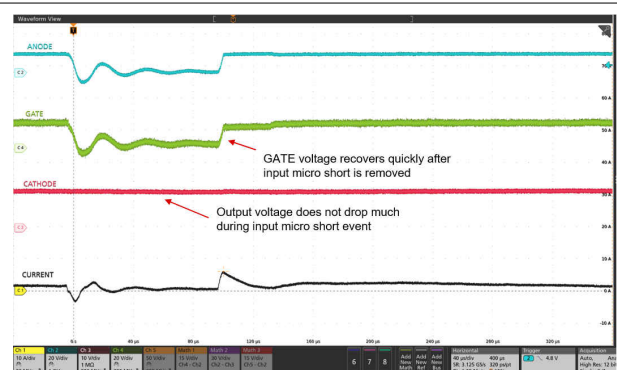
Time (200 ms/DIV)

Figure 9-7. Response to ISO 7637-2 Pulse 2B



Time (100 ms/DIV)

Figure 9-8. Response to ISO 16750-2 Pulse 5B



Time (40 μs/DIV)

Figure 9-9. Response to LV124 E-10 (Input Micro Short, 100 us)

9.3 What to Do and What Not to Do

- Place input decoupling capacitor (C_{IN}) close to ANODE pin.
- External MOSFET is used to dissipate transient energy in ISO7637-2 pulse 1 event. For the MOSFET with exposed thermal pad, make sure exposed thermal pad is in firm contact with PCB copper plane for efficient thermal transfer. Follow PCB layout and soldering guidelines mentioned in MOSFET data sheet.

10 Power Supply Recommendations

The LM74701-Q1 Ideal Diode Controller is designed for the supply voltage range of $3.2\text{ V} \leq V_{\text{ANODE}} \leq 65\text{ V}$. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 100 nF is recommended placed close to ANODE pin to GND. To prevent LM74701-Q1 and surrounding components from damage under the conditions of a direct output short circuit, it is necessary to use a power supply having over load and short circuit protection.

11 Layout

11.1 Layout Guidelines

- Place input capacitor close to ANODE pin to GND. Having smaller ground return path helps with better EMI performance.
- Connect ANODE, GATE and CATHODE pins of LM74701-Q1 close to the MOSFET's SOURCE, GATE and DRAIN pins.
- The high current path for this solution is through the MOSFET; therefore, it is important to use thick traces for source and drain of the MOSFET to minimize resistive losses.
- The charge pump capacitor across VCAP and ANODE pins must be kept away from the MOSFET to lower the thermal effects on the capacitance value.
- The Gate pin of the LM74701-Q1 must be connected to the MOSFET gate with short trace. Avoid excessively thin and long trace to the Gate Drive.
- Keep the GATE pin close to the MOSFET to avoid increase in MOSFET turn-off delay due to trace resistance.

11.2 Layout Example

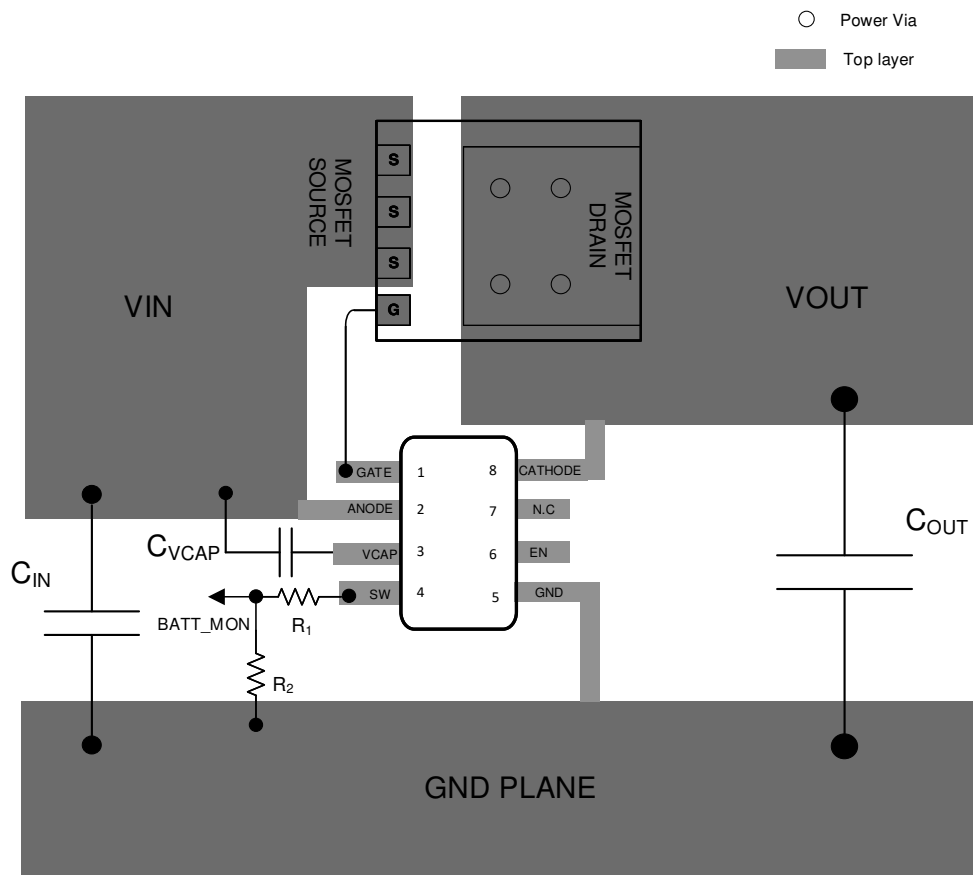


Figure 11-1. LM74701-Q1 Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

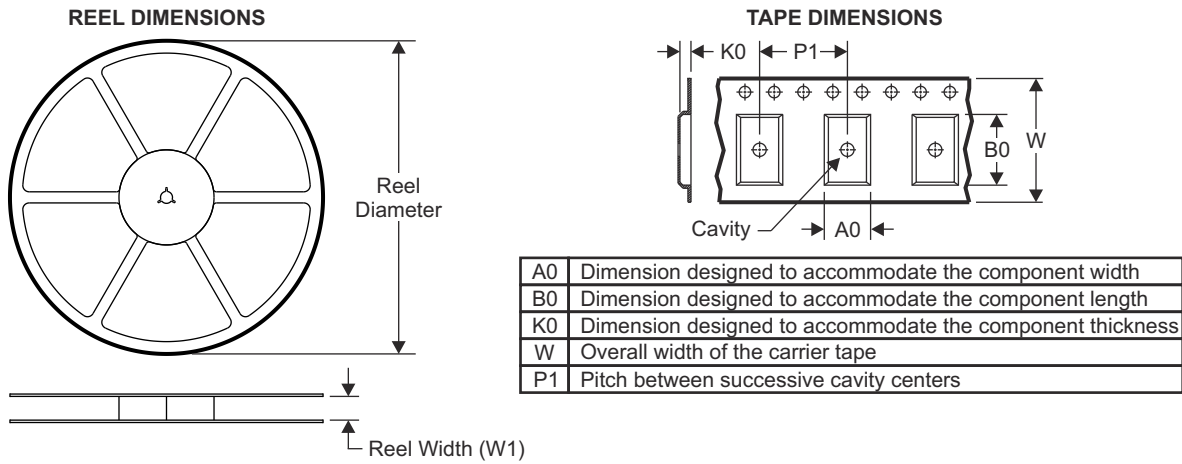
12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

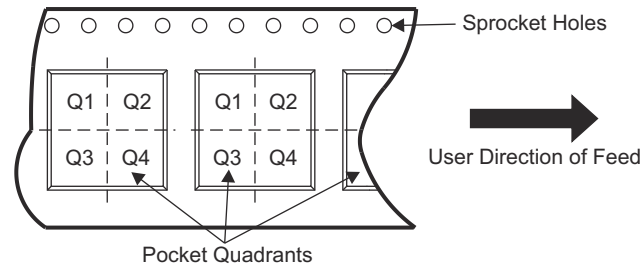
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Tape and Reel Information

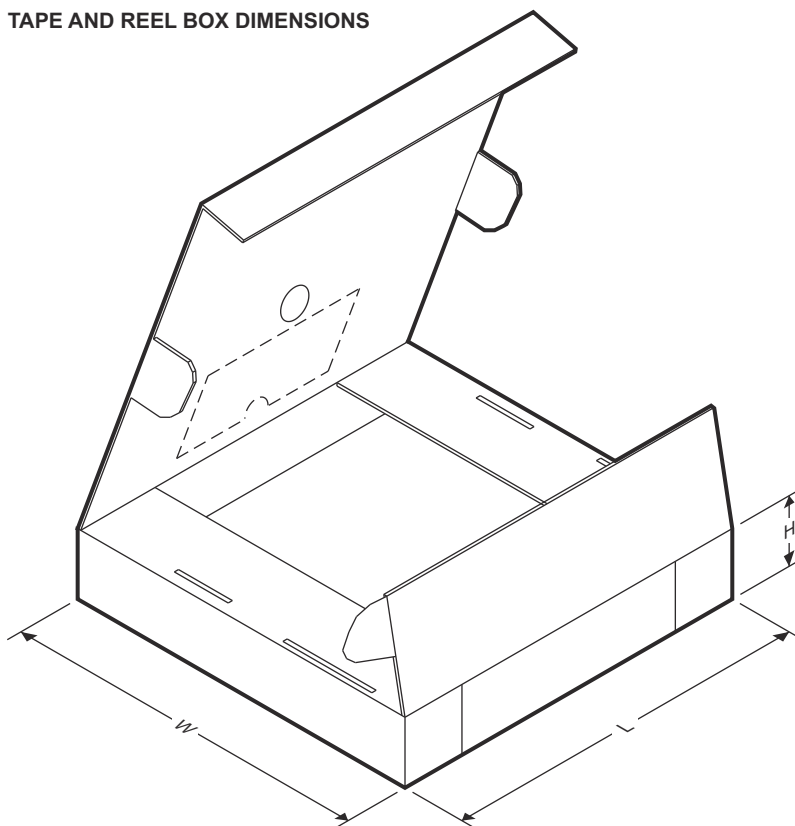


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM74701QDDFRQ1	SOT-23-THIN	DDF	8	3000	180	8.2	3.2	3.2	1.4	4	8	Q3

TAPE AND REEL BOX DIMENSIONS



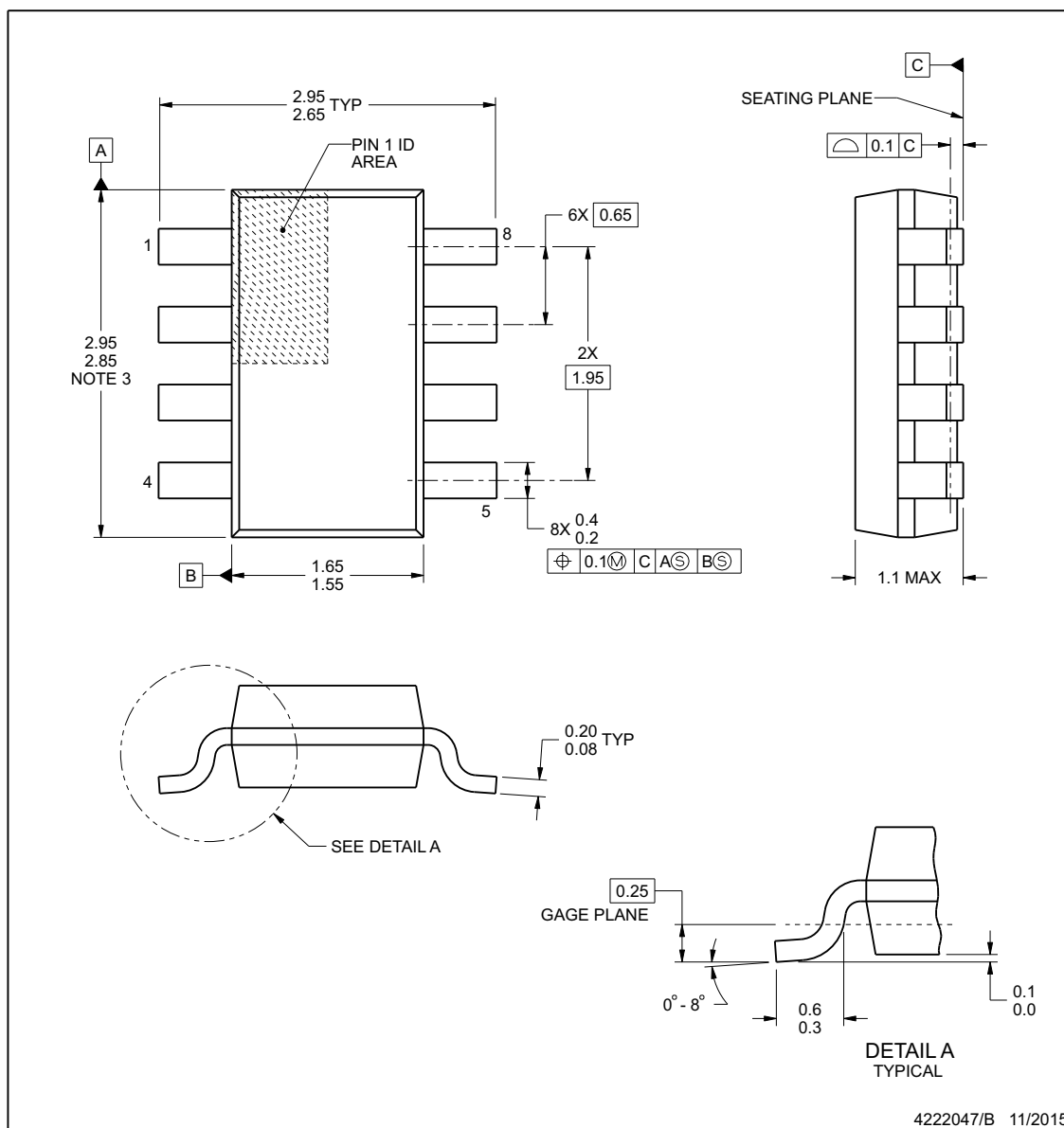
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM74701QDDFRQ1	SOT-23-THIN	DDF	8	3000	210	185	35



DDF0008A

PACKAGE OUTLINE
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

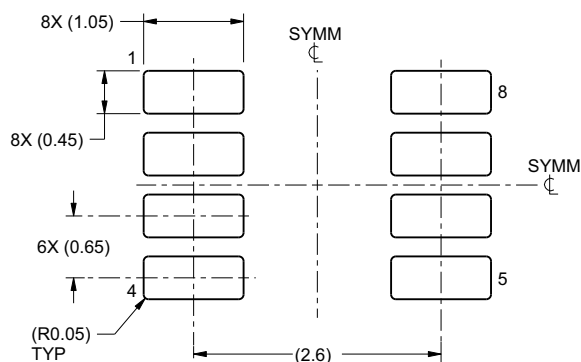
EXAMPLE BOARD LAYOUT

DDF0008A

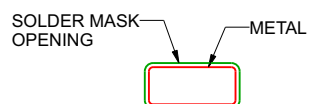
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE

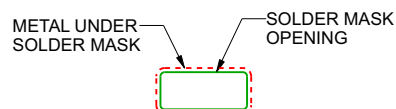
ADVANCE INFORMATION



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

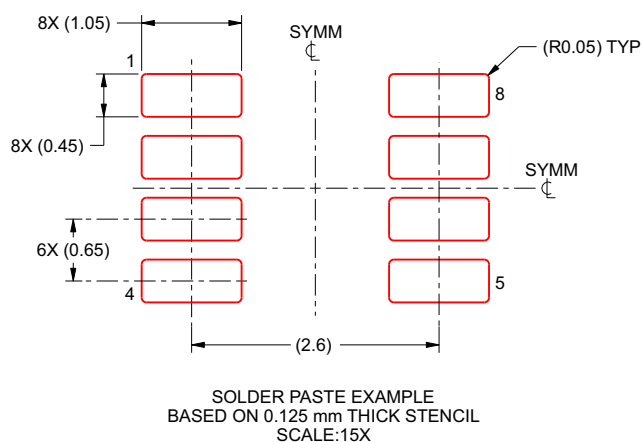
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/B 11/2015

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLM74701QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated