

Dual octal bus transceiver/registers (3-State)

MB2646

FEATURES

- Independent registers for A and B buses
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiplexed real-time and stored data
- Outputs sink 64mA and source 32mA

- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The MB2646 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The MB2646 dual transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{nOE}$) and Direction ($\overline{nDIR}$) pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

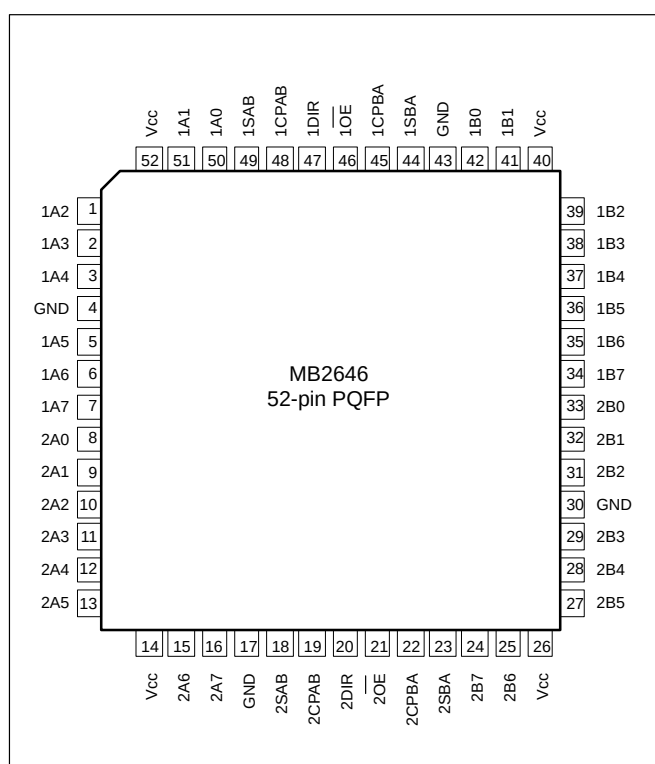
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nA_x to nB_x	$C_L = 50\text{pF}$; $V_{CC} = 5\text{V}$	3.2	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	$V_O = 0\text{V}$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	μA

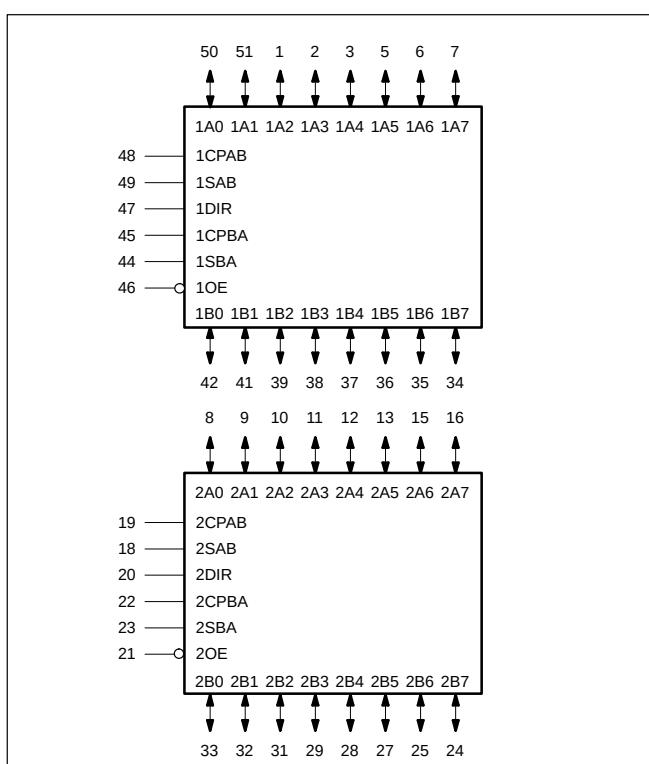
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
52-pin plastic Quad Flat Pack	-40°C to $+85^{\circ}\text{C}$	MB2646BB	1418B

PIN CONFIGURATION



LOGIC SYMBOL



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DESCRIPTION (continued)
The select (nSAB, nSBA) pins determine whether data is stored or transferred through the device in real-time. The nDIR determines which bus will receive data when the nOE is

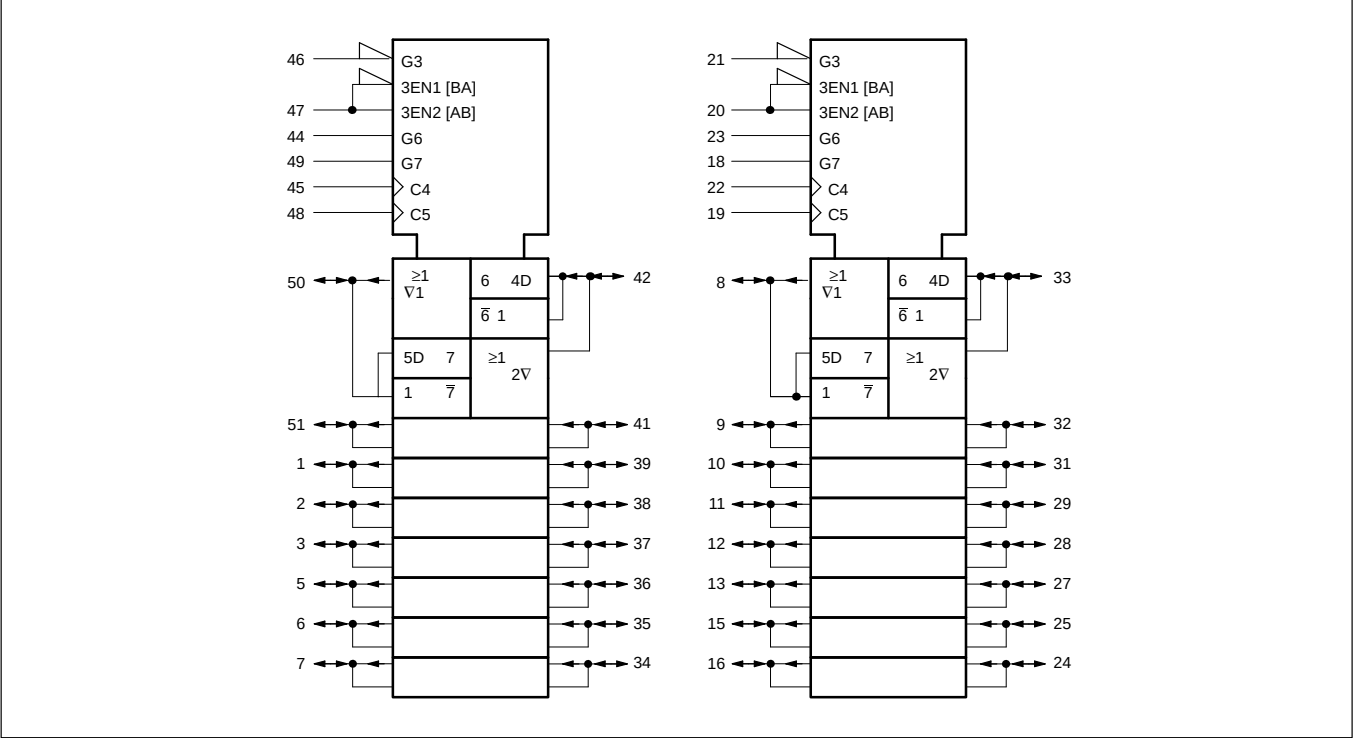
active Low. In the isolation mode (nOE = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output

function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
48, 45, 19, 22	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
49, 44, 18, 23	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
47, 20	1DIR, 2DIR	Direction control inputs
50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
46, 21	1OE, 2OE	Output enable inputs
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	VCC	Positive supply voltage

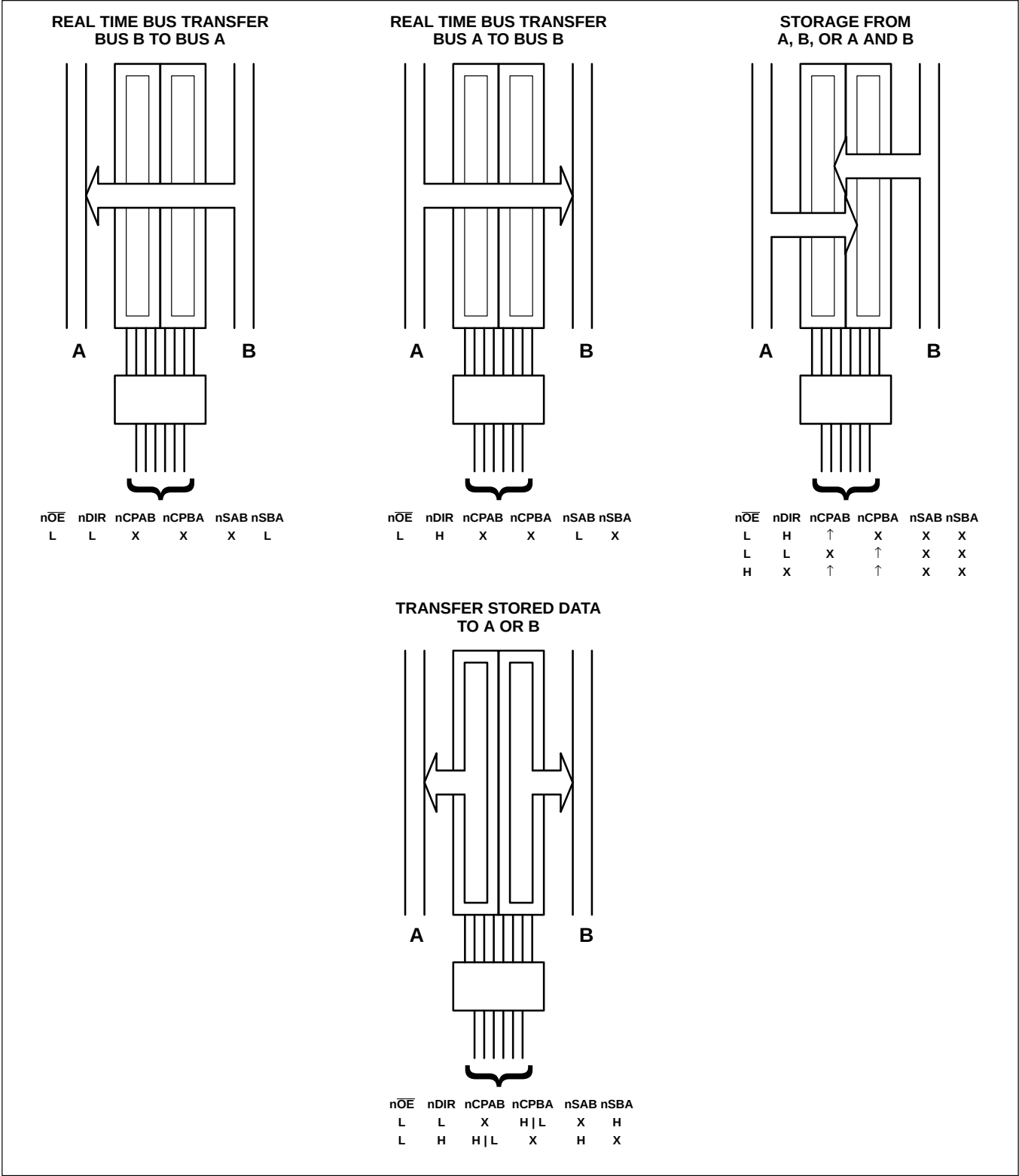
LOGIC SYMBOL (IEEE/IEC)



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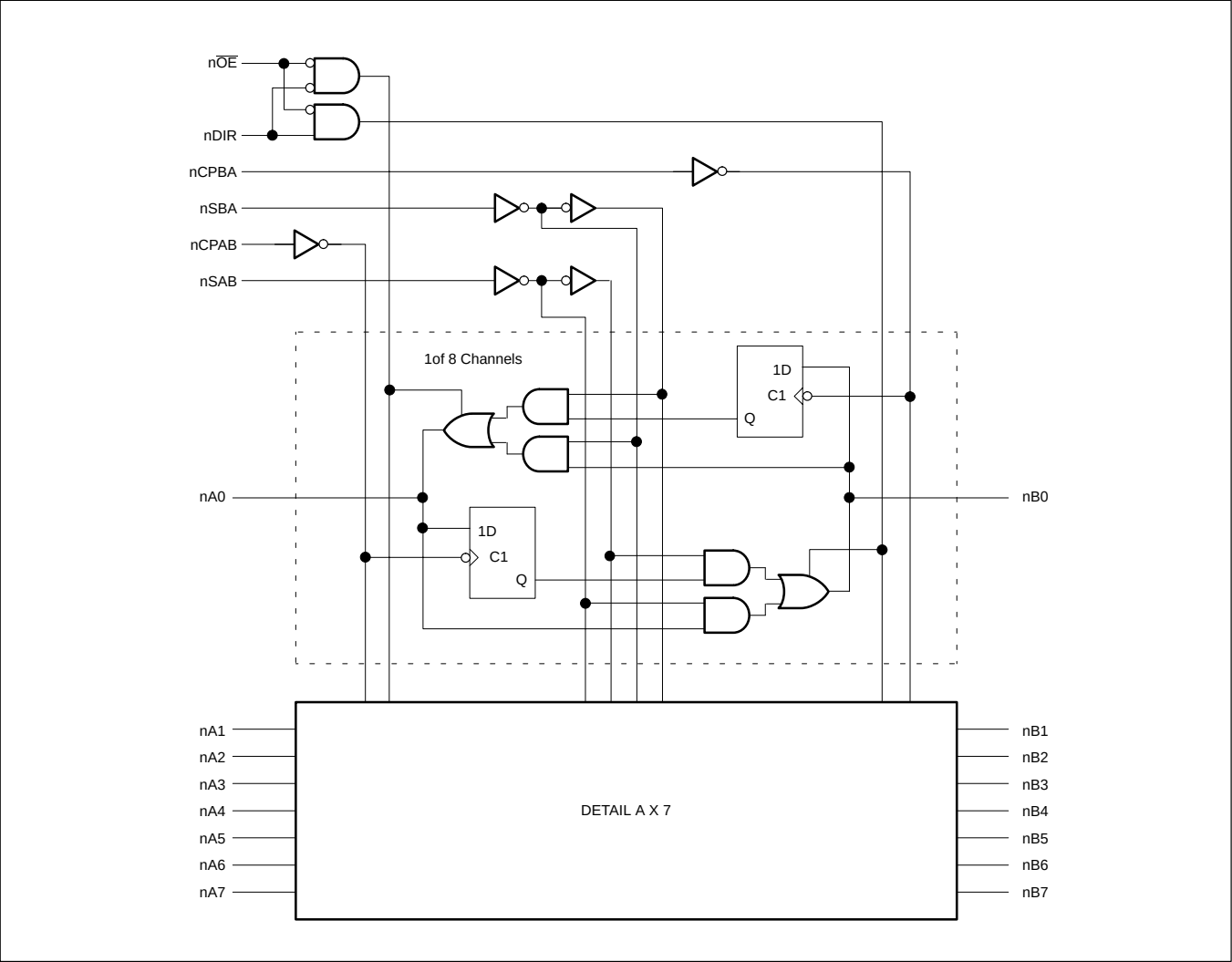
The following examples demonstrate the four fundamental bus-management functions that can be performed with the MB2646.



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOE	nDIR	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the nOE input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage ³		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = −40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage		V _{CC} = 4.5V; I _{IK} = −18mA		−0.9	−1.2		−1.2	V
V _{OH}	High-level output voltage		V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
			V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
			V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage		V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output voltage ^{NO TAG}		V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	Control pins	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
		Data pins	V _{CC} = 5.5V; V _I = GND or 5.5V		±5	±100		±100	μA
I _{OFF}	Power-off leakage current		V _{CC} = 0.0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴		V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	μA
I _{IH} + I _{OZH}	3-State output High current		V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{IL} + I _{OZL}	3-State output Low current		V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		−5.0	−50		−50	μA
I _{CEX}	Output High leakage current		V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹		V _{CC} = 5.5V; V _O = 2.5V	−50	−80	−180	−50	−180	mA
I _{CCH}	Quiescent supply current		V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		120	250		250	μA
I _{CCL}				37	60		60	mA	
I _{CCZ}				120	250		250	μA	
ΔI _{CC}	Additional supply current per input pin ²		V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$ a transition time of up to 100 μsec is permitted.

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AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	1	130	190		130		MHz
t _{PLH} t _{PHL}	Propagation delay nCPAB to nBx or nCPBA to nAx	1	2.2 2.4	3.9 4.6	5.1 5.4	2.2 2.4	5.6 5.9	ns
t _{PLH} t _{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.5 1.5	3.1 3.3	4.3 4.5	1.5 1.5	4.8 5.0	ns
t _{PLH} t _{PHL}	Propagation delay nSAB to nBx or nSBA to nAx	2, 3	1.5 1.8	3.7 3.9	4.8 4.9	1.5 1.8	5.5 5.6	ns
t _{PZH} t _{PZL}	Output enable time nOE to nAx or nBx	5 6	1.5 2.1	3.5 4.4	4.8 5.6	1.5 2.1	5.6 6.4	ns
t _{PHZ} t _{PLZ}	Output disable time nOE to nAx or nBx	5 6	2.1 1.5	3.8 3.1	5.0 4.2	2.1 1.5	5.7 4.7	ns
t _{PZH} t _{PZL}	Output enable time nDIR to nAx or nBx	5 6	1.5 2.3	4.2 4.9	5.4 6.2	1.5 2.3	6.2 6.9	ns
t _{PHZ} t _{PLZ}	Output disable time nDIR to nAx or nBx	5 6	2.1 1.5	3.8 3.2	5.0 4.3	2.1 1.5	5.7 5.0	ns

AC SETUP REQUIREMENTS

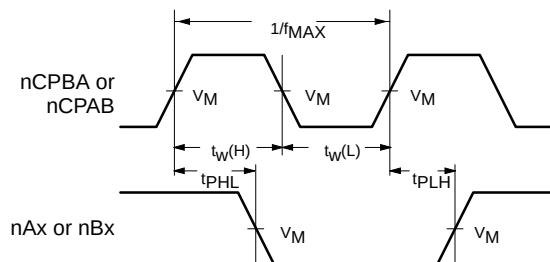
GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			MIN	TYP	MIN	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time nAx to nCPAB, nBx to nCPBA	4	2.0 1.5	0.7 0.0	2.0 1.5	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time nAx to nCPAB, nBx to nCPBA	4	1.5 1.0	0.0 -0.7	1.5 1.0	ns
$t_w(\text{H})$ $t_w(\text{L})$	Pulse width, High or Low nCPAB or nCPBA	1	4.5 3.0	2.5 2.0	4.5 3.0	ns

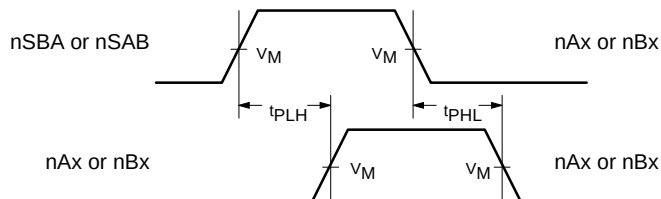
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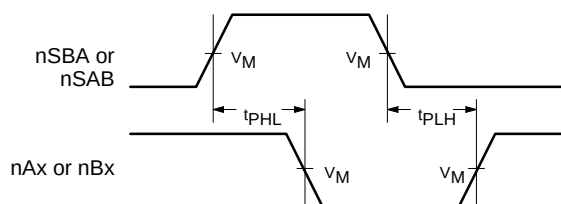
AC WAVEFORMS

 $V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$ 

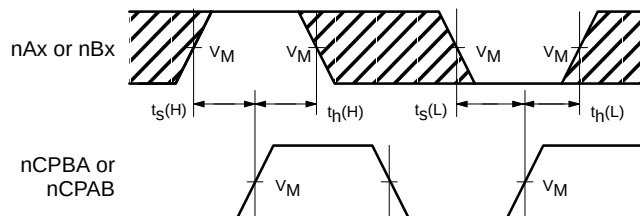
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



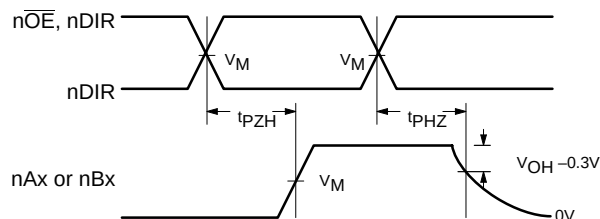
Waveform 2. Propagation Delay, nSAB to nBx or nSBA to nAx, nAx to nBx or nBx to nAx



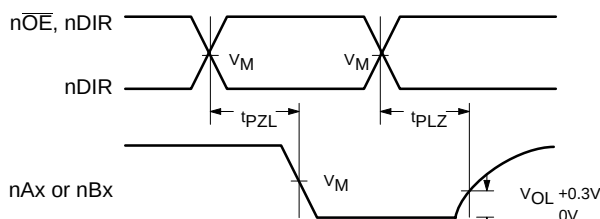
Waveform 3. Propagation Delay, nSBA to nAx or nSAB to nBx



Waveform 4. Data Setup and Hold Times



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

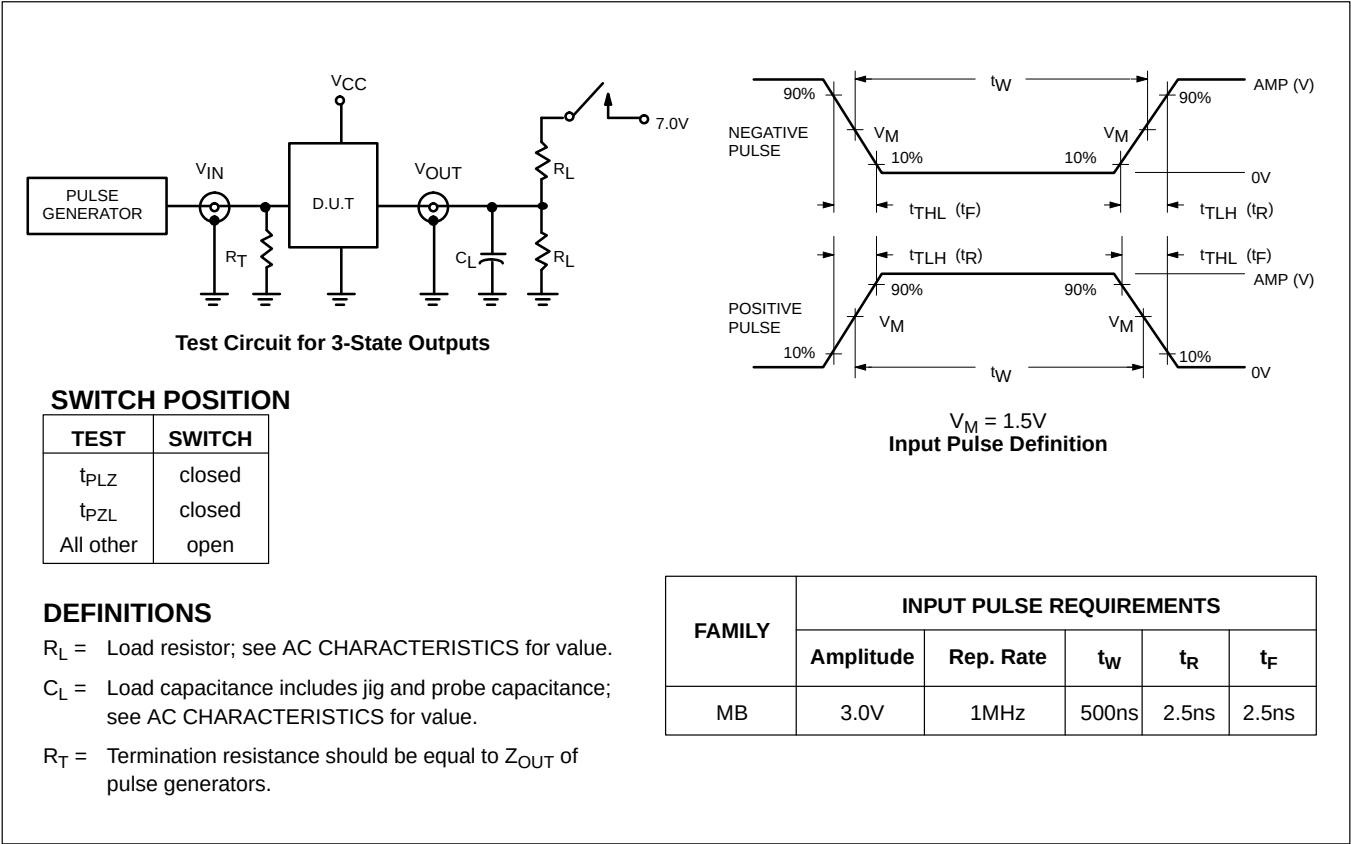


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

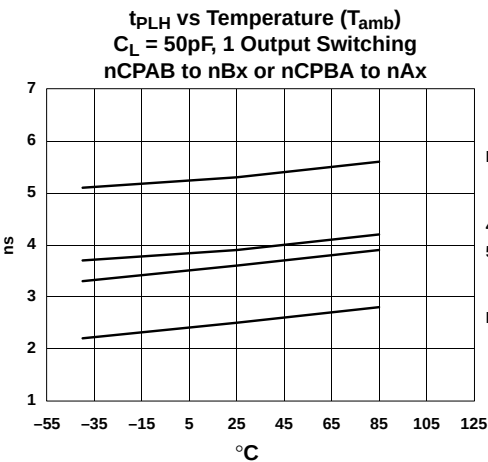
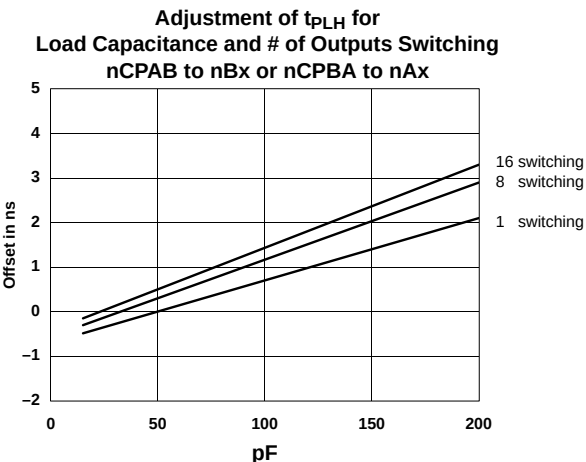
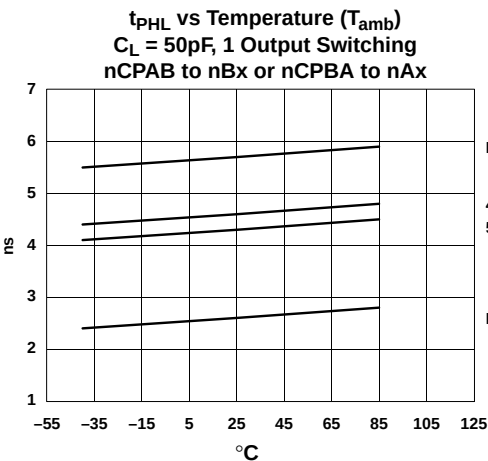
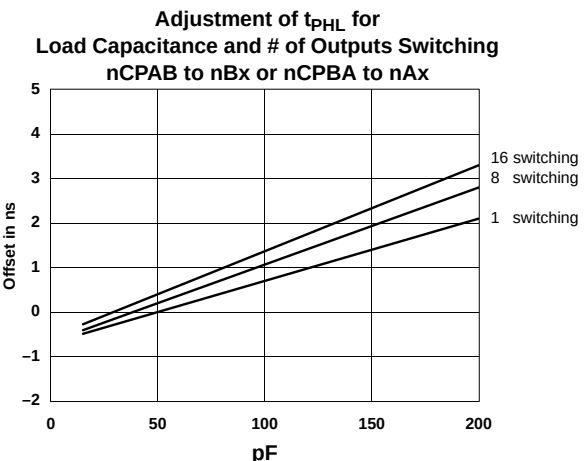
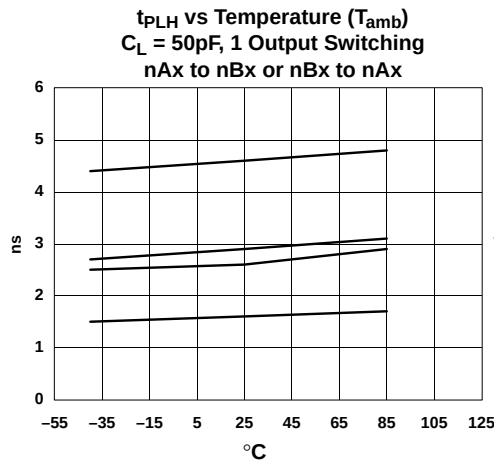
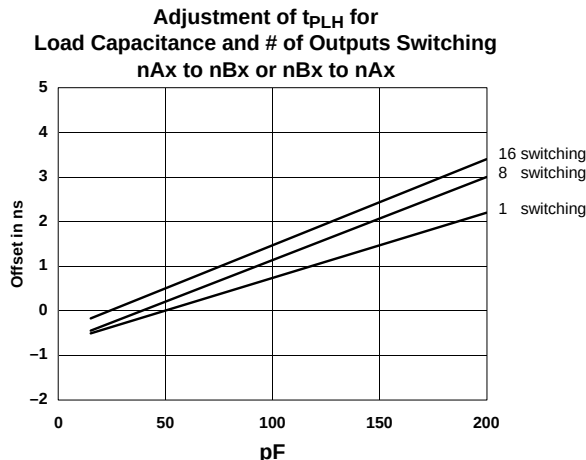
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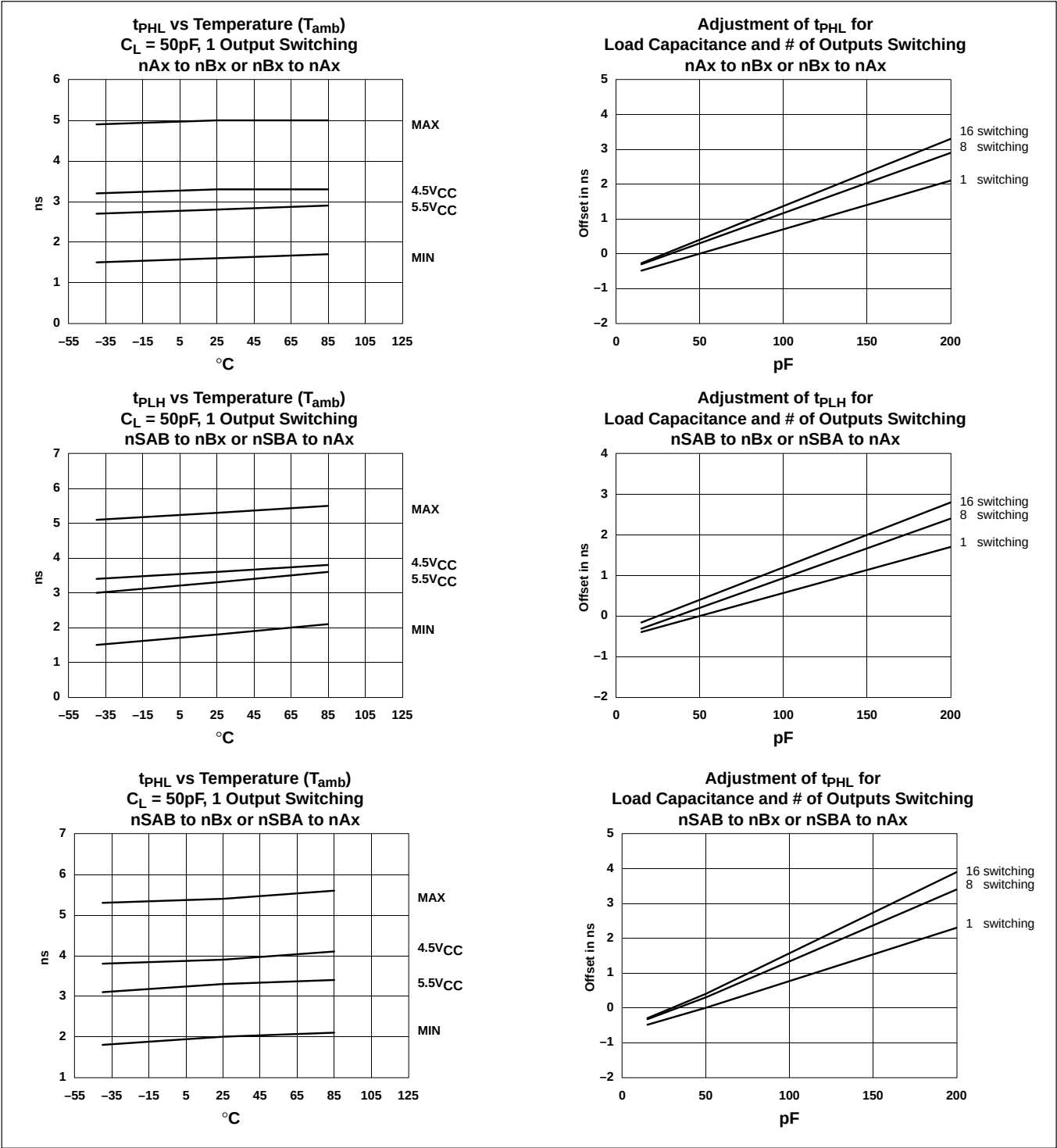
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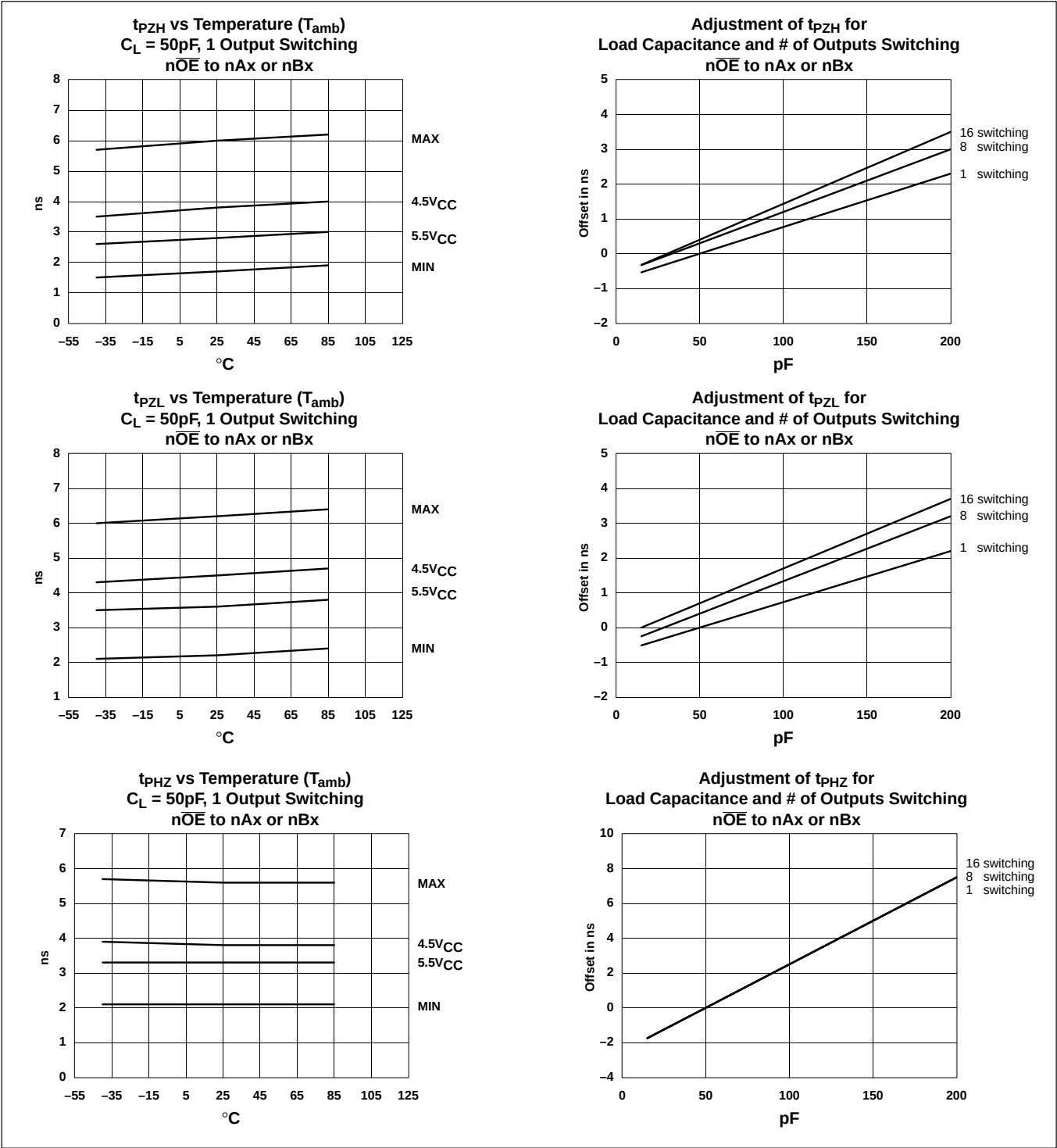
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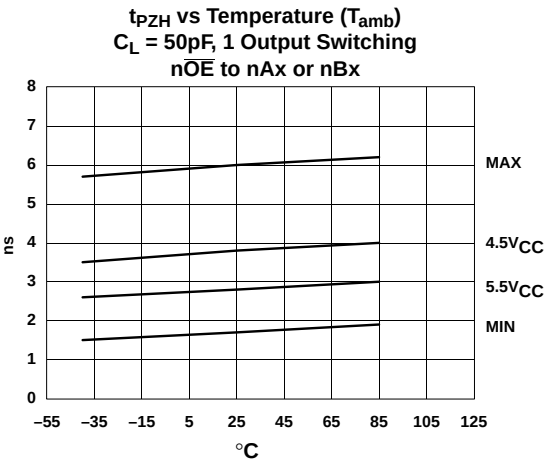
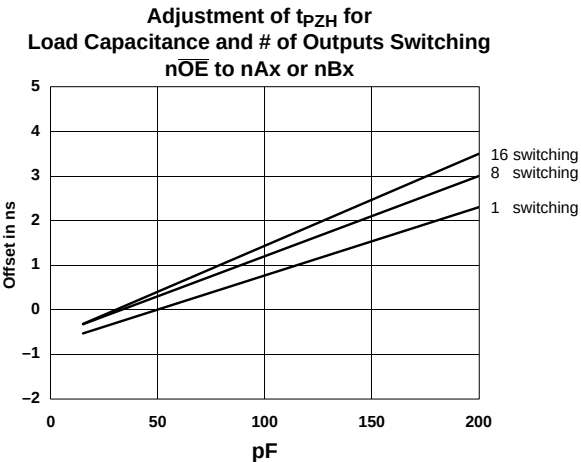
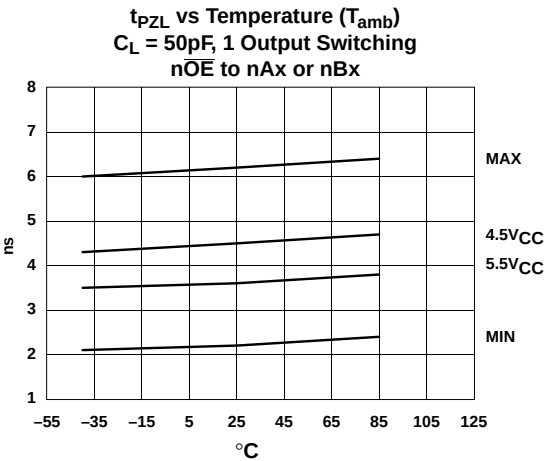
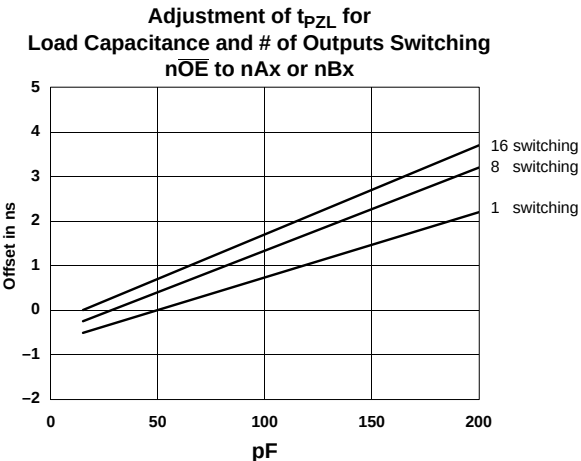
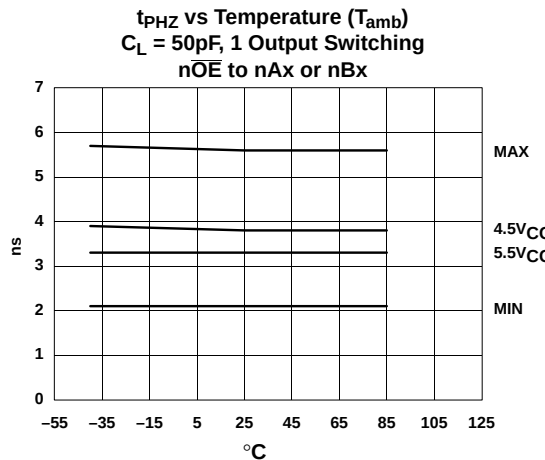
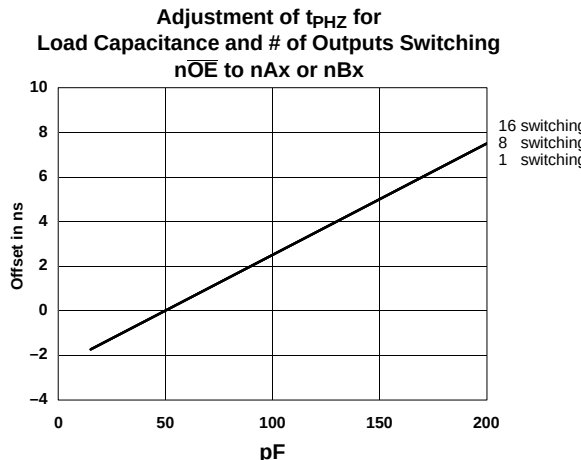
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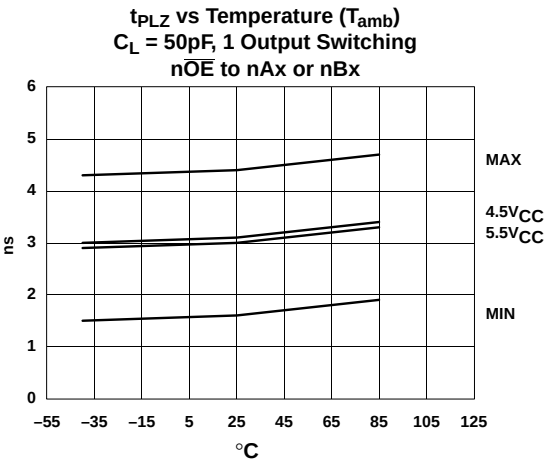
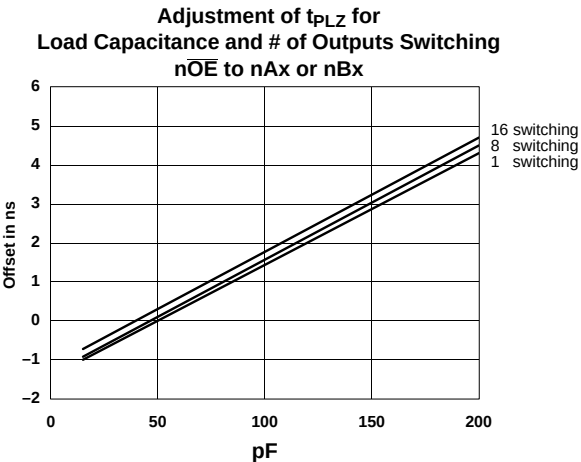
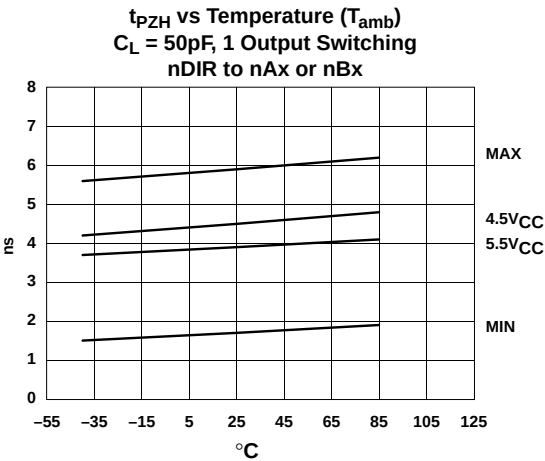
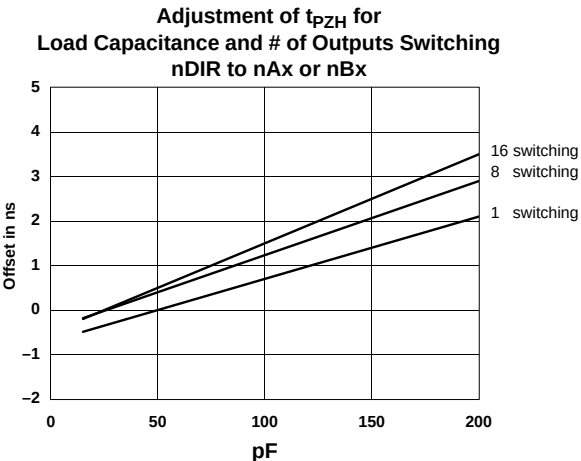
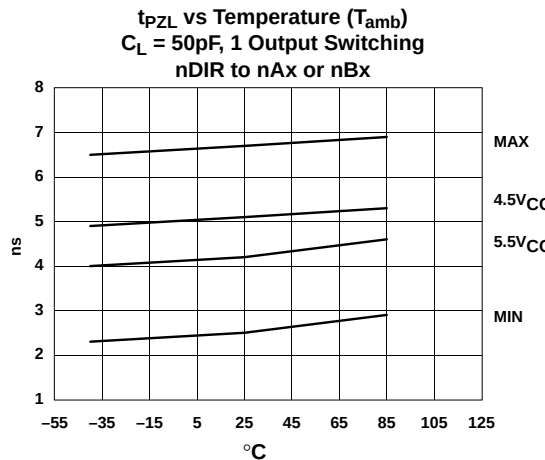
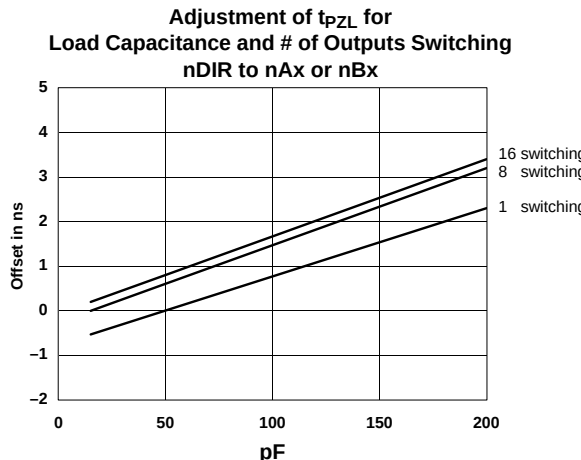
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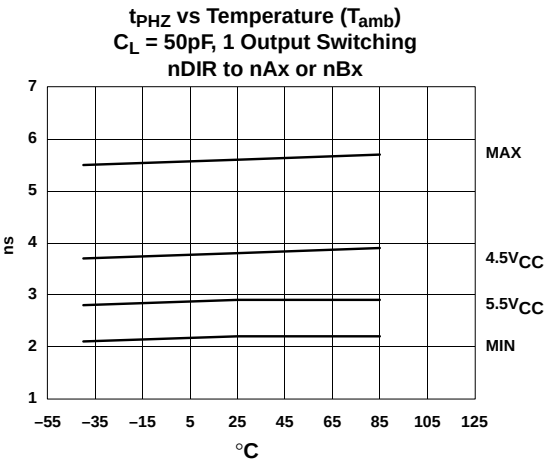
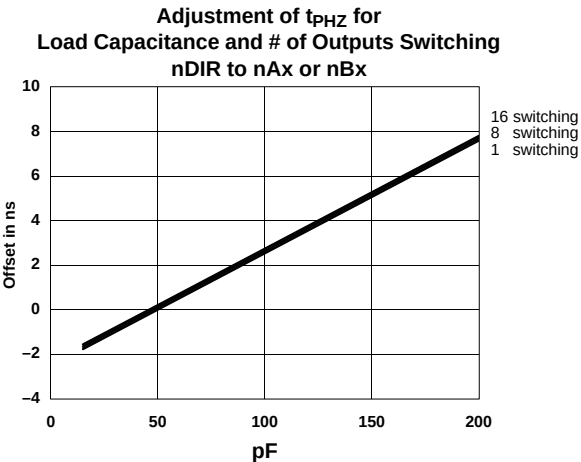
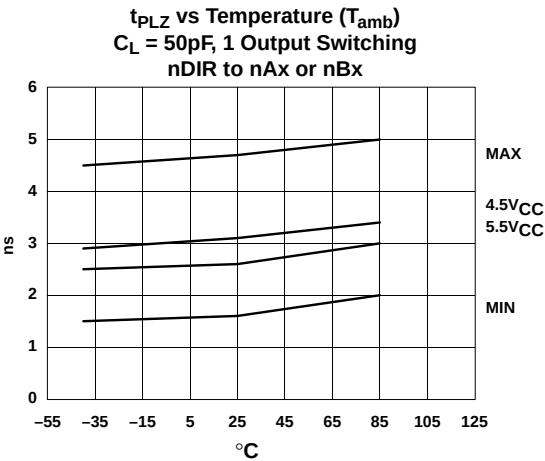
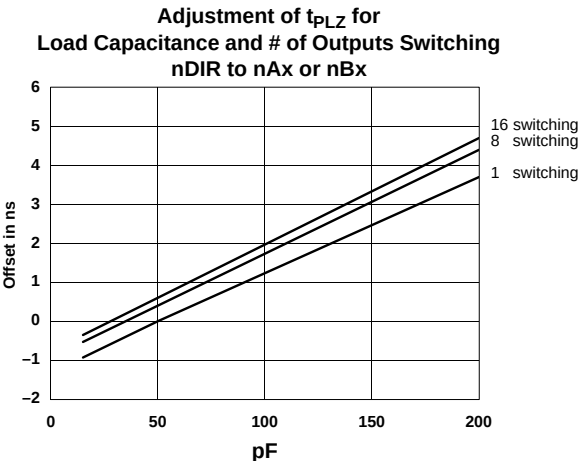
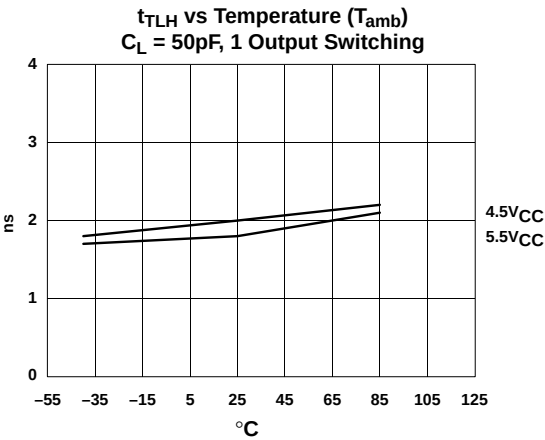
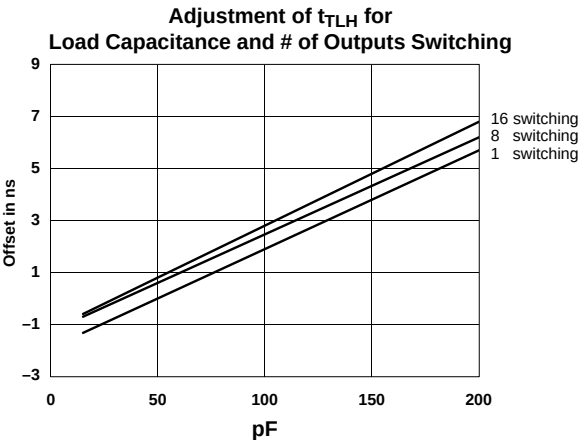
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