LAN8670/1/2

10BASE-T1S Ethernet PHY Transceiver Product Brief

Description

The LAN8670/1/2 is a high-performance 10BASE-T1S single-pair Ethernet PHY transceiver for 10 Mbit/s half-duplex networking over a single pair of conductors. Utilizing standard Ethernet technology in sensor/actuator networks reduces application costs by eliminating gateways necessary with legacy networking technologies. The ability to connect multiple PHYs onto a common mixing segment further saves implementation costs by reducing cabling and switch ports. The LAN8670/1/2 is designed for use in high-reliability cost sensitive industrial, backplane, and building automation sensor/actuator applications.

Highlights

- High-performance 10BASE-T1S Ethernet PHY
- Designed according to IEEE Std 802.3cg-2019™
  - 10 Mbit/s over single balanced pair
  - Half-duplex point-to-point link segments up to at least 15m
  - Half-duplex multidrop mixing segments up to at least 25m with up to at least 8 PHYs
- Media Independent Interface (MII) and Reduced Media Independent Interface (RMII)
  - 2.5 MHz MII clock mode
  - 50 MHz RMII clock mode
  - Serial Management Interface (SMI) for rapid register access
  - Comprehensive status interrupt support
- Carrier Sense Multiple Access / Collision Detection (CSMA/CD) media access control
- Physical Layer Collision Avoidance (PLCA)
  - Allows for high bandwidth utilization by avoiding collisions on the physical layer
  - Burst mode for transmission of multiple packets for high packet rate latency-sensitive applications
- Enhanced electromagnetic compatibility / electromagnetic interference (EMC/EMI) performance
  - Low RF emissions
  - Robust against injected currents and network cable shorts to ground or battery
  - Simple low cost analog front-end
- Single 3.3V supply with integrated 1.8V regulator
- Small footprint VQFN packaging with wettable flanks
  - LAN8670 32-pin (5 x 5 mm)
  - LAN8671 24-pin (4 x 4 mm)
  - LAN8672 36-pin (6 x 6 mm)
- -40°C to +125°C extended temperature range
- Microchip Functional Safety Ready

Target Applications

- Sensor/actuator networks operating at high bandwidth
- Microphone networks delivering audio streams for beamforming, hands-free microphones, etc.
- Backplane communication
- Industrial control cabinets and machine control
- Building automation

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1. Preface

1.1 Buffer Types

Table 1-1. LAN8670/1/2 Buffer Type Descriptions

Buffer	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-directional
ICLK	Oscillator input
OCLK	Crystal oscillator output
P	Power
PD	55 kΩ (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
PU	55 kΩ (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
VIS-VDDP	3.3V Schmitt-triggered input (VDDP power domain)
VO-VDDP	3.3V output (VDDP power domain)
VOH-VDDP	3.3V high-speed output (VDDP power domain)
VOD-VDDP	3.3V open-drain output (VDDP power domain)

Note: Digital signals are not 5V tolerant unless specified.

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2. Introduction

2.1 General Description

The Microchip LAN8670/1/2 is a compact, low power, and cost-effective single-port 10BASE-T1S Ethernet physical layer transceiver designed according to the IEEE Std 802.3cg-2019 specification. The device provides 10 Mbit/s half-duplex transmit and receive capability over single-balanced pair medium such as Unshielded Twisted Pair (UTP) cable. The LAN8670/1/2 is designed for use in applications requiring extended temperature range (-40°C to +125°C). The device is also compliant to industrial EMC and EMI requirements. The single power supply and simple analog front end simplifies its integration into small form factor applications.

The LAN8670/1/2 allows for the creation of both multidrop and point-to-point network topologies. Point-to-point link segments of up to at least 15m in length are supported. The multidrop mode supports up to at least 8 PHYs connected to a common mixing segment of up to at least 25m in length. The ability to connect multiple PHYs to a common mixing segment reduces weight and implementation costs by reducing cabling and switch ports.

The LAN8670/1/2 supports communication with an Ethernet MAC via standard MII/RMII interfaces. An integrated serial management interface (SMI) provides rapid register access and configuration at up to 4 MHz.

Access to the physical medium is managed by CSMA/CD and optionally supplemented by Physical Layer Collision Avoidance (PLCA).

The LAN8670/1/2 is designed to be used in functional safety related applications.

The Microchip LAN8670/1/2 family includes the following devices:

- LAN8670
- LAN8671
- LAN8672

Device specific features that do not pertain to the entire LAN8670/1/2 family are called out independently throughout this document. Table 2-1 below provides a summary of the feature differences between family members.

Table 2-1. LAN8670/1/2 Family Feature Matrix

Part Number	Package	MII Support	RMII Support	PLCA Support	-40^{O} to +125^{O}C
LAN8670	32-VQFN	X	X	X	X
LAN8671	24-VQFN		X	X	X
LAN8672	36-VQFN	X		X	X

A system-level block diagram and internal block diagram of the LAN8670/1/2 are shown in the following figures.

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Figure 2-1. LAN8670/1/2 System-Level Block Diagram

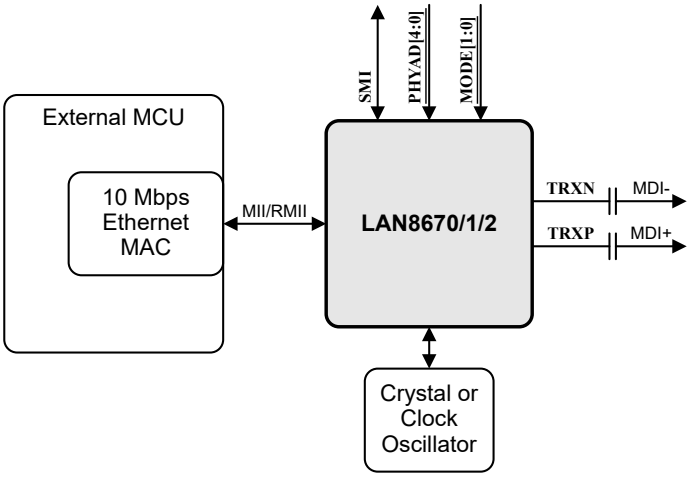
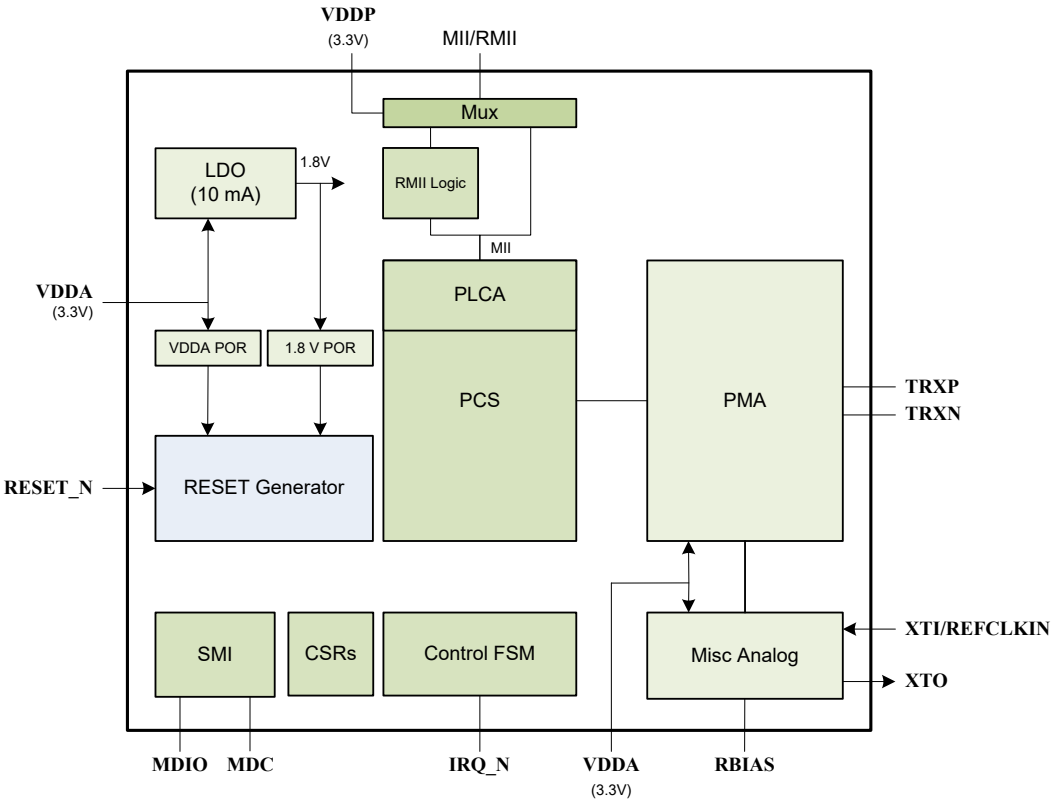


Figure 2-2. LAN8670/1/2 Internal Block Diagram



3. Pin Description and Configuration

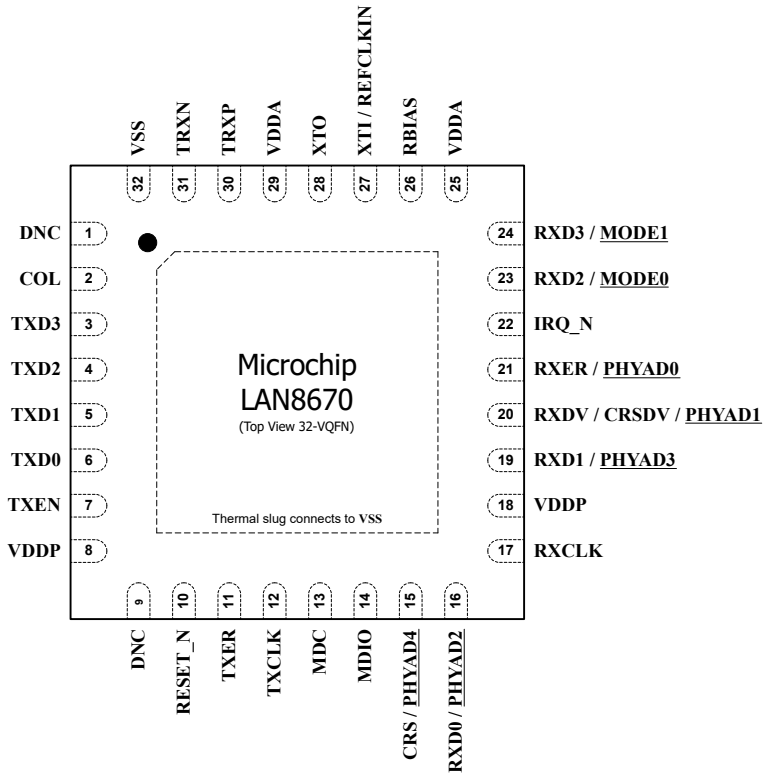
The pin assignments and descriptions for the LAN8670/1/2 are detailed in the following sections. Pin buffer type definitions are detailed in the Buffer Types section.

Related Links

1.1 Buffer Types

3.1 LAN8670 Pin Assignments

Figure 3-1. LAN8670 32-VQFN Pin Assignments



Note: Exposed pad (VSS) on bottom of package must be connected to ground.

Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor.

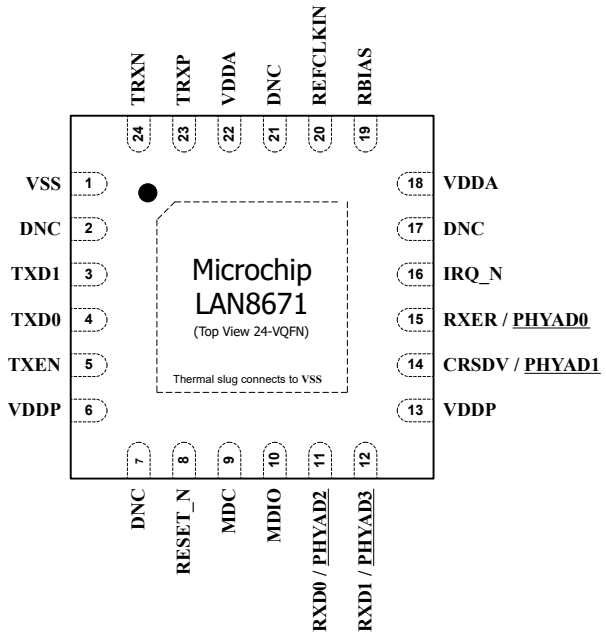
Table 3-1. LAN8670 32-VQFN Pin Assignments

Pin Num	Pin Name	Pin Num	Pin Name
1	DNC	17	RXCLK
2	COL	18	VDDP
3	TXD3	19	RXD1/PHYAD3
4	TXD2	20	RXDV/CRSDV/PHYAD1
5	TXD1	21	RXER/PHYAD0
6	TXD0	22	IRQ_N
7	TXEN	23	RXD2/MODE0
8	VDDP	24	RXD3/MODE1
9	DNC	25	VDDA
10	RESET_N	26	RBIAS
11	TXER	27	XTI/REFCLKIN
12	TXCLK	28	XTO
13	MDC	29	VDDA
14	MDIO	30	TRXP
15	CRS/PHYAD4	31	TRXN
16	RXD0/PHYAD2	32	VSS

Note: Exposed Pad (VSS) must be connected to ground.

3.2 LAN8671 Pin Assignments

Figure 3-2. LAN8671 24-VQFN Pin Assignments



Note: Exposed pad (VSS) on bottom of package must be connected to ground.

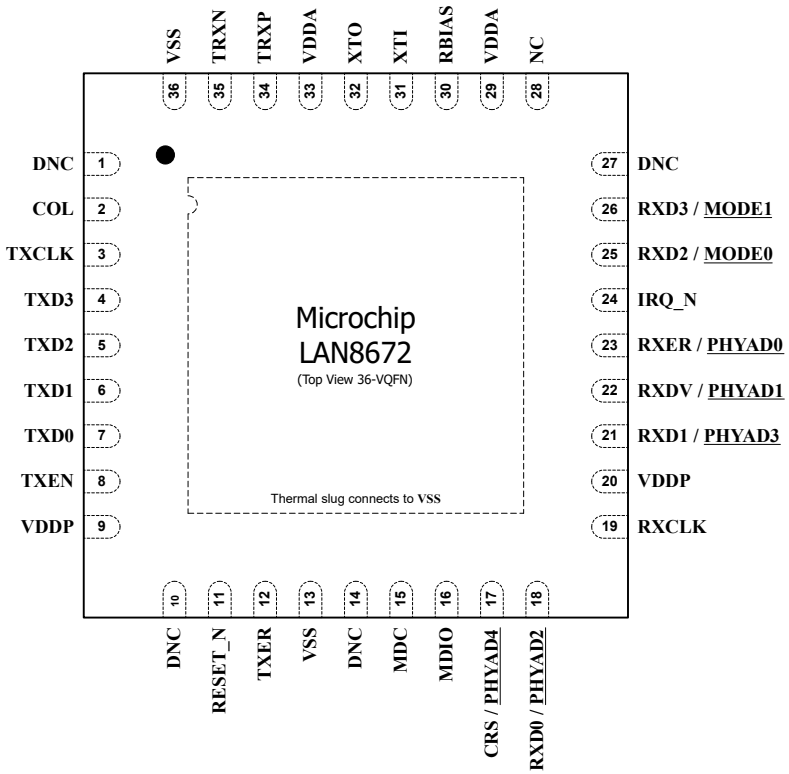
Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor.

Table 3-2. LAN8671 24-VQFN Pin Assignments

Pin Num	Pin Name	Pin Num	Pin Name
1	VSS	13	VDDP
2	DNC	14	CRSDV/PHYAD1
3	TXD1	15	RXER/PHYAD0
4	TXD0	16	IRQ_N
5	TXEN	17	DNC
6	VDDP	18	VDDA
7	DNC	19	RBIAS
8	RESET_N	20	REFCLKIN
9	MDC	21	DNC
10	MDIO	22	VDDA
11	RXD0/PHYAD2	23	TRXP
12	RXD1/PHYAD3	24	TRXN
Note: Exposed Pad (VSS) must be connected to ground.			

3.3 LAN8672 Pin Assignments

Figure 3-3. LAN8672 36-VQFN Pin Assignments



Note: Exposed pad (VSS) on bottom of package must be connected to ground.

Note: Configuration straps are identified by an underlined symbol name. Signals that function as configuration straps must be augmented with an external resistor.

Table 3-3. LAN8672 36-VQFN Pin Assignments

Pin Num	Pin Name	Pin Num	Pin Name
1	DNC	19	RXCLK
2	COL	20	VDDP
3	TXCLK	21	RXD1/PHYAD3
4	TXD3	22	RXDV/PHYAD1
5	TXD2	23	RXER/PHYAD0
6	TXD1	24	IRQ_N
7	TXD0	25	RXD2/MODE0
8	TXEN	26	RXD3/MODE1
9	VDDP	27	DNC
10	DNC	28	NC
11	RESET_N	29	VDDA
12	TXER	30	RBIAS
13	VSS	31	XTI
14	DNC	32	XTO
15	MDC	33	VDDA
16	MDIO	34	TRXP
17	CRS/PHYAD4	35	TRXN
18	RXD0/PHYAD2	36	VSS

Note: Exposed Pad (VSS) must be connected to ground.

3.4 Pin Descriptions

This section contains descriptions of the various LAN8670/1/2 pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, RESET_N indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Pin buffer type definitions are detailed in the Buffer Types section.

Table 3-4. MII/RMII Signals

Name	Symbol	Buffer Type	Description
Transmit Data 0	TXD0	VIS-VDDP	Transmit data bus bit 0 (all modes)
Transmit Data 1	TXD1	VIS-VDDP	Transmit data bus bit 1 (all modes)
Transmit Data 2 (MII Mode)	TXD2	VIS-VDDP	Transmit data bus bit 2 (MII mode) In RMII mode, this signal is not used and is internally pulled-down to VSS.
Transmit Data 3 (MII Mode)	TXD3	VIS-VDDP	Transmit data bus bit 3 (MII mode) In RMII mode, this signal is not used and is internally pulled-down to VSS.
Transmit Error (MII Mode)	TXER	VIS-VDDP	This signal is asserted to indicate that an error was detected somewhere in the packet presently being transferred to the transceiver. This pin is unused in RMII mode and should be connected to VSS.
Transmit Enable	TXEN	VIS-VDDP	Indicates that valid transmission data is present on TXD[3:0]. In RMII mode, only TXD[1:0] provide valid data. **Note:** A pull-down resistor is recommended to prevent incidental transmission if the MAC does not actively pull-down or drive this pin low at all times during its reset and initialization.
Transmit Clock (MII Mode)	TXCLK	VO-VDDP	2.5 MHz clock used to latch data from the MAC into the transceiver. In RMII mode, this pin is unused and is driven low. It should be left unconnected.
Receive Data 0	RXD0	VOH-VDDP	Receive data bus bit 0 (all modes)
Receive Data 1	RXD1	VOH-VDDP	Receive data bus bit 1 (all modes)
Receive Data 2 (MII Mode)	RXD2	VO-VDDP	Receive data bus bit 2 (MII mode) In RMII mode, this pin is unused and is driven low.
Receive Data 3 (MII Mode)	RXD3	VO-VDDP	Receive data bus bit 3 (MII mode) In RMII mode, this pin is unused and is driven low.
Receive Error	RXER	VOH-VDDP	This signal is asserted to indicate that an error was detected somewhere in the packet presently being transferred from the transceiver. This signal is optional in RMII mode.

.....continued

Name	Symbol	Buffer Type	Description
Receive Data Valid (MII Mode)	RXDV	VOH-VDDP	Indicates that recovered and decoded data is available on the RXD[3:0] pins. This signal is not used in RMII mode.
Receive Clock (MII Mode)	RXCLK	VO-VDDP	In MII mode, this pin is the 2.5 MHz receive clock output. In RMII mode, this pin is unused and is driven low. It should be left unconnected.
Carrier Sense / Receive Data Valid (RMII Mode)	CRSDV	VOH-VDDP	This signal is asserted to indicate the receive medium is non-idle in RMII mode. This signal is not used in MII mode.
Collision Detect (MII Mode)	COL	VO-VDDP	Collision Detect. In RMII mode, this pin is unused and is driven low.
Carrier Sense (MII Mode)	CRS	VO-VDDP	Carrier Sense. In RMII mode, this pin is unused and is driven low.

Table 3-5. Ethernet Transceiver Pins

Name	Symbol	Buffer Type	Description
Ethernet TX/RX Positive Terminal	TRXP	AIO	Positive terminal for transmit/receive signal.
Ethernet TX/RX Negative Terminal	TRXN	AIO	Negative terminal for transmit/receive signal.

Table 3-6. Serial Management Interface (SMI) Pins

Name	Symbol	Buffer Type	Description
SMI Data Input/Output	MDIO	VIS-VDDP / VO-VDDP	Serial Management Interface data input/output.
SMI Clock	MDC	VIS-VDDP	Serial Management Interface clock.

Table 3-7. Miscellaneous Pins

Name	Symbol	Buffer Type	Description
External 25 MHz Crystal Input	XTI	ICLK	External 25 MHz crystal input.
External Clock Input	REFCLKIN	ICLK	Single-ended clock oscillator input. A frequency of 25 MHz shall be used in all modes except RMII, which requires 50 MHz. **Note:** When using a single-ended clock oscillator, XTO must be left unconnected with <10 pF stray capacitance.
External 25 MHz Crystal Output	XTO	OCLK	External 25 MHz crystal output. **Note:** When using a single-ended clock oscillator on XTI/REFCLKIN, this pin must be left unconnected with <10 pF stray capacitance.
Interrupt	IRQ_N	VOD-VDDP	Device interrupt. Active low and open drain. **Note:** When used, this pin requires a 10 kΩ (typical) pull-up to VDDP. **Note:** This pin is to be unconnected when unused.
System Reset	RESET_N	VIS-VDDP	System reset. This pin is active low. If unused, this pin must be pulled-up to VDDP.

.....continued

Name	Symbol	Buffer Type	Description
Bias Resistor	RBIAS	AIO	External bias resistor connection pin. This pin requires connection of a 12.4 kΩ resistor to ground. **Note:** The resistor must be within ± 1% tolerance across the entire expected operating temperature range.
Do Not Connect	DNC	-	Pin is internally connected. The pin must be left floating externally.
No Connect	NC	-	Pin is not connected internally. The pin should be left floating externally.

Table 3-8. Configuration Straps

Name	Symbol	Buffer Type	Description
Operating Mode Configuration Straps 1-0	MODE[1:0]	VIS-VDDP	These configuration straps are used to select the device's default mode of operation. See Section 3.5, Configuration Straps for additional information.
PHY Address Configuration Straps 4-0	PHYAD[4:0]	VIS-VDDP	These configuration straps are used to select the device's default PHY SMI address. See Section 3.5, Configuration Straps for additional information.

Table 3-9. Power Pins

Name	Symbol	Buffer Type	Description
+3.3V Switched I/O Power Supply Input	VDDP	P	+3.3V switched I/O power supply input.
+3.3V Switched Analog Power Supply Input	VDDA	P	+3.3V switched analog power supply input.
Ground	VSS	P	Common ground. This exposed pad must be connected to the ground plane with a via array.

3.5 Configuration Straps

Configuration straps allow various features of the device to be automatically configured to user defined values. Configuration straps are identified by an underlined symbol name in the pin assignment lists and are latched on Power-On Reset (POR) and pin reset (RESET_N). Configuration straps do not have internal resistors to prevent the signal from floating when unconnected.

Important: External pull-up or pull-down resistors must be sized appropriately (10 kΩ, typical) to ensure that the configuration straps reach the required voltage level prior to latching at reset.

3.5.1 Device Mode (MODE[1:0])

The MODE[1:0] configuration straps control various device modes. When the RESET_N pin is negated, the associated register bit values are loaded according to the MODE[1:0] configuration straps and the device is configured. When a soft reset occurs via the Soft Reset bit of the Basic Control Register, the configuration of the device is controlled by the register bit values and the MODE[1:0] configuration straps have no affect.

The device's mode may be configured using the hardware configuration straps as summarized in Table 3-10 below.

Note: As the LAN8672 only supports operation in MII mode, the MODE[1:0] configuration straps must be set to 01b.

Table 3-10. MODE[1:0] Configuration Straps

MODE[1:0]	Definition
00b	Reserved
01b	PHY is placed in MII mode with 25 MHz crystal
10b	PHY is placed in RMII mode with 50 MHz REFCLKIN
11b	Reserved

3.5.2 PHY Address (PHYAD[4:0])

The PHYAD[4:0] configuration straps are driven high or low to give each PHY a unique SMI address. This address is latched into an internal register at the end of a hardware reset. In a multi-transceiver application (such as a switch), the controller is able to manage each transceiver via the unique address. Each transceiver checks each management data frame for a matching address in the relevant bits. When a match is recognized, the transceiver responds to that particular frame.

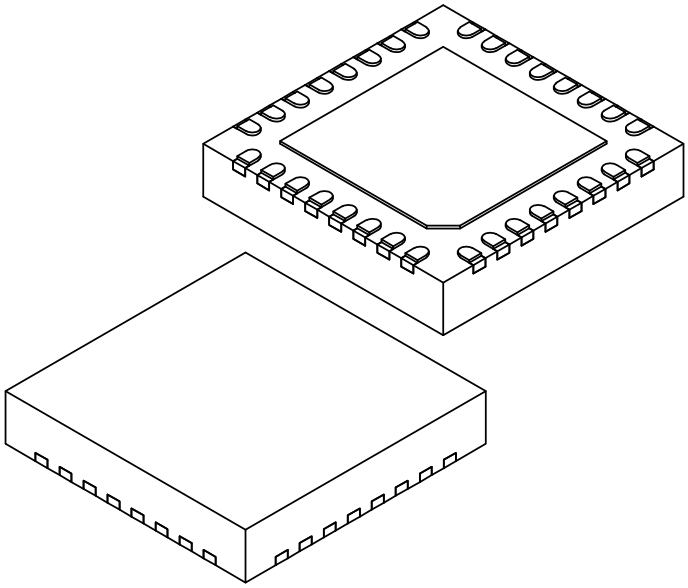
The LAN8670/2 SMI address must be configured using the PHYAD[4:0] hardware configuration straps to any value between 0x00 and 0x1F. The LAN8671 SMI address must be configured using the PHYAD[3:0] hardware configuration straps to any value between 0x00 and 0x0F.

4. Packaging Information

4.1 32-VQFN (LAN8670 Only)

32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN] With 3.4 mm Exposed Pad and Stepped Wettable Flanks

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.30	3.40	3.50
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.30	3.40	3.50
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-
Exposed Pad Corner Chamfer	CH		0.35 REF	
Step Height	A4	0.10	-	0.19
Step Length	D3	0.035	0.060	0.085

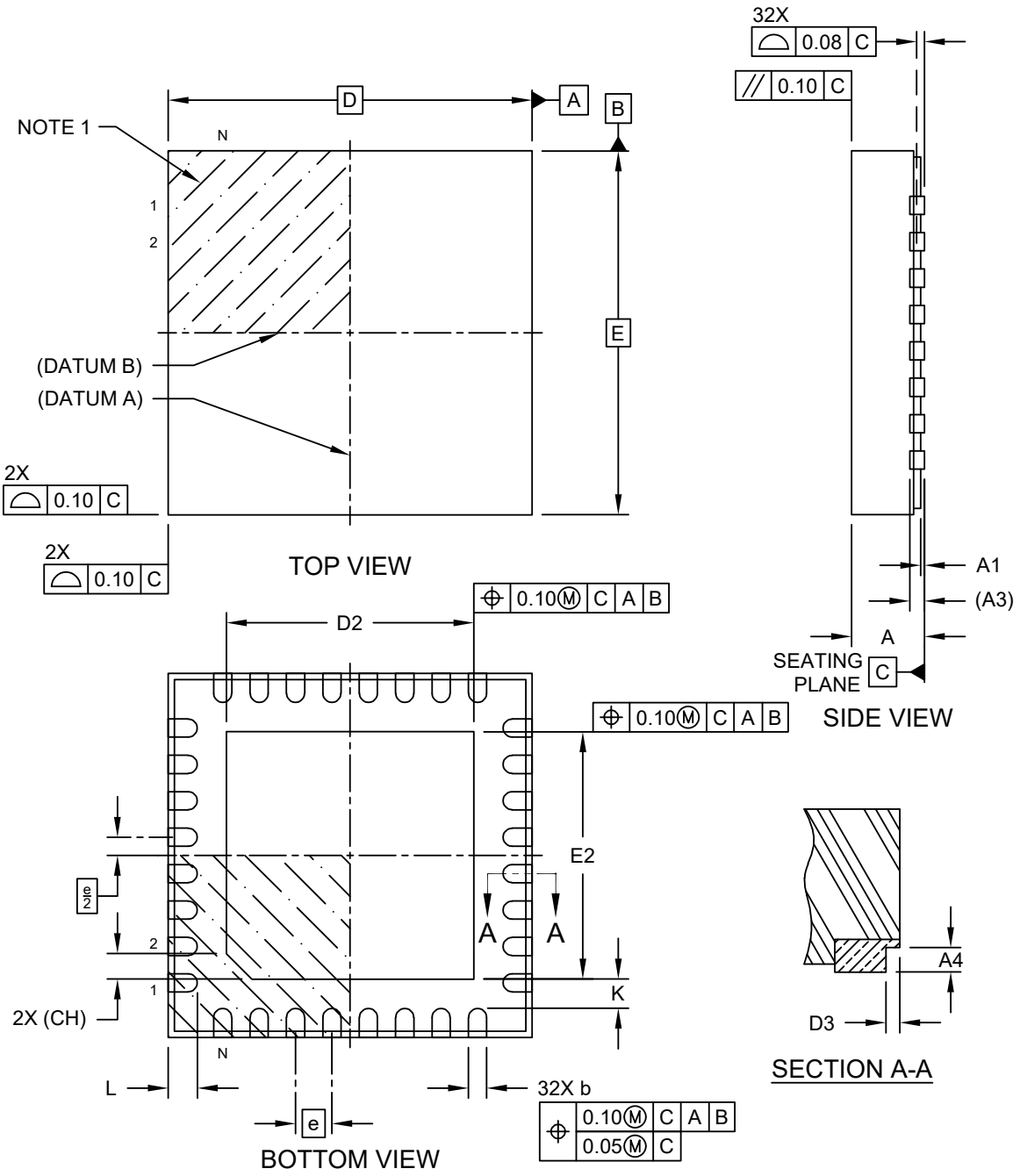
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-500 Rev B Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN] With 3.4 mm Exposed Pad and Stepped Wettable Flanks

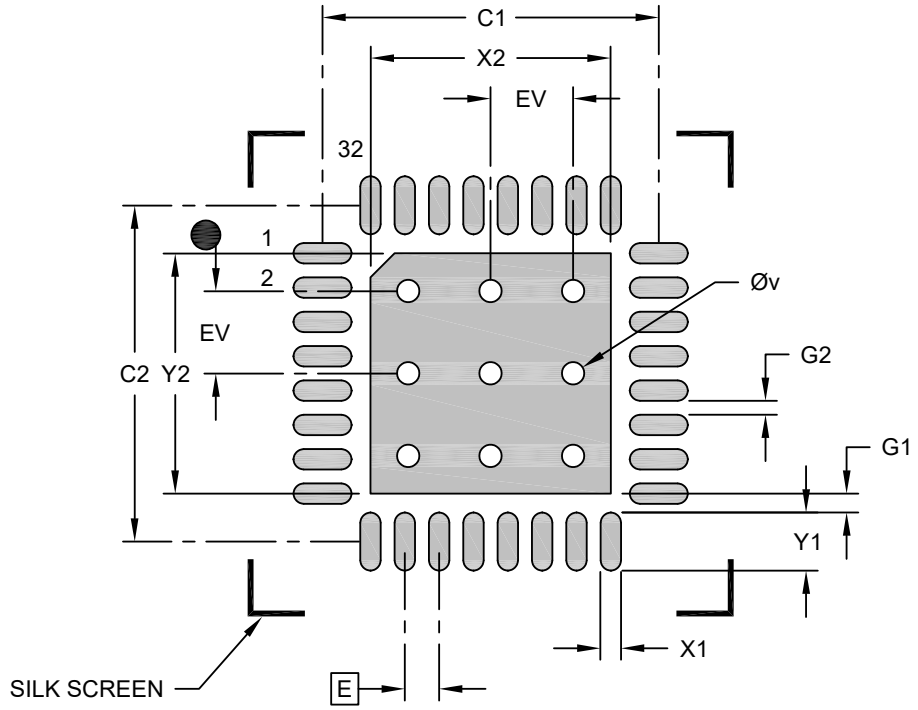
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN] With 3.4 mm Exposed Pad and Stepped Wettable Flanks

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.50
Center Pad Length	Y2			3.50
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (32)	X1			0.30
Contact Pad Length (32)	Y1			0.85
Contact Pad to Center Pad (32)	G1	0.20		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

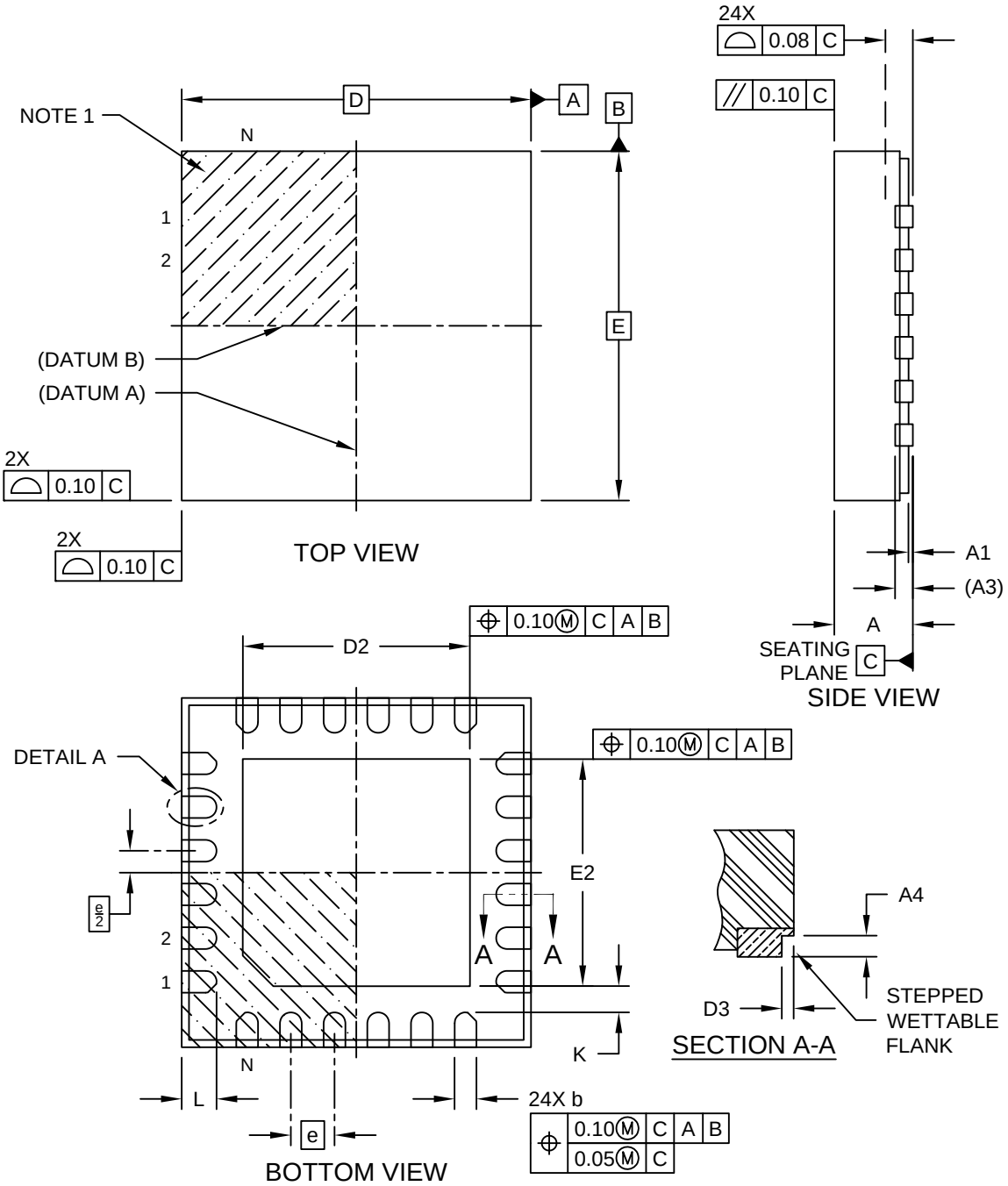
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2500 Rev B

4.2 24-VQFN (LAN8671 Only)

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

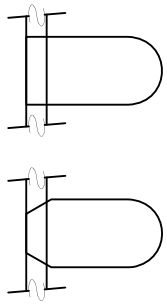
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



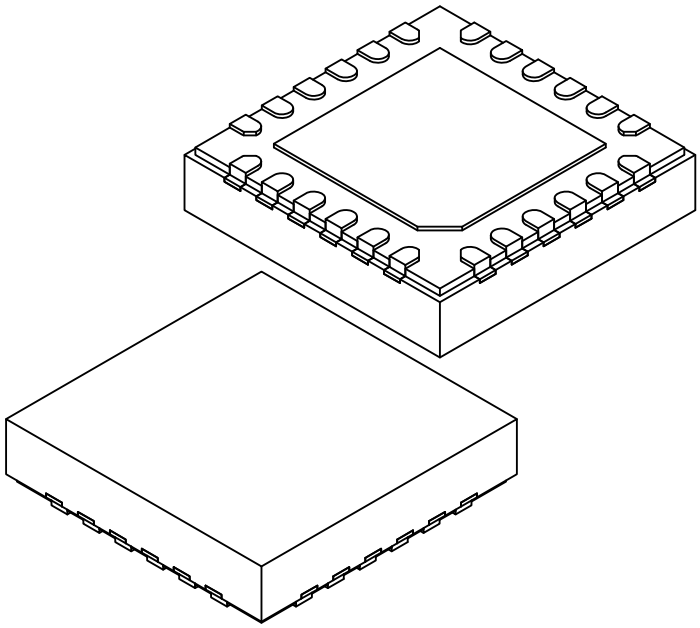
Microchip Technology Drawing C04-21483 Rev A Sheet 1 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		24	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.60	2.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Length	D3	-	-	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

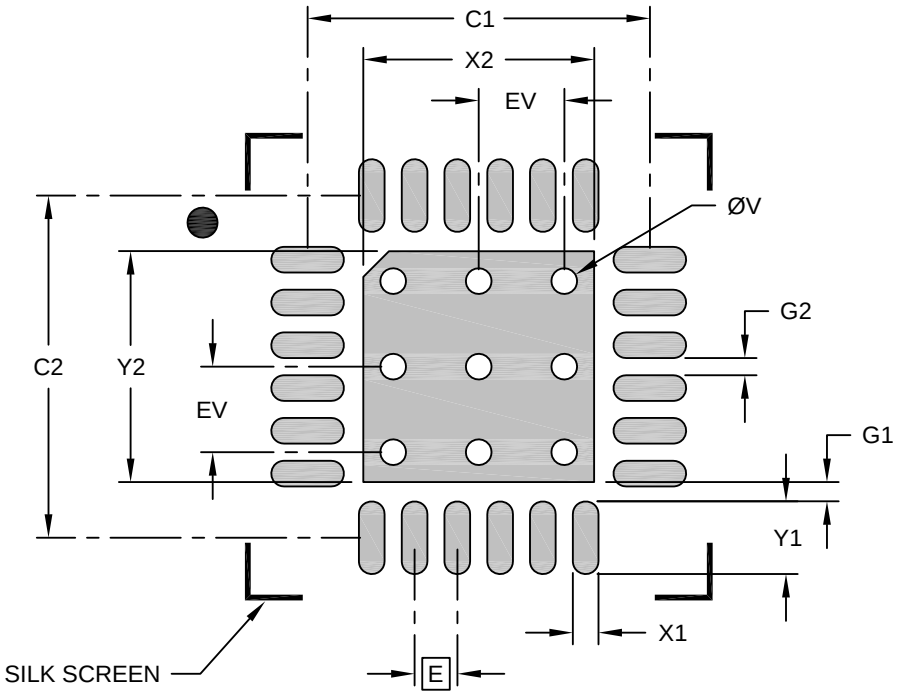
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21483 Rev A Sheet 2 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.70
Optional Center Pad Length	Y2			2.70
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X24)	X1			0.30
Contact Pad Length (X24)	Y1			0.85
Contact Pad to Center Pad (X24)	G1	0.23		
Contact Pad to Contact Pad (20)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

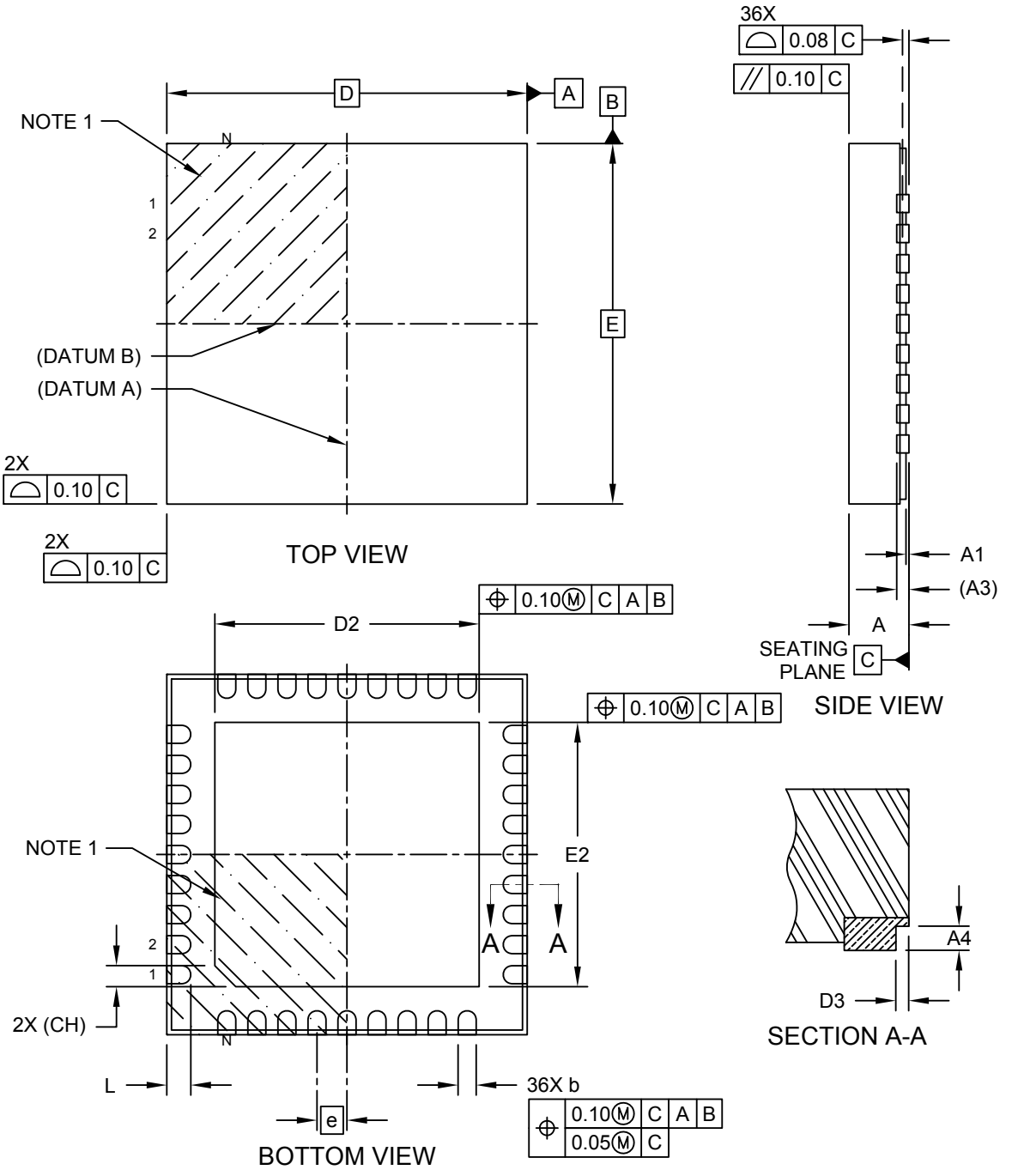
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23483 Rev A Sheet 1 of 2

4.3 36-VQFN (LAN8672 Only)

36-Lead Very Thin Plastic Quad Flat, No Lead Package (LNX) - 6x6x1.0 mm Body [VQFN] With 4.4 mm Exposed Pad and Stepped Wettable Flanks

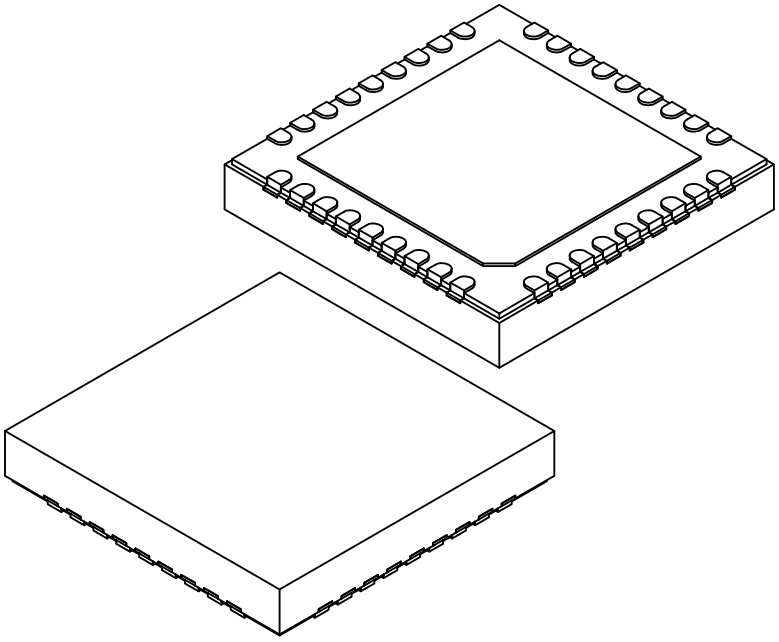
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-501 Rev B Sheet 1 of 2

36-Lead Very Thin Plastic Quad Flat, No Lead Package (LNX) - 6x6x1.0 mm Body [VQFN] With 4.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.30	4.40	4.50
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.30	4.40	4.50
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-
Exposed Pad Corner Chamfer	CH		0.35 REF	
Step Height	A4	0.10	-	0.19
Step Length	D3	0.035	0.060	0.085

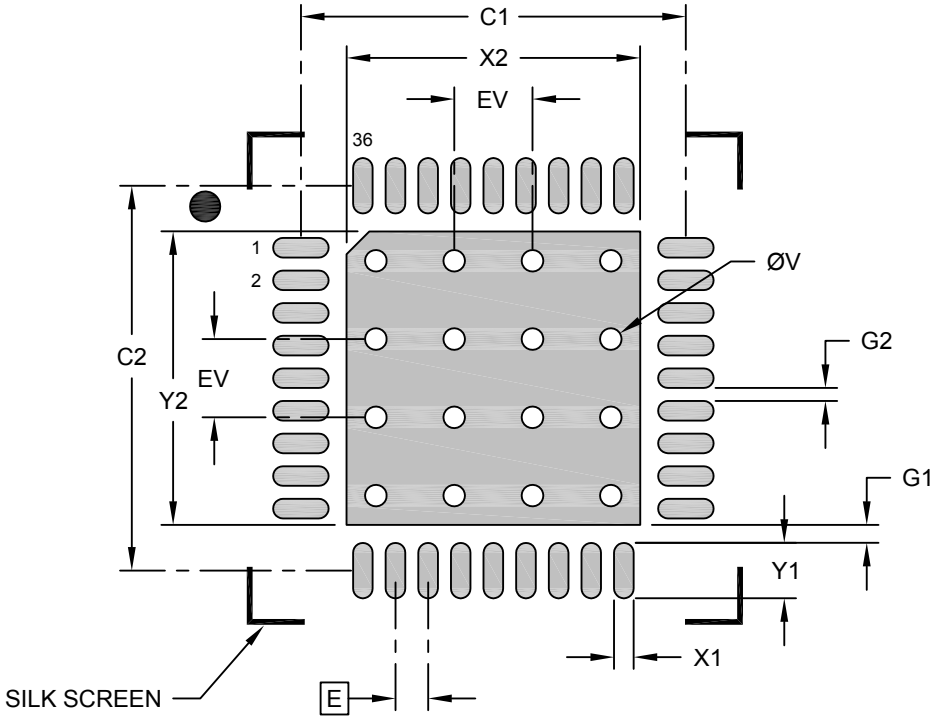
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-501 Rev B Sheet 2 of 2

36-Lead Very Thin Plastic Quad Flat, No Lead Package (LNX) - 6x6x1.0 mm Body [VQFN] With 4.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			4.50
Center Pad Length	Y2			4.50
Contact Pad Spacing	C1		5.90	
Contact Pad Spacing	C2		5.90	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.20		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2501 Rev B

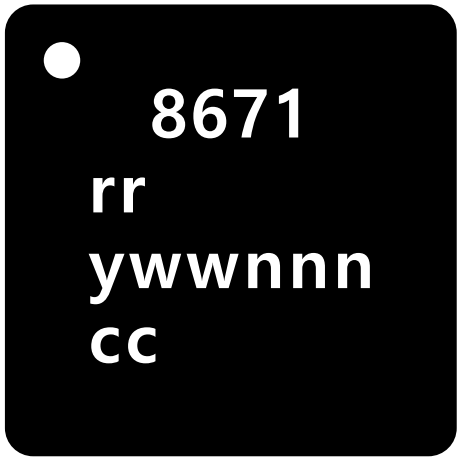
5. Package Marking Information

Figure 5-1. LAN8670 Top Mark



Legend:		
	LAN8670	Device Identifier
	rr	Product Revision Code
	yy	last two digits of Assembly Year
	ww	Assembly Work Week
	nnn	Tracking Number
	cc	Country of Origin Abbreviation (optional)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Figure 5-2. LAN8671 Top Mark



Legend:		
	8671	Device Identifier (LAN8671)
	rr	Product Revision Code
	y	last digit of Assembly Year
	ww	Assembly Work Week
	nnn	Tracking Number
	cc	Country of Origin Abbreviation (optional)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Figure 5-3. LAN8672 Top Mark



Legend:		
	LAN8672	Device Identifier
	rr	Product Revision Code
	yy	last two digits of Assembly Year
	ww	Assembly Work Week
	nnn	Tracking Number
	cc	Country of Origin Abbreviation (optional)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

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ISBN: 978-1-5224-8406-6

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