TENTATIVE TOSHIBA HYBRID DIGITAL INTEGRATED CIRCUIT

8,388,608-WORD BY 64-BIT SYNCHRONOUS DRAM MODULE

DESCRIPTION

The THMY648071BEG is a 8,388,608-word by 64-bit synchronous dynamic RAM module consisting of eight TC59S6408BFT DRAMs and an unbuffer on a printed circuit board.

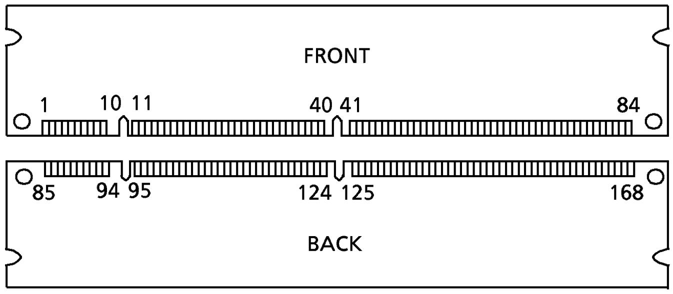
FEATURES

- 8,388,608-word by 64-bit (single-bank) organization

		-80	-10
t_{CK}	Clock Cycle Time (CL = 2)	10 ns	12 ns
t_{RAS}	Active-to-Precharge Command Period (min)	48 ns	60 ns
t_{AC}	Access Time from CLK (CL = 2)	6 ns	8 ns
t_{RC}	Ref/Active-to-Ref/Active Command Period (min)	68 ns	84 ns

- Single power supply of 3.3 V ± 0.3 V
- Pipeline architecture
- Auto-Refresh and Self-Refresh capability
- All inputs and outputs LVTTL-compatible
- 4096 Refresh cycles per 64 ms
- Package: 168-pin DIMM (gold contacts)
- Based on Intel Rev. 1.0 (4-clock)

PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

A0 ~ A11	Address Inputs
BA0, BA1	Bank Select
DQ0 ~ DQ63	Data Inputs / Outputs
/CS0, /CS2	Chip Select
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
DQMB0 ~ DQMB7	Output Disable / Write Mask
CLK0, CLK1	Clock Inputs
CKE	Clock Enable
SDA	Serial Data / Address for PD
SCL	Clock for PD
SA0 ~ SA2	Address for PD
VDD	Power (+3.3 V)
VSS	Ground
NC	No Connection

1	VSS	85	VSS	29	DQMB1	113	DQMB5	57	DQ18	141	DQ50
2	DQ0	86	DQ32	30	/CS0	114	NC	58	DQ19	142	DQ51
3	DQ1	87	DQ33	31	NC	115	/RAS	59	VDD	143	VDD
4	DQ2	88	DQ34	32	VSS	116	VSS	60	DQ20	144	DQ52
5	DQ3	89	DQ35	33	A0	117	A1	61	NC	145	NC
6	VDD	90	VDD	34	A2	118	A3	62	NC	146	NC
7	DQ4	91	DQ36	35	A4	119	A5	63	NC	147	NC
8	DQ5	92	DQ37	36	A6	120	A7	64	VSS	148	VSS
9	DQ6	93	DQ38	37	A8	121	A9	65	DQ21	149	DQ53
10	DQ7	94	DQ39	38	A10	122	BA0	66	DQ22	150	DQ54
11	DQ8	95	DQ40	39	BA1	123	A11	67	DQ23	151	DQ55
12	VSS	96	VSS	40	VDD	124	VDD	68	VSS	152	VSS
13	DQ9	97	DQ41	41	VDD	125	CLK1	69	DQ24	153	DQ56
14	DQ10	98	DQ42	42	CLK0	126	NC	70	DQ25	154	DQ57
15	DQ11	99	DQ43	43	VSS	127	VSS	71	DQ26	155	DQ58
16	DQ12	100	DQ44	44	NC	128	CKE	72	DQ27	156	DQ59
17	DQ13	101	DQ45	45	/CS2	129	NC	73	VDD	157	VDD
18	VDD	102	VDD	46	DQMB2	130	DQMB6	74	DQ28	158	DQ60
19	DQ14	103	DQ46	47	DQMB3	131	DQMB7	75	DQ29	159	DQ61
20	DQ15	104	DQ47	48	NC	132	NC	76	DQ30	160	DQ62
21	NC	105	NC	49	VDD	133	VDD	77	DQ31	161	DQ63
22	NC	106	NC	50	NC	134	NC	78	VSS	162	VSS
23	VSS	107	VSS	51	NC	135	NC	79	CLK2	163	CLK3
24	NC	108	NC	52	NC	136	NC	80	NC	164	NC
25	NC	109	NC	53	NC	137	NC	81	NC	165	SA0
26	VDD	110	VDD	54	VSS	138	VSS	82	SDA	166	SA1
27	/WE	111	/CAS	55	DQ16	139	DQ48	83	SCL	167	SA2
28	DQMB0	112	DQMB4	56	DQ17	140	DQ49	84	VDD	168	VDD

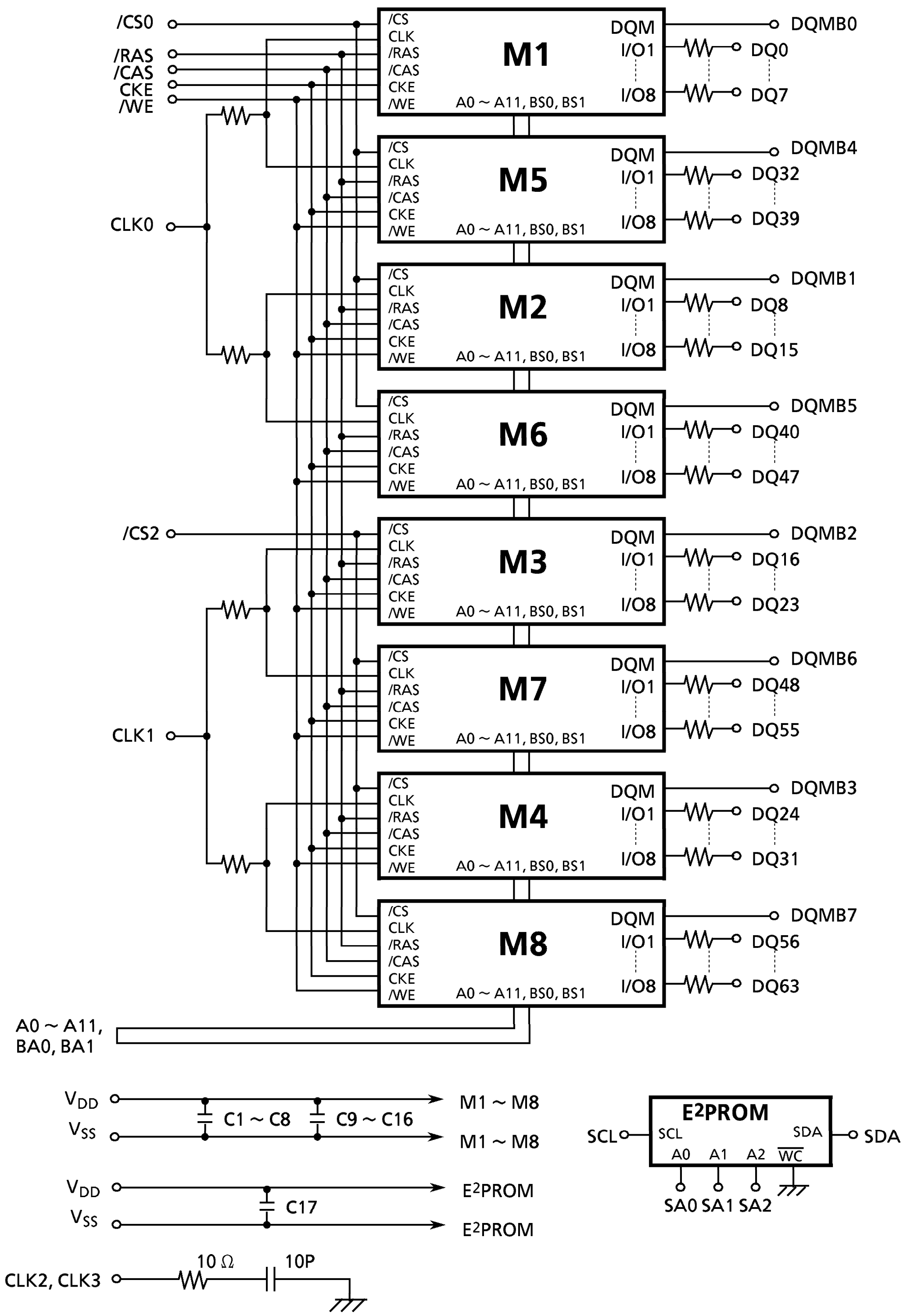
SERIAL PRESENCE DETECT (REV. 1.2A)

Byte Number	Function	-80		-10	
		Entry Value	Entry	Entry Value	Entry
0	Defines # of Bytes of information Written into Serial Memory by Module Manufacturer Group	128 Bytes	80h	128 Bytes	80h
1	Total # of Bytes in SPD Memory Device	256 Bytes	08h	256 Bytes	08h
2	Fundamental Memory Type (FPM, EDO, SDRAM...) from Appendix A	SDRAM	04h	SDRAM	04h
3	# of Row Addresses on this Assembly	RA0 ~ RA11	0Ch	RA0 ~ RA11	0Ch
4	# of Column Addresses on this Assembly	CA0 ~ CA8	09h	CA0 ~ CA8	09h
5	# of Module Banks on this Assembly	1 Bank	01h	1 Bank	01h
6	Data Width of this Assembly...	x64	40h	x64	40h
7	...Data Width Continuation	x64	00h	x64	00h
8	Voltage Interface Standard for this Assembly	LVTTL	01h	LVTTL	01h
9	SDRAM Cycle Time at Max. Supported CAS Latency (CL) @ CL = X	CL = 3, 8.0 ns	80h	CL = 3, 1.0 ns	A0h
10	SDRAM Access from Clock @ CL = X	CL = 3, 6.0 ns	60h	CL = 3, 7.0 ns	70h
11	DIMM Configuration Type (Non-parity, Parity, ECC)	Non-Parity	00h	Non-Parity	00h
12	Refresh Rate/Type	15.625 μs/Self-Refresh	80h	15.625 μs/Self-Refresh	80h
13	SDRAM Width, Primary DRAM	x8	08h	x8	08h
14	Error Checking SDRAM Data Width	NA	00h	NA	00h
15	Minimum Clock Delay, Back-to-Back Random Column Addresses	1 CLK	01h	1 CLK	01h
16	Burst Lengths Supported	1, 2, 4, 8, Full page	8Fh	1, 2, 4, 8, Full page	8Fh
17	# of Banks on Each SDRAM Device	4 Banks	04h	4 Banks	04h
18	CAS # Latencies Supported	2, 3	06h	2, 3	06h
19	CS # Latency		01h		01h
20	WE # Latency		01h		01h
21	SDRAM Module Attributes		00h		00h
22	SDRAM Device Attributes: General		0Eh		0Eh
23	Minimum Clock Cycle Time @ CL- X-1	CL = 2, 10 ns	A0h	CL = 2, 12 ns	C0h
24	Maximum Data Access Time from Clock @ CL X-1	CL = 2, 6.0 ns	60h	CL = 2, 8.0 ns	80h
25	Minimum Clock Cycle Time @ CL X-2		00h		00h
26	Maximum Data Access Time from Clock @ CL X-2		00h		00h
27	Minimum Row Precharge Time	20 ns	14h	24 ns	18h
28	Minimum Row-Active-to-Row-Active Delay	20 ns	14h	20 ns	14h
29	Minimum RAS-to-CAS Delay	20 ns	14h	24 ns	18h
30	Minimum RAS Pulse Width	48 ns	30h	60 ns	3Ch
31	Module/Bank Density	64 MB	10h	64 MB	10h
32	Command & addless signal input Set-up Time	2 ns	20 h	2.5 ns	25 h
33	Command & address signal input Hold Time	1 ns	10 h	1 ns	10 h
34	Data Signal input Set-up Time	2 ns	20 h	2.5 ns	25 h
35	Data Signal input Hold Time	1 ns	10 h	1 ns	10 h
36-61	Superset Information (may be used in future)		FFh		FFh
62	SPD Revision	Rev. 1.2A	12h	Rev. 1.2A	12h
63	Check sum for Bytes 0 ~ 62	1EC9h	C9h	1F57h	57h

OPTIONAL

64	Manufacturers JEDEC ID Code (JEP-106E)				
65-71					
72	Place of Manufacture				
73-90	Manufacturer's Part Number				
91-92	Revision Code				
93-94	Date of Manufacture				
95-98	Assembly Serial Number				
99-125	Manufacturer-Specific Data				
126	Reserved	Intel Specification	66h	Intel Specification	66h
127	Reserved	Intel Specification	C7h	Intel Specification	C7h
128-255					

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	$-0.5 \sim V_{DD} + 0.3$	V	1
V_{OUT}	Output Voltage	$-0.5 \sim V_{DD} + 0.3$	V	1
V_{DD}	Power Supply Voltage	$-0.3 \sim 4.6$	V	1
T_{OPR}	Operating Temperature	$0 \sim 70$	°C	1
T_{STG}	Storage Temperature	$-55 \sim 125$	°C	1
P_D	Power Dissipation	2.8	W	1
I_{OUT}	Short-Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0° ~ 70°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	LVTTL Input High Voltage	2.0	–	$V_{DD} + 0.3$	V	2
V_{IL}	LVTTL Input Low Voltage	–0.5	–	0.8	V	2

CAPACITANCE (V_{CC} = 3.3 V, f = 1 MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN	MAX	UNIT
C_I	Input Capacitance (A0 ~ A11)	–	TBD	pF
C_2	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1)	–	TBD	pF
C_3	Input Capacitance (CLK0, CLK1)	–	TBD	pF
C_4	Input Capacitance ($\overline{CS0}$, $\overline{CS2}$)	–	TBD	pF
C_5	Input Capacitance (DQMB0 ~ DQMB7)	–	TBD	pF
C_{DQ}	I/O Capacitance (DQ0 ~ DQ63)	–	TBD	pF

DC CHARACTERISTICS (V_{CC} = 3.3 V ± 0.3 V, Ta = 0° ~ 70°C)

SYMBOL	ITEM		-80 MIN	-80 MAX	-10 MIN	-10 MAX	UNIT	NOTES
I_{CC1} I_{CC1B}	OPERATING CURRENT Active-Precharge Command Cycling without Burst Operation (t_{CK} = min, t_{RC} = min)	1-Bank Operation	–	720	–	560	mA	3
I_{CC2}	STANDBY CURRENT (t_{CK} = min, $\overline{CS}$ = V_{IH}, $V_{IH/L}$ = V_{IH}(min) / V_{IL}(max) Bank: Inactive State)	CKE = V_{IH}	–	320	–	240	mA	3
I_{CC2P}		CKE = V_{IL} (Power-Down Mode)	–	8	–	8		
I_{CC2S}	STANDBY CURRENT (CLK = V_{IL}, $\overline{CS}$ = V_{IH}, $V_{IH/L}$ = V_{IH}(min) / V_{IL}(max) Bank: Inactive State)	CKE = V_{IH}	–	80	–	80	mA	
I_{CC2PS}		CKE = V_{IL} (Power-Down Mode)	–	8	–	8		
I_{CC3}	NO OPERATING CURRENT (t_{CK} = min, $\overline{CS}$ = V_{IH}(min) Bank: Active State (2 banks))	CKE = V_{IH}	–	480	–	360	mA	3
I_{CC3P}		CKE = V_{IL} (Power-Down Mode)	–	64	–	64		
I_{CC4}	BURST OPERATING CURRENT (t_{CK} = min, $\overline{CS}$ = V_{IH}(min), Read / Write Command Cycling)		–	960	–	720	mA	3, 4
I_{CC5}	AUTO-REFRESH CURRENT (t_{CK} = min, t_{RC} = min, Auto-Refresh Command Cycling)		–	1120	–	880	mA	3
I_{CC6}	SELF-REFRESH CURRENT (Self-Refresh Mode, CKE = 0.2 V)		–	8	–	8	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT (0 V ≦ V_{IN} ≦ V_{DD}, All Other Pins Not under Test = 0 V)		– 5	5	– 5	5	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} Is Disabled, 0 V ≦ V_{OUT} ≦ V_{DD})		– 5	5	– 5	5	μA	
V_{OH}	OUTPUT LEVEL LVTTL Output H-Level Voltage (I_{OUT} = – 2 mA)		2.4	–	2.4	–	V	
V_{OL}	OUTPUT LEVEL LVTTL Output L-Level Voltage (I_{OUT} = 2 mA)		–	0.4	–	0.4	V	

AC CHARACTERISTICS AND OPERATING CONDITIONS

(V_{CC} = 3.3 V ± 0.3 V, Ta = 0° ~ 70°C) (Notes 5, 6, 10)

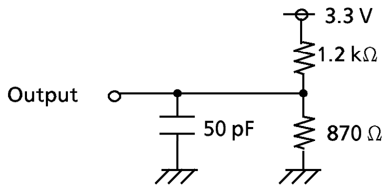
SYMBOL	PARAMETER		-80 MIN	-80 MAX	-10 MIN	-10 MAX	UNIT	NOTES
t_{RC}	Ref/Active-Ref/Active Command Period		68		84		ns	8
t_{RAS}	Active- Precharge Command Period		48	100000	60	100000	ns	8
t_{RCD}	Active-Read/Write Command Delay Time		20		24		ns	8
t_{CCD}	Read/Write(a) -Read/Write(b) Command Period		1		1		cycles	8
t_{RP}	Precharge-Active Command Period		20		24		ns	8
t_{RRD}	Active(a)-Active(b) Command Period		20		20		ns	8
t_{WR}	Write Recovery Time	CL* = 2	10		12		ns	
		CL* = 3	8		10		ns	
t_{CK}	CLK Cycle Time	CL* = 2	10	1000	12	1000	ns	
		CL* = 3	8	1000	10	1000	ns	
t_{CH}	CLK High-Level Width		3		3		ns	9
t_{CL}	CLK Low-Level Width		3		3		ns	9
t_{AC}	Access Time from CLK	CL* = 2		6		8	ns	
		CL* = 3		6		7	ns	
t_{OH}	Output Data Hold Time		3		3		ns	
t_{HZ}	Output Data High-Impedance Time		3	8	3	10	ns	7
t_{LZ}	Output Data Low-Impedance Time		0		0		ns	
t_{SB}	Power-Down Mode Entry Time		0	8	0	10	ns	
t_T	Transition Time of CLK (Rise and Fall)		0.5	10	0.5	10	ns	
t_{DS}	Data-In Set-up Time		2		2.5		ns	
t_{DH}	Data-In Hold Time		1		1		ns	
t_{AS}	Address Set-up Time		2		2.5		ns	
t_{AH}	Address Hold Time		1		1		ns	
t_{CKS}	CKE Set-up Time		2		2.5		ns	
t_{CKH}	CKE Hold Time		1		1		ns	
t_{CMS}	Command Set-up Time		2		2.5		ns	
t_{CMH}	Command Hold Time		1		1		ns	
t_{REF}	Refresh Time			64		64	ms	
t_{RSC}	Mode Register Set Cycle Time		16		20		ns	8

∗ CL is $\overline{CAS}$ latency.

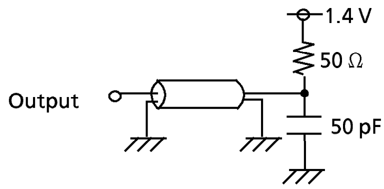
NOTES

1. Conditions outside the limits listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltages are referenced to Vss.
3. These parameters depend on the cycle rate and their values are measured at the cycle rate obtained using the minimum values of t_{CK} and t_{RC}. Input signals are changed once during t_{CK}.
4. These parameters depend on the output loading. The specified values are obtained with the output open.
5. AC TEST CONDITIONS

Reference Level for Output Signals	1.4 V / 1.4 V
Output Load	See the diagram for AC Test Load (B) below
Input Signal Levels	2.4 V / 0.4 V
Transition Time (Rise and Fall) of Input Signals	2 ns
Reference Level of Input Signals	1.4 V



AC Test Load (A)



AC Test Load (B)

6. Transition times are measured between the V_{IH} and V_{IL} levels. The transition (rise and fall) of input signals has a fixed slope.
7. t_{HZ} defines the time at which the outputs go open-circuit and are not reference levels.
8. These parameters are specified for a given number of clock cycles and a given operating frequency. The celation-ship between the number of clock cycles, the timing value and the frequency (a clock period) is as follows:

   number of clock cycles = specified timing value / clock period
   (Fractions are rounded up to a whole number.

9. t_{CH} is the pulse width of CLK measured from the positive edge to the negative edge and referenced to V_{IH} (min). t_{CL} is the pulse width of CLK measured from the negative edge to the positive edge and referenced to V_{IL} (max).

10. Power-up Sequence

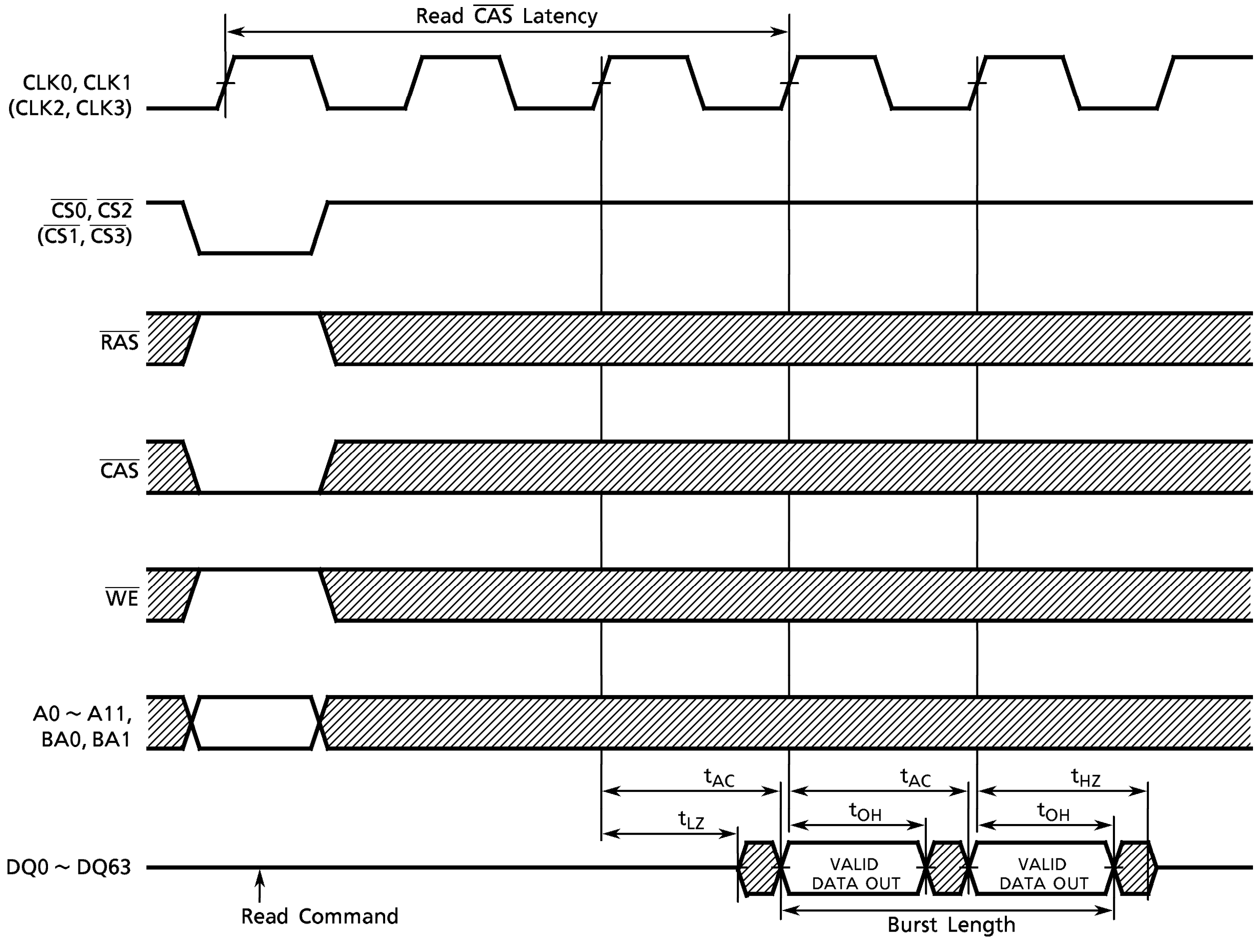
    Power-up must be performed in the following sequence.

    1) Power must be applied to V_{DD} with all input signals held in the NOP state. The CLK signal must be started at the same time as power is applied.
    2) After power-up a pause of at least 200 μseconds is required. Then, DQMB and CKE must be held High (at the V_{DD} level) to ensure that the DQ and CB outputs are High-Impedance.
    3) Both banks must be precharged.
    4) The Mode Register Set command must be asserted to initialize the Mode Register.
    5) An Auto-Refresh operation, consisting of at least eight Auto-Refresh cycles, must be performed.

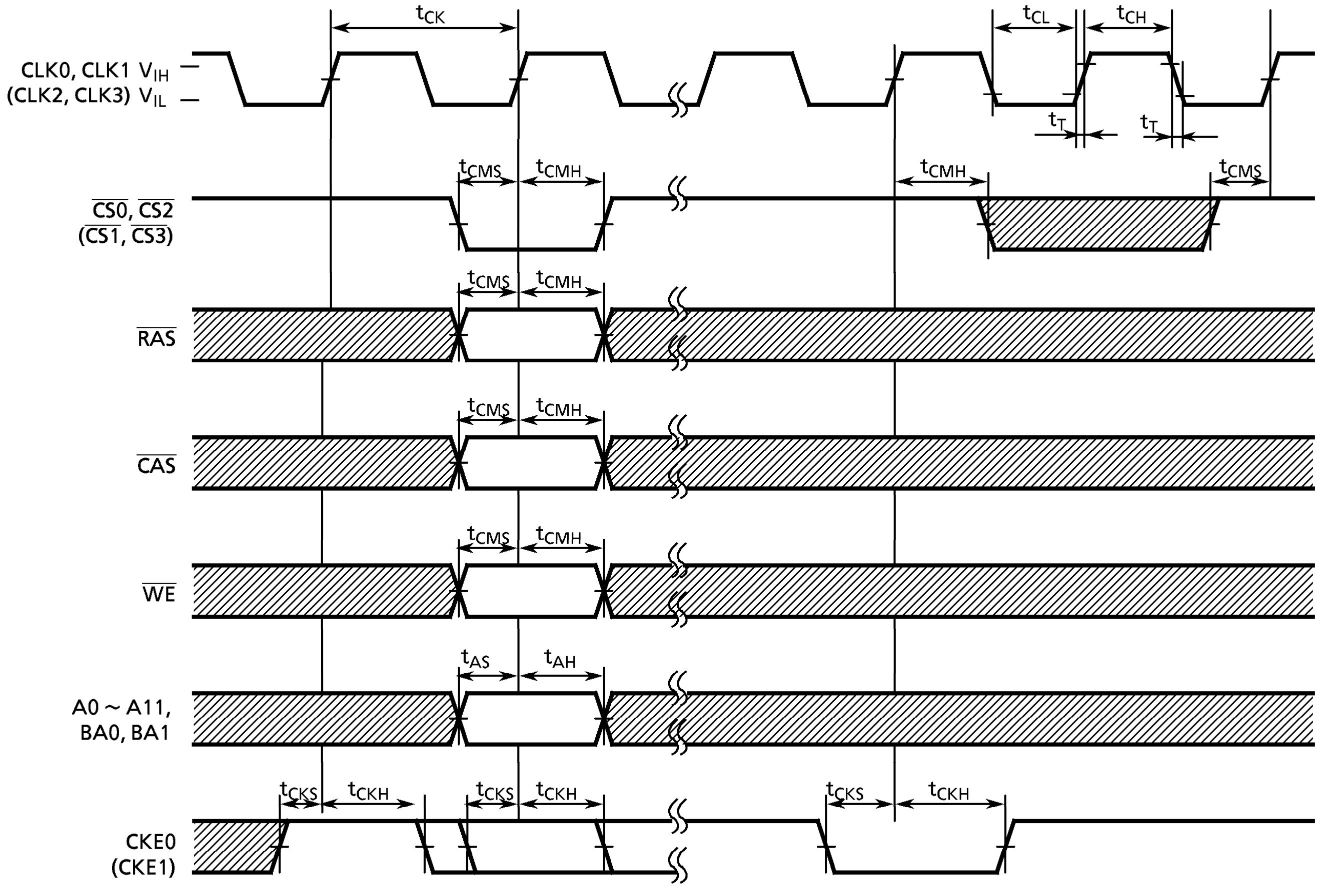
    The order in which 4) and 5) are performed is interchangeable.

TIMING DIAGRAMS

READ TIMING

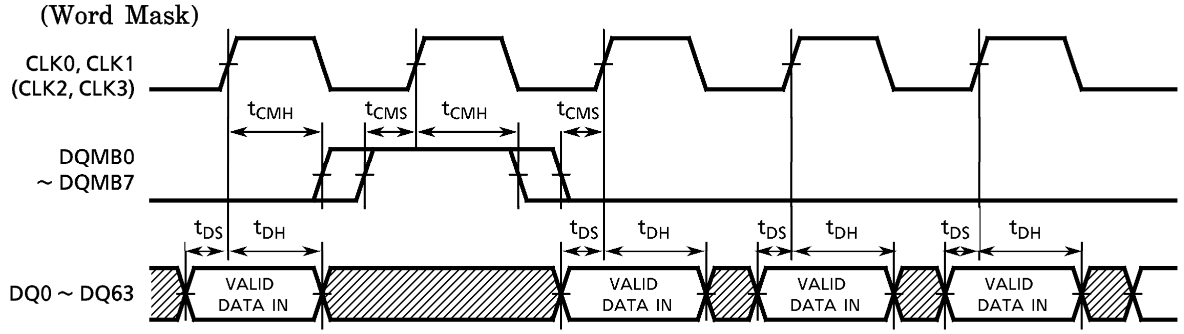


COMMAND INPUT TIMING

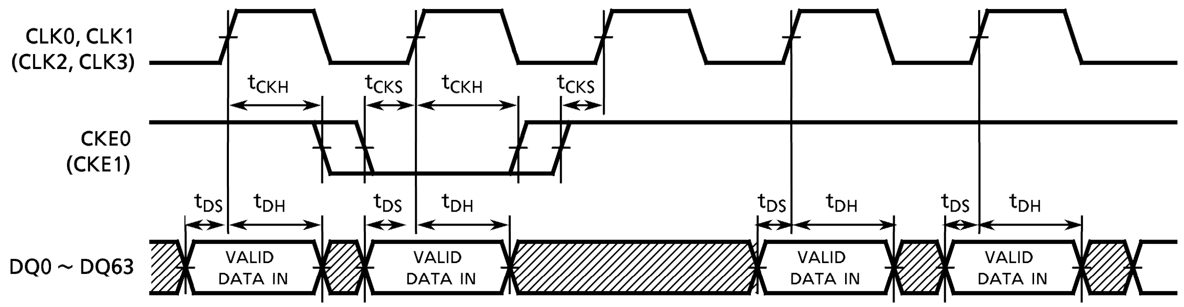


CONTROL TIMING FOR INPUT DATA

(Word Mask)

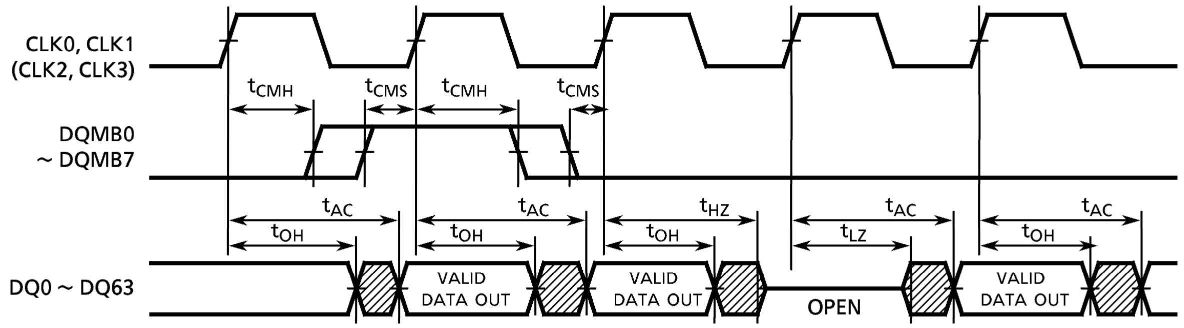


(Clock Mask)

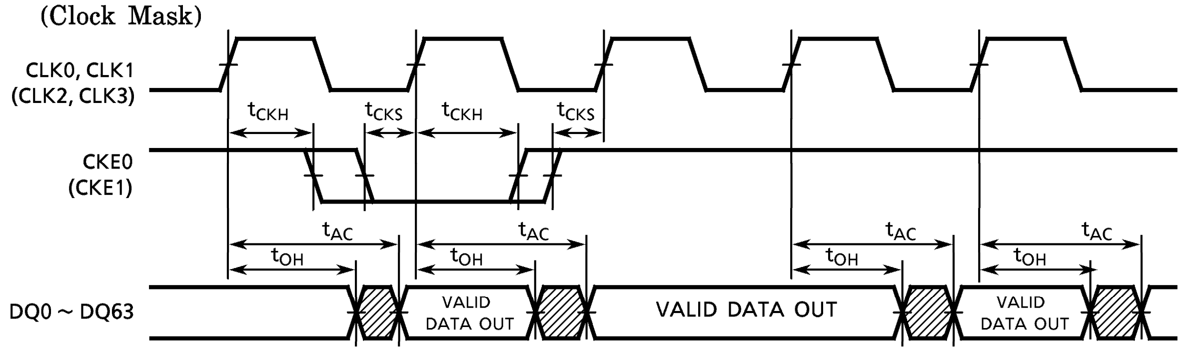


CONTROL TIMING FOR OUTPUT DATA

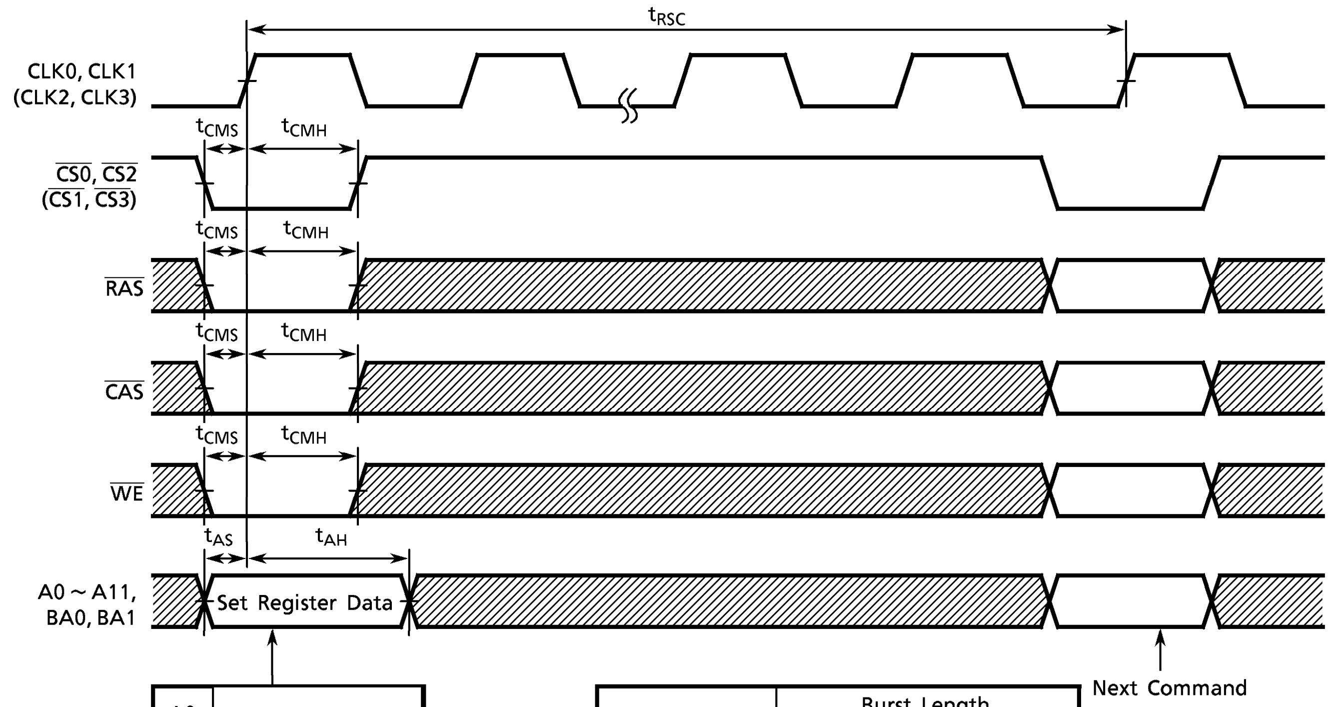
(Output Enable)



(Clock Mask)



MODE REGISTER SET CYCLE



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	$\overline{CAS}$ Latency	
A5		
A6		
A7	0	(Test Mode)
A8	0	Reserved
A9	Write Mode	
A10	0	Reserved
A11	0	
BA0	0	
BA1	0	

			Burst Length	
A2	A1	A0	Sequential	Interleaved
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1	Full Page	

A3	Addressing Mode
0	Sequential
1	Interleaved

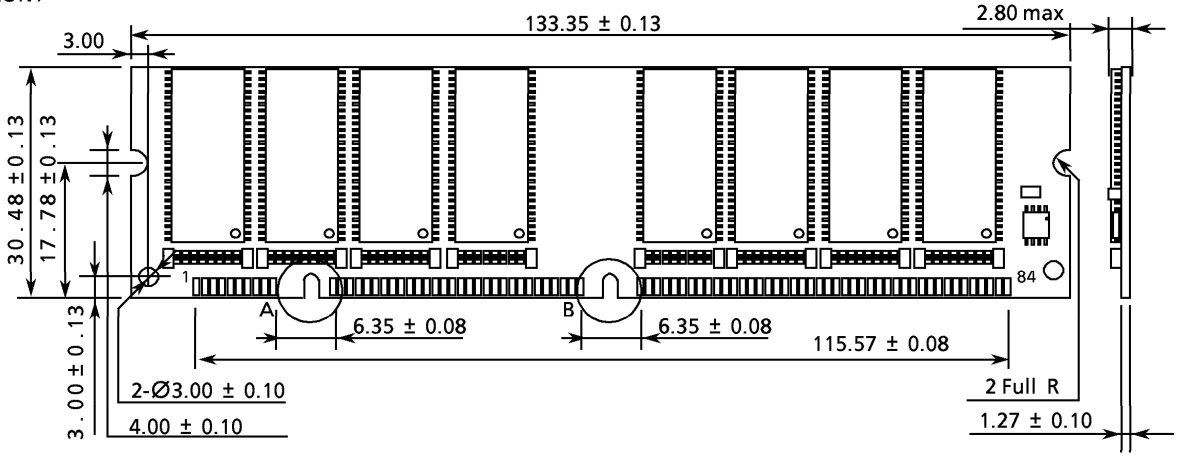
A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4

A9	Single Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

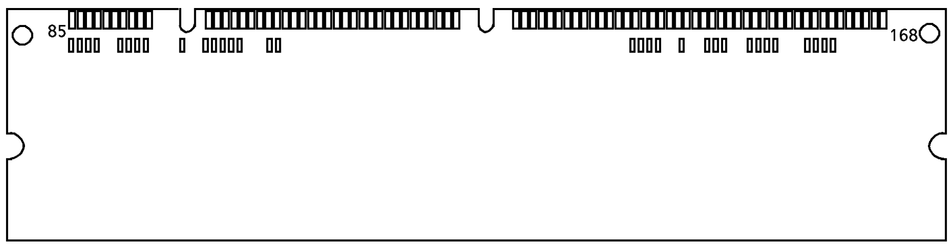
PACKAGE DIMENSIONS (THMY648071BEG)

Unit: mm

FRONT

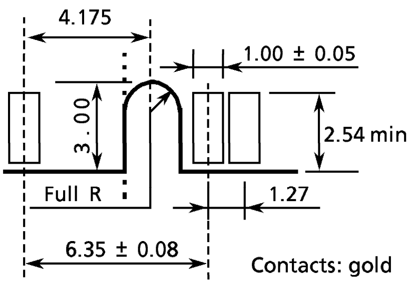


BACK



CONTACT DIMENSIONS

A: Unbuffered keying



B: 3.3-V keying