Integrated Circuit Systems, Inc.

ICS94241

Programmable TCH™ for Differential PIII™ Processor

Recommended Application:

VIA PL133-T style chipset with Intel differential PIII processor

Output Features:

- 2 - CPUs @2.5V
- 13 - SDRAM @ 3.3V
- 7 - PCI @3.3V,
- 1 - 48MHz, @3.3V
- 1 - 24MHz @ 3.3V
- 2 - REF @3.3V, 14.318MHz.

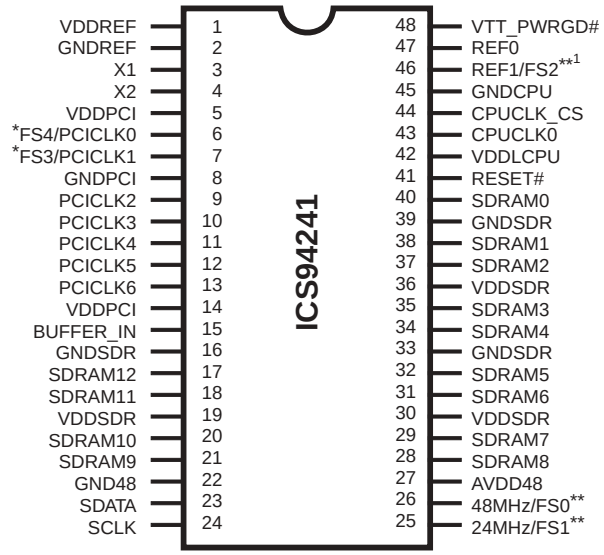
Features:

- Programmable ouput frequency
- Programmable ouput rise/fall time
- Programmable output to output skew
- Programmable spread spectrum for EMI control
- Real time system reset output
- Watchdog timer technology to reset system if over-clocking causes malfunction
- Uses external 14.318MHz crystal

Key Specifications:

- CPU – CPU: <175ps
- SDRAM - SDRAM: <500ps
- PCI – PCI: <500ps
- CPU-SDRAM: <500ps
- CPU(early)-PCI: Min=1.0ns, Typ=2.0ns, Max=4.0ns

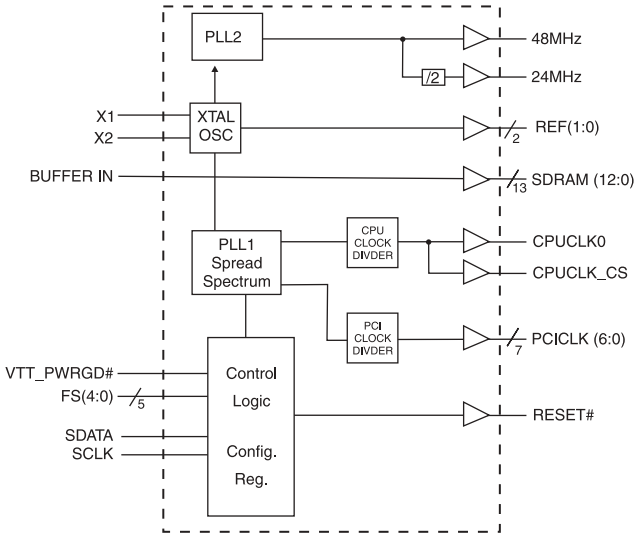
Pin Configuration



48-Pin 300mil SSOP

* Internal Pull-up Resistor of 120K to VDD
** Internal Pull-down resistor of 120K to GND
1. This output has 1.5 to 2X drive strength

Block Diagram



Functionality

Bit2	Bit7	Bit6	Bit5	Bit4	CPUCLK	PCICLK	Spread Percentage
FS4	FS3	FS2	FS1	FS0			
0	0	0	0	0	66.67	33.33	+/- 0.25 Center Spread
0	0	0	0	1	66.67	33.33	0 to -0.5% Down Spread
0	0	0	1	0	68.67	34.33	± 0.25 Center Spread
0	0	0	1	1	71.34	35.66	+/- 0.25 Center Spread
0	1	0	0	0	100.00	33.33	+/- 0.25 Center Spread
0	1	0	0	1	100.00	33.33	0 to -0.5% Down Spread
0	1	0	1	0	103.00	34.33	+/- 0.25 Center Spread
0	1	0	1	1	107.00	35.67	+/- 0.25 Center Spread
1	0	0	0	0	200.00	33.33	+/- 0.25 Center Spread
1	0	0	0	1	200.00	33.33	0 to -0.5% Down Spread
1	0	0	1	0	206.00	34.33	+/- 0.25 Center Spread
1	0	0	1	1	214.00	35.67	+/- 0.25 Center Spread
1	1	0	0	0	133.33	33.33	+/- 0.25 Center Spread
1	1	0	0	1	133.33	33.33	0 to -0.5% Down Spread
1	1	0	1	0	137.33	34.33	+/- 0.25 Center Spread
1	1	0	1	1	142.67	35.67	+/- 0.25 Center Spread

For additional margin testing frequencies refer to pg 5 frequency table.

General Description

The **ICS94241** is a single chip timing control hub for desktop designs using VIA PL133-T style chipset with Intel differential PIII processor. It provides all necessary clock signals for such a system.

The **ICS94241** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). ICS is the first to introduce a whole product line which offers full programmability and flexibility on a single clock device. This part incorporates ICS's newest clock technology which more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. TCH also incorporates ICS's Watchdog Timer technology in having a frequency reset feature to provide a safe setting under unstable system conditions.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 5, 14, 19, 30, 36	VDD	PWR	Power supply, nominal 3.3V
2, 8, 16, 22, 33, 39, 45	GND	PWR	Ground
3	X1	IN	Crystal input, has internal load cap (36pF) and feedback resistor from X2
4	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (36pF)
6	FS4[1,3]	IN	Frequency select pin. Latched Input. Internal Pull-down to GND
	PCICLK0	OUT	PCI clock outputs. Synchronous to CPU clocks with 1-4ns skew (CPU early)
7	FS3[1,3]	IN	Frequency select pin. Latched Input. Internal Pull-down to GND
	PCICLK1	OUT	PCI clock outputs. Synchronous to CPU clocks with 1-4ns skew (CPU early)
13, 12, 11, 10, 9	PCICLK (6:2)	OUT	PCI clock outputs. Synchronous to CPU clocks with 1-4ns skew (CPU early)
15	BUFFER IN	IN	Input to Fanout Buffers for SDRAM outputs.
17, 18, 20, 21, 28, 29, 31, 32, 34, 34, 35, 37, 38, 40	SDRAM (12:0)	OUT	SDRAM clock outputs, Fanout Buffer outputs from BUFFER IN pin (controlled by chipset)
23	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
24	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
25	FS1[2,3]	IN	Frequency select pin. Latched Input.
	24MHz	OUT	24MHz output clock
26	48MHz	OUT	48MHz output clock
	FS0[2,3]	IN	Frequency select pin. Latched Input
27	AVDD48	PWR	Analog power for 48MHz outputs
41	RESET	OUT	Real time system reset signal for frequency ratio change or watchdog timmer timeout. This signal is active low.
42	VDDLCPU	PWR	Supply for CPU clocks 2.5V nominal
43	CPUCLK0	OUT	CPU clock outputs
44	CPUCLK_CS	OUT	CPU clock output for chipset host clock
46	FS2[2,3]	IN	Frequency select pin. Latched Input
	REF1	OUT	14.318 MHz reference clock.
47	REF0	OUT	14.318 Mhz reference clock.
48	VTT_PWRGD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when FS inputs are valid and are ready to be sampled (active low)

Notes:

1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs
2: Internal Pull-down to GND on indicated inputs
3: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

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General I²C serial interface information for the ICS94241

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte 0 through Byte 20*** (see Note)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
○	
○	○
○	○
	○
Byte 18	
	ACK
Byte 19	
	ACK
Byte 20	
	ACK
Stop Bit	

*See notes on the following page.

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends ***Byte 0 through byte 8 (default)***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
If 7_H has been written to B6	***Byte 7***
ACK	
○	○
○	○
○	○
If 12_H has been written to B6	***Byte18***
ACK	
If 13_H has been written to B6	***Byte 19***
ACK	
If 14_H has been written to B6	***Byte 20***
ACK	
Stop Bit	

Brief I²C registers description for ICS94241 Programmable System Frequency Generator

Register Name	Byte	Description	PWD Default
Functionality & Frequency Select Register	0	Output frequency, hardware / I²C frequency select, spread spectrum & output enable control register.	See individual byte description
Output Control Registers	1-6	Active / inactive output control registers/latch inputs read back.	See individual byte description
Vendor ID & Revision ID Registers	7	Byte 7 bit (7:4) is ICS vendor id - 001. Other bits in this register designate device revision ID of this part.	See individual byte description
Byte Count Read Back Register	8	Writing to this register will configure byte count and how many byte will be read back. Do not write 00_H to this byte.	08_H
Watchdog Timer Count Register	9	Writing to this register will configure the number of seconds for the watchdog timer to reset.	10_H
Watchdog Control Registers	10 Bit [6:0]	Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register.	000,0000
VCO Control Selection Bit	10 Bit [7]	This bit select whether the output frequency is control by hardware/byte 0 configurations or byte 11&12 programming.	0
VCO Frequency Control Registers	11-12	These registers control the dividers ratio into the phase detector and thus control the VCO output frequency.	Depended on hardware/byte 0 configuration
Spread Spectrum Control Registers	13-14	These registers control the spread percentage amount.	Depended on hardware/byte 0 configuration
Group Skews Control Registers	15-16	Increment or decrement the group skew amount as compared to the initial skew.	See individual byte description
Output Rise/Fall Time Select Registers	17-20	These registers will control the output rise and fall time.	See individual byte description

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to readback is defined by writing to byte 8.**
2. **When writing to byte 11 - 12, and byte 13 - 14, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
3. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
4. The input is operating at 3.3V logic levels.
5. The data byte format is 8 bit bytes.
6. To simplify the clock generator I²C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
7. At power-on, all registers are set to a default condition, as shown.

Byte 0: Functionality and frequency select register (Default=0)

Bit	Description								PWD
	Bit2	Bit7	Bit6	Bit5	Bit4	CPUCLK	PCICLK	Spread Percentage	
	FS4	FS3	FS2	FS1	FS0				
Bit 2, (7:4)	0	0	0	0	0	66.67	33.33	Center Spread +/- 0.25%	Note 1
	0	0	0	0	1	66.67	33.33	Down Spread 0 to - 0.5%	
	0	0	0	1	0	68.67	34.33	Center Spread +/- 0.25%	
	0	0	0	1	1	71.34	35.66	Center Spread +/- 0.25%	
	0	0	1	0	0	73.34	36.66	Center Spread +/- 0.25%	
	0	0	1	0	1	76.67	38.33	Center Spread +/- 0.25%	
	0	0	1	1	0	150.00	30.00	Center Spread +/- 0.25%	
	0	0	1	1	1	166.67	33.33	Center Spread +/- 0.25%	
	0	1	0	0	0	100.00	33.33	Center Spread +/- 0.25%	
	0	1	0	0	1	100.00	33.33	Down Spread 0 to - 0.5%	
	0	1	0	1	0	103.00	34.33	Center Spread +/- 0.25%	
	0	1	0	1	1	107.00	35.67	Center Spread +/- 0.25%	
	0	1	1	0	0	110.00	36.67	Center Spread +/- 0.25%	
	0	1	1	0	1	115.00	38.33	Center Spread +/- 0.25%	
	0	1	1	1	0	100.90	33.63	Center Spread +/- 0.25%	
	0	1	1	1	1	90.00	30.00	Center Spread +/- 0.25%	
	1	0	0	0	0	200.00	33.33	Center Spread +/- 0.25%	
	1	0	0	0	1	200.00	33.33	Down Spread 0 to - 0.5%	
	1	0	0	1	0	206.00	34.33	Center Spread +/- 0.25%	
	1	0	0	1	1	214.00	35.67	Center Spread +/- 0.25%	
	1	0	1	0	0	220.00	36.67	Center Spread +/- 0.25%	
	1	0	1	0	1	230.00	38.33	Center Spread +/- 0.25%	
	1	0	1	1	0	201.80	33.63	Center Spread +/- 0.25%	
	1	0	1	1	1	180.00	30.00	Center Spread +/- 0.25%	
	1	1	0	0	0	133.33	33.33	Center Spread +/- 0.25%	
	1	1	0	0	1	133.33	33.33	Down Spread 0 to - 0.5%	
	1	1	0	1	0	137.33	34.33	Center Spread +/- 0.25%	
	1	1	0	1	1	142.67	35.67	Center Spread +/- 0.25%	
	1	1	1	0	0	146.67	36.67	Center Spread +/- 0.25%	
	1	1	1	0	1	153.33	38.33	Center Spread +/- 0.25%	
	1	1	1	1	0	133.90	33.48	Center Spread +/- 0.25%	
	1	1	1	1	1	120.00	30.00	Center Spread +/- 0.25%	
Bit 3	0=Frequency selected by hardware; 1=Frequency selected by Bit2, (7:4)								0
Bit 1	0=Spread off; 1=Spread Spectrum Enable								1
Bit 0	0=Running; 1=Tristate								0

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

Byte 1: CPU, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Latched FS2#
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	40	1	SDRAM0
Bit 2	-	1	(Reserved)
Bit 1	43	1	CPUCLK0
Bit 0	44	1	CPUCLK_CS

Byte 2: PCI, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	6	1	PCICLK0
Bit 5	13	1	PCICLK6
Bit 4	12	1	PCICLK5
Bit 3	11	1	PCICLK4
Bit 2	10	1	PCICLK3
Bit 1	9	1	PCICLK2
Bit 0	7	1	PCICLK1

Byte 3: SDRAM, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	X	Latched FS0#
Bit 5	26	1	48MHz
Bit 4	25	1	24 MHz
Bit 3	-	1	(Reserved)
Bit 2	17, 18, 20, 21	1	SDRAM (12:9)
Bit 1	28, 29, 31, 32	1	SDRAM (8:5)
Bit 0	34, 35, 37, 38	1	SDRAM (4:1)

Byte 4: Reserved , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	X	Latched FS1#
Bit 2	-	X	Latched FS4#
Bit 1	-	X	Latched FS3#
Bit 0	-	1	(Reserved)

Byte 5: Peripheral , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	46	1	REF1
Bit 0	47	1	REF0

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 6: Peripheral , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	1	Reserved (Note)
Bit5	-	X	Reserved (Note)
Bit4	-	X	Reserved (Note)
Bit3	-	X	Reserved (Note)
Bit2	-	X	Reserved (Note)
Bit1	-	X	Reserved (Note)
Bit0	-	X	Reserved (Note)

Note: This is an unused register writing to this register will not affect device performance or functinality.

Byte 7: Vendor ID and Revision ID Register

Bit	PWD	Description
Bit 7	0	Vendor ID
Bit 6	0	Vendor ID
Bit 5	1	Vendor ID
Bit 4	X	Revision ID
Bit 3	X	Revision ID
Bit 2	X	Revision ID
Bit 1	X	Revision ID
Bit 0	X	Revision ID

Byte 8: Byte Count and Read Back Register

Bit	PWD	Description
Bit 7	0	Reserved
Bit 6	0	Reserved
Bit 5	0	Reserved
Bit 4	0	Reserved
Bit 3	1	Reserved
Bit 2	0	Reserved
Bit 1	0	Reserved
Bit 0	0	Reserved

Byte 9: Watchdog Timer Count Register

Bit	PWD	Description
Bit 7	0	The decimal representation of these 8 bits correspond to 290ms or 1ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 16X 290ms = 4.6 seconds.
Bit 6	0	
Bit 5	0	
Bit 4	1	
Bit 3	0	
Bit 2	0	
Bit 1	0	
Bit 0	0	

Byte 10: VCO Control Selection Bit & Watchdog Timer Control Register

Bit	PWD	Description
Bit 7	0	0=Hw/B0 freq / 1=B11&12 freq
Bit 6	0	WD Enable 0=disable / 1=enable
Bit 5	0	WD Status 0=normal / 1=alarm
Bit 4	1	WD Safe Frequency, FS4
Bit 3	1	WD Safe Frequency, FS3
Bit 2	0	WD Safe Frequency, FS2
Bit 1	0	WD Safe Frequency, FS1
Bit 0	0	WD Safe Frequency, FS0

Note: FS values in bit (4:0) will correspond to Byte 0 FS values. Default safe frequency is same as 00000 entry in byte0.

Byte 11: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit0
Bit 6	X	REF Divider Bit6
Bit 5	X	REF Divider Bit5
Bit 4	X	REF Divider Bit4
Bit 3	X	REF Divider Bit3
Bit 2	X	REF Divider Bit2
Bit 1	X	REF Divider Bit1
Bit 0	X	REF Divider Bit0

Note: The decimal representation of these 7 bits (Byte 11 [6:0]) + 2 is equal to the REF divider value .

Notes:

1. PWD = Power on Default

Byte 12: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit8
Bit 6	X	VCO Divider Bit7
Bit 5	X	VCO Divider Bit6
Bit 4	X	VCO Divider Bit5
Bit 3	X	VCO Divider Bit4
Bit 2	X	VCO Divider Bit3
Bit 1	X	VCO Divider Bit2
Bit 0	X	VCO Divider Bit1

Note: The decimal representation of these 9 bits (Byte 12 bit [7:0] & Byte 11 bit [7]) + 8 is equal to the VCO divider value. For example if VCO divider value of 36 is desired, user need to program 36 - 8 = 28, namely, 0, 00011100 into byte 12 bit & byte 11 bit 7.

Byte 13: Spread Sectrum Control Register

Bit	PWD	Description
Bit 7	X	Spread Spectrum Bit7
Bit 6	X	Spread Spectrum Bit6
Bit 5	X	Spread Spectrum Bit5
Bit 4	X	Spread Spectrum Bit4
Bit 3	X	Spread Spectrum Bit3
Bit 2	X	Spread Spectrum Bit2
Bit 1	X	Spread Spectrum Bit1
Bit 0	X	Spread Spectrum Bit0

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 14: Spread Sectrum Control Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Spread Spectrum Bit12
Bit 3	X	Spread Spectrum Bit11
Bit 2	X	Spread Spectrum Bit10
Bit 1	X	Spread Spectrum Bi 9
Bit 0	X	Spread Spectrum Bit8

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 15: Output Skew Control

Bit	PWD	Description
Bit 7	0	PCICLK0 Skew Control
Bit 6	1	
Bit 5	1	
Bit 4	0	
Bit 3	0	PCICLK (6:1) Skew Control
Bit 2	1	
Bit 1	1	
Bit 0	0	

Byte 16: Output Skew Control

Bit	PWD	Description
Bit 7	0	SDRAM (12:1) Skew Control
Bit 6	0	
Bit 5	0	CPUCLK_CS Skew Control
Bit 4	0	
Bit 3	0	CPUCLK0 Skew Control
Bit 2	0	
Bit 1	0	SDRAM0 Skew Control
Bit 0	0	

Byte 17: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	CPUCLK_CS Slew Rate Control
Bit 6	0	
Bit 5	1	CPUCLK0 Slew Rate Control
Bit 4	0	
Bit 3	1	SDRAM0 Slew Rate Control
Bit 2	0	
Bit 1	1	SDRAM (12:1) Slew Rate Control
Bit 0	0	

Byte 18: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7	1	PCICLK (6:1) Slew Rate Control
Bit 6	0	
Bit 5	1	PCICLK0 Slew Rate Control
Bit 4	0	
Bit 3	1	48MHz Slew Rate Control
Bit 2	0	
Bit 1	1	24MHz Slew Rate Control
Bit 0	0	

Notes:

1. PWD = Power on Default
2. The power on default for byte 13-20 depends on the harware (latch inputs FS[0:4]) or I^2C (Byte 0 bit [1:7]) setting. Be sure to read back and re-write the values of these 8 registers when VCO frequency change is desired for the first pass.

Byte 19: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Byte 20: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Note: Byte 19 and 20 are reserved registers, these are unused registers writing to these registers will not affect device performance or functionality.

VCO Programming Constrains

VCO Frequency ..... 150MHz to 500MHz

VCO Divider Range ..... 8 to 519

REF Divider Range ..... 2 to 129

Phase Detector Stability ..... 0.3536 to 1.4142

Useful Formula

VCO Frequency = 14.31818 x VCO/REF divider value

Phase Detector Stabiliy = 14.038 x (VCO divider value)$^{-0.5}$

To program the VCO frequency for over-clocking.

0. Before trying to program our clock manually, consider using ICS provided software utilities for easy programming.

1. Select the frequency you want to over-clock from with the desire gear ratio (i.e. CPU:SDRAM:3V66:PCI ratio) by writing to byte 0, or using initial hardware power up frequency.

2. Write 0001, 1001 (19_H) to byte 8 for readback of 21 bytes (byte 0-20).

3. Read back byte 11-20 and copy values in these registers.

4. Re-initialize the write sequence.

5. Write a '1' to byte 9 bit 7 and write to byte 11 & 12 with the desired VCO & REF divider values.

6. Write to byte 13 to 20 with the values you copy from step 3. This maintains the output spread, skew and slew rate.

7. The above procedure is only needed when changing the VCO for the 1st pass. If VCO frequency needed to be changed again, user only needs to write to byte 11 and 12 unless the system is to reboot.

Note:

1. User needs to ensure step 3 & 7 is carried out. Systems with wrong spread percentage and/or group to group skew relation programmed into bytes 13-16 could be unstable. Step 3 & 7 assure the correct spread and skew relationship.

2. If VCO, REF divider values or phase detector stability are out of range, the device may fail to function correctly.

3. Follow min and max VCO frequency range provided. Internal PLL could be unstable if VCO frequency is too fast or too slow. Use 14.31818MHz x VCO/REF divider values to calculate the VCO frequency (MHz).

4. ICS recommends users, to utilize the software utility provided by ICS Application Engineering to program the VCO frequency.

5. Spread percent needs to be calculated based on VCO frequency, spread modulation frequency and spread amount desired. See Application note for software support.

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD}, V_{DDL} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with no pull-up resistors	-200			mA
Operating	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz		90	180	mA
Supply Current	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz		90		
Input frequency	F_i	V_{DD} = 3.3 V	12		16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization1	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating	$I_{DD2.5OP66}$	C_L = 0 pF; Select @ 66.8 MHz		10	72	mA
Supply Current	$I_{DD2.5OP100}$	C_L = 0 pF; Select @ 100 MHz		15	100	
Skew[1]	$t_{CPU-PCI}$	V_T = 1.5 V; VTL = 1.25 V	1.5		4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-19	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	19			mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.5V, V_{OH} = 2.0 V		0.95	1.3	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0V, V_{OL} = 0.5 V		0.95	1.3	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	49	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		145	175	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V		225	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -11 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	25			mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V,V_{OH} = 2.4 V		1.6	2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V,V_{OL} = 0.4 V		1.9	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	52	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		50	500	ps
Jitter, Cycle-to-cycle	$t_{jcyc-cyc2B}$[1]	V_T= 1.5 V		240	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -28mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 23 mA			0.4	V
Output High Current	I_{OH3}	V_{OH} = 2.0 V			-54	mA
Output Low Current	I_{OL3}	V_{OH} = 0.8 V	41			mA
Rise Time	T_{r31}	V_{OL} = 0.4V, V_{OH} = 2.4 V		0.85	2	ns
Fall Time	T_{f31}	V_{OH} = 2.4V, V_{OL}= 0.4 V		0.85	2	ns
Duty Cycle	D_{t31}	V_T= 1.5 V	45	50	55	%
Skew1	T_{sk1}	V_T= 1.5 V		200	500	ps
Propagation Delay	T_{prop}	V_T= 1.5 V			5	ns

1Guarenteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz, 48MHz, REF

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -16 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, VOH = 2.4 V		1.5	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, VOL = 0.4 V		1.5	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	53	55	%
Jiter, Cycle-to-cycle (24, 48MHz)	$t_{jcyc-cyc2B}$[1]	V_T = 1.5 V		250	500	ps

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

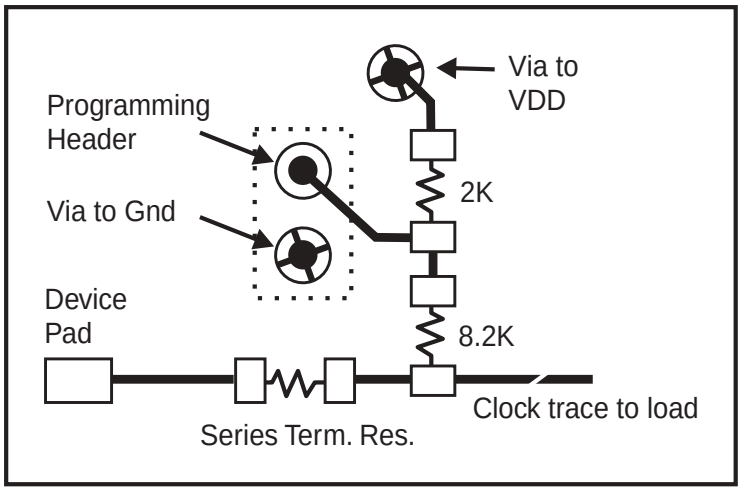
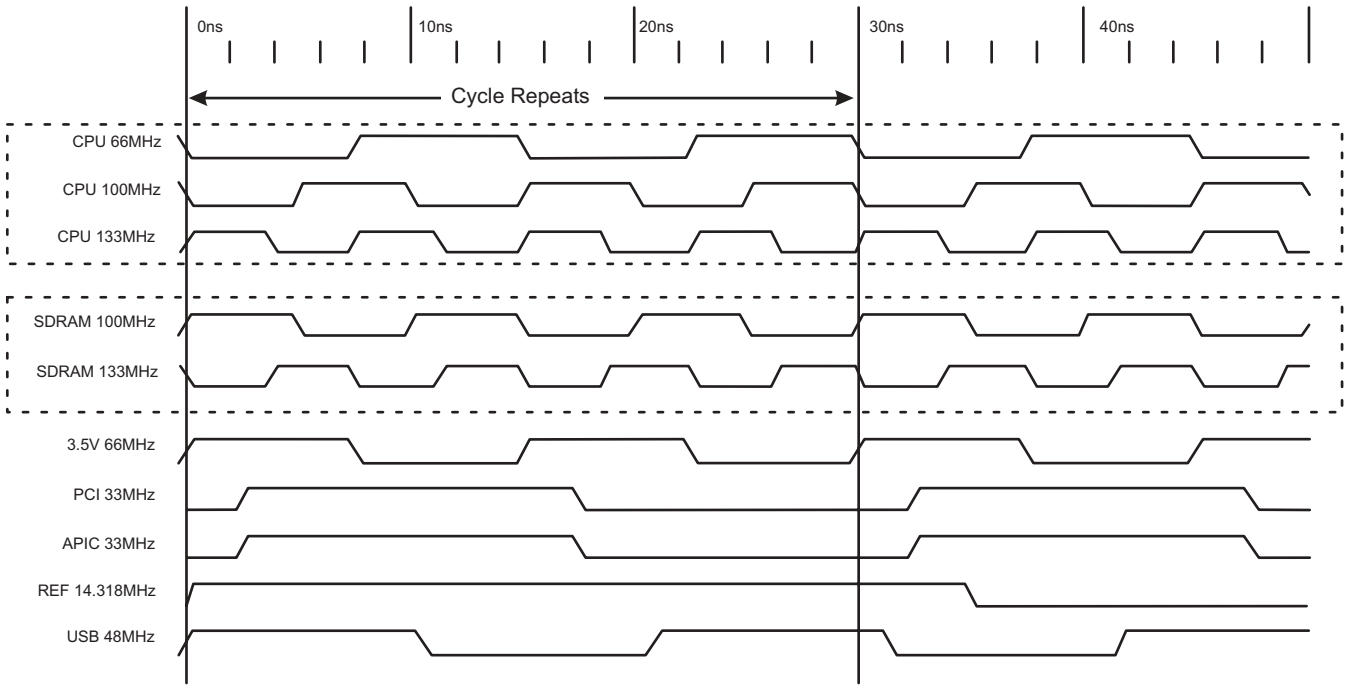
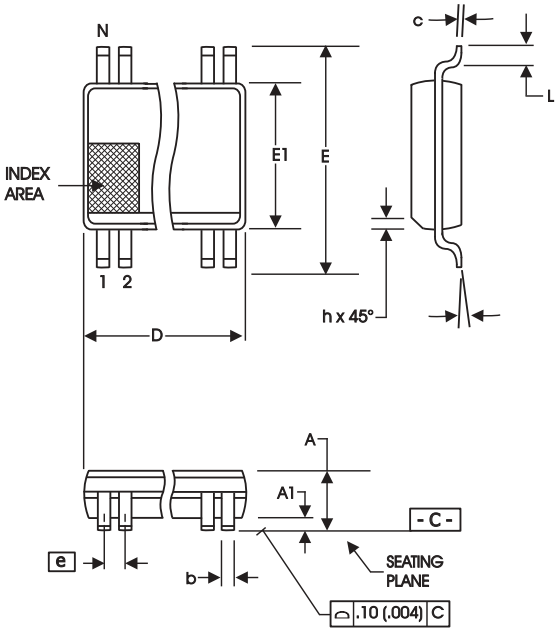


Fig. 1



Group Offset Waveforms



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS94241yFLF-T

Example:

ICS XXXX y **F LF-T**

- **Designation for tape and reel packaging**
- **Lead Free (optional)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device

0453C—10/26/04

Revision History

Rev.	Issue Date	Description	Page #
C	10/26/2004	Added Lead Free Ordering Information	15