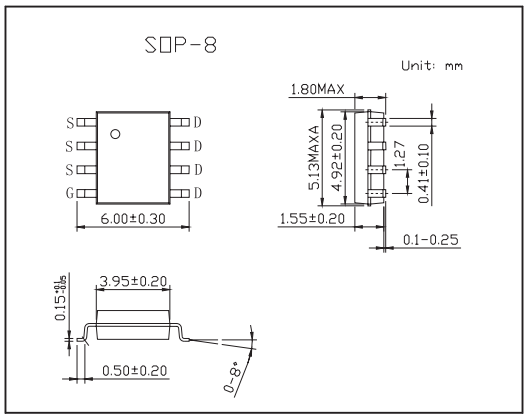
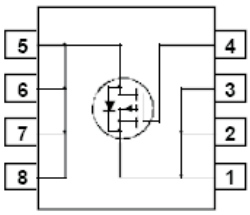
P-Channel 2.5V Specified PowerTrench MOSFET

KDS6375



■ Features

- -8 A, -20 V. $R_{DS(ON)}$ = 24mΩ @ V_{GS} = -4.5 V
  $R_{DS(ON)}$ = 32mΩ @ V_{GS} =-2.5V
- Low gate charge(26nC typical)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	-20	V
Gate to Source Voltage	V_{GS}	±8	V
Drain Current Continuous (Note 1a)	I_D	-8	A
Drain Current Pulsed		-50	A
Power Dissipation for Single Operation (Note 1a)	P_D	2.5	W
Power Dissipation for Single Operation (Note 1b)		1.2	
Power Dissipation for Single Operation (Note 1c)		1	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	℃
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	50	℃/W
Thermal Resistance Junction to Ambient (Note 1c)	$R_{\theta JA}$	125	℃/W
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	25	℃/W

KDS6375

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = -250 μA	-20			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = -250 μA, Referenced to 25℃		-13		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16 V, V_{GS} = 0 V			-1	μA
Gate-Body Leakage, Forward	I_{GSSF}	V_{GS} = 8V, V_{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
Gate Threshold Voltage(Not 2)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 μA	-0.4	-0.7	-1.5	V
Gate Threshold Voltage Temperature Coefficient(Not 2)	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = -250 μA, Referenced to 25℃		3		mV/℃
Static Drain-Source On-Resistance(Not 2)	$R_{DS(on)}$	V_{GS} = -4.5 V, I_D =-8 A		14	24	mΩ
		V_{GS} = -2.5 V, I_D = -7 A		19	32	
		V_{GS} = -4.5 V, I_D =-8 A,TJ = 125℃		18	39	
On-State Drain Current	$I_{D(on)}$	V_{GS} = -4.5 V, V_{DS} = -5V	-50			A
Forward Transconductance	g_{FS}	V_{DS} = -5 V, I_D = -8A		35		S
Input Capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V,f = 1.0 MHz		2694		pF
Output Capacitance	C_{oss}			480		pF
Reverse Transfer Capacitance	C_{rss}			229		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -10 V, I_D = -1 A,V_{GS} = -4.5 V, R_{GEN} = 6 Ω (Note 2)		12	22	ns
Turn-On Rise Time	tr			9	17	ns
Turn-Off Delay Time	$t_{d(off)}$			124	197	ns
Turn-Off Fall Time	tf			57	92	ns
Total Gate Charge	Q_g	V_{DS} = -10 V, I_D =-8 A,V_{GS}=-4.5V(Note 2)		26	36	nC
Gate-Source Charge	Q_{gs}			5		nC
Gate-Drain Charge	Q_{gd}			6		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				-2.1	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = -2.1A (Not 2)		-0.7	-1.2	V

Notes:

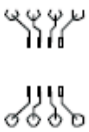
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W when mounted on a 1in² pad of 2 oz copper



b) 105 °C/W when mounted on a .04 in² pad of 2 oz copper



c) 125 °C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%