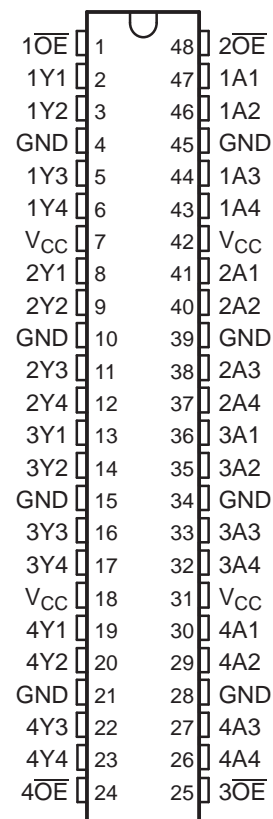


## FEATURES

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVTH162240 . . . WD PACKAGE  
SN74LVTH162240 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The 'LVTH162240 devices are 16-bit buffers/drivers designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation and to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. They have the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer and provide inverting outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**SN54LVTH162240, SN74LVTH162240**  
**3.3-V ABT 16-BIT BUFFERS/DRIVERS**  
**WITH 3-STATE OUTPUTS**

SCBS685F – MARCH 1997 – REVISED NOVEMBER 2006

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

The SN54LVTH162240 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LVTH162240 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**ORDERING INFORMATION**

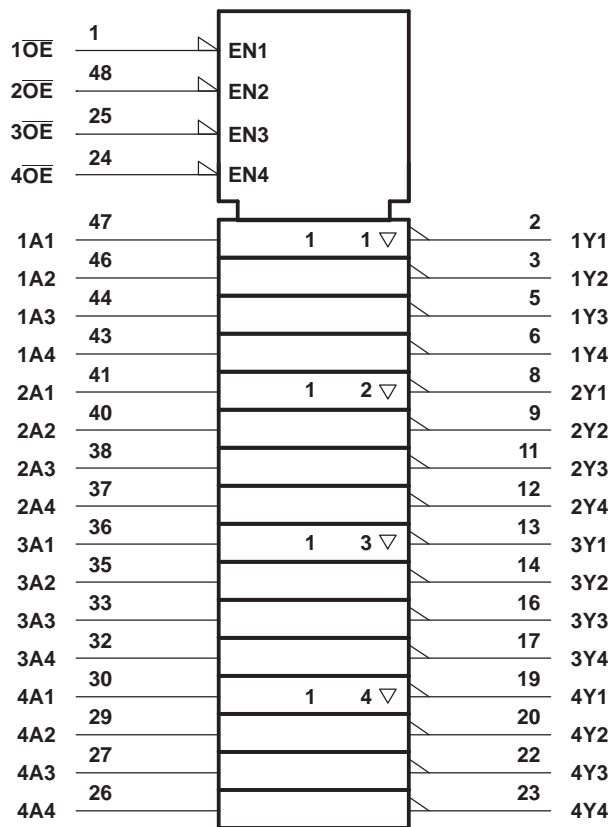
$T_A$	PACKAGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	SSOP – DL	Reel of 1000	LVTH162240	
				74LVTH162240DLRG4
				SN74LVTH162240DLR
				74LVTH162240DLG4
	Tube of 25		SN74LVTH162240DL	
			74LVTH162240DGGRE4	
TSSOP – DGG	Reel of 2000		LVTH162240	
				SN74LVTH162240DGGR

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**FUNCTION TABLE**  
**(each 4-bit buffer)**

INPUTS		OUTPUT Y
$\overline{\text{OE}}$	A	
L	H	L
L	L	H
H	X	Z

**LOGIC SYMBOL <sup>(1)</sup>**

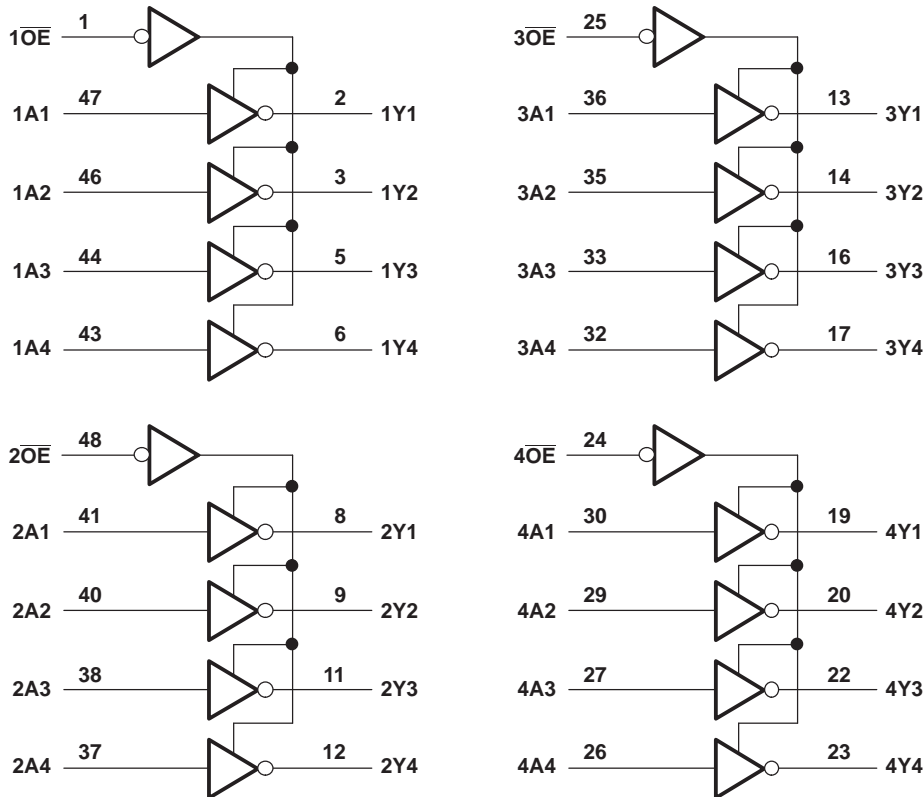


(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN54LVTH162240, SN74LVTH162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## LOGIC DIAGRAM (POSITIVE LOGIC)



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high state <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_O$	Current into any output in the low state		30	mA
$I_O$	Current into any output in the high state <sup>(3)</sup>		30	mA
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	89	°C/W
		DL package	94	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
- (4) The package thermal impedance is calculated in accordance with JESD 51.

**Recommended Operating Conditions<sup>(1)</sup>**

		SN54LVTH162240 <sup>(2)</sup>		SN74LVTH162240		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage		5.5		5.5	V
I <sub>OH</sub>	High-level output current		–12		–12	mA
I <sub>OL</sub>	Low-level output current		12		12	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
	Outputs enabled					
Δt/ΔV <sub>C</sub>	Power-up ramp rate	200		200		μs/V
T <sub>A</sub>	Operating free-air temperature	–55	125	–40	85	°C

(1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Product preview

# SN54LVTH162240, SN74LVTH162240 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS685F—MARCH 1997—REVISED NOVEMBER 2006

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTH162240 <sup>(1)</sup>			SN74LVTH162240			UNIT
			MIN	TYP <sup>(2)</sup>	MAX	MIN	TYP <sup>(2)</sup>	MAX	
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 3\text{ V}$ ,	$I_{OH} = -12\text{ mA}$	2			2			V
$V_{OL}$	$V_{CC} = 3\text{ V}$ ,	$I_{OL} = 12\text{ mA}$			0.8			0.8	V
$I_I$	Control inputs	$V_{CC} = 0\text{ or }3.6\text{ V}$ ,	$V_I = 5.5\text{ V}$		10			10	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$ ,	$V_I = V_{CC}\text{ or GND}$		$\pm 1$			$\pm 1$	
		$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$	1			1		
$V_I = 0$	-5				-5				
$I_{off}$	$V_{CC} = 0$ ,	$V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$					$\pm 100$	$\mu\text{A}$	
$I_{I(hold)}$	Data inputs	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	75		75		$\mu\text{A}$	
			$V_I = 2\text{ V}$	-75		-75			
		$V_{CC} = 3.6\text{ V}$ , <sup>(3)</sup>	$V_I = 0\text{ to }3.6\text{ V}$				500 -750		
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ ,	$V_O = 3\text{ V}$			5		5	$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ ,	$V_O = 0.5\text{ V}$			-5		-5	$\mu\text{A}$	
$I_{OZPU}$	$V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$				$\pm 100$ <sup>(4)</sup>		$\pm 100$	$\mu\text{A}$	
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$				$\pm 100$ <sup>(4)</sup>		$\pm 100$	$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19	mA	
		Outputs low		5			5		
		Outputs disabled		0.19			0.19		
$\Delta I_{CC}$ <sup>(5)</sup>	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$				0.2		0.2	mA	
$C_i$	$V_I = 3\text{ V or }0$				4		4	pF	
$C_o$	$V_O = 3\text{ V or }0$				9		9	pF	

(1) Product preview

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(5) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

## Switching Characteristics

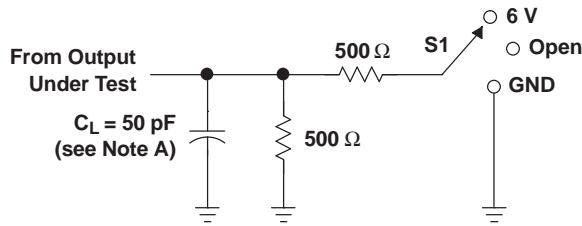
over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162240 <sup>(1)</sup>				SN74LVTH162240				UNIT	
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(2)</sup>	MAX	MIN		MAX
$t_{PLH}$	A	Y	1	4.2	5		1	2.5	4	4.6		ns
$t_{PHL}$			1	4.2	5		1	2.9	4	4.6		
$t_{PZH}$	$\overline{OE}$	Y	1	5	5.5		1	2.8	4.8	5.7		ns
$t_{PZL}$			1	4.9	5.1		1	2.8	4.7	4.9		
$t_{PHZ}$	$\overline{OE}$	Y	1.9	4.9	5.4		2	3.5	4.7	5.2		ns
$t_{PLZ}$			1.9	4.7	4.8		2	3.4	4.5	4.5		
$t_{sk(LH)}$								0.5	0.5		ns	
$t_{sk(HL)}$								0.5	0.5			

(1) Product preview

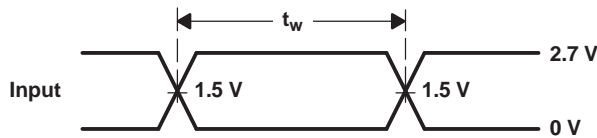
(2) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

PARAMETER MEASUREMENT INFORMATION

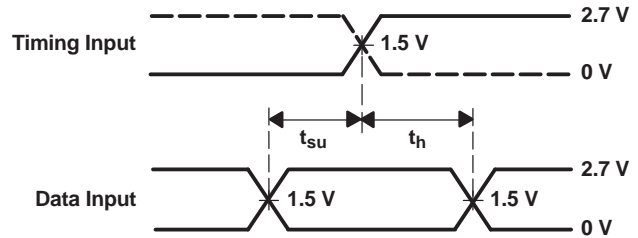


LOAD CIRCUIT

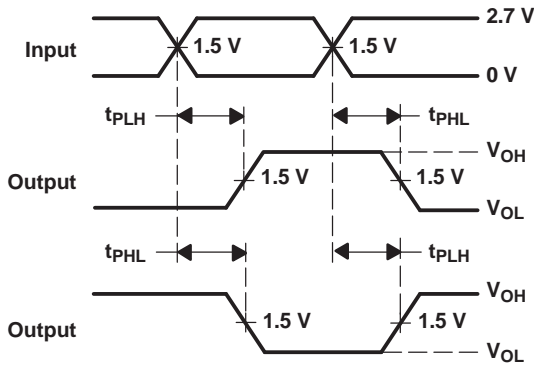
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



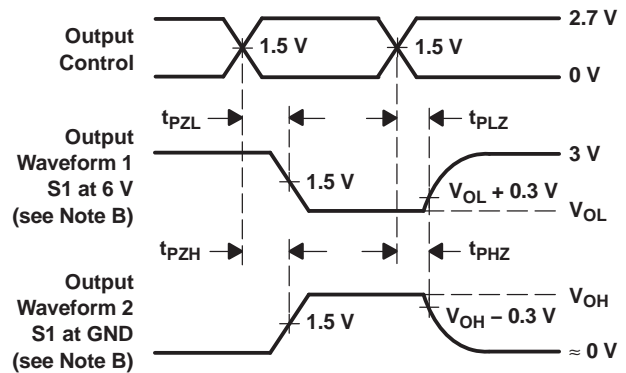
VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74LVTH162240DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVTH162240DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVTH162240DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162240DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162240DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH162240DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

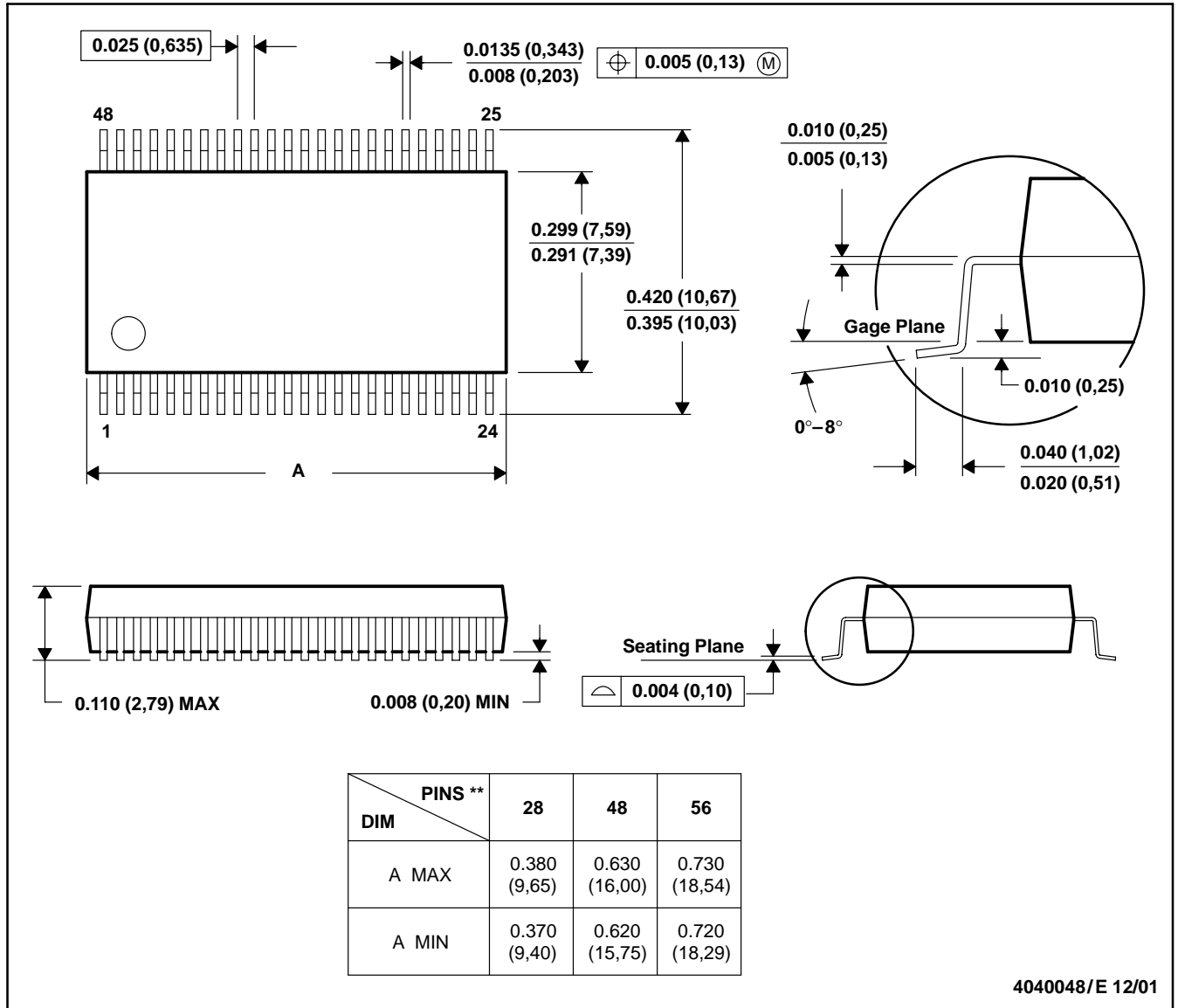
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DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
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Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Low Power Wireless	<a href="http://www.ti.com/lpw">www.ti.com/lpw</a>	Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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