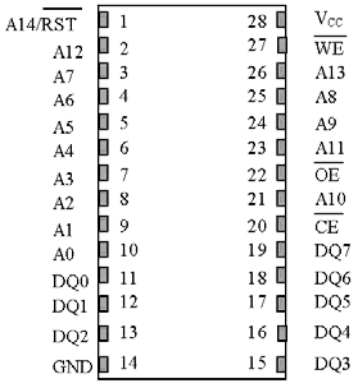
# DS1244/DS1244P
# 256k NV SRAM
# with Phantom Clock

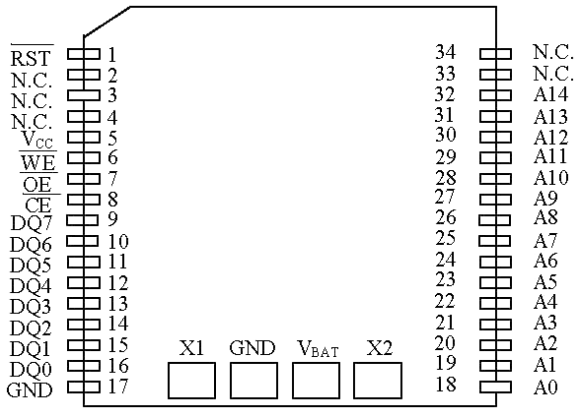
## FEATURES

- Real-time clock (RTC) keeps track of hundredths of seconds, minutes, hours, days, date of the month, months, and years.
- 32k x 8 NV SRAM directly replaces volatile static RAM or EEPROM
- Embedded lithium energy cell maintains calendar operation and retains RAM data
- Watch function is transparent to RAM operation
- Month and year determine the number of days in each month; valid up to 2100
- Full 10% operating range
- Operating temperature range: 0℃ to +70℃
- Over 10 years of data retention in the absence of power
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- DIP module only
- Standard 28-pin JEDEC pinout
- PowerCap® module board only
  - Surface mountable package for direct connection to PowerCap containing battery and crystal
  - Replaceable battery (PowerCap)
  - Pin-for-pin compatible with DS1248P and DS1251P
- Underwriters Laboratory (UL) recognized

**PIN ASSIGNMENT (Top View)**




DS2144
28-PDIP Module(740mil)

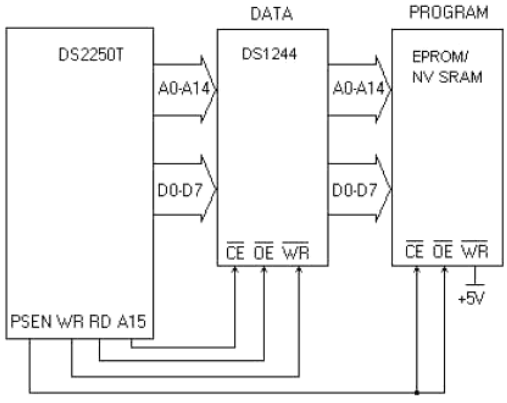



DS2144P
34-Pin PowerCap Module
(Uses DS9034PCX PowerCap)

## PIN DESCRIPTION

| | |
|---|---|
| A0-A14 | -Address Inputs |
| $\overline{CE}$ | -Chip Enable |
| $\overline{OE}$ | -Output Enable |
| $\overline{WE}$ | -Write Enable |
| Vcc | -Power-Supply Input |
| GND | -Ground |
| DQ0-DQ7 | -Data In/Data Out |
| N.C. | -No Connection |
| X1, X2 | -Crystal Connection |
| $V_{BAT}$ | -Battery Connection |
| $\overline{RST}$ | -Reset |

## TYPICAL OPERATING CIRCUIT



**ORDERING INFORMATION**

| PART | PIN-PACKAGE | TEMP RANGE | TOP MARK |
|---|---|---|---|
| DS1244Y-70 | 28-Module (740 mil) | 0℃ to +70℃ | DS1244Y-70 |
| DS1244YP-70 | 34-PowerCap* | 0℃ to +70℃ | DS1244YP-70 |
| DS1244W-120 | 28-Module (740mil) | 0℃ to +70℃ | DS1244W-120 |
| DS1244W-120IND | 28-Module (740mil) | -40℃ to +85℃ | DS1244W-120IND |
| DS1244WP-120 | 34-PowerCap* | 0℃ to +70℃ | DS1244WP-120 |
| DS1244WP-120IND | 34-PowerCap* | -40℃ to +85℃ | DS1244WP-120IND |

*DS9034PCX (PowerCap) Required. (Must be ordered separately.)

**DESCRIPTION**

The DS1244 256k NV SRAM with a Phantom clock is a fully static nonvolatile RAM (NV SRAM) (organized as 32k words by 8 bits) with a built-in real-time clock. The DS1244 has a self-contained lithium energy source and control circuitry, which constantly monitors Vcc for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data in both the memory and real-time clock.

The phantom clock provides timekeeping information for hundredths of seconds, seconds, minutes, hours, days, date, months, and years. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including correction for leap years. The phantom clock operates in either 24-hour or 12-hour format with an AM/PM indicator.

**PACKAGES**

The DS1244 is available in two packages: 28-pin DIP and 34-pin PowerCap module. The 28-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap module board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1244P after the completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap module board and PowerCap are ordered separately and shipped in separate containers. The part number for the PowerCap is DS9034PCX.

**RAM READ MODE**

The DS1244 executes a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (chip enable) is active (low). The unique address specified by the 15 address inputs (A0-A14) defines which of the 32,768 bytes of data is to be accessed. Valid data is available to the eight data-output drivers within $t_{ACC}$ (access time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (output enable) access times and states are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$, rather than address access.

**RAM WRITE MODE**

The DS1244 is in the write mode whenever the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge.

**DATA RETENTION MODE**

The 5V device is fully accessible and data can be written or read only when Vcc is greater than $V_{PF}$. However, when Vcc is below the power fail point, $V_{PF}$ (point at which write protection occurs), the internal clock registers and SRAM are blocked from any access. When Vcc falls below the battery switch point, Vso (battery supply level), device power is switched from the Vcc pin to the backup battery. RTC operation and SRAM data are maintained from the battery until Vcc is returned to nominal levels.

The 3.3V device is fully accessible and data can be written or read only when Vcc is greater than $V_{PF}$. When Vcc fall as below the $V_{PF}$, access to the device is inhibited. If $V_{PF}$ is less than $V_{BAT}$, the device power is switched from Vcc to the backup supply ($V_{BAT}$) when Vcc drops below $V_{PF}$. If $V_{PF}$ is greater than $V_{BAT}$, the device power is switched from Vcc to the backup supply ($V_{BAT}$) when Vcc drops below $V_{BAT}$. RTC operation and SRAM data are maintained from the battery until Vcc is returned to nominal levels.

All control, data, and address signals must be powered down when Vcc is powered down.

**PHANTOM CLOCK OPERATION**

Communication with the phantom clock is established by pattern recognition on a serial bit stream of 64 bits, which must be matched by executing 64 consecutive write cycles containing the proper data on DQ0. All accesses that occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 read or write cycles either extract or update data in the phantom clock, and memory access is inhibited.

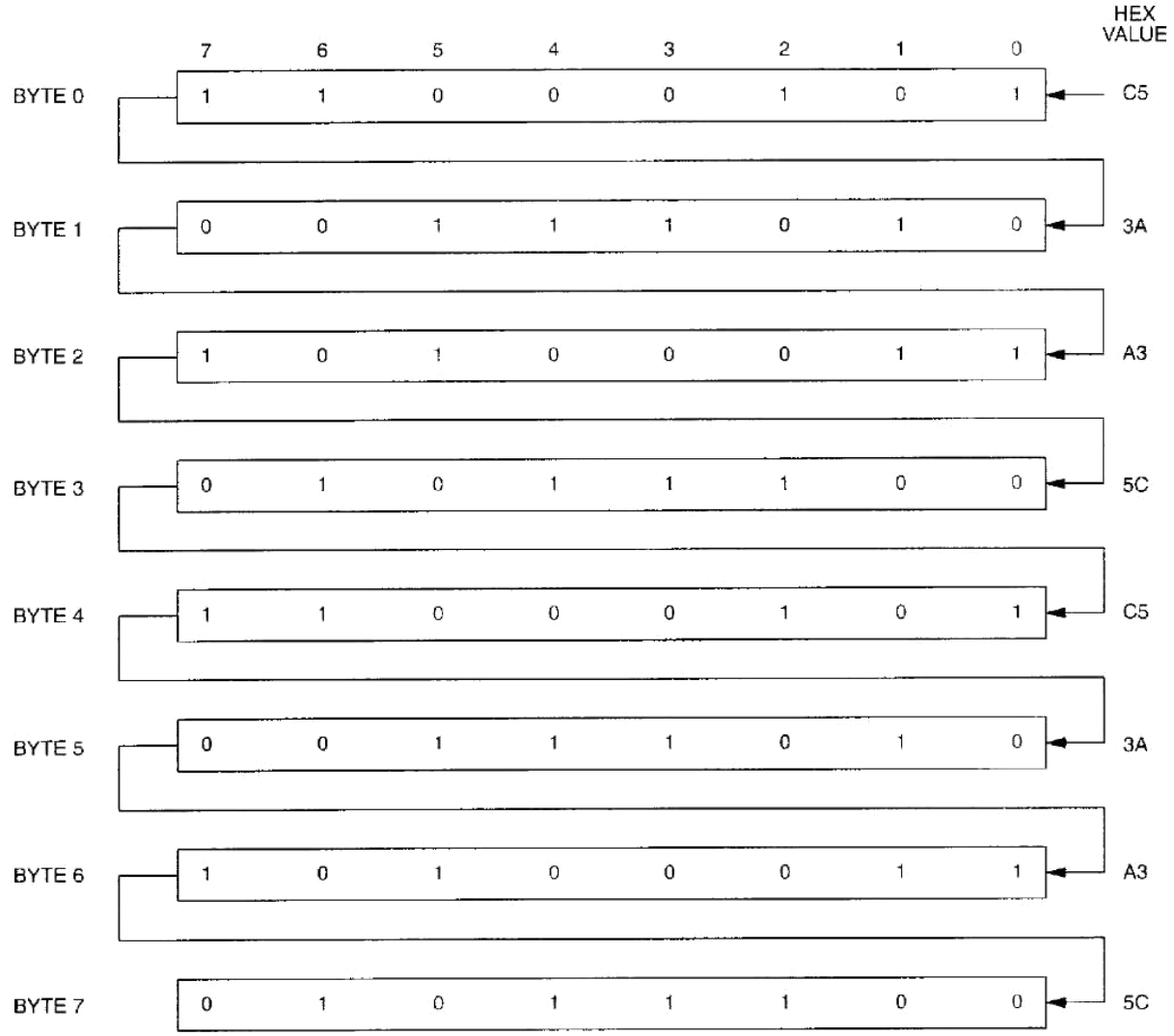
Data transfer to and from the timekeeping function is accomplished with a serial bit stream under control of the chip enable, output enable, and write enable. Initially, a read cycle to any memory location using the $\overline{CE}$ and $\overline{OE}$ control of the phantom clock starts the pattern recognition sequence by moving a pointer to the first bit of the 64-bit comparison register. Next, 64 consecutive write cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the Smartwatch. These 64 write cycles are used only to gain access to the phantom clock. Therefore, any address to the memory in the socket is acceptable. However, the write cycles generated to gain access to phantom clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a phantom clock scratch pad. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above until all the bits in the comparison register have been matched (Figure 1). With a correct match for 64 bits, the phantom clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the phantom clock to either receiver or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the phantom clock.

**PHANTOM CLOCK REGISTER INFORMATION**

The phantom clock information is contained in eight registers of 8 bits, each of which is sequentially accessed 1 bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the phantom clock registers, each register must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

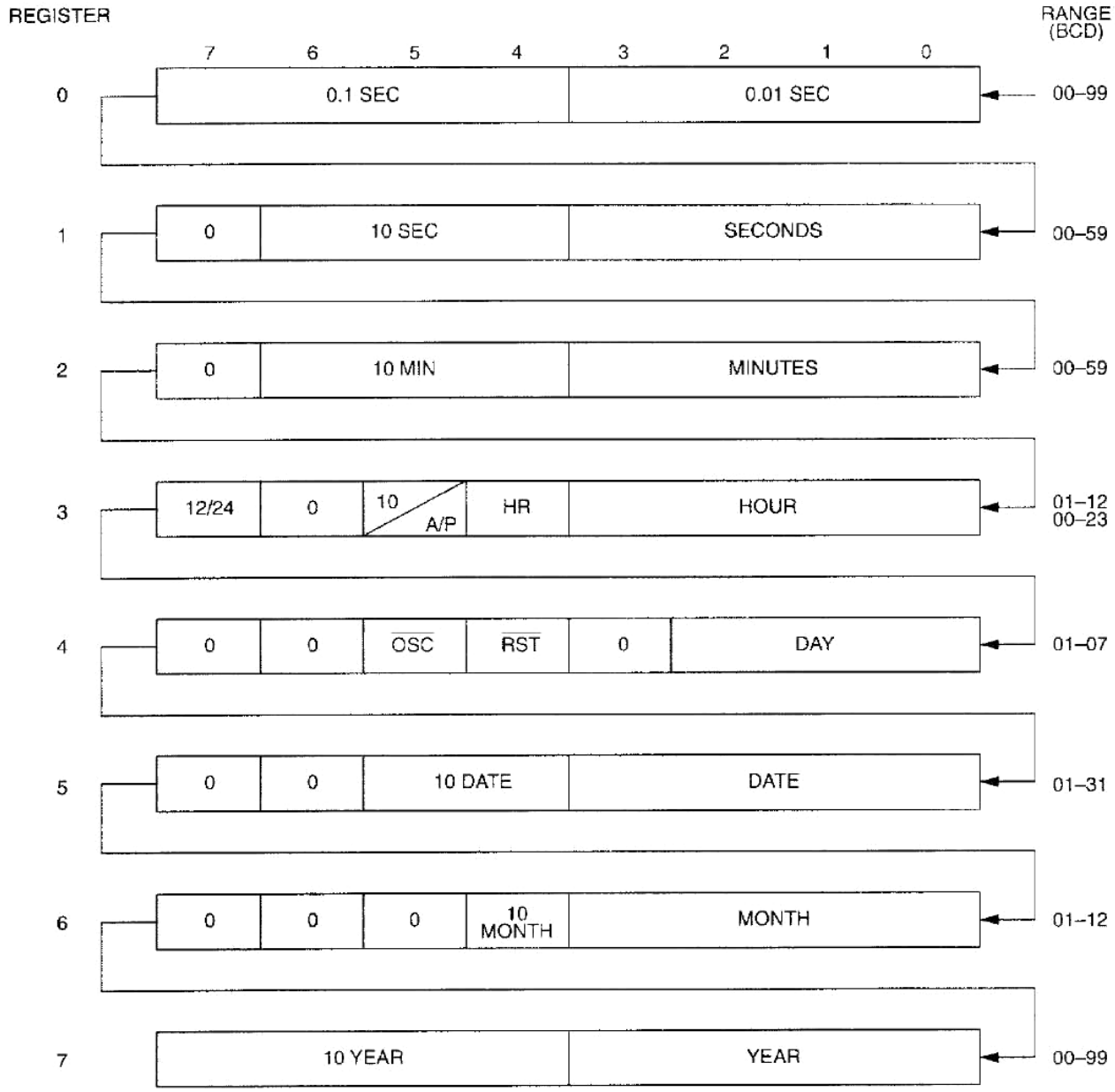
Data contained in the phantom clock register is in binary coded decimal (BCD) format. Reading and writing the registers is always accomplished by stepping through all eight registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

**Figure 1. PHANTOM CLOCK REGISTER DEFINITION**




**Note:** The pattern recognition in hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern being accidentally duplicated and causing inadvertent entry to the phantom clock is less than 1 in $10^{19}$. This pattern is sent to the phantom clock LSB to MSB.

**Figure 2. PHANTOM CLOCK REGISTER DEFINITION**




**AM/PM/12/24 MODE**

Bit 7 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

**OSCILLATOR AND RESET BITS**

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logic 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logic 0, a low input on the $\overline{\text{RESET}}$ pin will cause the phantom clock to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. When set to logic 1, the oscillator is off. When set to logic 0, the oscillator turns on and the watch becomes operational. These bits are shipped from the factory set to a logic 1.

**ZERO BITS**

Registers 1,2,3,4,5, and 6 contain one or more bits that always read logic 0. When writing these locations, either a logic 1 or 0 is acceptable.

**BATTERY LONGEVITY**

The DS1244 has a lithium power source that is designed to provided energy for clock activity and clock and RAM data retention when the Vcc supply is not present. The capability of this internal power supply is sufficient to power the DS1244 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at +25℃ with the internal clock oscillator running in the absence of Vcc power. Each DS1244 is shipped from ARTSCHIP Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When Vcc is first applied at a level greater than $V_{PF}$, the lithium energy source is enabled for battery-backup operation. Actual life expectancy of the DS1244 will be much longer than 10 years since no lithium battery energy is consumed when Vcc is present.

**CLOCK ACCURACY (DIP MODULE)**

The DS1244 is guaranteed to keep time accuracy to within ±1 minute per month at +25℃. The clock is calibrated at the factory by ARTSCHIP Semiconductor using special calibration nonvolatile tuning elements and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary.

**CLOCK ACCURACY (POWERCAP MODULE)**

The DS1244P and DS9034PCX are each individually tested for accuracy. Once mounted together, the module will typically keep time accuracy to within ±1.53 minutes per month (35 ppm) at +25℃.

**ABSOLUT MAXIMUM RATINGS ***

| | |
|---|---|
| Voltage Range on Any Pin Relative to Ground | -0.3V to +6.0V |
| Storage Temperature Range | -40℃ to +85℃ |
| Soldering Temperature Range | See IPC/JEDEC J-STD-020A (DIP) (Note 13) |

**OPERATING RANGE**

| RANGE | TEMP RANGE | Vcc |
|---|---|---|
| Commercial | 0℃ to +70℃ | 3.3V ± 10% or 5V ±10% |
| Industrial | -40℃ to +85℃ | 3.3V ±10% or 5V ±10% |

*This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS** Over the operating range

| PARAMETER | | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input Logic 1 | Vcc=5V ±10% | $V_{IH}$ | 2.2 | | Vcc+0.3V | V | 11 |
| | Vcc=3.3V ±10% | | 2.0 | | Vcc+0.3V | | |
| Input Logic 0 | Vcc=5V ±15% | $V_{IL}$ | -0.3 | | 0.8 | V | 11 |
| | Vcc=3.3V ±10% | | -0.3 | | 0.6 | | |

**DC ELECTRICAL CHARACTERISTICS** Over the operating range (5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | -1.0 | | +1.0 | µA | 12 |
| I/O Leakage Current $\overline{CE}$ ≥$V_{IH}$ ≤Vcc | $I_{IO}$ | -1.0 | | +1.0 | µA | |
| Output Current at 2.4V | $I_{OH}$ | -1.0 | | | mA | |
| Output Current at 0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}$=2.2V | $I_{CCS1}$ | | 5 | 10 | mA | |
| Standby Current $\overline{CE}$=Vcc-0.5V | $I_{CCS2}$ | | 3.0 | 5.0 | mA | |
| Operating Current $t_{CYC}$=70ns | $I_{CC01}$ | | | 85 | mA | |
| Write Protection Voltage | $V_{PF}$ | 4.25 | 4.37 | 4.50 | V | 11 |
| Battery Switchover Voltage | $V_{SO}$ | | $V_{BAT}$ | | V | 11 |

**DC ELECTRICAL CHARACTERISTICS** Over the operating range (3.3V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | -1.0 | | +1.0 | µA | 12 |
| I/O Leakage Current $\overline{CE}$ ≥$V_{IH}$ ≤Vcc | $I_{IO}$ | -1.0 | | +1.0 | µA | |
| Output Current at 2.4V | $I_{OH}$ | -1.0 | | | mA | |
| Output Current at 0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}$=2.2V | $I_{CCS1}$ | | 5 | 7 | mA | |
| Standby Current $\overline{CE}$=Vcc-0.5V | $I_{CCS2}$ | | 2.0 | 3.0 | mA | |
| Operating Current $t_{CYC}$=70ns | $I_{CC01}$ | | | 50 | mA | |
| Write Protection Voltage | $V_{PF}$ | 2.8 | 2.86 | 2.97 | V | 11 |
| Battery Switchover Voltage | $V_{SO}$ | | $V_{BAT}$ or $V_{PF}$ | | V | 11 |

**CAPACITANCE** ($T_A$=+25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | | 5 | 10 | pF | |

**MEMORY AC ELECTRICAL CHARACTERISTICS**

Over the operating range (5V)

| PARAMETER | SYMBOL | DS1244Y-70 | | UNITS | NOTES |
|---|---|---|---|---|---|
| | | MIN | MAX | | |
| Real Cycle Time | $t_{RC}$ | 70 | | ns | |
| Access Time | $t_{ACC}$ | | 70 | ns | |
| $\overline{OE}$ to output Valid | $t_{OE}$ | | 35 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | 70 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 5 | | ns | 5 |
| Output High-Z from Deselection | $t_{OD}$ | | 25 | ns | 5 |
| Output Hold from Address Change | $t_{OH}$ | 5 | | ns | |
| Write Cycle Time | $t_{WC}$ | 70 | | ns | |
| Write Pulse Width | $t_{WP}$ | 50 | | ns | 3 |
| Address Setup Time | $t_{AW}$ | 0 | | ns | |
| Write Recovery Time | $t_{WR}$ | 0 | | ns | |
| Output High-Z from $\overline{WE}$ | $t_{ODW}$ | | 25 | ns | 5 |
| Output Active from $\overline{WE}$ | $t_{OEW}$ | 5 | | ns | 5 |
| Data Setup Time | $t_{DS}$ | 30 | | ns | 4 |
| Data Hold Time from $\overline{WE}$ | $t_{DH}$ | 5 | | ns | 4 |

**PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS**

Over the operating range (5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 65 | | | ns | |
| $\overline{CE}$ Access Time | $t_{CO}$ | | | 55 | ns | |
| $\overline{OE}$ Access Time | $t_{OE}$ | | | 55 | ns | |
| $\overline{CE}$ to Output Low-Z | $t_{COE}$ | 5 | | | ns | |
| $\overline{OE}$ to Output Low-Z | $t_{OEE}$ | 5 | | | ns | |
| $\overline{CE}$ to Output High-Z | $t_{OD}$ | | | 25 | ns | 5 |
| $\overline{OE}$ to Output High-Z | $t_{ODO}$ | | | 25 | ns | 5 |
| Read Recovery | $t_{RR}$ | 10 | | | ns | |
| Write Cycle Time | $t_{WC}$ | 65 | | | ns | |
| Write Pulse Width | $t_{WP}$ | 55 | | | ns | 3 |
| Write Recovery | $t_{WR}$ | 10 | | | ns | 10 |
| Data Setup Time | $t_{DS}$ | 30 | | | ns | 4 |
| Data Hold Time | $t_{DH}$ | 0 | | | ns | 4 |
| $\overline{CE}$ Pulse Width | $t_{CW}$ | 60 | | | ns | |
| $\overline{RESET}$ Pulse Width | $t_{RST}$ | 65 | | | ns | |

**POWER-DOWN/POWER-UP TIMING** Over the operating range (5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ at $V_{IH}$ before Power-Down | $t_{PD}$ | 0 | | | µs | |
| Vcc Slew from $V_{PF(max)}$ to $V_{PF(min)}$($\overline{CE}$ at $V_{PF}$) | $t_F$ | 300 | | | µs | |
| Vcc Slew from $V_{PF(min)}$ to $V_{SO}$ | $t_{FB}$ | 10 | | | µs | |
| Vcc Slew from $V_{PF(max)}$ to $V_{PF(min)}$($\overline{CE}$ at $V_{PF}$) | $t_R$ | 0 | | | µs | |
| $\overline{CE}$ at $V_{IH}$ before Power-Up | $t_{REC}$ | 1.5 | | 2.5 | ms | |

($T_A$=+25℃)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Expected Data Retention Time | $t_{DR}$ | 10 | | | years | 9 |

Warning: Under no circumstances are negative undershoots of any amplitude allowed when device is in battery-backup mode.

**MEMORY AC ELECTRICAL CHARACTERISTICS**

Over the Operating range (3.3V)

| PARAMETER | SYMBOL | DS1244W-120 | | UNITS | NOTES |
|---|---|---|---|---|---|
| | | MIN | MAX | | |
| Read Cycle Time | $t_{RC}$ | 120 | | ns | |
| Access Time | $t_{ACC}$ | | 120 | ns | |
| $\overline{OE}$ to Output Vaild | $t_{OE}$ | | 60 | ns | |
| $\overline{CE}$ to Output Valid | $t_{CO}$ | | 120 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | $t_{COE}$ | 5 | | ns | 5 |
| Output High-Z from Deselection | $t_{OD}$ | | 40 | ns | 5 |
| Output Hold from Address Change | $t_{OH}$ | 5 | | ns | |
| Write Cycle Time | $t_{WC}$ | 120 | | ns | |
| Write Pulse Width | $t_{WP}$ | 90 | | ns | 3 |
| Address Setup Time | $t_{AW}$ | 0 | | ns | |
| Write Recovery Time | $t_{WR}$ | 20 | | ns | 10 |
| Output High-Z from $\overline{WE}$ | $t_{ODW}$ | | 40 | ns | 5 |
| Output Active from $\overline{WE}$ | $t_{OEW}$ | 5 | | ns | 5 |
| Data Setup Time | $t_{DS}$ | 50 | | ns | 4 |
| Data Hold Time from $\overline{WE}$ | $t_{DH}$ | 20 | | ns | 4 |

**PHANTOM CLOCK AC ELECTRICAL CHARACTERISTICS**

Over the operating range (3.3V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 120 | | | ns | |
| $\overline{CE}$ Access Time | $t_{CO}$ | | | 100 | ns | |
| $\overline{OE}$ Access Time | $t_{OE}$ | | | 100 | ns | |
| $\overline{CE}$ to Output Low-Z | $t_{COE}$ | 5 | | | ns | |
| $\overline{OE}$ to Output Low-Z | $t_{OEE}$ | 5 | | | ns | |
| $\overline{CE}$ to Output High-z | $t_{OD}$ | | | 40 | ns | |
| $\overline{OE}$ to Output High-Z | $t_{ODO}$ | | | 40 | ns | 5 |
| Read Recovery | $t_{RR}$ | 20 | | | ns | 5 |
| Write Cycle Time | $t_{WC}$ | 120 | | | ns | |
| Write Pulse Width | $t_{WP}$ | 100 | | | ns | 3 |
| Write Recovery | $t_{WR}$ | 20 | | | ns | 10 |
| Data Setup Time | $t_{DS}$ | 45 | | | ns | 4 |
| Data Hold Time | $t_{DH}$ | 0 | | | ns | 4 |
| $\overline{CE}$ Pulse Width | $t_{CW}$ | 105 | | | ns | |
| $\overline{RESET}$ Pulse Width | $t_{RST}$ | 120 | | | ns | |

**POWER-DOWN/POWER-UP TIMING**

Over the operating range (3.3V)

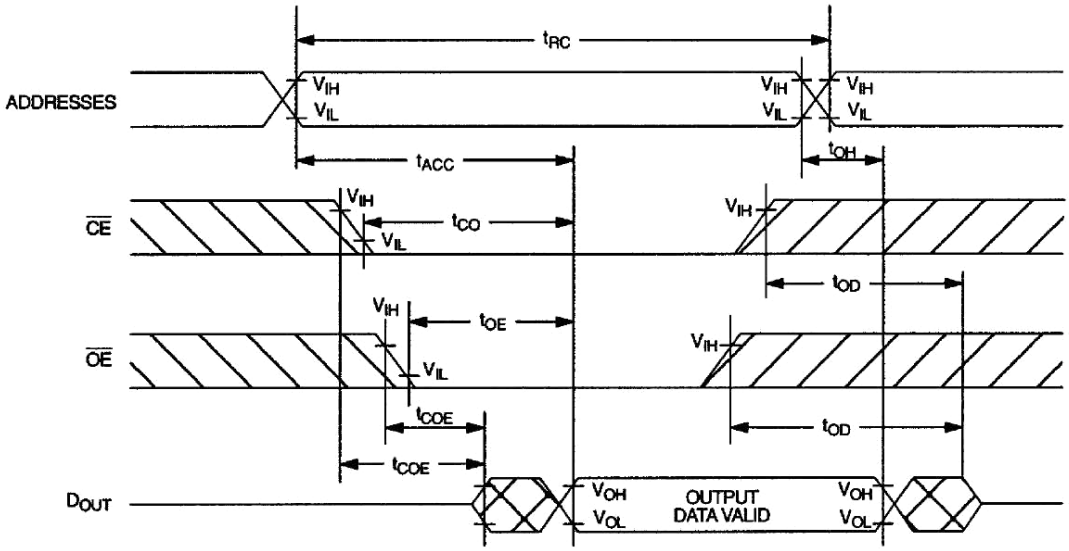
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ at $V_{IH}$ before Power-Down | $t_{PD}$ | 0 | | | µs | |
| Vcc Slew from $V_{PF(MAX)}$ to $V_{PF(MIN)}$ ($\overline{CE}$ at $V_{IH}$) | $t_F$ | 300 | | | µs | |
| Vcc Slew from $V_{PF(MAX)}$ to $V_{PF(MIN)}$ ($\overline{CE}$ at $V_{IH}$) | $t_R$ | 0 | | | µs | |
| $\overline{CE}$ at $V_{IH}$ after Power-Up | $t_{REC}$ | 1.5 | | 2.5 | ms | |

($T_A$=+25℃)

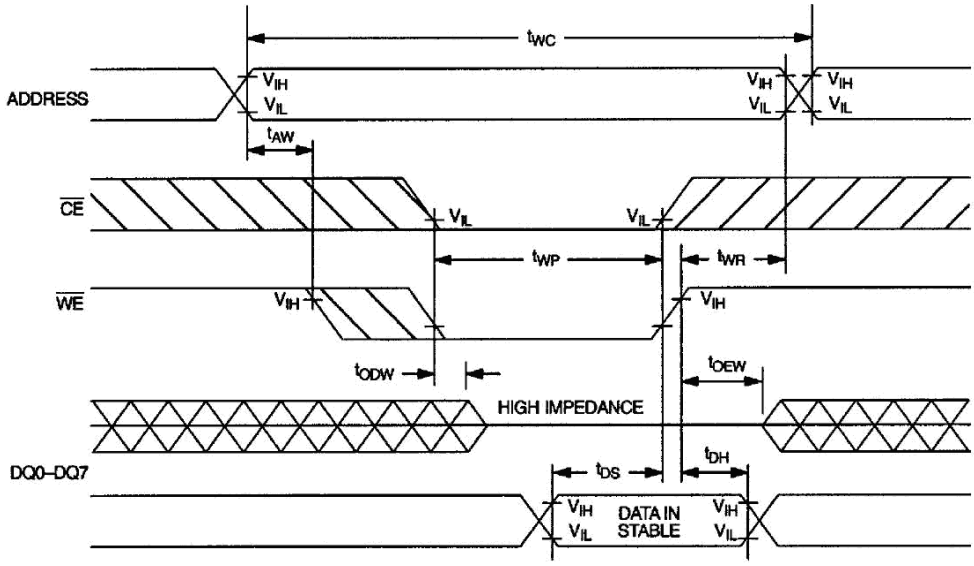
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Expected Data Retention Time | $t_{DR}$ | 10 | | | years | 9 |

Warning: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery-backup mode.

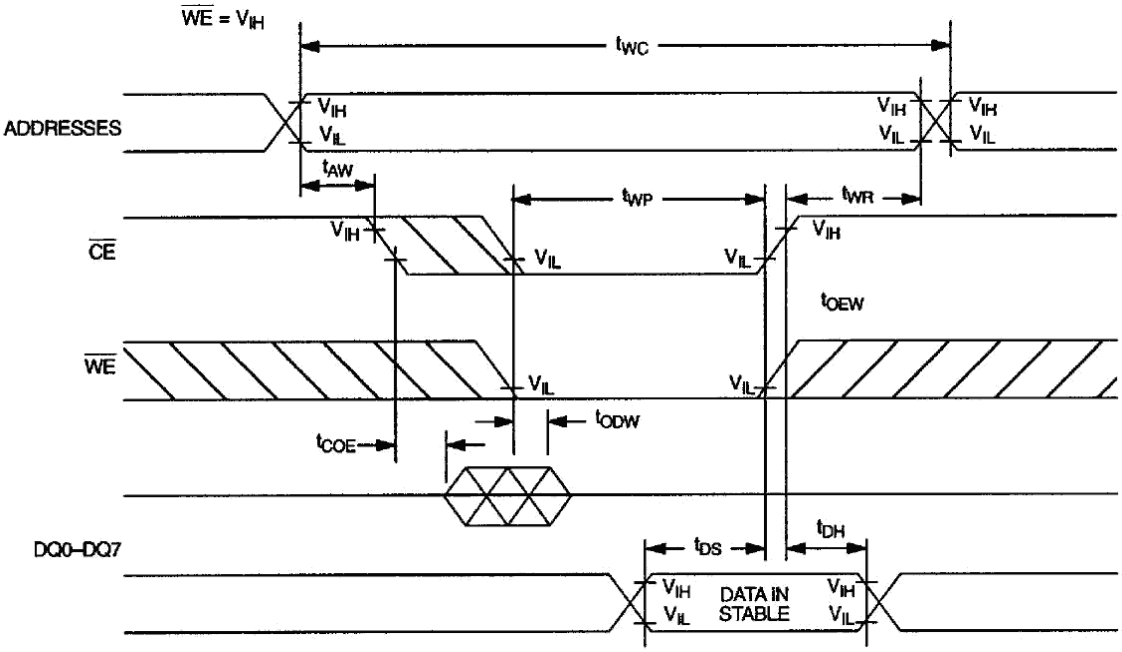
**MEMORY READ CYCLE** (Note 1)



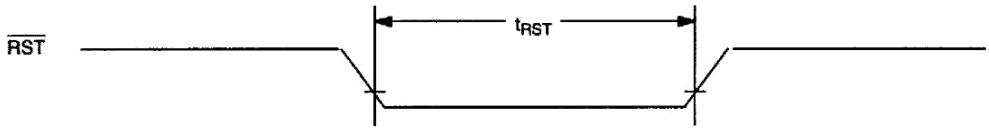

**MEMORY WRITE CYCLE 1 (Notes 2,6, and 7)**



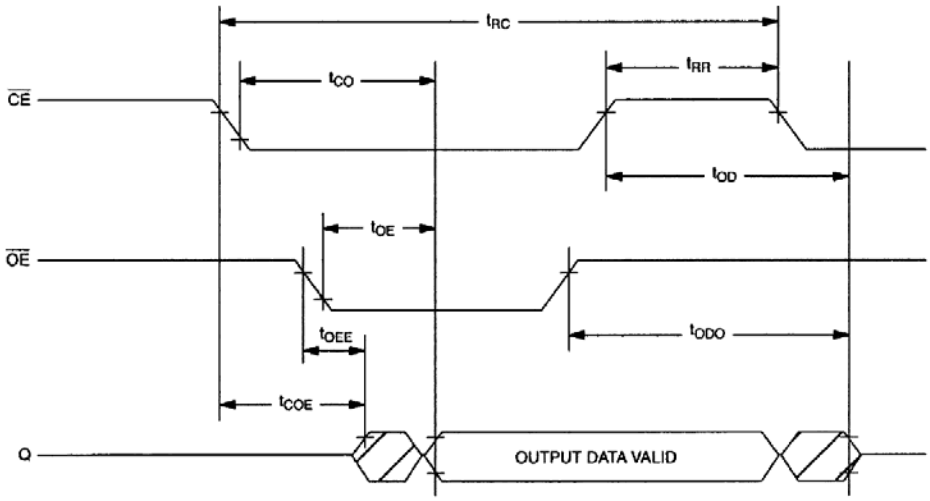
**MEMORY WRITE CYCLE 2 (Notes 2 and 8)**



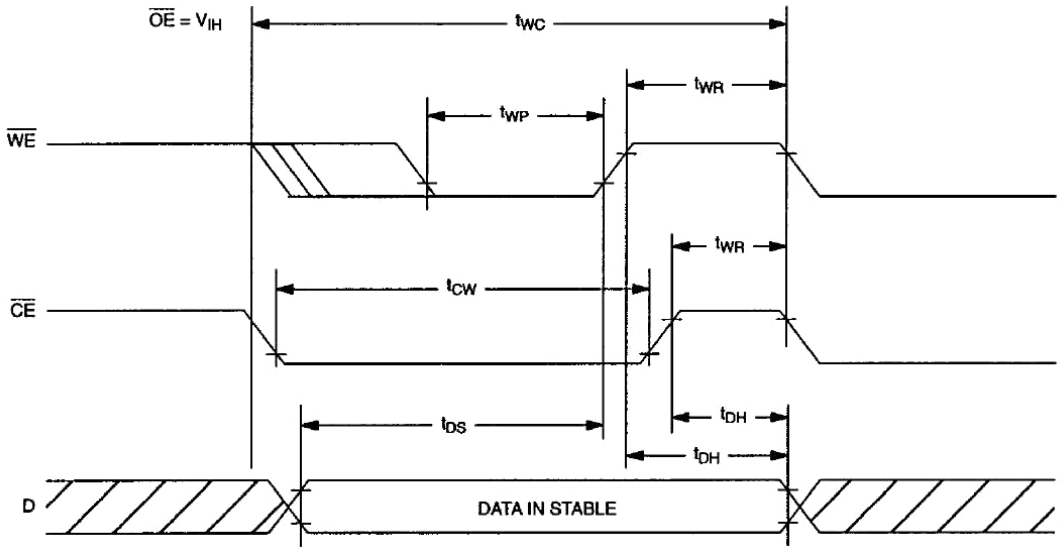

**RESET FOR PHANTOM CLOCK**



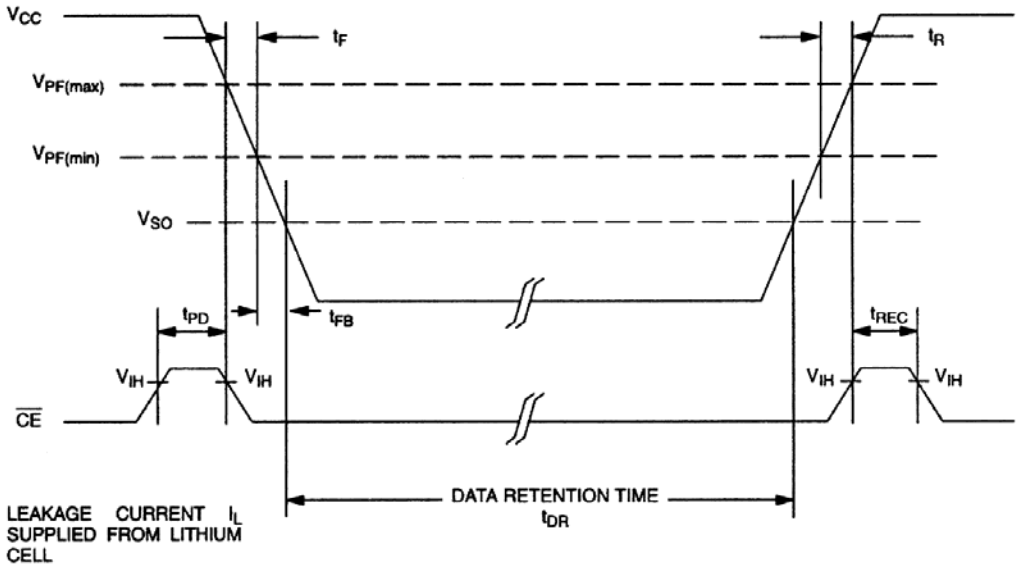

**READ CYCLE TO PHANTOM CLOCK**



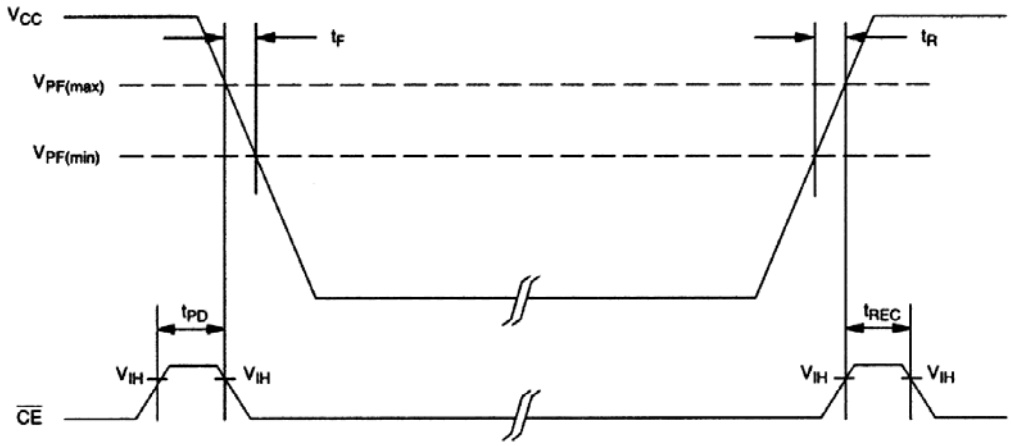
**WRITE CYCLE TO PHANTOM CLOCK**




**POWER-DOWN/POWER-UP CONDITION, 5V**



**POWER-DOWN/POWER-UP CONDITION, 3.3V**




**AC TEST CONDITIONS**

Output Load: 50pF +1TTL Gate

Input Pulse Levels: 0 to 3V

Timing Measurement Reference Levels

Input: 1.5V

Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

**NOTES:**

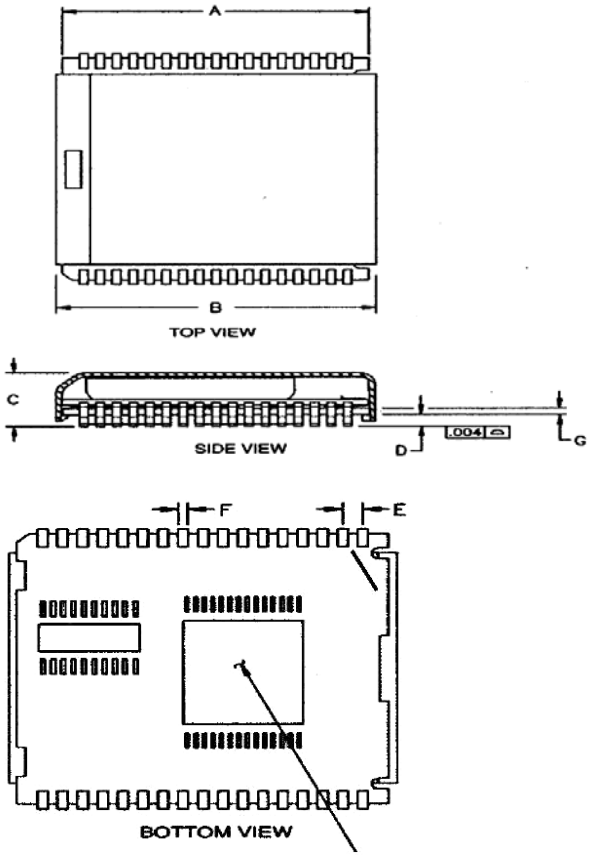
1) $\overline{WE}$ is high for a read cycle.
2) $\overline{OE}$ = $V_{IH}$ or $V_{IL}$. If $\overline{OE}$ = $V_{IH}$ during write cycle, the output buffers remain in a high-impedance state.
3) $t_{WP}$ is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. $t_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4) $t_{DH}$, $t_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5) These parameters are sampled with a 50pF load and are not 100% tested.
6) If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in Write Cycle 1, the output buffers remain in a high-impedance state during this period.
7) If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high-impedance state during this period.
8) If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition the output buffers remain in a high impedance state during this period.
9) The expected $t_{DR}$ is defined as cumulative time in the absence of Vcc with the clock oscillator running.
10) $t_{WR}$ is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.
11) Voltages are referenced to ground.
12) $\overline{RST}$ (Pin 1) has an internal pullup resistor.
13) RTC modules can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85℃. Post solder cleaning with water-washing techniques is acceptable, provided that ultrasonic vibration is not used.

In addition, for the PowerCap:

1) ARTSCHIP Semiconductor recommends that PowerCap module bases experience one pass through solder reflow oriented with the label side up (“live-bug”).
2) Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than three seconds.
   -To solder, apply flux to the pad, heat the lead frame pad, and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows, and use a solder wick to remove solder.

**DS1244P WITH DS9034PCX ATTACHED**

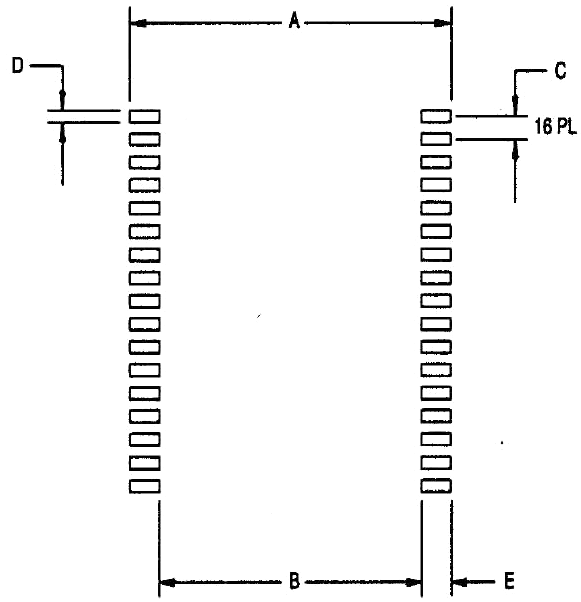
| PKG | INCHES | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.920 | 0.925 | 0.930 |
| B | 0.955 | 0.960 | 0.965 |
| C | 0.240 | 0.245 | 0.250 |
| D | 0.052 | 0.055 | 0.058 |
| E | 0.048 | 0.050 | 0.052 |
| F | 0.015 | 0.020 | 0.025 |
| G | 0.020 | 0.025 | 0.030 |




COMPONENTS AND PLACEMENT MIGHT VARY FROM EACH DEVICE TYPE

**RECOMMENDED POWERCAP MODULE LAND PATTERN**

| PKG | INCHES | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | — | 1.050 | — |
| B | — | 0.826 | — |
| C | — | 0.050 | — |
| D | — | 0.030 | — |
| E | — | 0.112 | — |




Note: ARTSCHIP Semiconductor recommends that PowerCap module bases experience one pass through solder reflow oriented with the label side up (“live-bug”).

Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than three seconds.

To solder, apply flux to the pad, heat the lead frame pad, and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows, and use a solder wick to remove solder.