Z86C93

CMOS Z8® MULT/DIV MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C93 is a CMOS ROMless Z8 microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier, 32-bit/16-bit divider, and three 16-bit counter timers (see Functional Block Diagram). A capture register and a fast decrement mode are also provided. It is offered in 40-pin PDIP, 44-pin PLCC, 44-pin QFP, and 48-pin VQFP packages. The Z86C93 is functionally compatible with the Z86C91, yet it offers a more powerful mathematical capability. In the PDIP package, the Z86C93 is fully pin compatible with the Z86C91. In the PLCC package, the Z86C93 is also pin compatible to the Z86C91, with the addition of four signals (SCLK, /IACK, /SYNC, and /WAIT). The /WAIT signal is only available on the 25 MHz and 33 MHz devices.

The Z86C93 provides up to 16 output address lines permitting an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

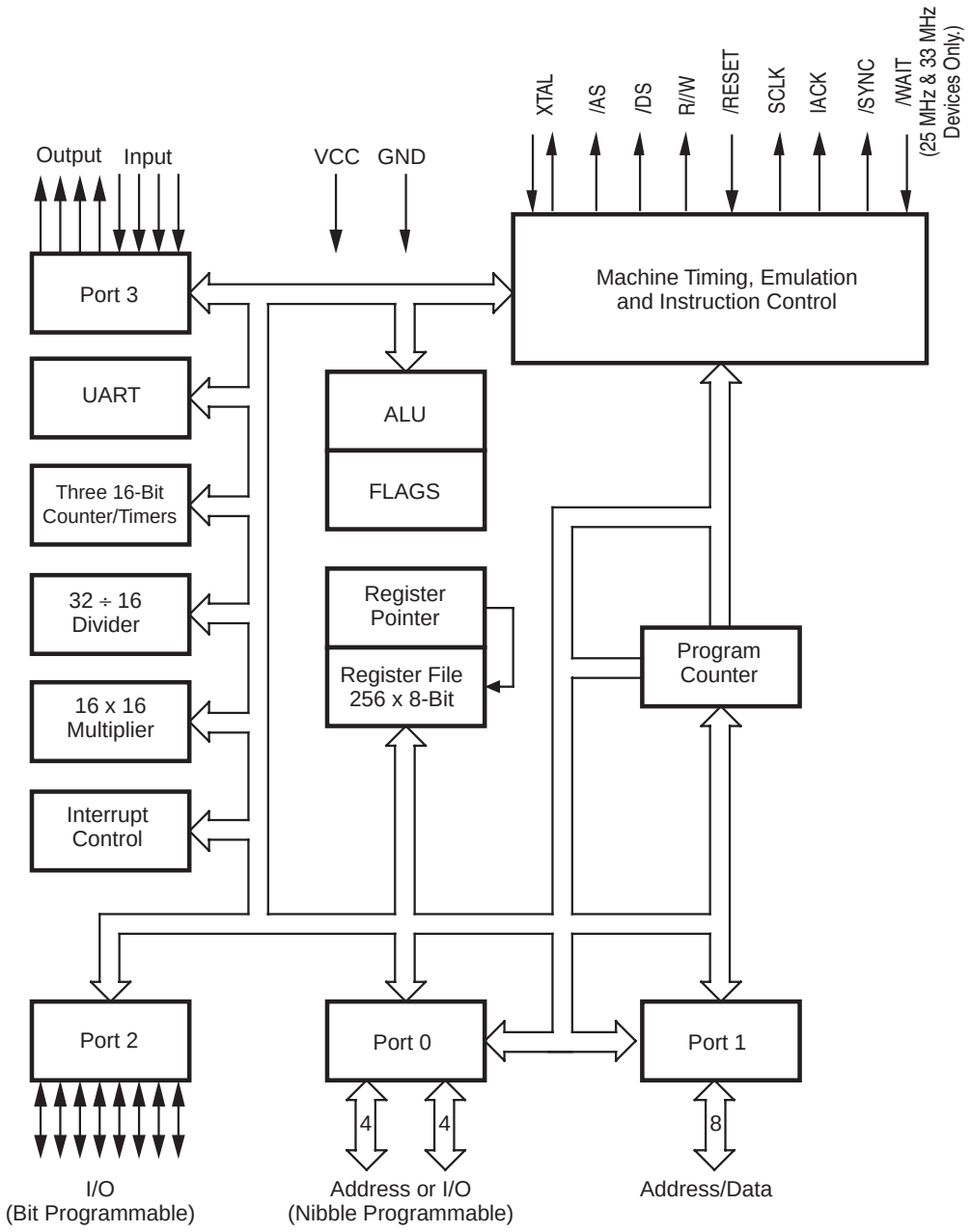
There are 256 registers located on chip and organized as 236 general-purpose registers, 16 control and status registers, one reserved register, and up to three I/O port registers. The register file can be divided into 16 groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. There are an additional 17 registers implemented in the Expanded Register File in Banks D and E. Two of the registers may be used as general-purpose registers, while 15 registers supply the data and control functions for the Multiply/Divide Unit and additional Counter/Timer blocks.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

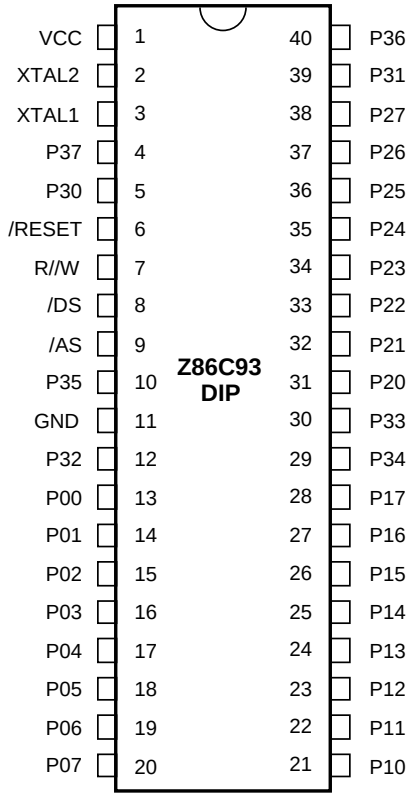
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

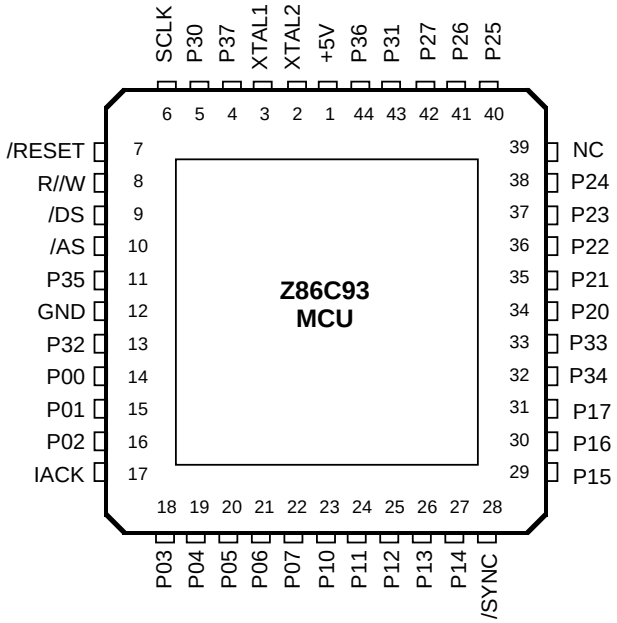


Functional Block Diagram

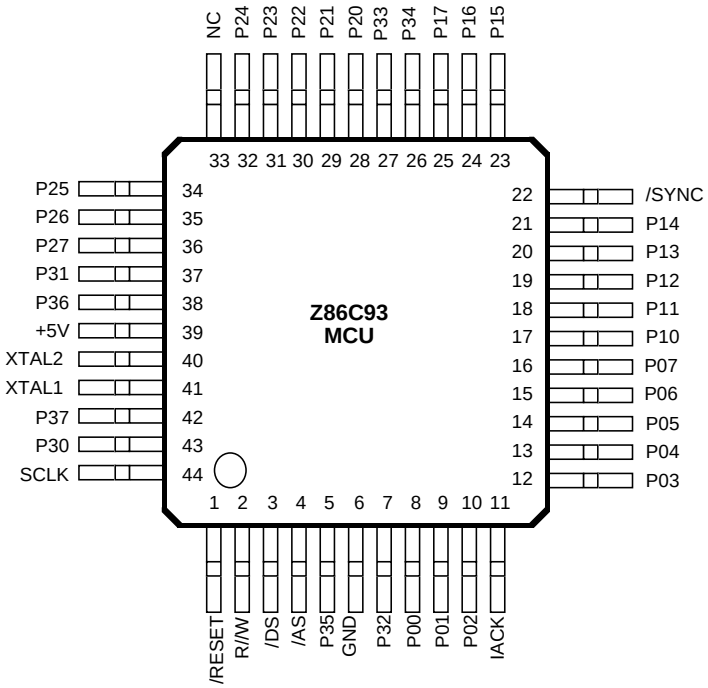
PIN CONFIGURATION



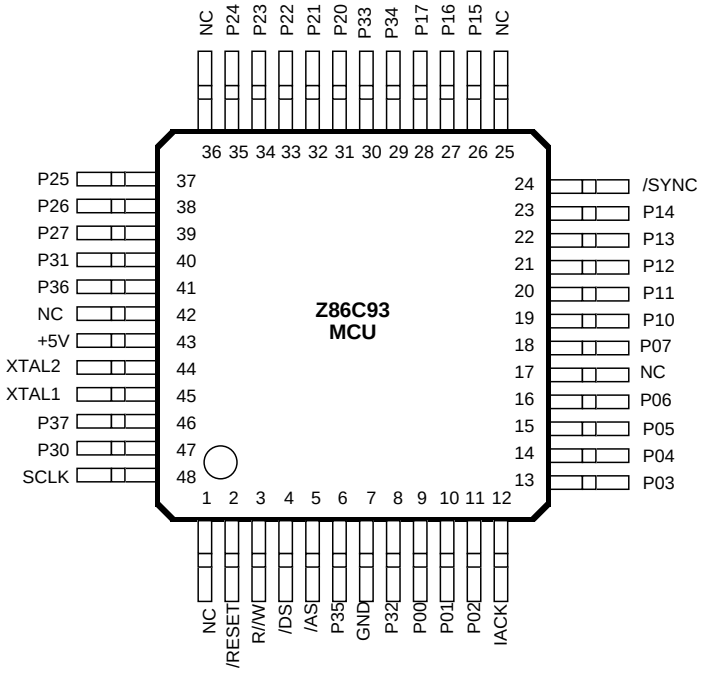
40-Pin DIP Package
(20 MHz)



44-Pin PLCC Package
(20 MHz)

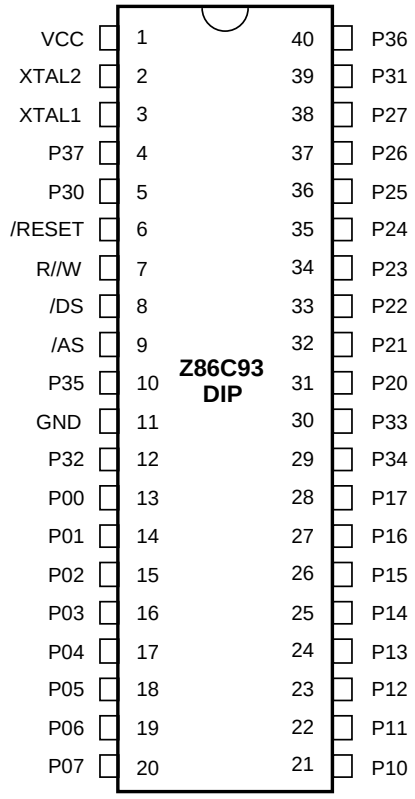


44-Pin QFP Package
(20 MHz)

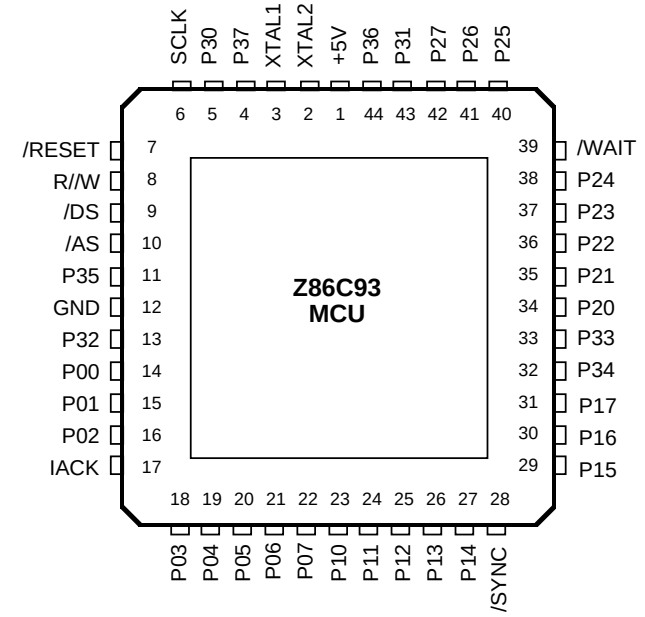


48-Pin VQFP Package
(20 MHz)

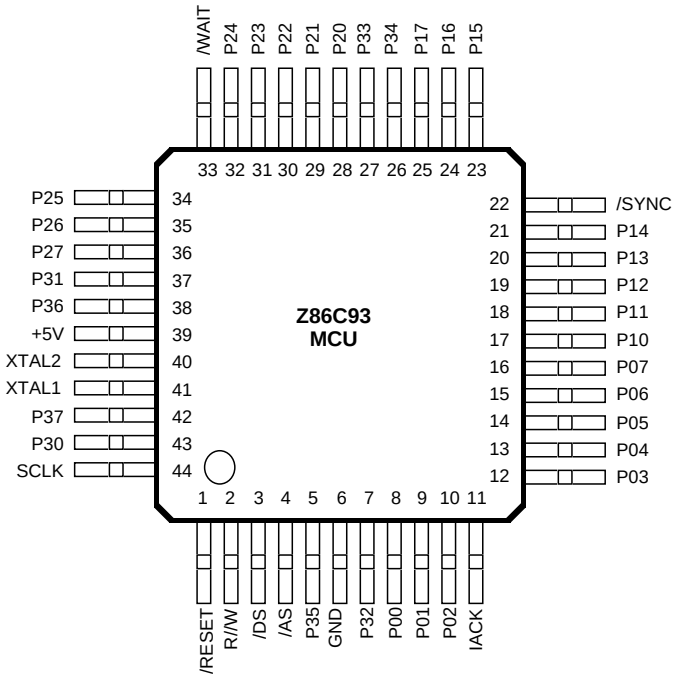
PIN CONFIGURATIONS (Continued)



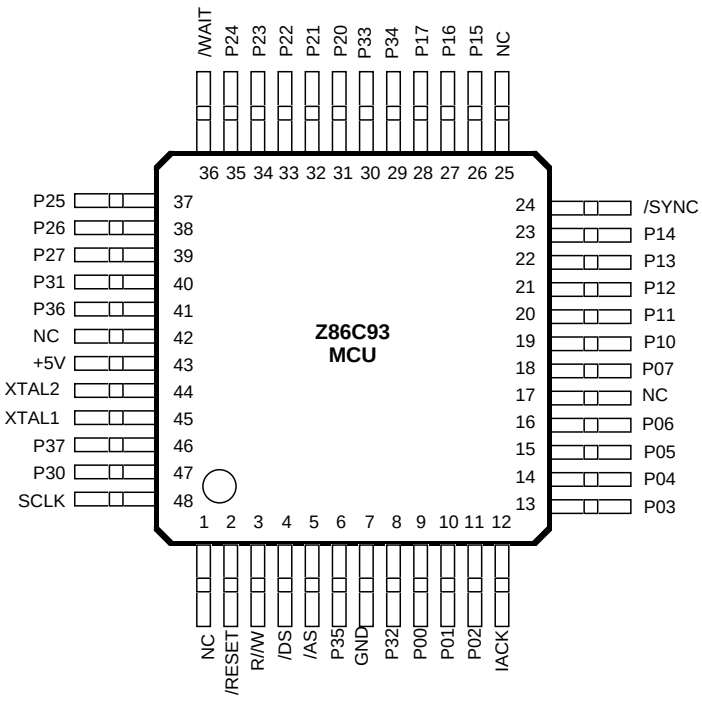
40-Pin DIP Package
(25 MHz and 33 MHz)



44-Pin PLCC Package
(25 MHz and 33 MHz)



44-Pin QFP Package
(25 MHz and 33 MHz)



48-Pin VQFP Package
(25 MHz and 33 MHz)

ABSOLUTE MAXIMUM RATINGS

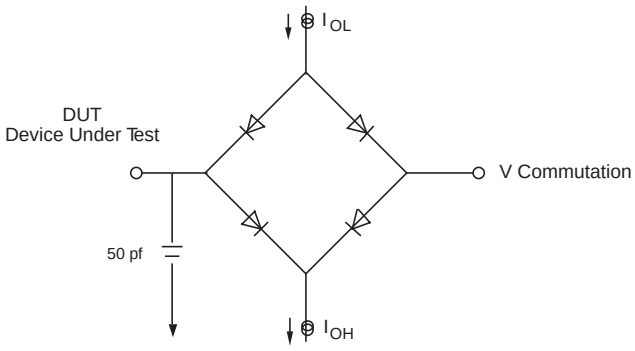
Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†	†	C

* Voltages on all pins with respect to GND.
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram).



Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

VCC = 3.3V ± 10%

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} 250 µA
V_{CH}	Clock Input High Voltage	0.8 V_{CC}	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.03	0.1xV_{CC}		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	0.7xV_{CC}	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.1xV_{CC}		V	
V_{OH}	Output High Voltge	1.8			V	I_{OH}= –1.0 mA
V_{OH}	Output High Voltage	V_{CC} –100mV			V	I_{OH} = –100 µA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +1.0 mA
V_{RH}	Reset Input High Voltage	0.8xV_{CC}	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	-0.03	0.1xV_{CC}		V	
I_{IL}	Input Leakage	–2	2		µA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	–2	2		µA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		–180		µA	V_{RL} = 0V
I_{CC}	Supply Current		30	20	mA	@ 25 MHz [1]
I_{CC1}	Standby Current (HALT Mode)		12	8	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 25 MHz [1]
I_{CC2}	Standby Current (HALT Mode)		8	1	µA	STOP Mode V_{IN} = 0V, V_{CC} [1]
I_{AL}	Auto Latch Current	–10	10	5	µA	

Note:
[1] All inputs driven to 0V, or V_{cc} and outputs floating.

DC ELECTRICAL CHARACTERISTICS

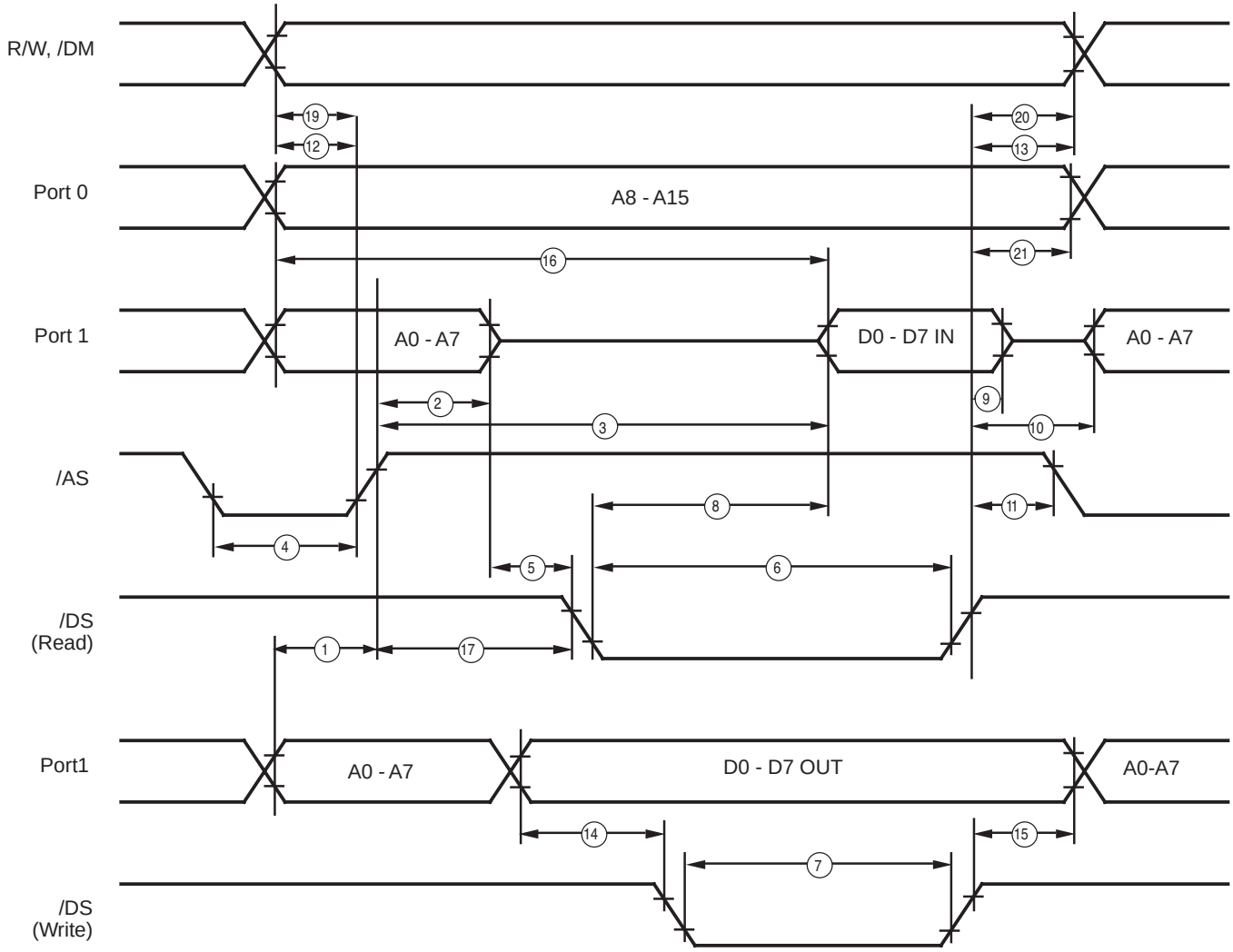
VCC = 5.0V ± 10%

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions
	Max Input Voltage		7		V	I_{IN} 250 µA
V_{CH}	Clock Input High Voltage	3.8	V_{CC}		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	–0.03	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage (P0,P1,P2)	2.0	V_{CC}		V	
V_{IH}	Input High Voltage (P3)	2.2	V_{CC}		V	
V_{IL}	Input Low Voltage	–0.3	0.8		V	
V_{OH}	Output High Voltge	2.4			V	I_{OH}= –2.0 mA
V_{OH}	Output High Voltage	V_{CC} –100mV			V	I_{OH} = –100 µA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +5 mA
V_{RH}	Reset Input High Voltage	3.8	V_{CC}		V	
V_{RI}	Reset Input Low Voltage	–0.03	0.8		V	
I_{IL}	Input Leakage	–2	2		µA	Test at 0V, V_{CC}
I_{OL}	Output Leakage	–2	2		µA	Test at 0V, V_{CC}
I_{IR}	Reset Input Current		–180		µA	V_{RL} = 0V
I_{CC}	Supply Current		55	35	mA	@ 33 MHz [1]
			40	25	mA	@ 25 MHz [1]
			30	20	mA	@ 20 MHz [1]
I_{CC1}	Standby Current (HALT Mode)		20	15	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 33 MHz [1]
			15	9	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 25 MHz [1]
			12	7	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 20 MHz [1]
I_{CC2}	Standby Current		10	1	µA	STOP Mode V_{IN} = 0V, V_{CC} [1]
I_{AL}	Auto Latch Current	–16	16	5	µA	

Note:
[1] All inputs driven to 0V, or V_{cc} and outputs floating.

AC CHARACTERISTICS

External Memory Read/Write Timing Diagram



External Memory Read/Write Timing

AC CHARACTERISTICS

External I/O or Memory Read and Write; DSR/DSW; WAIT Timing Table

			T_A = 0°C to +70°C						
			33 MHz		25 MHz		20 MHz		
No	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
1	TdA(AS)	Address Valid To /AS Rise Delay	15		22		26		ns
2	ThAS(A)	/AS Rise To Address Hold Time	20		25		28		ns
3	TdAS(DI)	/AS Rise To Data In Req'd Valid Delay		96	130		160		ns
4	TwAS	/AS Low Width	15		28		36		ns
5	TdAZ(DSR)	Address Float To /DS Fall (Read)	0		0		0		ns
6	TwDSR	/DS (Read) Low Width	65		100		130		ns
7	TwDSW	/DS (Write) Low Width	40		65		75		ns
8	TdDSR(DI)	/DS Fall (Read) To Data in Req'd Valid Delay		55		85		100	ns
9	ThDSR(DI)	/DS Rise (Read) to Data In Hold Time	0		0		0		ns
10	TdDS(A)	/DS Rise To Address Active Delay	25		40		48		ns
11	TdDS(AS)	/DS Rise To /AS Delay	16		30		36		ns
12	TdR/W(AS)	R/W Valid To /AS Rise Delay	12		26		32		ns
13	TdDS(R/W)	/DS Rise To R/W Not Valid Delay	12		30		36		ns
14	TdDO(DSW)	Data Out To /DS Fall (Write) Delay	12		34		40		ns
15	ThDSW(DO)	/DS Rise (Write) To Data Out Hold Time	12		34		40		ns
16	TdA(DI)	Address Valid To Data In Req'd Valid Delay		115		160		200	ns
17	TdAS(DSR)	/AS Rise To /DS Fall (Read) Delay	30		40		48		ns
19	TdDM(AS)	/DM Valid To /AS Rise Delay	15		22		26		ns
20	TdDS(DM)	/DS Rise To /DM Valid Delay	15		34*				ns
21	ThDS(A)	/DS Rise To Address Valid Hold Time		35					ns
22	TdXT(SCR)	XTAL Falling to SCLK Rising**		35					ns
23	TdXT(SCF)	XTAL Falling to SCLK Falling**		45					ns
24	TdXT(DSRF)	XTAL Falling to/DS Read Falling**		35					ns
25	TdXT(DSRR)	XTAL Falling to /DS Read Rising**		35					ns
26	TdXT(DSWF)	XTAL Falling to /DS Write Falling**		45					ns
27	TdXT(DSWF)	XTAL Falling to /DS Write Rising**		35					ns
28	TsW(XT)	Wait Set-up Time	5		10*				ns
29	ThW(XT)	Wait Hold Time	15		15*				ns
30	TwW	Wait Width (One Wait Time)	20		25*				ns

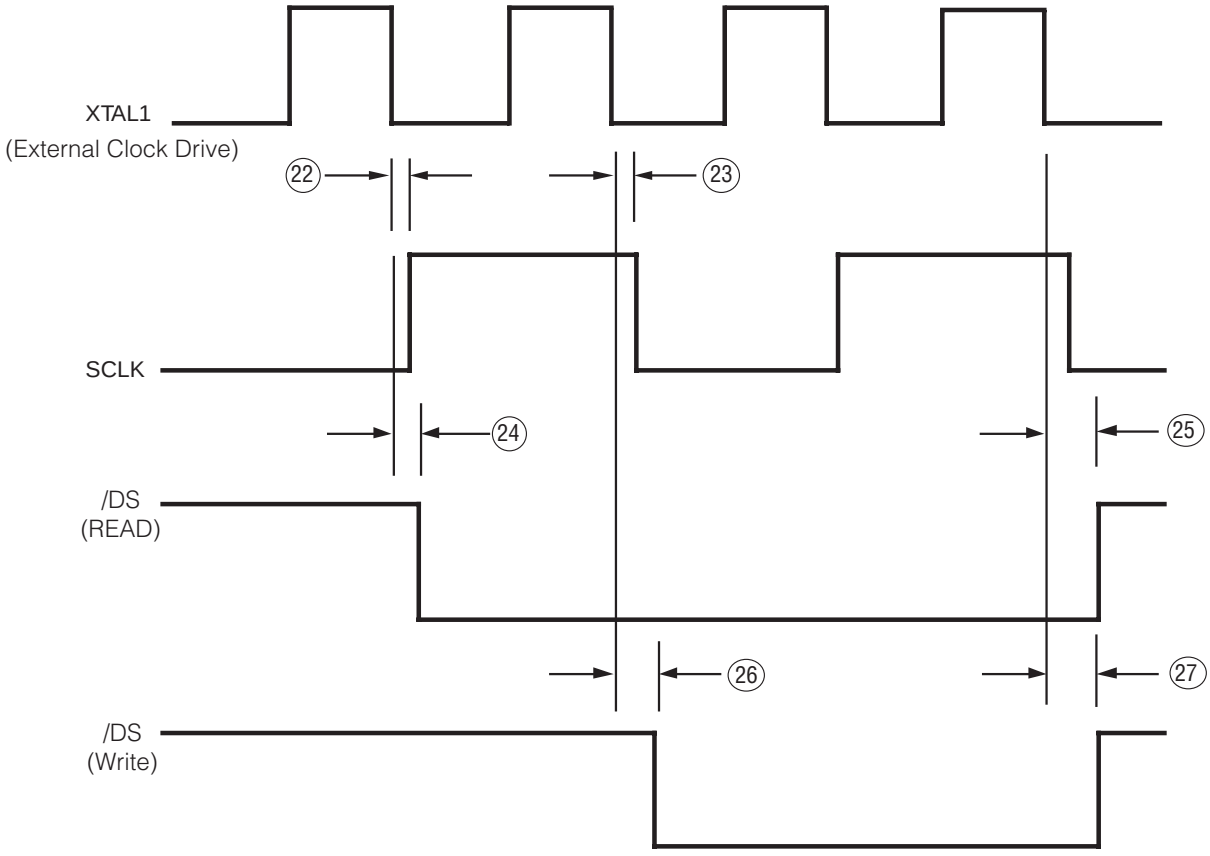
Notes:

When using extended memory timing add 2 TpC.

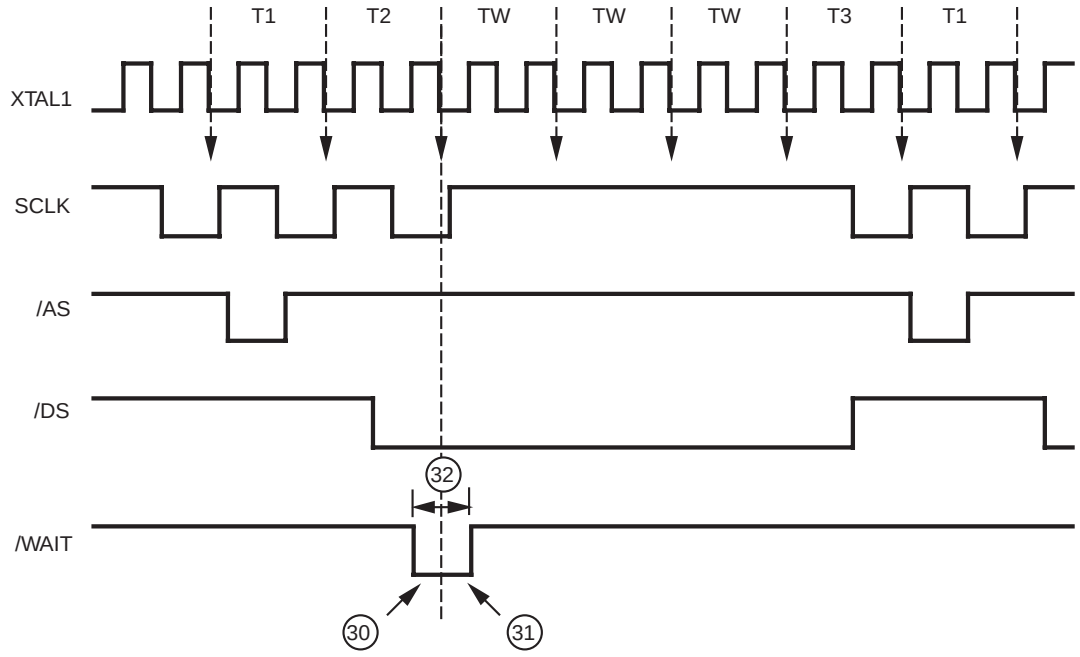
Timing numbers given are for minimum TpC.

* Typical value to be characterized (25 MHz).

** External clock drive.

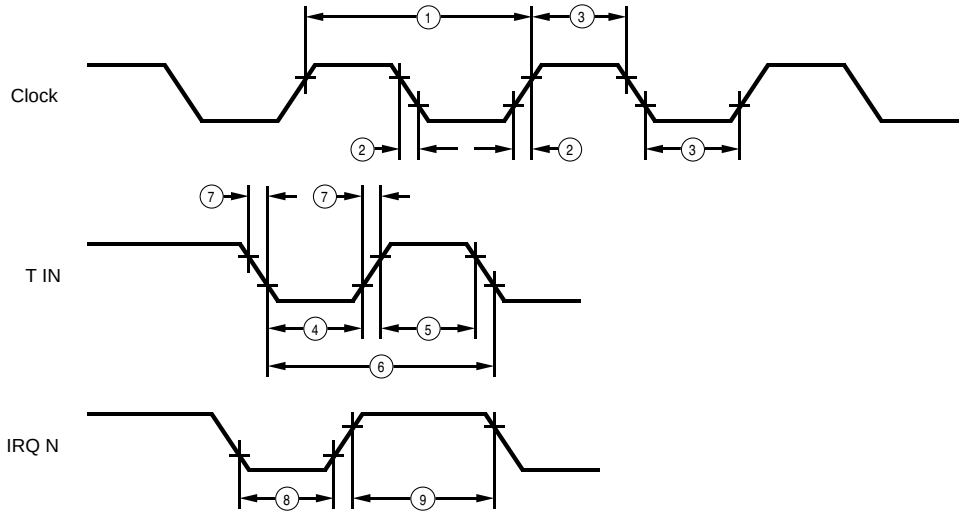


XTAL/SCLK To DSR and DSW Timing



XTAL/SCLK To WAIT Timing
(25 MHz and 33 MHz Devices Only)

AC CHARACTERISTICS
Additional Timing Diagram



Additional Timing

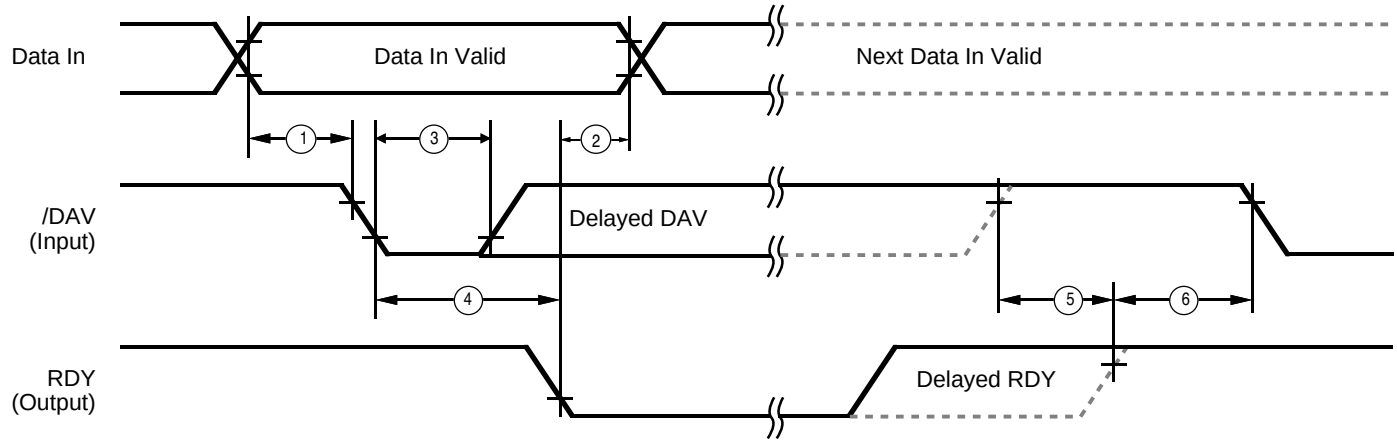
AC CHARACTERISTICS
Additional Timing Table

			T_A = 0°C to +70°C							
			33 MHz		25 MHz		20 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	30	1000	42	1000	50	1000	ns	[1]
2	TrC,TfC	Clock Imput Rise & Fall Times		5		10		10	ns	[1]
3	TwC	Input Clock Width	10		11		15		ns	[1]
4	TwTinL	Timer Input Low Width	75		75		75		ns	[2]
5	TwTinH	Timer Input High Width	3 TpC		3 TpC		3 TpC			[2]
6	TpTin	Timer Input Period	8 TpC		8 TpC		8 TpC			[2]
7	TrTin,TfTin	Timer Input Rise & Fall Times	100		100		100		ns	[2]
8A	TwIL	Interrupt Request Input Low Times	70		70		70		ns	[2,4]
8B	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		5 TpC			[2,5]
9	TwIH	Interrupt Request Input High Times	3 TpC		3 TpC		3 TpC			[2,3]

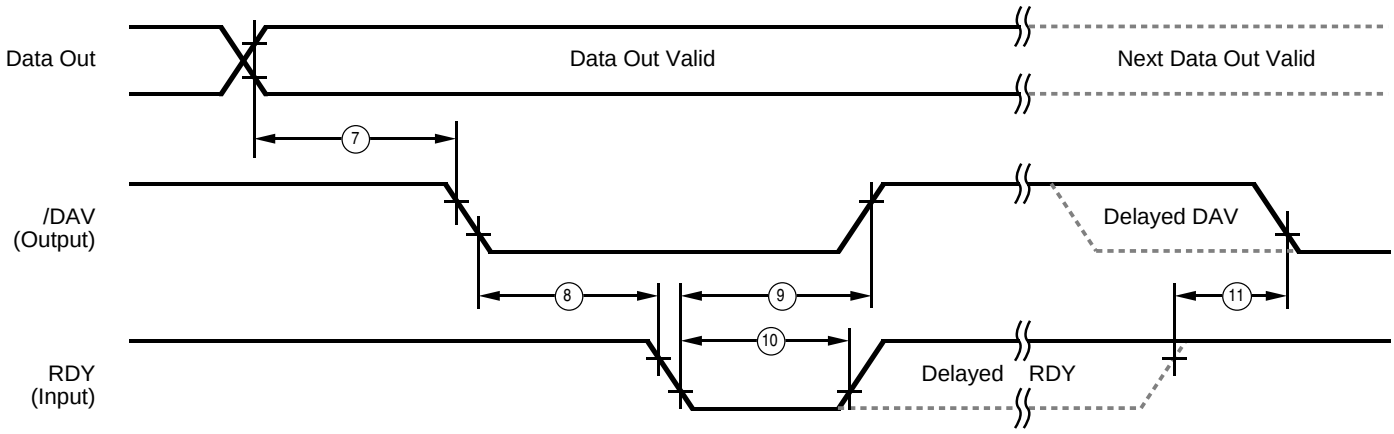
Notes:
[1] Clock timing references use 3.8V for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request via Port 3 (P33-P31)`.
[5] Interrupt request via Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams



Input Handshake Timing



Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing Table

No	Symbol	Parameter	T_A = 0°C to +70°C Min	Max	Units	Data Direction
1	TsDI(DAV)	Data In Setup Time to /DAV	0		ns	In
2	ThDI(DAV)	RDY to Data In Hold Time	0		ns	In
3	TwDAV	/DAV Width	40		ns	In
4	TdDAVIf(RDYf)	/DAV to RDY Delay		70	ns	In
5	TdDAVIr(RDYr)	DAV Rise to RDY Wait Time		40	ns	In
6	TdRDYOr(DAVIf)	RDY Rise to DAV Delay	0		ns	In
7	TdDO(DAV)	Data Out to DAV Delay		TpC	ns	Out
8	TdDAVOf(RDYIf)	/DAV to RDY Delay	0		ns	Out
9	TdRDYIf(DAVOr)	RDY to /DAV Rise Delay		70	ns	Out
10	TwRDY	RDY Width	40		ns	Out
11	TdRDYIr(DAVOf)	RDY Rise to DAV Wait Time		40	ns	Out

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