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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4501C - Preliminary

Video Front End

Features

- DC restore and sync separator
- Wideband (100MHz) DC restore
- Advanced sync separator
- Programmable data slicer
- Single 5 volt operation
- Differential Gain = 0.1%
- Differential Phase = 0.1°
- Low power (<75mW)

Applications

- Video Capture & Editing
- Video Projectors
- Set Top Boxes
- Security Video
- Embedded data recovery

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4501CS	-40°C to +85°C	24-Pin SOIC	MDP0027
EL4501CU	-40°C to +85°C	24-Pin QSOP	MDP0031

General Description

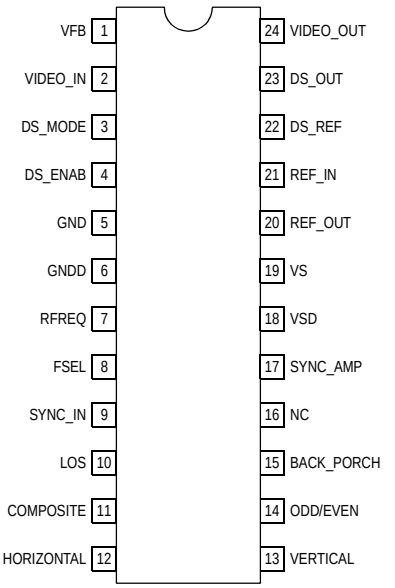
The EL4501C Video Front End (VFE) is an integrated solution that provides the key analog signal conditioning functions for analog video signals. It forms the front end interface for either an analog or analog/digital video system. The VFE contains a high bandwidth DC Restore, a sophisticated Sync Separator, and a Data Slicer for embedded data recovery.

The VFE will perform the restoration of the DC reference level (blanking level) and the extraction of all of the necessary timing signals needed for synchronization and control. The sync separator is designed for very good noise immunity by incorporating a signal qualification scheme and internal brick wall filter. A data slicer is also included to help decode data embedded in the active video or VBI areas of the signal.

The VFE operates from a single 5 volt supply and is available in a small 24 pin QSOP package that takes only $0.08in^2(54mm^2)$ of board area, as well as a standard 24 pin SOIC.

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Connection Diagram



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Absolute Maximum Ratings (T_A = 25°C)

Values beyond absolute maximum ratings can cause the device to be prematurely damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V_S to GND)	+6V
Input Voltage	GND - 0.3V, V_S +0.3V
Storage Temperature Range	-65°C to +150°C
Ambient Operating Temperature	-40°C to +85°C
Operating Junction Temperature	125°C
Power Dissipation	See Curves

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$.

Electrical Characteristics

V_S = +5V, GND = 0V, T_A = 25°C, Input Video = 1V_{P-P} unless otherwise specified.

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_S	Supply Current	No Load, V_{IN} = 0V			20	mA
Video Amplifier Section						
V_{OP}	Positive Output Voltage Swing	R_L = 150Ω to $V_{S/2}$	4.70	4.85		V
		R_L = 150Ω to GND	4.20	4.60		V
		R_L = 1k to $V_{S/2}$	4.95	4.97		V
V_{ON}	Negative Output Voltage Swing	R_L = 150Ω to $V_{S/2}$		0.15	0.30	V
		R_L = 150Ω to GND		0		V
		R_L = 1k to $V_{S/2}$		0.03	0.05	V
$+I_{OUT}$	Positive Output Current	RL = 10Ω to $V_{S/2}$	60	80	120	mA
$-I_{OUT}$	Negative Output Current	RL = 10Ω to $V_{S/2}$	-50	-60	-80	mA
dG	Differential Gain Error [1]	Standard NTSC test, A_V = 2, R_L = 150Ω		0.1		%
dP	Differential Phase Error [1]	Standard NTSC test, A_V = 2, R_L = 150Ω		0.1		°
BW	Bandwidth	-3dB, G = 1, RL = 10kΩ to GND		100		MHz
		-3dB, G = 1, RL = 150Ω to GND		60		MHz
BW1	Bandwidth	+/-0.1dB, G = 2, RL = 150Ω to GND		8		MHz
SR	Slew Rate	25% to 75%, 3.5V_{P-P}, R_L = 150Ω	150	200		V/µs
V_{RL}	Ref Level Range		0		3.5	V
ts	Settling Time	to 0.1%, V_{IN} = 0V to 3V		35		ns
R_{IN}	Input Resistance (VIDEO_IN)		90	115	140	kΩ
C_{IN}	Input Capacitance (VIDEO_IN)			1.5		pF
A_{VOL}	Open Loop Voltage Gain	R_L = no load, V_{OUT} = 0.5V to 3V	54	65		dB
		R_L = 150Ω to GND, V_{OUT} = 0.5V to 3V	40	50		dB
DC Restore Section						
CMIR	Common Mode Input Range (REF_IN)	CMRR ≥ TBD dB	0		3.5	V
V_{OS}	Input Offset Voltage	DC restored	-20		+20	mV
TCV_{OS}	Input Offset Voltage Temperature Coefficient			10		µV/°C
I_B	Input Bias Current (REF_IN)	V_{CM} = 0V to 3.5V		1	100	nA
Data Slicer Section						
I_{IH}	Input High Current (DS_MODE & DS_ENAB)	V_{IH} = 5V		4	6	µA
I_{IL}	Input Low Current (DS_MODE & DS_ENAB)	V_{IL} = 0V		1	100	nA
V_{IH}	Input High Voltage (DS_MODE & DS_ENAB)		4.5			V
V_{IL}	Input Low Voltage (DS_MODE & DS_ENAB)				0.5	V
V_{OH}	Output High Voltage (DS_OUT)	I_{OUT} = -1mA	4.75	4.9		V
V_{OL}	Output Low Voltage (DS_OUT)	I_{OUT} = 1mA		0.1	0.25	V
I_{OUT}	Short Circuit Current (DS_OUT)	R_L = 10Ω to 2.5V	15	20		mA

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Electrical Characteristics

V_S = +5V, GND = 0V, T_A = 25°C, Input Video = $1V_{P-P}$ unless otherwise specified.

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_B	Input Bias Current (DS_REF)	DS_REF = 0V & 5V	-100	1	100	nA
Vos	Input Offset Voltage		-20		+20	mV
V_{HYS}	Hysteresis			10	15	mV
t_{PD}	Propagation Delay	50% to 50%		18	28	ns
$t_{R/F}$	Rise/Fall Time	10% to 90%, RL = 150k, CL = 5pF		1.2	1.8	ns
Sync Separator Section						
V_{OH}	Output High Voltage	I_{OH} = -1.6mA	4.6			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA			0.4	V
V_{THSRH}	Slicing Level		45	50	55	%
T_{CD}	Composite Sync Delay	With Filter	TBD		TBD	
T_{CD}	Composite Sync Delay	Without Filter	TBD		TBD	
V_{SR}	Sync In Reference Level			1.5		V
R_{INSR}	Sync Reference Input Impedance			90		kΩ
V_{RANGE}	Input Dynamic Range		0.5		2.0	Vp-p
t_{CD}	Comp Sync Delay	From 50% point of leading edge of sync	50	75	100	ns
t_{BD}	Back Porch Delay	From 50% point of trailing edge of sync	340	430	520	ns
t_{BW}	Back Porch Width		2.7	3.0	3.3	µs
t_{HD}	Horiz Sync Delay	From 50% point of leading edge of sync	350	450	550	ns
t_{HW}	Horiz Sync Width		3.7	4.7	5.7	µs
t_{VW}	Vert Sync Width	Serrations	185	195	205	µs
t_{VDD}	Vert Sync Default Delay	No serrations	51	63.5	76	µs
f_H	Horiz Scan Rate	R_{FREQ} = xx to yy kΩ	15		130	kHz
V_{LOS}	LOS Detect Threshold	Compared to Sync Tip Amplitude		72		mV
t_{JIT}	Output Jitter	All sync separator outputs			5	ns
Reference Section						
VREF	Reference Output Voltage (REF_OUT)	I_{OUT} = +2mA to -0.5mA	1.2	1.3	1.4	V

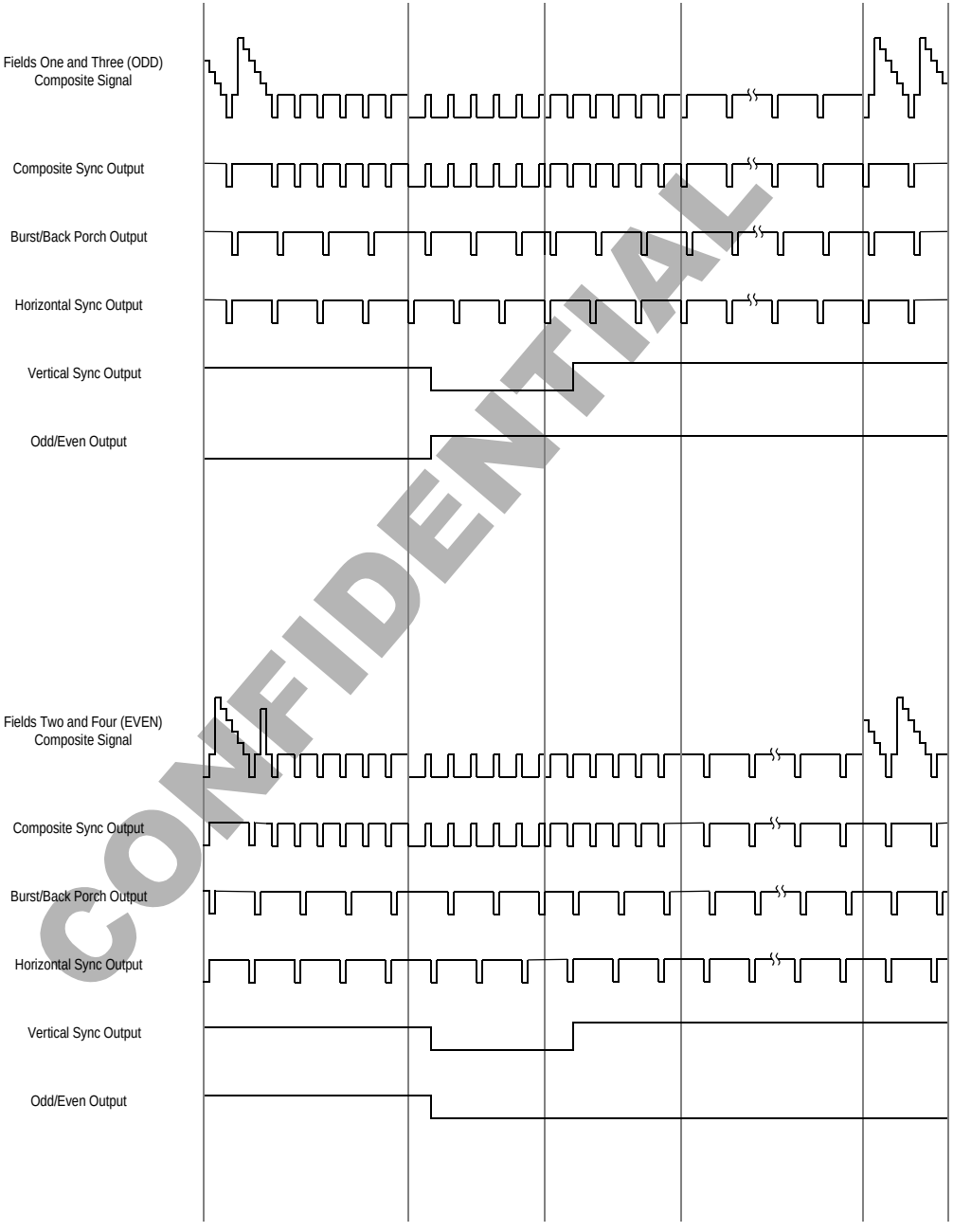
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Typical Performance Curves

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Timing Diagrams

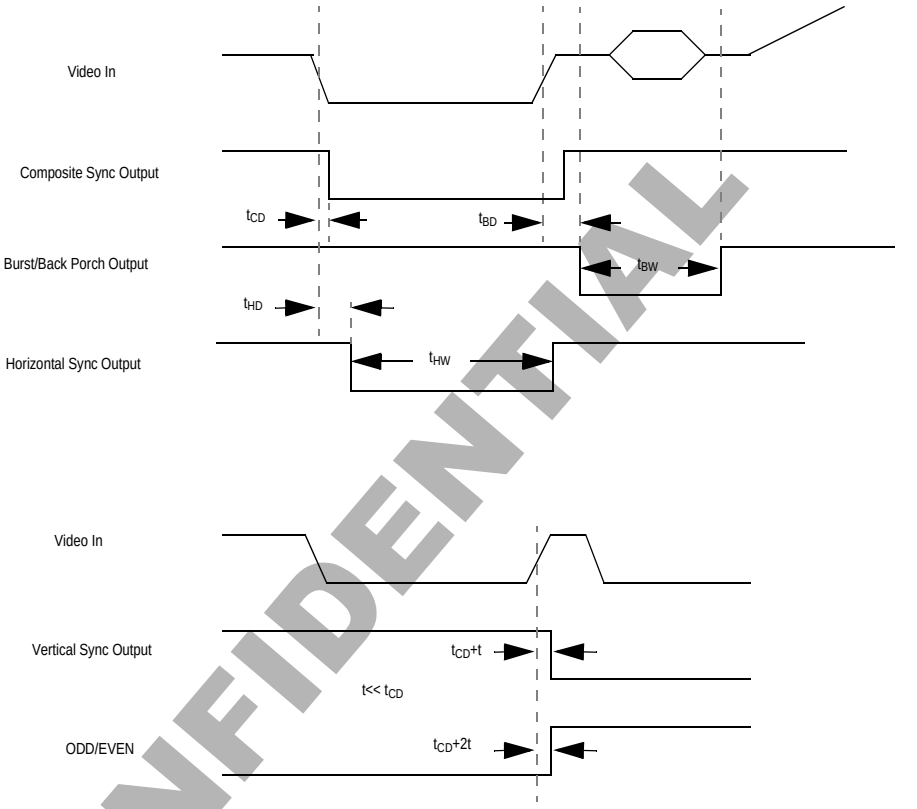


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Timing Diagrams (cont.)



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Pin Description

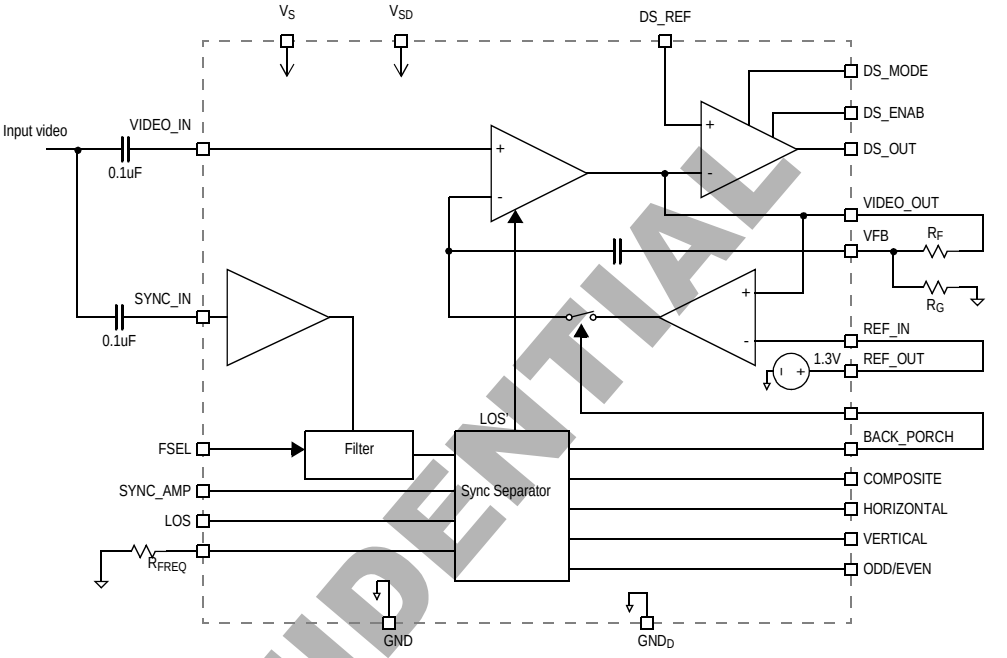
Pin Number	Pin Name	Pin Type	Pin Description
1	VFB	Input	Connection for gain and feedback resistors, R_F and R_G.
2	VIDEO_IN	Input	Input to DC restore amplifier. Input coupling capacitor connects from here to video source.
3	DS_MODE	Input	Sets the mode of the DS comparator. Logic high selects a standard logic output. Logic low selects an open drain/collector.
4	DS_ENAB	Input	Enables the output of the comparator. A logic high enables the comparator. A logic low tri-states it.
5	GND	Input	Analog ground.
6	GND_D	Input	Digital ground
7	R_{FREQ}	Input	Connection for bias resistor that sets the overall timing.
8	FSEL	Input	Enable/ bypass internal brick wall filter. A logic high is used to enable the filter, a logic low to disable it.
9	SYNC_IN	Input	Input to the sync separator. Connects to the video source via a coupling capacitor, or to a color burst input filter.
10	LOS	Output	Loss of signal output. Goes high if no input video signal is detected.
11	COMPOSITE	Output	Composite sync output.
12	HORIZONTAL	Output	Horizontal sync output.
13	VERTICAL	Output	Vertical sync output.
14	ODD/EVEN	Output	Odd/Even field indicator output.
15	BACK_PORCH	Output	Back porch output.
17	SYNC_AMP	Output	Amplitude of sync tip. Can be used to control AGC circuit.
18	V_{SD}	Input	Digital power supply. Nominally +5V
19	V_S	Input	Analog power supply. Nominally +5V.
20	REF-OUT	Output	Voltage reference for use as blanking level in low cost system
21	REF_IN	Input	Dc voltage on this pin sets the DC restore voltage and output blanking level.
22	DS_REF	Input	Sets the slicing level or reference level for the comparator.
23	DS_OUT	Output	Output of the data slicing comparator. The output is either open drain/collector or standard symmetrical logic depending on the DS_MODE pin.
24	VIDEO_OUT	Output	Output of DC restore amplifier.

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Block Diagram



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Description of Operation

The EL4501C incorporates the following functional blocks:

- DC restore amplifier
- Advanced sync separator
- Data Slicer

Combined they provide the key analog processing functions for a number of video system applications. The operation of each of these blocks is described below.

Sync Separator

The sync separator contained in the EL4501C has been designed to be compatible with a wide range of video signal standards, operating with horizontal line rates from PAL/NTSC rates up to 150kHz. The sync separator also includes a qualification scheme which rejects noise pulses and other video artifacts. The horizontal line rate timing is controlled with the use of a resistor, R_{FREQ}.

The following outputs are available:

- Composite sync
- Horizontal sync
- Vertical sync
- Burst gate
- Odd/Even field identification
- Loss of signal detected
- Sync amplitude detected

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General Disclaimer

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