# HM624100HC Series

4M High Speed SRAM (1-Mword × 4-bit)

HITACHI

ADE-203-1198 (Z)
Preliminary
Rev. 0.0
Nov. 30, 2000

## Description

The HM624100HC is a 4-Mbit high speed static RAM organized 1-Mword × 4-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed and high density memory, such as cache and buffer memory in system. The HM624100HC is packaged in 400-mil 32-pin SOJ for high density surface mounting.

## Features

- Single 5.0 V supply : 5.0 V ± 10 %
- Access time 10 ns (max)
- Completely static memory
  - — No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
  - — All inputs and outputs
- Operating current : 140 mA (max)
- TTL standby current : 40 mA (max)
- CMOS standby ccurrent : 5 mA (max)
  : 1.2 mA (max) (L-version)
- Data retension current : 0.8 mA (max) (L-version)
- Data retension voltage : 2.0 V (min) (L-version)
- Center $V_{CC}$ and $V_{SS}$ type pinout

Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.

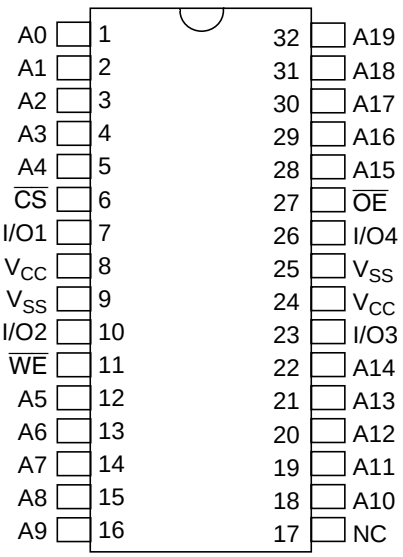
Hitachi semiconductor

## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM624100HCJP-10 | 10 ns | 400-mil 32-pin plastic SOJ (CP-32DB) |
| HM624100HCLJP-10 | 10 ns | |

## Pin Arrangement

32-pin SOJ

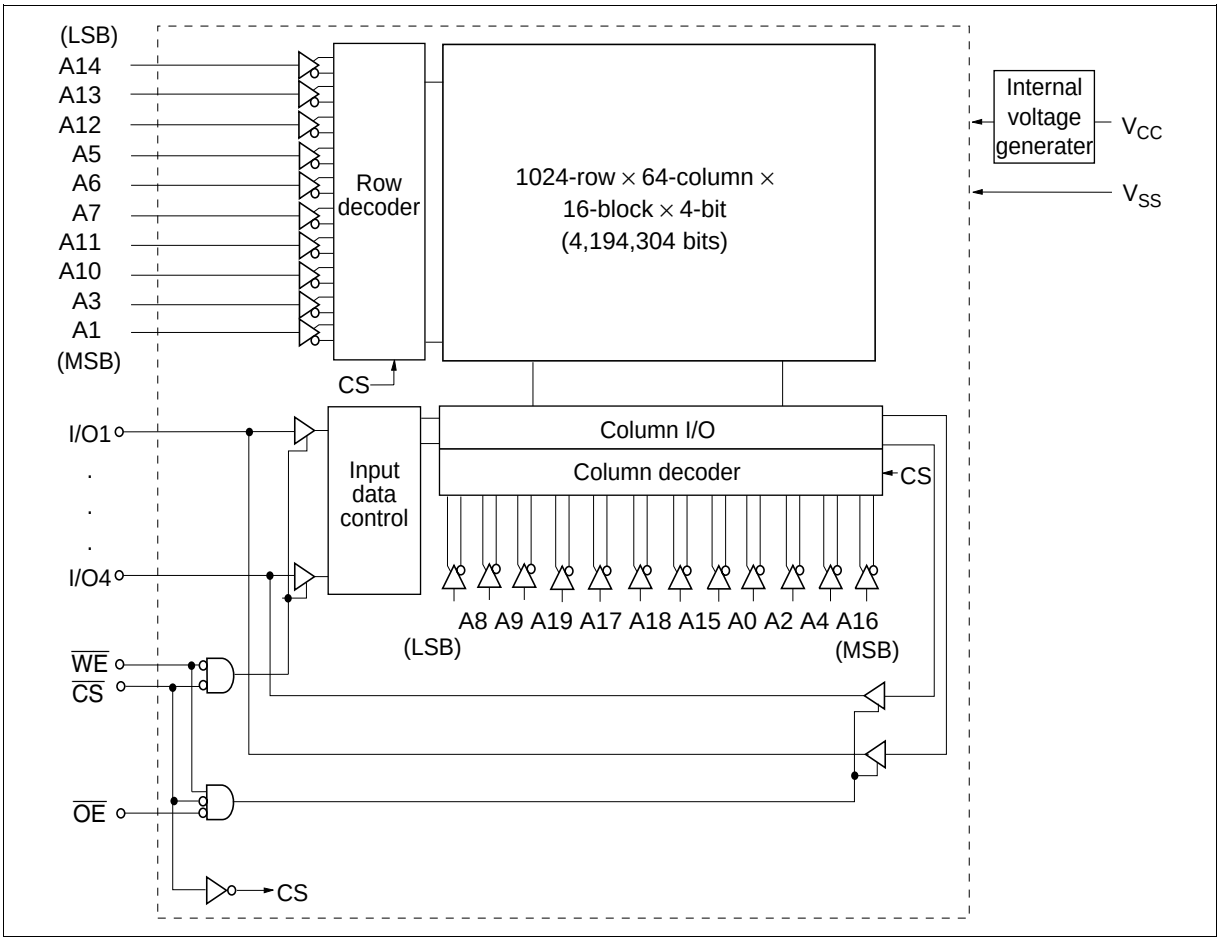



(Top view)

## Pin Description

| Pin name | Function |
|---|---|
| A0 to A19 | Address input |
| I/O1 to I/O4 | Data input/output |
| $\overline{CS}$ | Chip select |
| $\overline{OE}$ | Output enable |
| $\overline{WE}$ | Write enable |
| $V_{CC}$ | Power supply |
| $V_{SS}$ | Ground |
| NC | No connection |

## Block Diagram



## Operation Table

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | $V_{CC}$ current | I/O | Ref. cycle |
|---|---|---|---|---|---|---|
| H | × | × | Standby | $I_{SB}$, $I_{SB1}$ | High-Z | — |
| L | H | H | Output disable | $I_{CC}$ | High-Z | — |
| L | L | H | Read | $I_{CC}$ | Dout | Read cycle (1) to (3) |
| L | H | L | Write | $I_{CC}$ | Din | Write cycle (1) |
| L | L | L | Write | $I_{CC}$ | Din | Write cycle (2) |

Note: ×: H or L

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +7.0 | V |
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | –0.5*[1] to $V_{CC}$+0.5*[2] | V |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |
| Storage temperature under bias | Tbias | –10 to +85 | °C |

Notes: 1. $V_T$ (min) = –2.0 V for pulse width (under shoot) 6 ns.
2. $V_T$ (max) = $V_{CC}$ + 2.0 V for pulse width (over shoot) 6 ns.

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$*[3] | 4.5 | 5.0 | 5.5 | V |
| | $V_{SS}$*[4] | 0 | 0 | 0 | V |
| Input voltage | $V_{IH}$ | 2.2 | — | $V_{CC}$ + 0.5*[2] | V |
| | $V_{IL}$ | –0.5*[1] | — | 0.8 | V |

Notes: 1. $V_{IL}$ (min) = –2.0 V for pulse width (under shoot) 6 ns.
2. $V_{IH}$ (max) = $V_{CC}$ + 2.0 V for pulse width (over shoot) 6 ns.
3. The supply voltage with all $V_{CC}$ pins must be on the same level.
4. The supply voltage with all $V_{SS}$ pins must be on the same level.

## DC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5.0 V ± 10 %, $V_{SS}$ = 0V)

| Parameter | Symbol | Min | Typ*[1] | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $\|I_{LI}\|$ | — | — | 2 | µA | Vin = $V_{SS}$ to $V_{CC}$ |
| Output leakage current | $\|I_{LO}\|$ | — | — | 2 | µA | Vin = $V_{SS}$ to $V_{CC}$ |
| Operation power supply current | $I_{CC}$ | — | — | 140 | mA | Min cycle<br>$\overline{CS}$ = $V_{IL}$, Iout = 0 mA<br>Other inputs = $V_{IH}$/$V_{IL}$ |
| Standby power supply current | $I_{SB}$ | — | — | 40 | mA | Min cycle, $\overline{CS}$ = $V_{IH}$,<br>Other inputs = $V_{IH}$/$V_{IL}$ |
| | $I_{SB1}$ | — | TBD | 5 | mA | f = 0 MHz<br>$V_{CC}$ $\overline{CS}$ $V_{CC}$ - 0.2 V,<br>(1) 0 V Vin 0.2 V or<br>(2) $V_{CC}$ Vin $V_{CC}$ - 0.2 V |
| | | —*[2] | TBD*[2] | 1.2*[2] | | |
| Output voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 8 mA |
| | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = –4 mA |

Notes: 1. Typical values are at $V_{CC}$ = 5.0 V, Ta = +25°C and not guaranteed.
2. This characteristics is guaranteed only for L-version.

## Capacitance (Ta = +25°C, f = 1.0 MHz)

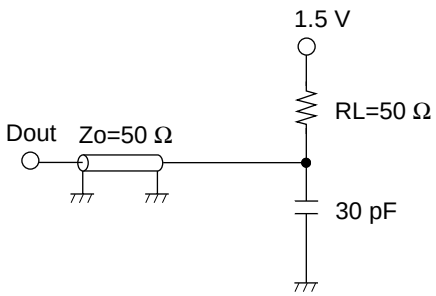
| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input capacitance*[1] | Cin | — | — | 6 | pF | Vin = 0 V |
| Input/output capacitance*[1] | $C_{I/O}$ | — | — | 8 | pF | $V_{I/O}$ = 0 V |

Note: 1. This parameter is sampled and not 100% tested.

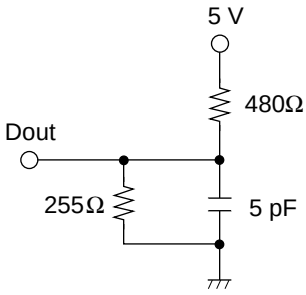
## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 5.0 V ± 10 %, unless otherwise noted.)

### Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)




Output load (A)




Output load (B)
(for $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{WHZ}$, and $t_{OW}$)

### Read Cycle

| | | HM624100HC | | | |
|---|---|---|---|---|---|
| | | -10 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** | **Notes** |
| Read cycle time | $t_{RC}$ | 10 | — | ns | |
| Address access time | $t_{AA}$ | — | 10 | ns | |
| Chip select access time | $t_{ACS}$ | — | 10 | ns | |
| Output enable to outpput valid | $t_{OE}$ | — | 5 | ns | |
| Output hold from address change | $t_{OH}$ | 3 | — | ns | |
| Chip select to output in low-Z | $t_{CLZ}$ | 3 | — | ns | 1 |
| Output enable to output in low-Z | $t_{OLZ}$ | 0 | — | ns | 1 |
| Chip deselect to output in high-Z | $t_{CHZ}$ | — | 5 | ns | 1 |
| Output disable to output in high-Z | $t_{OHZ}$ | — | 5 | ns | 1 |

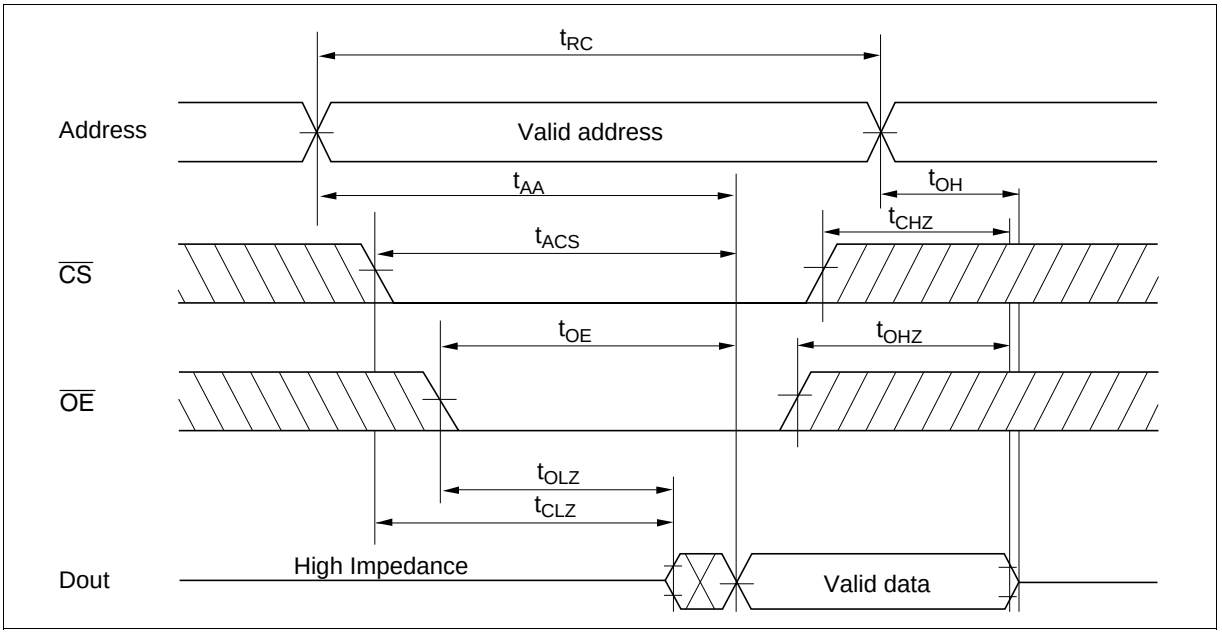
### Write Cycle

| | | HM624100HC | | | |
|---|---|---|---|---|---|
| | | -10 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Unit** | **Notes** |
| Write cycle time | $t_{WC}$ | 10 | — | ns | |
| Address valid to end of write | $t_{AW}$ | 7 | — | ns | |
| Chip select to end of write | $t_{CW}$ | 7 | — | ns | 9 |
| Write pulse width | $t_{WP}$ | 7 | — | ns | 8 |
| Address setup time | $t_{AS}$ | 0 | — | ns | 6 |
| Write recovery time | $t_{WR}$ | 0 | — | ns | 7 |
| Data to write time overlap | $t_{DW}$ | 5 | — | ns | |
| Data hold from write time | $t_{DH}$ | 0 | — | ns | |
| Write disable to output in low-Z | $t_{OW}$ | 3 | — | ns | 1 |
| Output disable to output in high-Z | $t_{OHZ}$ | — | 5 | ns | 1 |
| Write enable to output in high-Z | $t_{WHZ}$ | — | 5 | ns | 1 |

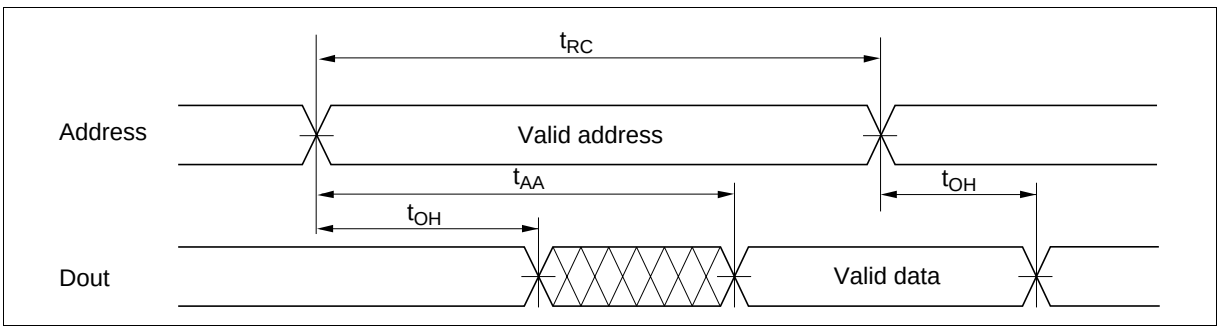
Note:
1. Transition is measured ±200 mV from steady voltage with Load (B). This parameter is sampled and not 100% tested.
2. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{WE}$ and/or $\overline{CS}$ must be high during address transition time.
4. if $\overline{CS}$ and $\overline{OE}$ are low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains a high impedance state.
6. $t_{AS}$ is measured from the latest address transition to the later of $\overline{CS}$ or $\overline{WE}$ going low.
7. $t_{WR}$ is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the first address transition.
8. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high. $t_{WP}$ is measured from the beginnig of write to the end of write.
9. $t_{CW}$ is measured from the later of $\overline{CS}$ going low to the the end of write.

## Timing Waveforms

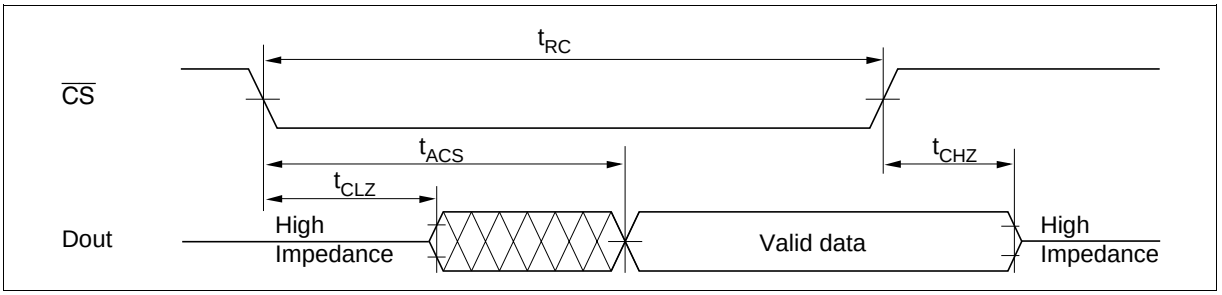
**Read Timing Waveform (1)** ($\overline{WE}$ = $V_{IH}$)



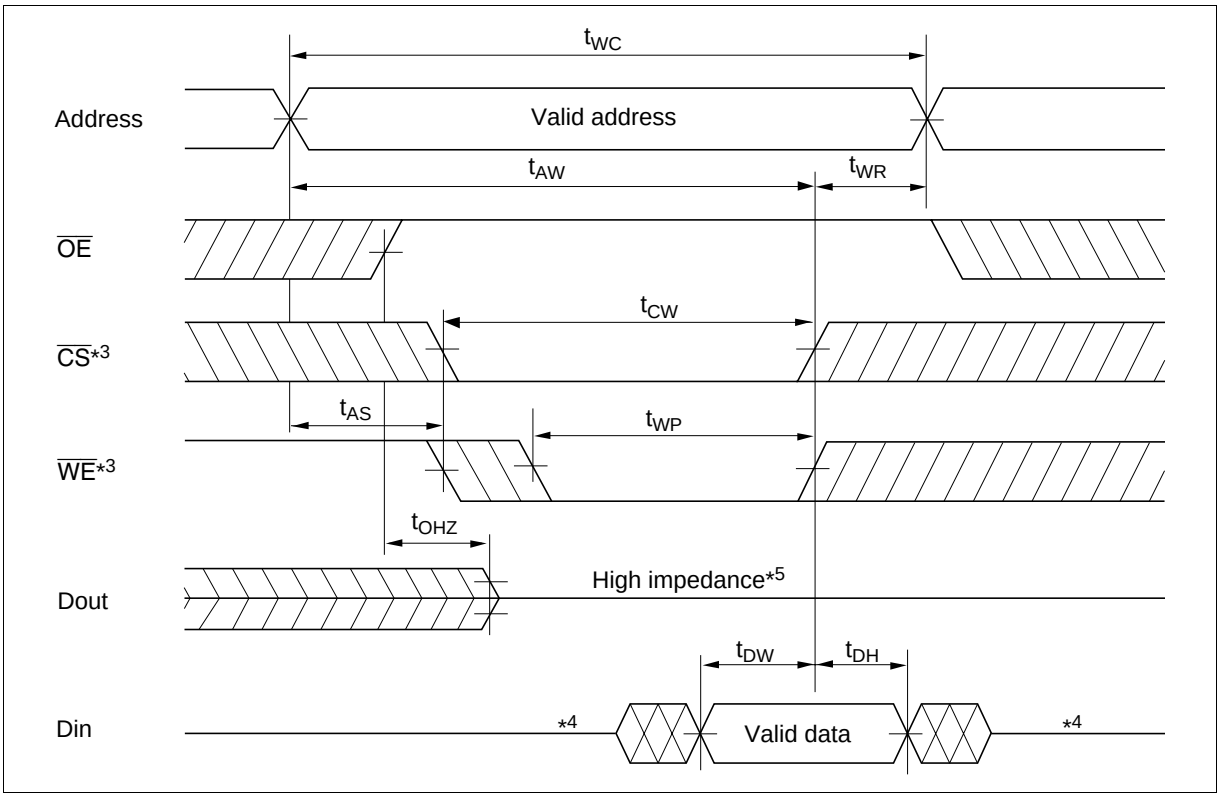

**Read Timing Waveform (2)** ($\overline{WE}$ = $V_{IH}$, $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IL}$)



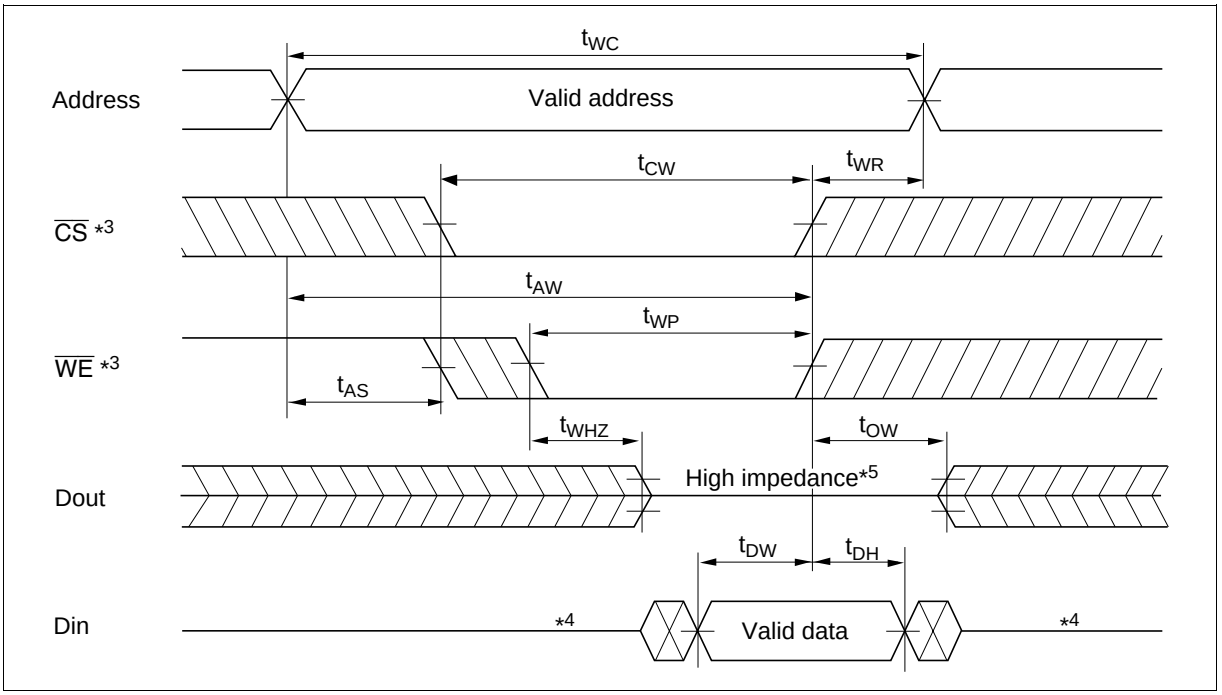
**Read Timing Waveform (3)** ($\overline{WE}$ = $V_{IH}$, $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IL}$)*2




**Write Timing Waveform (1)** ($\overline{WE}$ Controlled)



**Write Timing Waveform (2)** ($\overline{CS}$ Controlled)



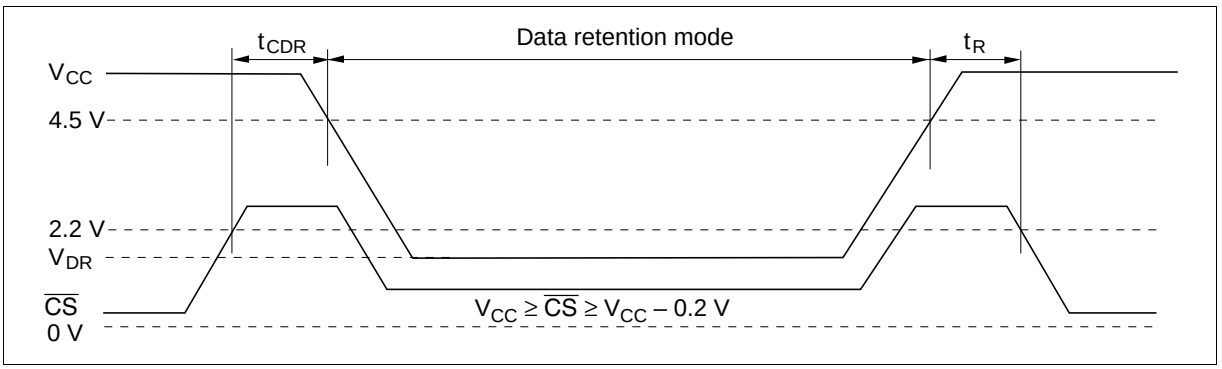
## Low $V_{CC}$ Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

| Parameter | Symbol | Min | Typ*[1] | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| $V_{CC}$ for data retention | $V_{DR}$ | 2.0 | — | — | V | $V_{CC}$ $\overline{CS}$ $V_{CC}$ – 0.2 V<br>(1) 0 V Vin 0.2 V or<br>(2) $V_{CC}$ Vin $V_{CC}$ – 0.2 V |
| Data retention current | $I_{CCDR}$ | — | TBD | 800 | µA | $V_{CC}$ = 3 V, $V_{CC}$ $\overline{CS}$ $V_{CC}$ – 0.2 V<br>(1) 0 V Vin 0.2 V or<br>(2) $V_{CC}$ Vin $V_{CC}$ – 0.2 V |
| Chip deselect to data retention time | $t_{CDR}$ | 0 | — | — | ns | See retention waveform |
| Operation recovery time | $t_R$ | 5 | — | — | ms | |

Note: 1. Typical values are at $V_{CC}$ = 3.0 V, Ta = +25°C, and not guaranteed.

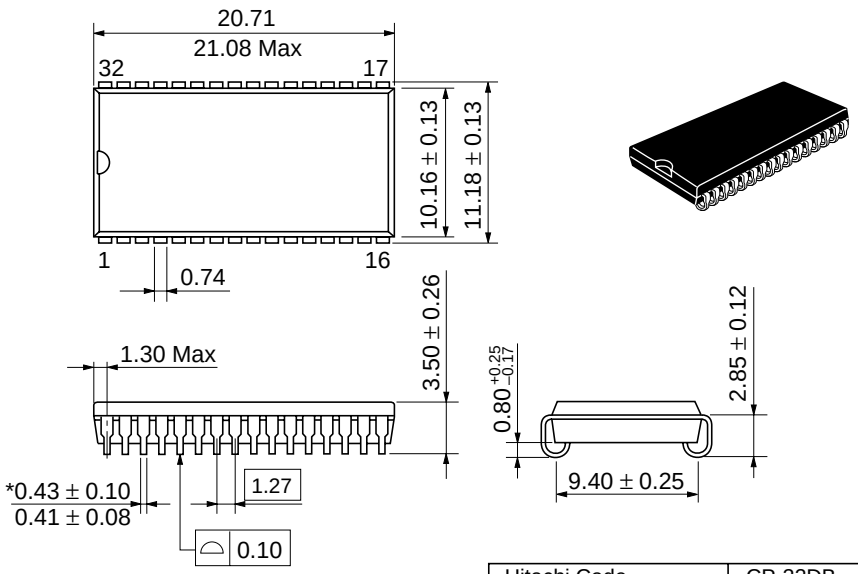
### Low $V_{CC}$ Data Retention Timing Waveform



## Package Dimensions

**HM624100HCJP/HCLJP Series** (CP-32DB)

Unit: mm




*Dimension including the plating thickness
Base material dimension

| | |
|---|---|
| Hitachi Code | CP-32DB |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Mass (reference value) | 1.2 g |

## Cautions

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