# LM3279 Buck-Boost Converter With MIPI® RFFE Interface for 3G And 4G RF Power Amplifiers

## 1 Features

- MIPI® RFFE Digital Control Interface
- High-Efficiency PFM and PWM Modes with Internal Seamless Transition
- Operates from a Single Li-Ion Cell: 2.7 V to 5.5 V
- Adjustable Output Voltage:
  - RFFE Digital Control: 0.4 V to 4.2 V
  - Analog Control: 0.5 V to 4.2 V
- 1-A Maximum Load Capability for $V_{BATT} \geq 3.2$ V, $V_{OUT} = 3.6$ V
- 2.4-MHz (typ.) Switching Frequency
- Seamless Buck-Boost Mode Transition
- Fast Output Voltage Transition: 0.8 V to 4 V in 20 µs
- High-Efficiency: 95% typ. at $V_{BATT} = 3.7$ V, $V_{OUT} = 3.3$ V, at 300 mA
- Input Overcurrent Limit
- Output Overvoltage Clamp
- Internal Compensation

## 2 Applications

- 3G/4G Smartphones
- RF PC Cards
- Tablets, eBooks Readers
- Battery-Powered RF Devices

## 3 Description

The LM3279 is a buck-boost DC/DC converter designed to generate output voltages above or below a given input voltage and is particularly suitable for Power Amplifiers operating from single-cell Li-Ion batteries in portable applications.

The LM3279 has four modes of operation: Pulse Width Modulation (PWM), Pulse Frequency Modulation (PFM), standby, and shutdown. During normal conditions, the LM3279 operates in full synchronous PWM mode at 2.4-MHz typical switching frequency, providing seamless transitions between buck and boost operating regimes. Energy-saving PFM mode increases efficiencies and current savings during low-power RF transmission modes. For high-transmit power, the device operates in PWM buck or boost mode, whereas the device can transition between PWM and PFM modes during low-power transmit. The LM3279 can be controlled either via an included MIPI RFFE Digital Control Interface or by using an analog control from an external MCU, offering design flexibility.

The power converter topology enables minimum total solution size by using one small footprint and case size inductor and two surface mount capacitors.

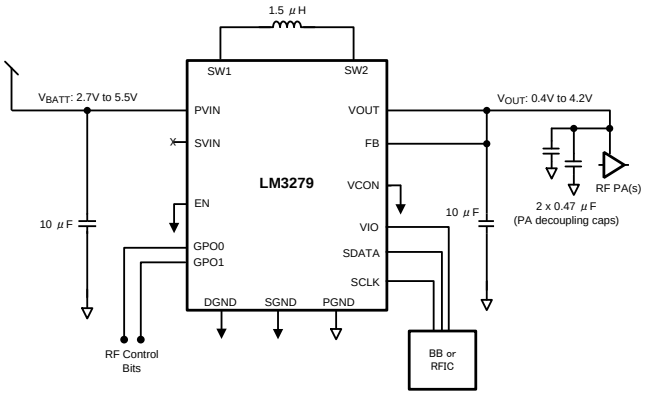
The LM3279 is internally compensated for buck and boost modes of operation thus providing an optimal transient response.

**Device Information(1)**

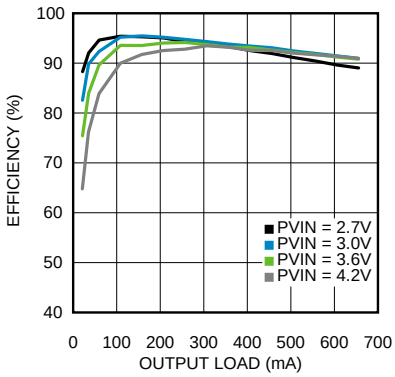
| PART NUMBER | PACKAGE | BODY SIZE (MAX) |
|---|---|---|
| LM3279 | DSBGA (16) | 2.529 mm x 2.146 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Schematic**




**PWM Efficiency ($V_{OUT}$ = 2.4 V)**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision B (November 2013) to Revision C** — **Page**

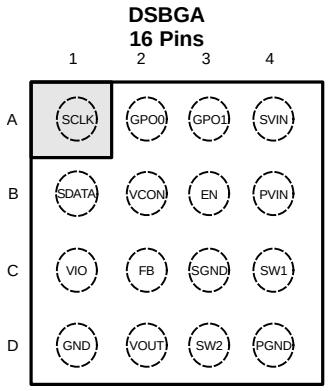
- Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section ... 1

**Changes from Revision A (May 2013) to Revision B** — **Page**

- Changed Analog control 0.6V to 0.5V ... 1
- Changed 0.2V ≤ VCON ≤ 1.4V to 0.167V ≤ VCON ≤ 1.4V ... 6
- Changed 0.2 V to 0.167 V ... 6
- Changed 0.6 V to 3.4 V to 1.6 V to 3.4 V ... 7
- Changed 200 from max. to typ. ... 7
- Changed 0.2V (min.) to 1.4V (max. typ.) to 0.167V (min.) to 1.4V (max. typ.); from 0.6V to 4.2V output to from 0.5V to 4.2V output ... 14
- Added (default) ... 19
- Added (default) ... 19


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# 5 Pin Configuration and Functions




Top View (Bumps Down)

**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NUMBER | NAME | | |
| A1 | SCLK | IN | Digital control interface (DCON) RFFE Bus clock input. Typically connected to RFFE master on RF or Baseband IC. SCLK must be held low when VIO is not applied. |
| B1 | SDATA | I/O | Digital control interface (DCON) RFFE Bus data input/output. Typically connected to RFFE master on RF or Baseband IC. SDATA must be held low when VIO is not applied. |
| C1 | VIO | IN | Digital control interface (DCON) 1.8-V supply input. VIO functions as the RFFE interface reference voltage. VIO also functions as a reset and enable input to LM3279. Bypass capacitor should be connected between VIO and GND. Typically connected to voltage regulator controlled by RF or Baseband IC. When VIO = HIGH, EN shall be connected to GND. |
| D1 | GND | Ground | Digital Ground. |
| A2 | GPO0 | I/O | Multipurpose GPIO. When VIO = HIGH, GPO0 is a general purpose output for configuring RF front end circuitry. When the GPO0 control bit in Register 02 is set to 1, the output is driven to a 1.8-V (VIO) high logic level. The output is pulled to a low logic level when the GPO0 control bit is set to 0. (Input has an internal pull-up resistor.) |
| B2 | VCON | IN | Voltage Control Analog input. When EN = HIGH, VCON controls the output voltage in PWM and PFM modes. When in Digital control, VCON can be left as no connect or connected to system ground. |
| C2 | FB | Ground | Feedback input to inverting input of error amplifier. Connect output voltage directly to this node at load point. |
| D2 | VOUT | PWR | Regulated output voltage of LM3279. Connect this to a 10-µF ceramic output filter capacitor to GND. |
| A3 | GPO1 | I/O | Multipurpose GPIO. When VIO = HIGH, GPO1 is a general purpose output for configuring RF front end circuitry. When the GPO1 control bit in Register 02 is set to 1, the output is driven to a 1.8-V (VIO) high logic level. The output is pulled to a low logic level when the GPO1 control bit is set to 0. (Input has an internal pull-up resistor.) |
| B3 | EN | IN | Enable Pin. Pulling this pin higher than 1.2 V enables part to function in analog control mode. VIO must be tied to ground. |
| C3 | SGND | Ground | Signal Ground for analog circuits and control circuitry. |
| D3 | SW2 | PWR | Switch pin for Internal Power Switches M3 and M4. Connect inductor between SW1 and SW2. |
| A4 | SVIN | PWR | SVIN is no connect. Analog supply is internally connected to PVIN. |
| B4 | PVIN | PWR | Power MOSFET input and power current input pin. Optional low-pass filtering may help reduce radiated EMI and noise during buck and buck-boost modes. |
| C4 | SW1 | PWR | Switch pin for Internal Power Switches M1 and M2. Connect inductor between SW1 and SW2. |
| D4 | PGND | Ground | Power Ground for Power MOSFETs and gate drive circuitry. |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

| | MIN | MAX | UNIT |
|---|---|---|---|
| PVIN, VOUT to GND | −0.2 | 6 | V |
| PGND to SGND, GND | PGND −0.2 | 0.2 | |
| VIO, SDATA, SCLK, EN, VCON, GPO1/GPO0 to SGND, GND | −0.2 | 6 | |
| FB to PGND | −0.2 | 6 | |
| SW1, SW2 | (PGND −0.2V) | 6 | |
| Continuous power dissipation (3) | Internally limited | | |
| Maximum operating junction temperature ($T_{J-MAX}$) | | 150 | °C |
| Maximum lead temperature (soldering) | See (4) | | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J$ = 150°C (typ.) and disengages at $T_J$ = 125°C (typ.).
(4) For detailed soldering specifications and information, please refer to Texas Instruments Application Note 1112: *DSBGA Wafer Level Chip Scale Package* (SNVA009).

## 6.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –45 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 0 | 1000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)(2)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | 2.7 | | 5.5 | V |
| Output voltage (digital control) | 0.4 | | 4.212 | |
| Recommended current load | 0 | | 1000 | mA |
| Operating ambient temperature ($T_A$) (3) | –30 | | 85 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature ($T_{A-MAX}$) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D-MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.


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## 6.4 Thermal Information

| THERMAL METRIC(1) | | DSBGA YZR 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 70.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 14.4 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 10 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.7 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 10 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics(1)

Limits are for $T_A = T_J = 25°C$, and specifications apply to the LM3279 Typical Application Circuits with: PVIN = 3.8 V, VIO or EN = 1.8 V, unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{FB,MIN}$ | Minimum FB voltage | $V_{SET}$ = 0Bh | 0.35 | 0.40 | 0.45 | V |
| | | VCON = 0.167 V | 0.43 | 0.5 | 0.570 | |
| $V_{FB,MAX}$ | Maximum FB voltage | $V_{SET}$ = 75h | 4.122 | 4.212 | 4.302 | |
| | | VCON = 1.4 V | 4.11 | 4.2 | 4.29 | |
| $I_{Q_PWM}$ | DC bias current in PVIN, SVIN | No switching (2) FB = HIGH<br>Max limits = −30°C ≤ $T_J$ = $T_A$ ≤ 85°C | | 1.4 | 2 | mA |
| $I_{SHDN}$ | Shutdown supply current | VIO = EN = 0 V, VCON = 0 V,<br>SW1 = SW2 = $V_{OUT}$ = 0 V<br>Max limits = −30°C ≤ $T_J$ = $T_A$ ≤ 85°C | | 0.2 | 2 | µA |
| $I_{Q\ STBY}$ | Standby supply current | VIO = 1.8 V, $V_{SET_CTRL}$ = 02h,<br>SW1 = SW2 = $V_{OUT}$ = 0 V | | 1.2 | | mA |
| $I_{LIM_L}$ | Input current limit (large) | Open Loop (3) VCON = 1.2 V | 1500 | 1700 | | mA |
| $I_{LIM_S}$ | Input current limit (small) | Open Loop (3) VCON = 0.2 V | 700 | 850 | | |
| $f_{OSC_PWM}$ | Internal oscillator frequency | PWM<br>Min and Max limits = −30°C ≤ $T_J$ = $T_A$ ≤ 85°C | 2.1 | 2.4 | 2.7 | MHz |
| $f_{SCLK}$ | SCLK clock frequency | | 0.032 | | 26 | |
| $I_{VIO-IN}$ | VIO voltage average input current | VIO = 1.8 V, Average during 26-MHz write | | | 1.25 | mA |
| $I_{IL}$ | $I_{SDATA}$ | VIN = 0.2*VIO | −2 | | 1 | µA |
| | $I_{SCLK}$ | | −1 | | 1 | |
| $I_{IH}$ | $I_{SDATA}$ | VIN = 0.8*VIO | −2 | | 10 | |
| | $I_{SCLK}$ | | −1 | | 10 | |
| $V_{IH}$ | Input high-level threshold EN, GPO0, GPO1 | Min and Max limits = −30°C ≤ $T_J$ = $T_A$ ≤ 85°C | 1.2 | | | V |
| $V_{IL}$ | Input low-level threshold EN, GPO0, GPO1 | | | | 0.6 | |
| $V_{IH-SDATA,\ SCLK}$ | Input high-level threshold SDATA, SCLK | | 0.4*VIO | | 0.7*VIO | V |
| $V_{IL-SDATA,\ SCLK}$ | Input low-level threshold SDATA, SCLK | | 0.3*VIO | | 0.6*VIO | |
| $V_{OH-SDATA}$ | Output high-level threshold SDATA | $I_{SDATA}$ = −2 mA | 0.8*VIO | | VIO + 0.01 | |
| $V_{OL-SDATA}$ | Output low-level threshold SDATA | $I_{SDATA}$ = 2 mA | | | 0.2*VIO | |
| $V_{OH-GPO}$ | Output high-level threshold GPO | $I_{OUT}$ = ±200 µA | VIO−0.15V | | VIO+0.1V | |
| $V_{OL-GPO}$ | Output low-level threshold GPO | $I_{OUT}$ = ±200 µA | −0.4 | | 0.3 | V |
| $V_{SET-LSB}$ | Output voltage LSB | $V_{SET_CTRL}$ = 40h to 41h | | 36 | | mV |
| $I_{EN}$ | EN pin pulldown current | VIO = 0 V | | 5 | 10 | µA |

(1) Min and Max limits are specified by design, test, or statistical analysis.
(2) $I_Q$ specified here is when the part is not switching.
(3) The parameters in the electrical characteristics table are tested under open loop conditions at $P_{VIN}$ = 3.8 V. For performance over the input voltage range and closed loop results refer to the datasheet curves.

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## Electrical Characteristics(1) (continued)

Limits are for $T_A = T_J = 25°C$, and specifications apply to the LM3279 Typical Application Circuits with: PVIN = 3.8 V, VIO or EN = 1.8 V, unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Gain | Internal gain (4) | 0.167 V ≤ VCON ≤ 1.4 V | | 3 | | V/V |
| $I_{CON}$ | VCON pin input leakage | EN = 3.8 V | –1 | | 1 | µA |
| $I_{OUT_LEAKAGE}$ | Leakage into VOUT pin of the buck-boost | EN = 0, $V_{OUT}$ ≤ 4.2 V, $V_{BATT}$ ≤ 5.5 V<br>Max limits = −30°C ≤ $T_J$ = $T_A$ ≤ 85°C | | | 5 | |

(4) When using analog control (EN = HIGH) to calculate $V_{OUT}$, use the following equation: $V_{OUT}$ = VCON × 3.

## 6.6 System Characteristics

The following spec table entries are specified by design and verifications, providing the component values in the typical application circuits are used: L = 1.5 µH, DFE201610C-1R5M (2016)/TOKO; $C_{IN}$ and $C_{OUT}$ each = 10 µF 6.3 V, C105A106MQ5NUNC (0402)/Samsung; PA decoupling cap emulation = 0.47 µF, GRM033R60J474ME90 (0201)/Murata. **These parameters are not verified by production testing.** Typical limits are $T_A$ = 25°C. Min and Max limits apply over the full ambient temperature range (−30°C ≤ $T_A$ ≤ 85°C) and over the $V_{IN}$ range = 2.7 V to 5.5 V, unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{ON}$ | Turn-on time (time for output to reach 0V→90% × 3.4 V) | $V_{BATT}$ = 3.8 V, VIO = 1.8 V, RFFE write $V_{SET}$ = 3.42 V ($V_{SET_CTRL}$ = 5Fh), $I_{OUT}$ = 0mA | | 35 | 50 | µs |
| | | EN = L to H, $V_{BATT}$ = 3.8 V, VCON = 1.14 V, $I_{OUT}$ = 0 mA | | | | |
| $I_{OUT_MAX}$ | Max output current | $V_{BATT}$ ≥ 3 V, $V_{OUT}$ = 3.8 V | 750 | | | mA |
| | | $V_{BATT}$ ≥ 3.2 V, $V_{OUT}$ = 4.2 V | 650 | | | |
| $D_{MAX}$ | Maximum duty cycle | Boost (% M4 on) | | | 50% | |
| | | Buck (% M1 on) | | | 100% | |
| $F_{OSC_PFM}$ | Internal oscillator frequency | PFM: $V_{OUT}$ = 0.6V, $P_{VIN}$ = 3.7 V<br>$I_{OUT}$ = 13 mA | | 63 | | kHz |
| $C_L$ | Load capacitance | Half speed readback SCLK = 13 MHz, not including LM3279 capacitance.<br>$T_A$ = 25°C | 10 | | 50 | pF |
| $C_{VCON}$ | VCON input capacitance | VCON = 1V, Test frequency = 100 kHz, $T_A$ = 25°C | | | 10 | pF |
| $VCON_{LIN}$ | VCON linearity | 0.167 V ≤ VCON ≤ 1.4 V | –2.5% | | 2.5% | |
| VIO | VIO I/O voltage level | 1.8V Bus, $T_A$ = 25°C | 1.65 | 1.8 | 1.95 | V |
| $V_{O_RIPPLE}$ | Ripple voltage | $V_{BATT}$ ≥ 3.2 V, 0.6 ≤ $V_{OUT}$ ≤ 4.2 V,<br>0 mA ≤ $I_{OUT}$ ≤ 430 mA, $T_A$ = 25°C | | 15 | 50 | mV |
| | PFM ripple | $V_{OUT}$ = 0.6 V, $I_{OUT}$ = 5mA | | 40 | | |
| | Ripple voltage in mode transition | $V_{BATT}$ = 3 V to 5 V, Tr = Tf = 30s<br>3.3 V ≤ $V_{OUT}$ ≤ 4.2 V | | | 50 | |
| $\Delta V_{OUT}$ | Line regulation | $V_{BATT}$ = 3.2 V to 4.9 V, $V_{OUT}$ = 3.5 V,<br>PWM Operation | | | 10 | mV |
| | Load regulation | $I_{OUT}$ = 0 mA to 500 mA, $V_{BATT}$ = 3.2 V to 4.9 V,<br>PWM Operation | | | 20 | |
| Line_tr | Line transient response | $V_{BATT}$ = 3.6 V to 4.2 V, Tr = Tf = 10 µs,<br>$V_{OUT}$ = 3.5 V, $R_{LOAD}$ = 11.4 Ω, PWM | –100 | | 100 | mV |
| | | $V_{BATT}$ = 3.6 V to 4.2 V, Tr = Tf = 10 µs,<br>$V_{OUT}$ = 0.8 V, $R_{LOAD}$ = 20 Ω, PFM | –5 | | 5 | |
| Load_tr | Load transient response | $I_{OUT}$ = 1 mA to 200 mA, Tr = Tf = 1 µs,<br>$V_{BATT}$ = 4.2 V, $V_{OUT}$ = 3.5 V, PWM | –100 | | 100 | mV |
| | | $I_{OUT}$ = 10 mA to 90 mA, Tr = Tf = 1 µs,<br>$V_{BATT}$ = 4.2 V, $V_{OUT}$ = 0.8 V, PFM | –10 | | 10 | |


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## System Characteristics (continued)

The following spec table entries are specified by design and verifications, providing the component values in the typical application circuits are used: L = 1.5 µH, DFE201610C-1R5M (2016)/TOKO; $C_{IN}$ and $C_{OUT}$ each = 10 µF 6.3 V, C105A106MQ5NUNC (0402)/Samsung; PA decoupling cap emulation = 0.47 µF, GRM033R60J474ME90 (0201)/Murata. **These parameters are not verified by production testing.** Typical limits are $T_A$ = 25°C. Min and Max limits apply over the full ambient temperature range (−30°C ≤ $T_A$ ≤ 85°C) and over the $V_{IN}$ range = 2.7 V to 5.5 V, unless otherwise specified.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OUT_TR}$ | VOUT transient response overshoot | $V_{BATT}$ = 3.2 V to 4.2 V, $V_{OUT}$ = 1.6 V to 3.4 V, Tr = Tf = 1 µs, $R_{LOAD}$ = 5 Ω | | 200 | | mV |
| | VOUT transient response rise time | | | | 20 | µs |
| | VOUT transient response fall time | | | | 50 | |
| η | Efficiency | $V_{BATT}$ = 3 V, $V_{OUT}$ = 1.9 V, $I_{OUT}$ = 20 mA (PWM) | | 77% | | |
| | | $V_{BATT}$ = 3 V, $V_{OUT}$ = 2.41 V, $I_{OUT}$ = 60 mA (PWM) | | 91% | | |
| | | $V_{BATT}$ = 3 V, $V_{OUT}$ = 2.71 V, $I_{OUT}$ = 200 mA (PWM) | | 94% | | |
| | | $V_{BATT}$ = 3 V, $V_{OUT}$ = 3.31 V, $I_{OUT}$ = 480 mA (PWM) | | 93% | | |
| | | $V_{BATT}$ = 3.8 V, $V_{OUT}$ = 0.60 V, $I_{OUT}$ = 10 mA (PFM) | | 57% | | |
| | | $V_{BATT}$ = 3.8 V, $V_{OUT}$ = 1 V, $I_{OUT}$ = 20 mA (PFM) | | 75% | | |
| | | $V_{BATT}$ = 3.8 V, $V_{OUT}$ = 1.9 V, $I_{OUT}$ = 20 mA (PWM) | | 68% | | |
| | | $V_{BATT}$ = 3.8 V, $V_{OUT}$ = 2.41 V, $I_{OUT}$ = 70 mA (PWM) | | 88% | | |
| | | $V_{BATT}$ = 3.8 V, $V_{OUT}$ = 2.71 V, $I_{OUT}$ = 200 mA (PWM) | | 94% | | |
| | | $V_{BATT}$ = 3.8 V, $V_{OUT}$ = 3.31 V, $I_{OUT}$ = 480 mA (PWM) | | 94% | | |
| | | $V_{BATT}$ = 3 V, $V_{OUT}$ = 3.6 V, $I_{OUT}$ = 200 mA (PWM) | | 94% | | |
| $T_S$ | Data setup time | $T_A$ = 25°C | 1 | | | ns |
| $T_H$ | Data hold time | | 5 | | | |
| $T_{SDATAOTR}$ | SDATA output transition time (rise/fall time) | VIO range = 1.65 V to 1.95 V, $T_A$ = 25°C | 2.1 | | 6.5 | |

## 6.7 System Characteristics Recommended Capacitance Specifications

| BUS | MIN (µF) | TYP (µF) | MAX (µF) |
|---|---|---|---|
| VBATT | 4.7 | 10 | — |
| VOUT | 3.0 | | 13 |

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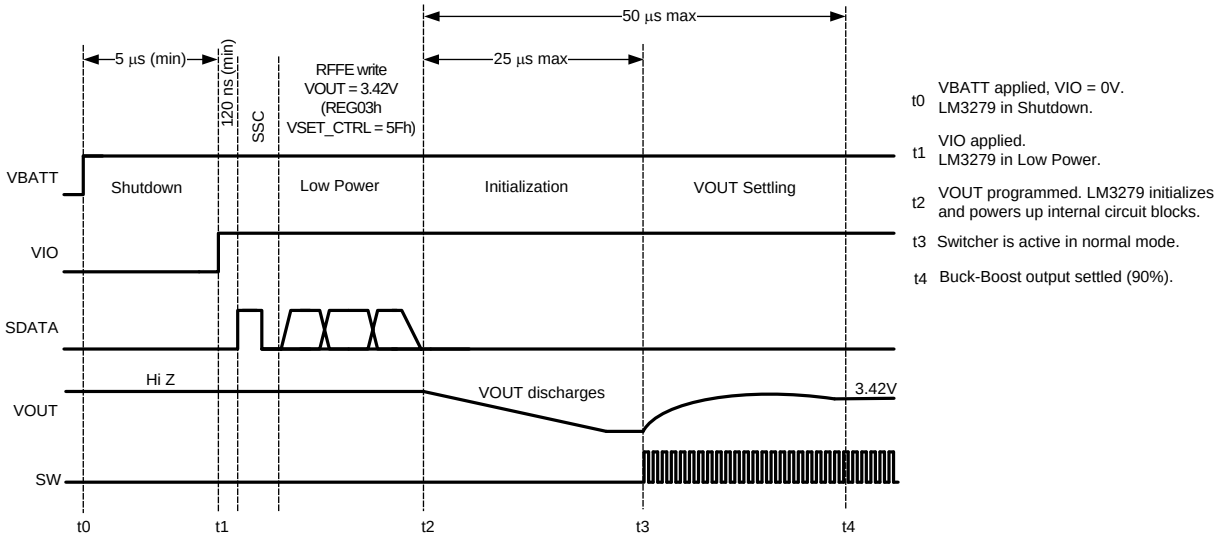



**Figure 1. Cold Power-Up**

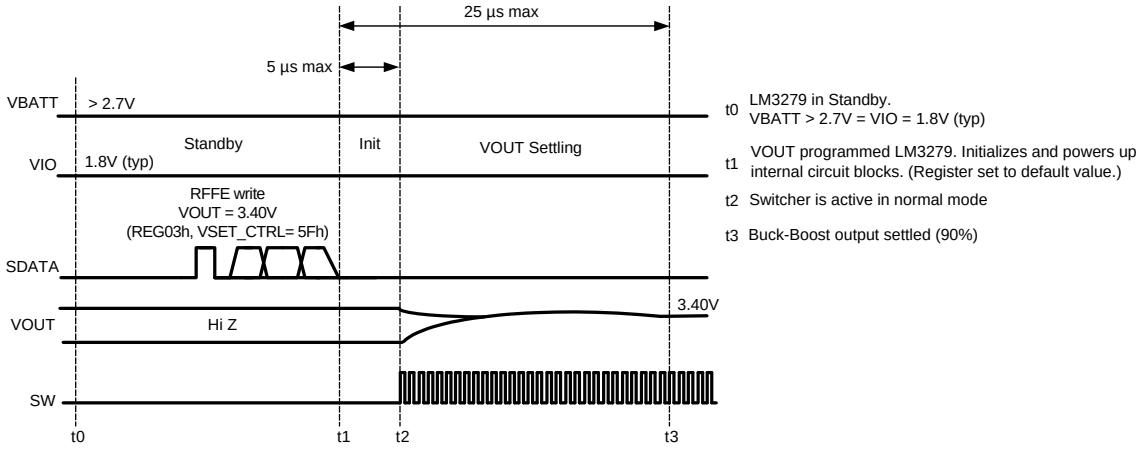
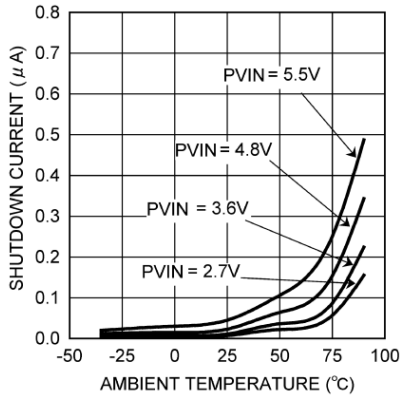



**Figure 2. Standby To Active**


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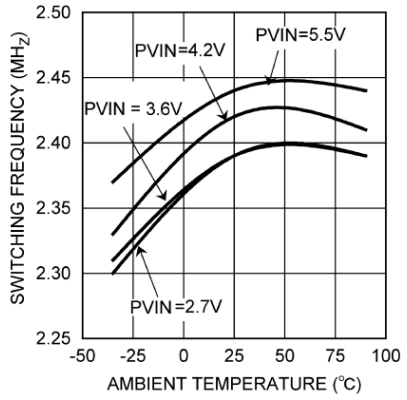
## 6.8 Typical Performance Characteristics

($P_{VIN}$ = EN = 3.6 V and $T_A$ = 25°C, unless otherwise noted)



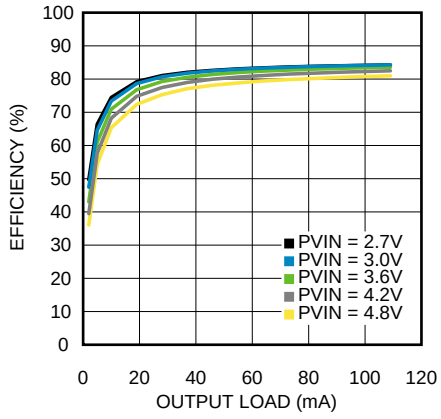

$V_{CON}$ = $V_{OUT}$ = SW1 = SW2 = EN = 0 V

**Figure 3. Shutdown Current vs Temperature**



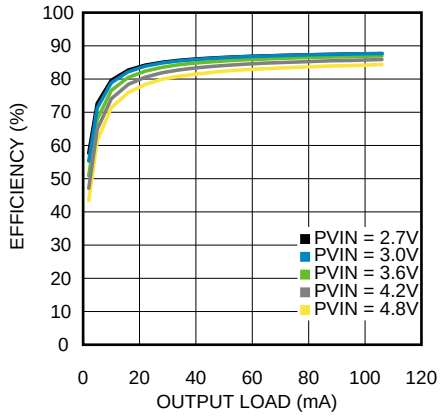

$V_{OUT}$ = 3.5 V $I_{OUT}$ = 300 mA

**Figure 4. Switching Frequency vs Temperature**



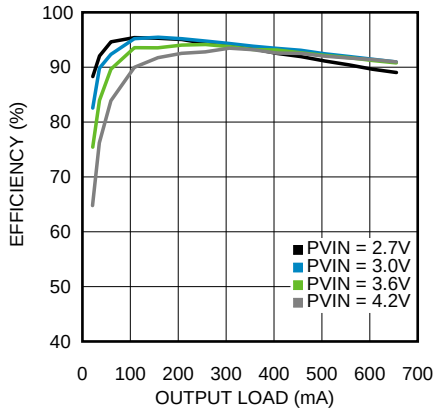

$V_{OUT}$ = 1 V

**Figure 5. PFM Efficiency**



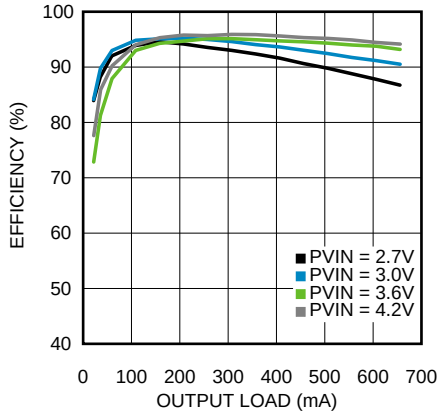

$V_{OUT}$ = 1.4 V

**Figure 6. PFM Efficiency**




$V_{OUT}$ = 2.4 V

**Figure 7. PWM Efficiency**



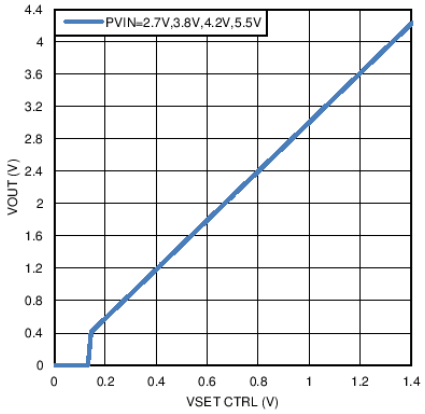

$V_{OUT}$ = 3.6 V

**Figure 8. PWM Efficiency**

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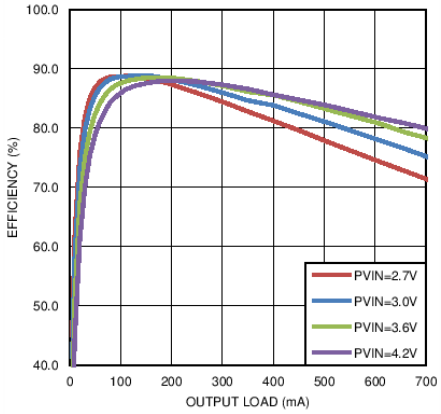
## Typical Performance Characteristics (continued)

($P_{VIN}$ = EN = 3.6 V and $T_A$ = 25°C, unless otherwise noted)



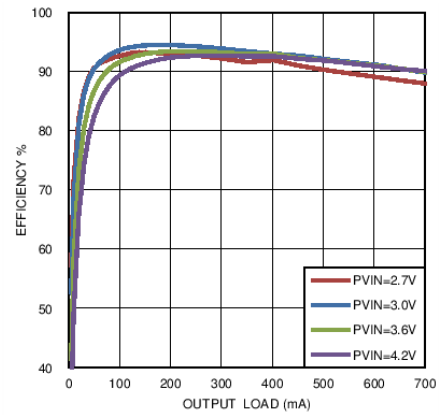

No Load, RFFE Digital Control Mode

**Figure 9. VSET_CTRL Voltage vs Output Voltage**



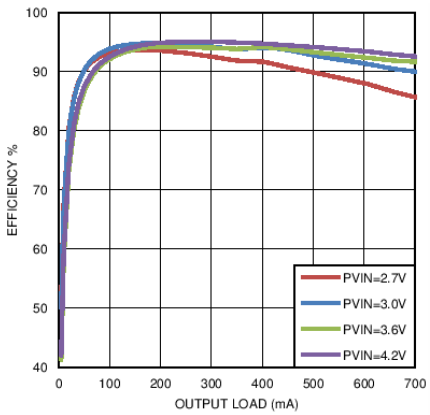

$V_{OUT}$ = 1.5 V

**Figure 10. Auto Efficiency Mode**



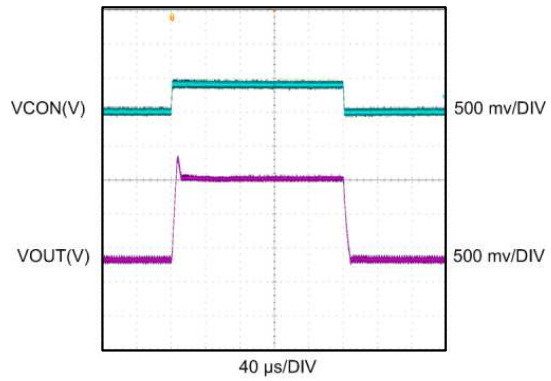

$V_{OUT}$ = 2.5 V

**Figure 11. Auto Efficiency Mode**



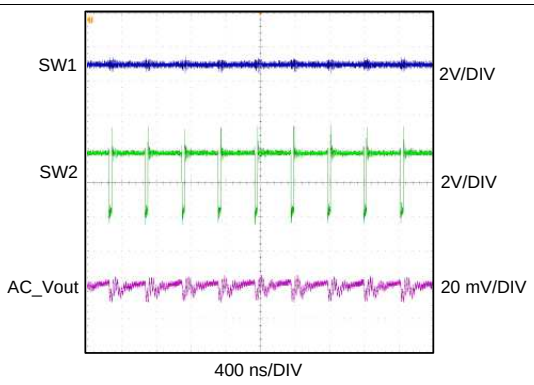

$V_{OUT}$ = 3.4 V

**Figure 12. Auto Efficiency Mode**




$V_{OUT}$ = 0.8 ↔ 2 V PVIN = 3.8 V $R_{LOAD}$ = 20 Ω

**Figure 13. $V_{OUT}$ Transient**



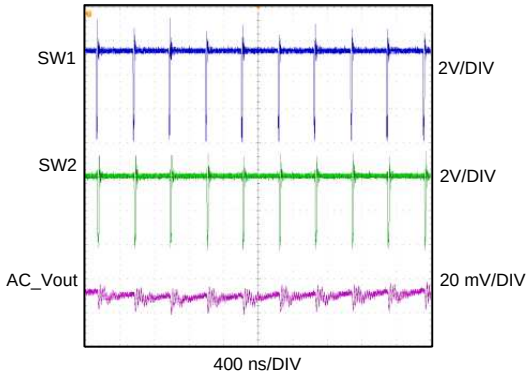

$V_{OUT}$ = 3.45 V PVIN = 3.37 V LOAD = 500 mA

**Figure 14. Boost Mode Operation**


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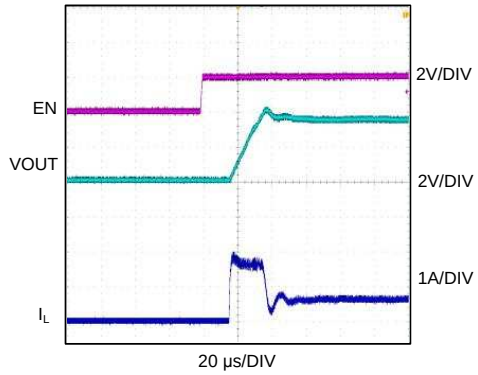
## Typical Performance Characteristics (continued)

($P_{VIN}$ = EN = 3.6 V and $T_A$ = 25°C, unless otherwise noted)



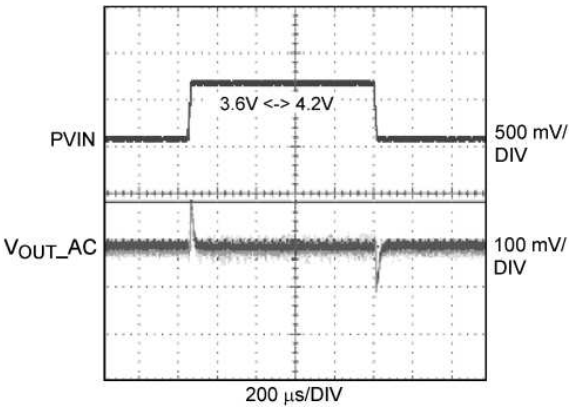

$V_{OUT}$ = 3.6 V PVIN = 3.8 V LOAD = 600 mA

**Figure 15. Buck-Boost Operation**



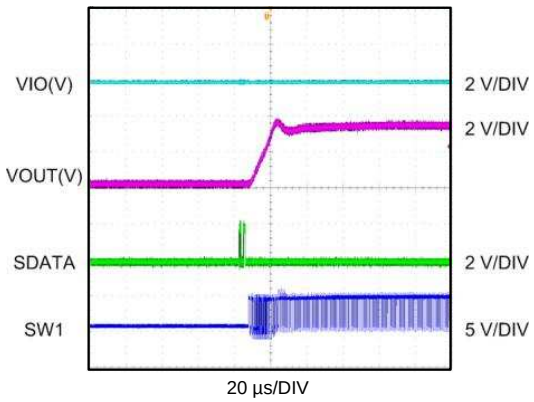

$V_{OUT}$ = 3.45 V PVIN = 3.6 V LOAD = 350 mA

**Figure 16. Start-Up**




$V_{OUT}$ = 3 V PVIN Step = 3.6 V ↔ 4.2 V LOAD = 3200 mA

**Figure 17. Line Transient For DC/DC**




$V_{OUT}$ = 3.5 V PVIN = 4.2 V VIO = 1.8 V
VSET_CTRL = 0x5F

**Figure 18. Standby-To-Active Mode**

# 7 Detailed Description

## 7.1 Overview

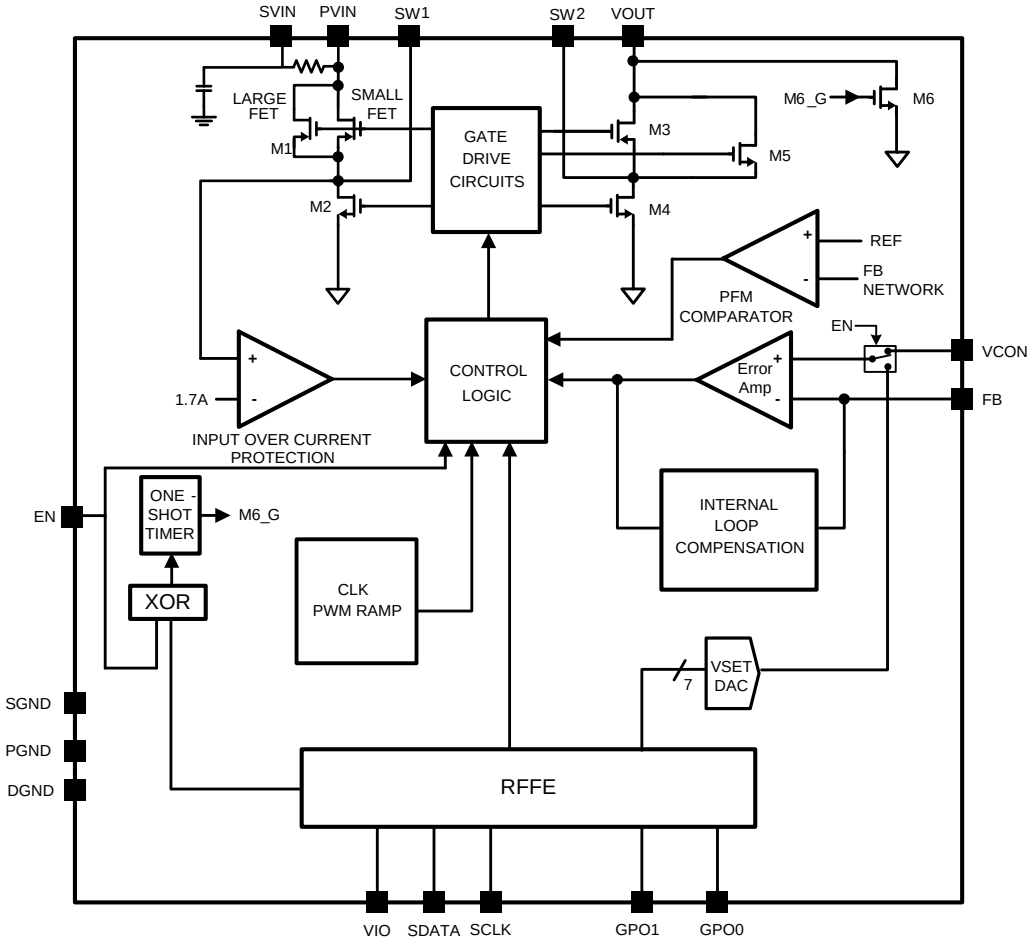
The LM3279 buck-boost converter provides high-efficiency, low-noise power for RF power amplifiers (PAs) in mobile phones, portable communicators and similar battery powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency for a wide range of power levels from a single Li-Ion battery cell. The capability of LM3279 to provide an output voltage lower than as well as higher than the input battery voltage enables the PA to operate with high linearity for a wide range of battery voltages, thereby extending the usable voltage range of the battery. The converter feedback loop is internally compensated for both buck and boost operation, and the architecture is such that it provides seamless transition between buck and boost mode of operation. The LM3279 operates in energy-saving Pulse Frequency Modulation (PFM) mode for increased efficiencies and current savings during low-power RF transmission modes. The output voltage is dynamically programmable from 0.4 V to 4.2 V by either programming the VSET value in register 00h, or adjusting the voltage on the control pin VCON. The fast output voltage transient response of LM3279 makes it suitable for adaptively adjusting the PA supply voltage depending on its transmitting power which improves systems efficiency and prolongs battery life

Additional features include current-overload protection, output overvoltage clamp, and thermal-overload shutdown.

The LM3279 is constructed using a chip-scale 16-bump DSBGA package that offers the smallest possible size for space-critical applications such as cell phones where board area is an important design consideration. Use of a high switching frequency (2.4 MHz, typ.) reduces the size of external components. As shown in Figure 24 and Figure 27, only three external power components are required for circuit operation. Use of a DSBGA package requires special design considerations for implementation. (See *DSBGA Package Assembly And Use* in the *Layout* section.) Its fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications where its edges are not subjected to high-intensity ambient red or infrared light. In addition, the system controller should set VIO = LOW (or EN if system implementation with analog VCON) during power-up and other low supply-voltage conditions.


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## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Dynamically Adjustable Output Voltage

The LM3279 features a dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.4 V to 4.2 V by either programming the VSET value in register 00h, or by changing the voltage on the analog VCON pin when implementing analog control. This feature is useful in cell-phone RF PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances, the transmitting power can be reduced. Hence, the supply voltage to the PA can be reduced, promoting longer battery life. In order to adaptively adjust the supply voltage to the PA in real time in a cell-phone application, the output-voltage transition should be fast enough in order to meet the RF transmit signal specifications. The LM3279 offers ultra-fast output-voltage transition without drawing very large currents from the battery supply. For a current limit of 1700 mA (typ.), the output voltage can transition from 0.6 V to 3.4 V in less than 20 µs with a load resistance of 5 Ω at $V_{BATT}$ = 3.8 V.

## Feature Description (continued)

### 7.3.2 Seamless Mode Transition

In a typical non-inverting buck-boost converter, all four power switches M1 through M4 are switched every cycle. This operation increases MOSFET drive losses and lowers the converter efficiency. The LM3279 switches only two power switches every cycle to improve converter efficiency. Hence, it operates either as buck converter or a boost converter depending upon the input and output voltage conditions. This creates a boundary between the buck and boost mode of operation. When the input battery voltage is close to the set output voltage, the converter automatically switches to a four-switch operation seamlessly such that the output voltage does not see any perturbations at the mode boundary. The excellent mode-transition capability of the LM3279 enables low-noise output with highest efficiency. Internal feedback loop compensation ensures stable operation in buck, boost, and buck-boost modes, as well as during mode transitions.

### 7.3.3 Setting The Output Voltage

The output voltage can be set by two methods: via Analog Control or Digital Control.

In the Analog Control method, the VCON pin is an external analog control input pin. It can be enabled (EN = HIGH) or disabled (EN = LOW). An analog voltage is provided by an external MCU (either a D/A or averaged PWM output) to the VCON pin. The range of this signal is 0.167V (min.) to 1.4V (max. typ.) to provide the full range of the possible output voltage. This signal is internally amplified by a gain of 3 to go from 0.5V to 4.2V output.

For the Digital Control method, the output voltage is set by writing a 7-bit value to reg 00h, bits 0 through 6. Programming a value 00h will force the LM3279 into low-power mode where the entire device except the RFFE interface is turned off. Programming register 00h with the value 02h will place the LM3279 into Standby mode where the SW pin is tri-stated. Values programmed above 0Bh will determine the output voltage from 0.4 V to 4.212 V in 36 mV (typ.) increments.

The output voltage quickly adjusts to the new output voltage value within 20 microseconds both in the positive and negative directions. To accomplish this, the LM3279 buck-boost output can both source and sink current. In the positive direction the buck may assume a 100-percent duty cycle or enter boost mode at up to 50% duty cycle to provide the required current. In the negative direction, the synchronous rectifier (NFET) will remain on to sink current from the output capacitor.

### 7.3.4 General Purpose Outputs

The LM3279 provides two general-purpose outputs to control the RF front-end circuitry. These outputs have a maximum output voltage of 1.8 V. These bits are set by writing to register 02h bits 6 (GPO1) and bit 7 (GPO0).

### 7.3.5 $VCON_{ON}$

When EN = HIGH, the output is disabled when VCON is below 125 mV (typ.). It is enabled when VCON is above 150 mV (typ.). The threshold has 25 mV (typ.) of hysteresis.

### 7.3.6 $R_{DSON}$ Management

The LM3279 has a unique $R_{DSON}$-management function to improve efficiency in both the low-output voltage and high-output voltage conditions. For VSET < 2.1 V (typ.) or VCON < 0.7 V (typ.), the device uses only a small part of the PMOSFET M1 to minimize drive loss of the PMOSFET. When VSET > 2.175 V or VCON > 0.725 V, a large PMOSFET is also used along with the small PMOSFET. The threshold has a 25 mV of hysteresis. For RF PAs, the current consumption typically increases with its supply voltage; thus, higher supply voltage for a PA also means higher power delivered to it. Hence, adding a large PMOSFET for VSET > 2.175 V or VCON > 0.725 V reduces the conduction losses, thereby achieving high efficiency. The LM3279 can also provide output voltages higher than the battery voltage. This boost mode of operation is typically used when the battery voltage has discharged to a low voltage that is not sufficient to provide the required linearity in the PA. A special $R_{DSON}$-management scheme is designed for operation well into boost mode so that an auxiliary PMOSFET switch is also turned on along with Large and Small PMOSFET switches, effectively reducing the $R_{DSON}$ of M1 to a very low value in order to keep the efficiency maximum. Since M1 conducts all the time in boost mode, reducing the $R_{DSON}$ of M1 achieves significant improvement in efficiency.


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## Feature Description (continued)

### 7.3.7 Supply Current Limit

A current limit feature allows the LM3279 to protect itself and external components during overload conditions. In Pulse Width Modulation (PWM) mode, a 1700 mA (typ.) cycle-by-cycle current limit is normally used when $V_{OUT}$ is above 2.1 V (typ.) and an 850 mA (typ.) limit is used when $V_{OUT}$ is below 2.1 V (typ.). If an excessive load pulls the output voltage down to approximately 0.30 V, the device switches to a timed current-limit mode, and the current limit in this mode is 850 mA (typ.), independent of the set $V_{OUT}$ voltage. In timed current limit mode, the internal PMOSFET switch M1 is turned off after the current limit is hit, and the beginning of the next cycle is inhibited for 3.5 µs to force the instantaneous inductor current to ramp down to a safe value.

### 7.3.8 Reverse Current Limit

Since the LM3279 features a dynamically adjustable output voltage, the inductor current can build up to high values in either direction depending on the output voltage transient. For a low-to-high output voltage transient, the inductor current flows from SW1 pin to SW2 pin; this current is limited by the current-limit feature monitoring of MOSFET M1. For a high-to-low output voltage transient, the inductor current flows from SW2 pin to SW1 pin and this current needs to be limited to protect the LM3279 as well as the external components. A reverse current limit feature allows monitoring the reverse inductor current that also flows through MOSFET M2. A −1.2 A (typ.) cycle-by-cycle current limit is used to limit the reverse current. When the reverse current hits the reverse current limit during a PWM cycle, MOSFET M2 is turned off, and MOSFET M1 and M4 are turned on, for the rest of that switching cycle. This allows the inductor to build current in the opposite direction thereby limiting the reverse current. It should be noted that the power MOSFET switches M3 and M4 do not have their own current limiting circuits and are dependent on the current-limit operation implemented for power MOSFETs M1 and M2 to protect them. The implication of this is that any external forcing of voltage/current on SW2 pin or misuse of SW2 pin may be detrimental to the part and may damage the internal circuits.

### 7.3.9 VCON Overvoltage Clamp

The LM3279 features an internal clamp on the analog VCON pin voltage to limit the output voltage to a maximum safe value. The VCON voltage is internally switched to a reference voltage of approximately 1.6 V when the VCON pin voltage exceeds 1.6 V. This limits the output voltage to approximately 4.8 V and protects the part from overvoltage stress. When implementing digital control, the VSET inherently limits the output voltage to the required range.

### 7.3.10 Thermal Overload Protection

The LM3279 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 150°C, the device inhibits operation. All power MOSFET switches are turned off in PWM mode. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

## 7.4 Device Functional Modes

### 7.4.1 Enable And Shutdown Mode

Setting the VIO and EN digital pins low (< 0.6 V) places the LM3279 in shutdown mode (0.01 µA typ. for VIO or EN = 0 V). During shutdown, the output of LM3279 is in tri-state mode. Setting VIO or EN high (>1.2 V) enables normal operation. VIO and EN should be set low to turn off the LM3279 during power-up and undervoltage conditions when the power supply ($V_{BATT}$) is less than the 2.7V minimum operating voltage. When VIO is HIGH, EN must be GND, and when EN = HIGH, VIO must be GND. When EN goes logic low →logic high, for the first 20 µs the dump-switch M6 turns ON to discharge the output capacitor. The duration of M6 being ON is about 20 µs. This enables discharge of (an initially charged) output capacitor to voltages much less than 4.2 V. The switcher feedback-control loops continues the discharge process (if need be) so that the charge in the output capacitor is regulated to the correct output voltage value. When VIO is applied, the default values are loaded into the control registers.

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## Device Functional Modes (continued)

### 7.4.2 Low-Power Mode

The low-power mode is a very low current state where the VIO voltage remains at 1.8 V, and the RFFE interface continues to operate. Here, the current drawn from the $V_{BATT}$ is < 0.1 µA (typ.). This mode can be entered by writing a value of 00h into register 00h (VSET Control Register) or by programming PWR_MODE[1:0] to 10b (bits 6 and 7 of register 1Ch PM-TRIG Register).

During low power mode, the LM3279 maintains the previous programmable register settings upon resuming normal operation.

### 7.4.3 Standby Mode

The standby mode is a mode where the switching is stopped and the power control circuit is off, but the control and the RFFE interface continue to operate. The VIO voltage remains at 1.8 V. Here, the current drawn from the $V_{BATT}$ is 1 mA (typ.). This mode can be entered by writing a value of 02h into register 00h (VSET Control Register) when the PWR_MODE bits are set to normal operation 00b (bits 6 and 7 of register 1Ch PM-TRIG Register).

In this mode the SW pins are tri-stated.

### 7.4.4 PFM Mode

The LM3279 enters PFM mode and operates with reduced switching frequency and supply current to maintain very high efficiencies for light-load operation. The conditions for entering and exiting the PFM and PWM mode are provided in Table 1. In PFM mode, the LM3279 will support up to 100 mA max. In Analog Control Mode the PWM/PFM mode transition has a 60 mV $V_{OUT}$ hysteresis.

For STATE_CTRL[1:0] = 10, the PWM/PFM load current threshold has a 30 mA hysteresis.

During output voltage transients, the LM3279 will automatically shift temporarily to PWM mode before settling to the final output voltage in either PFM or PWM mode depending on the conditions in Table 1.

**Table 1. PWM-PFM Operation Truth Table**

| STATE_CTRL [1:0] or GPO1, GPO0 | ANALOG CONTROL (EN = HIGH, EXTERNAL DAC CONNECTED TO VCON) | DIGITAL CONTROL (VIO = HIGH, $V_{SET_CTRL}$ IN REGISTER 00h PROGRAMMED VIA RFFE) |
|---|---|---|
| 00 | Forced PFM | |
| 01 | PWM if VCON > 0.5V; PFM if VCON < 0.5V | PWM if $V_{SET_CTRL}$ ≥ 29h; PFM if $V_{SET_CTRL}$ < 29h |
| 10 | PWM if VCON > 0.7V OR load >130 mA;<br>PFM if VCON < 0.7V AND $I_{OUT}$ < 100 mA | PWM if $V_{SET_CTRL}$ ≥ 39h OR load > 130 mA;<br>PFM if $V_{SET_CTRL}$ < 39h AND $I_{OUT}$ < 100 mA |
| 11 | Forced PWM | |

## 7.5 Programming

### 7.5.1 Digital Control Serial Bus Interface

The Digital Control Serial Bus Interface provides MIPI RF Front-End Control Interface-compatible access to the programmable functions and registers on the device. When VIO voltage supply is applied to the Bus, it enables the Slave interface and resets the user-defined Slave registers to the default settings. The LM3279 uses a three-pin digital interface; two for bidirectional communications between the ICs connected to the Bus, along with an interface voltage reference VIO that also acts as asynchronous enable and reset. When VIO voltage supply is applied to the Bus, it enables the Slave interface and resets the user-defined Slave registers to the default settings. The device can be set to power-down mode via the asynchronous VIO signal or by setting the appropriate register via Serial Bus Interface. The two communication lines are serial data (SDATA) and clock (SCLK). SCLK and SDATA must be held low until VIO is present. The LM3279 connects as a slave on a single-master Serial Bus Interface.

The SDATA signal is bidirectional, driven by the Master or a Slave. Data is written on the rising edge (transition from logical level zero to logical level one) of the SCLK signal by both Master and Slaves. Master and Slave both read the data on the falling edge (transition from logical level one to logical level zero) of the SCLK signal. A logic-low level applied to VIO signal powers off the digital interface.


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## Programming (continued)

Programming the VSET_CTRL register dynamically adjusts the Buck-Boost output voltage. The feedback voltage changes from $V_{FB,MIN}$ to $V_{FB,MAX}$ depending upon the register value. The digital interface is also used to program the LM3279 for PWM or into PWM and PFM mode.

### 7.5.2 Supported Command Sequences

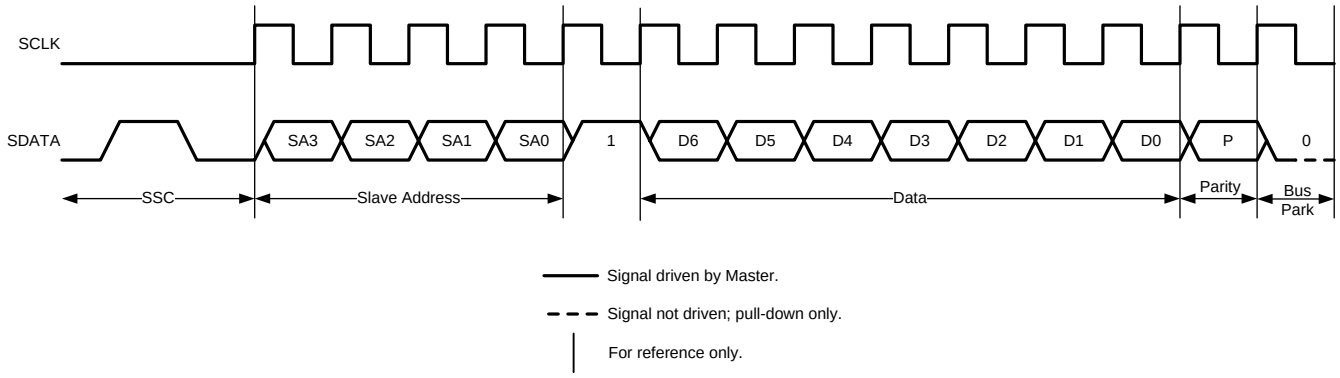



**Figure 19. Register 0 Write**

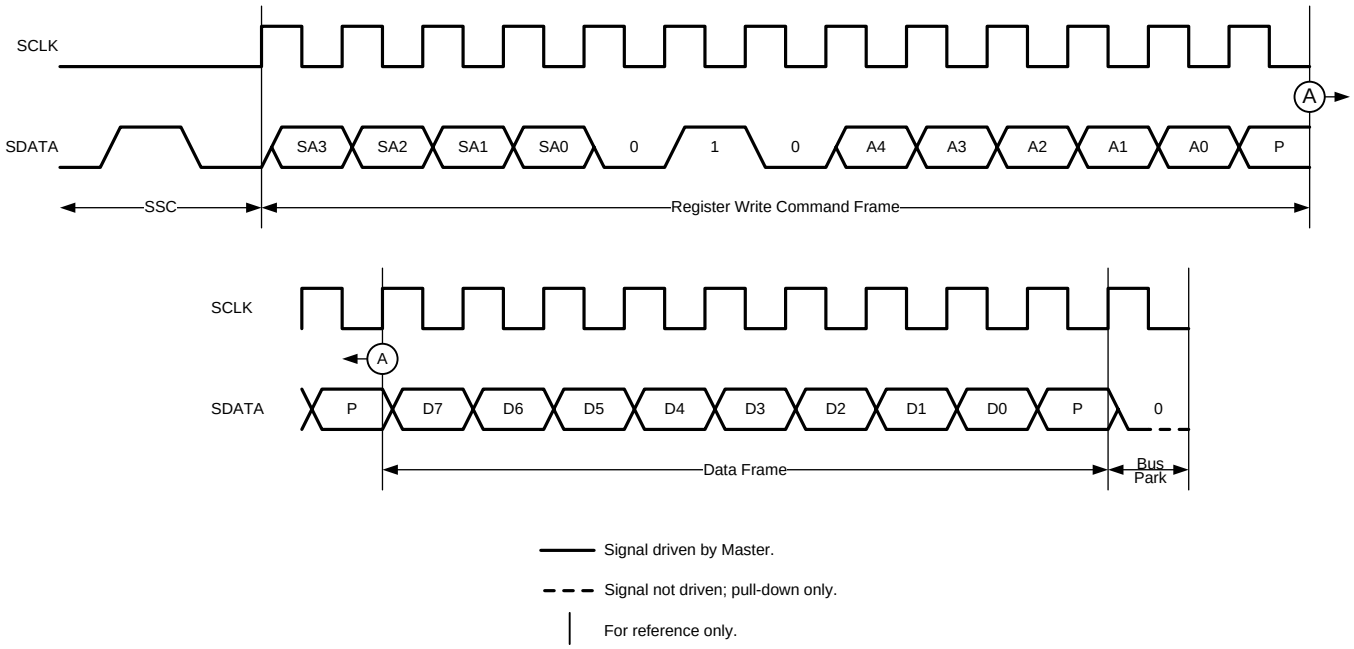



**Figure 20. Register Write**

## Programming (continued)

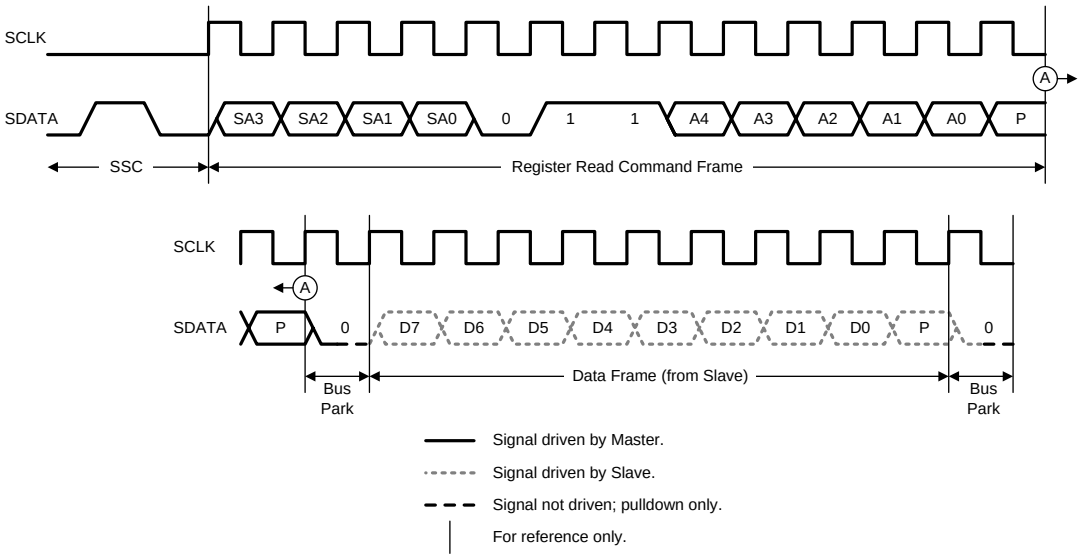



**Figure 21. Register Read**

### 7.5.3 Device Enumeration

The interface component recognizes broadcast Slave Address (SID) of 0000b and is configured, via internal interface signals, with a Unique SID address (USID) and a Group SID address (GSID). The USID is set to 0101b and GSID set to 0000b. The register-set component will typically set the USID to a fixed value; however, it is also possible to construct a register-set component that allows the USID to be programmed via the RFFE bus.

### 7.5.4 I/O

This RFFE interface supports a 1.8-V VIO supply level. A power-on reset circuit will be included that resets the RFFE interface and register-set components when VIO is removed.

### 7.5.5 Control Interface Timing Parameters

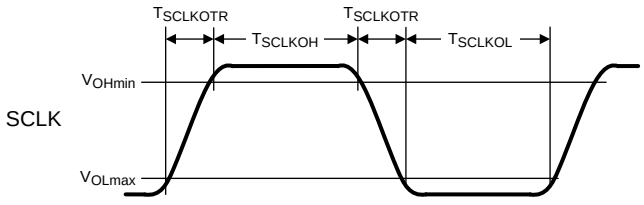



**Figure 22. Clock Timing**


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## Programming (continued)

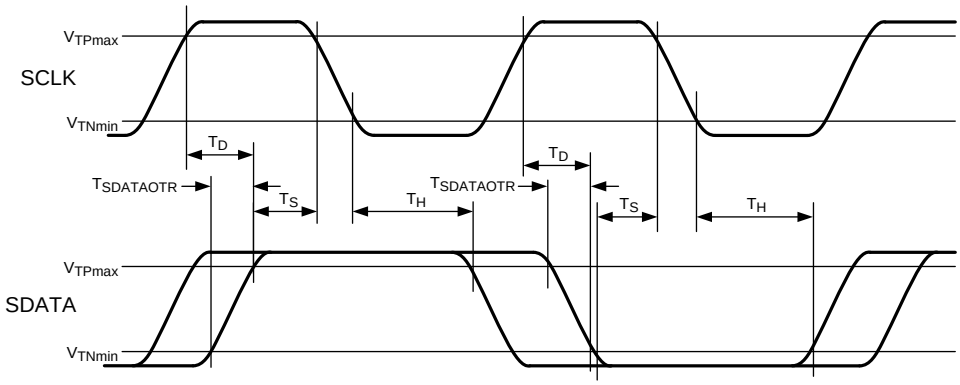



**Figure 23. Setup And Hold Timing**

## 7.6 Registers

### 7.6.1 Programmable Registers

| ADDRESS | REGISTER CONTENTS | | |
|---|---|---|---|
| **00h** | **VSET_CTRL** | | |
| | **Bits** | **Name** | **Description** |
| | 7 | Reserved | Reserved bit. Default = 0. |
| | 6:0 | VSET_CTRL[6:0] | DC-DC voltage control bits. $V_{SET_CTRL}$ = 00h **(default)**puts the part into a low power mode. $V_{SET_CTRL}$ = 02h puts the part in a standby mode. $V_{SET_CTRL}$ = 0Bh corresponds to 0.4 V and 75h corresponds to 4.212 V. |
| **01h** | **STATE_CTRL** | | |
| | **Bits** | **Name** | **Description** |
| | 7:6 | STATE_CTRL[1:0] | PWM and PFM state control bits.<br>00b = Force PFM<br>01b = PFM if $V_{OUT}$ < 1.5 **(default)**<br>10b = PFM if $V_{OUT}$ < 2.1 and $I_{OUT}$ < 100 mA<br>11b = Force PWM |
| | 5:0 | Reserved | |
| **02h** | **GPO_CTRL** | | |
| | **Bits** | **Name** | **Description** |
| | 7 | GPO0 | GPO0 control bit.<br>0b = Output set to low level **(default)**<br>1b = Output set to high level |
| | 6 | GPO1 | GPO1 control bit.<br>0b = Output set to low level **(default)**<br>1b = Output set to high level |
| **03h-1Bh** | **RESERVED** | | |
| | **Bits** | **Name** | **Description** |
| | | | Reserved registers for configuration, test, and trim. |
| **1Ch** | **PM_TRIG** | | |
| | **Bits** | **Name** | **Description** |
| | 7:6 | PWR_MODE[1:0] | Power Mode Bits.<br>00b = Normal operation<br>01b = Default settings **(default)**<br>10b = Low power<br>11b = Reserved |
| | 5:0 | TRIG_REG[5:0] | Reserved for trigger bits. |

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## Registers (continued)

| ADDRESS | REGISTER CONTENTS | | |
|---|---|---|---|
| **1Dh** | **PRODUCT_ID** | | |
| | **Bits** | **Name** | **Description** |
| | 7:0 | PRODUCT_ID[7:0] | Product identification bits. Set to A0h. |
| **1Eh** | **MANUFACTURER_ID** | | |
| | **Bits** | **Name** | **Description** |
| | 7:0 | MANUFACTURER_ID[7:0] | Manufacturer identification bits.<br>7:0 1Eh are LSB for TI. |
| **1Fh** | **USID** | | |
| | **Bits** | **Name** | **Description** |
| | 7:6 | SPARE[1:0] | This is a read-only register that is reserved and yields a value of 00b at readback. Potentially used in future for extending manufacturer ID field. |
| | 5:4 | MANUFACTURER_ID[5:4] | Manufacturer identification bits.<br>5:4 01h are MSB for TI. |
| | 3:0 | USID[3:0] | Unique slave identifier.<br>Default 0101b. |


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LM3279 is a high-efficiency buck boost DC-DC converter optimized to power 3G/4G power amplifier in cell phones, portable communication devices, or other battery-powered RF devices. The device is designed to operate from an input supply voltage between 2.7 V and 5.5 V with a maximum load current of 1 A. It operates in PWM mode for medium-to-heavy load conditions and in PFM mode for light load conditions to optimize for best efficiency, transient performance, and output voltage ripple at varying load conditions. In PWM mode the LM3279 converter operates with nominal switching frequency of 2.4 MHz, thus enabling use of smaller size capacitors and inductor. The converter operates in PFM mode at lighter load conditions to maintain high efficiency. The LM3279 switches between PFM and PWM based on load current and /or the output voltage, and Figure 24 shows one of many application configurations for LM3279. A battery-connected system provides input supply to LM3279 which in turn very efficiently converts this input to a variable output with superior transient response and output noise, thereby saving the 3G/4G power amplifiers from having to operate from a higher supply voltage, such as a direct connection to a battery. This results in significant power dissipation savings and consequently cooler operation and also lower current consumption for the power amplifier without sacrificing its RF performance. In applications where low voltage battery operation is a significant feature; the buck-boost can seamlessly transition to boost and power the 3G/4G PA for high peak-to-average ratio signals as well.

To control the output voltage there are two methods in which the LM3279 can be used : Analog Control where an analog control voltage (VCON) which is equal to VOUT/3 need to feed into the LM3279 from an external DAC. In the digital mode RFFE signaling is used to control the register address 0x00 to set the output voltage, and the LM3279 acts as a slave device on the RFFE bus.

## 8.2 Typical Application

### 8.2.1 Typical Application Circuit: Digital Control

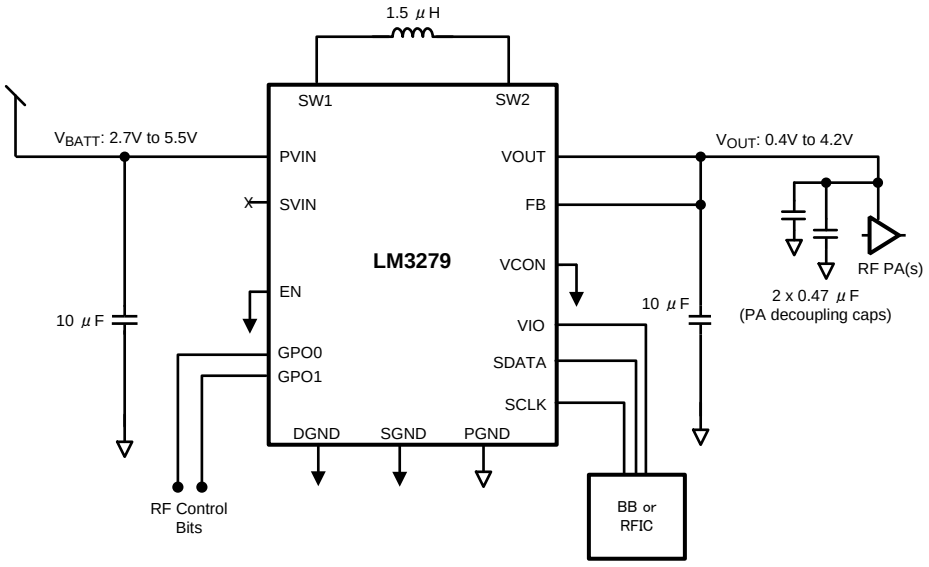



**Figure 24. LM3279 Digital Control**

## Typical Application (continued)

### 8.2.1.1 Design Requirements

The LM3279 buck-boost converter has internal loop compensation. Therefore, the external LC filter has to be selected according to the internal compensation. Nevertheless, it's important to consider, that the effective inductance, due to inductor tolerance and current derating can vary between 20% and –30%. The same for the capacitance of the output filter: the effective capacitance can vary between 20% and –50% of the specified datasheet value, due to capacitor tolerance and bias voltage. For this reason Table 3 and Table 4 show the typical inductor and capacitor used with the LM3279 device.

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Output Current Capability

The typical LM3279 load capability vs. input voltage is as shown in Table 2. There are 3 distinct regions of current capability. In the low output-voltage region, $V_{OUT}$ < 2.1 V (also known as the $R_{DSON}$-managed region), the output-current capability is determined by the current capability of the $R_{DSON}$-managed MOSFET, typically 600 mA. When the output voltage is greater than 2.1 V, and in buck mode, the current capability increases to 1400 mA as determined by the overcurrent limit setting and the magnitude of ripple current. While in boost-mode operation, the output-current capability is determined by the output-input voltage ratio. It is expected for the typical RF PA to have an approximate resistive load characteristic. Refer to Table 2 for output current capability.

**Table 2. Output Voltage vs Maximum Output Current Derating**

| $V_{OUT}$ (V) | $V_{IN}$ (V) | MAXIMUM $I_{OUT}$ CAPABILITY (mA) |
|---|---|---|
| 4.2 | ≤ 3 | 450 |
| | > 3 | 650 |
| 3.8 | ≥ 2.5 | 500 |
| | ≥ 2.7 | 750 |
| | ≥ 3 | 950 |
| 3.4 | ≥ 2.5 | 750 |
| | ≥ 2.7 | 950 |
| | ≥ 3 | 1100 |
| < 1.5 | 2.7 to 5 | 100 (in PFM mode) |

#### 8.2.1.2.2 Recommended External Components

##### 8.2.1.2.2.1 Inductor Selection

A 1.5-µH inductor with a saturation current rating over 1900 mA and low inductance drop at the full DC bias condition is recommended for almost all applications. An inductor with a DC resistance of less than 0.1 Ω and smaller ESR should be used to get good efficiency for all output current conditions.

**Table 3. Suggested Inductors**

| MODEL | VENDOR | DIMENSIONS (mm) | $I_{SAT}$ mA (30% DROP IN INDUCTANCE) | DCR (mΩ) |
|---|---|---|---|---|
| DFE201610C-1R5M (1285A5-H-1R5M) (1.5 µH) | TOKO | 2.0 x 1.6 x 1.0 | 2200 | 120 |
| TFM201610A-1R5M (1.5 µH) | TDK | 2.0 x 1.6 x 1.0 | 2000 | 140 |
| ELGUEA1R5NA (1.5 µH) | Panasonic | 2.0 x 1.6 x 1.0 | 1900 | 100 |


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If a smaller inductance inductor is used in the application, the VOUT transient response time is affected. If a winding type inductor is used, the efficiency at light load current condition may not be so good due to bigger DCR.

#### *8.2.1.2.2.2 Input Capacitor Selection*

A ceramic input capacitor of 10 µF, 6.3V, 0402 or higher is sufficient for most applications. Place the input capacitor as close as possible to the PVIN pin and PGND pin of the device. A larger value of higher voltage rating may be used to improve input filtering. Use X7R, X5R, or B types; do not use Y5V or F. The input filter capacitor supplies current to the PFET (high-side) switch in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current.

#### 8.2.1.2.3 Output Capacitor Selection

Use a 10-µF, 6.3-V, 0402 capacitor for the output capacitor. Use of capacitor types such as X5R, X7R is recommended for the filter. These provide an optimal balance between small size, cost, reliability, and performance for cell phones and similar applications. Table 4 lists suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered while selecting the voltage rating and case size of the capacitor. Smaller case sizes for the output capacitor mitigate piezo-electric vibrations of the capacitor when the output voltage is stepped up and down at fast rates. However, they have a bigger percentage drop in value with DC bias. A 0402 case size output capacitor is recommended for small solution size. For RF Power Amplifier applications, the output capacitor loading is combined between the DC-DC converter and the RF Power Amplifier(s). (10 µF (0402) + PA input cap 3 x 1µF (0402/0201) is recommended.) The optimum capacitance split is application-dependent. Place all the output capacitors very close to their respective device. If using a 4.7 µF, 0402 as the output capacitor, the total recommended actual capacitance on the VOUT bus should be at least > 6.8 µF (4.7 µF + PA decoupling caps), to take into account the 0402 DC bias degradation and other tolerances. The minimum capacitance under DC bias conditions should be > 3 µF.

**Table 4. Suggested Capacitors**

| MODEL | VENDOR |
|---|---|
| **10 µF for $C_{IN}$ = $C_{OUT}$** | |
| CL05A106MQ5NUN (0402) | Samsung |
| **1.0 µF for PA Decoupling Caps (x 3)** | |
| C0603X5R0G105M(0201(0603)) | TDK |
| **0.47 µF for PA Decoupling Caps (x 2)** | |
| GRM033R60J474ME90 (0201(0603)) | Murata |

### *8.2.1.3 Application Curves*

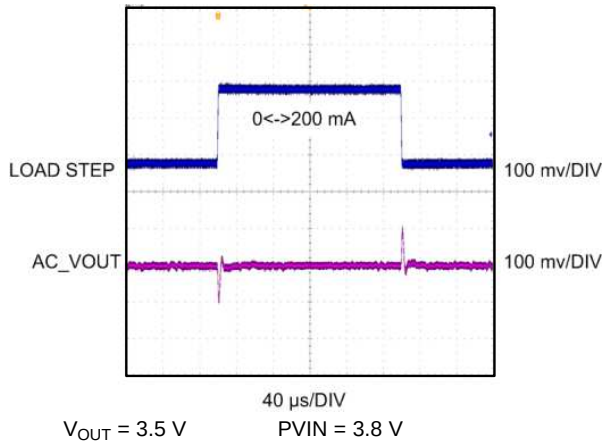



**Figure 25. Load Transient, Forced PWM Mode**

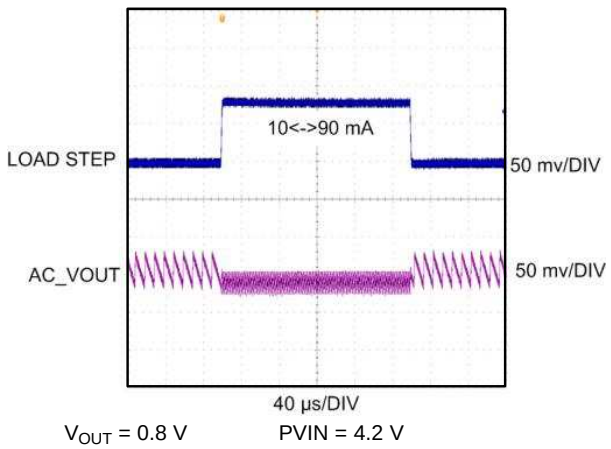



**Figure 26. Load Transient, Forced PFM Mode**

### 8.2.2 Typical Application Circuit: Analog Control

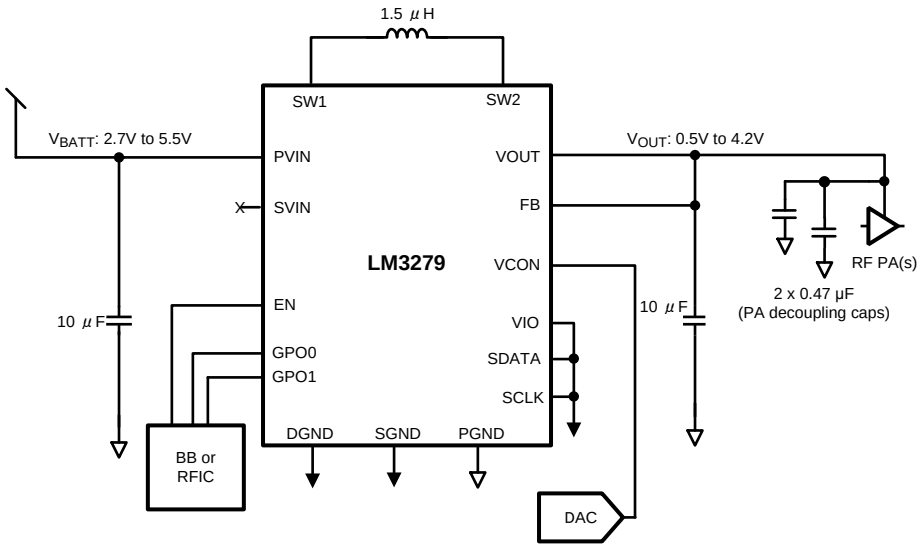



**Figure 27. LM3279 Analog Control**

#### *8.2.2.1 Design Requirements*

See *Design Requirements* above.

#### *8.2.2.2 Detailed Design Procedure*

See *Detailed Design Procedure* above.

#### *8.2.2.3 Application Curves*

See *Application Curves* above.

## 9 Power Supply Recommendations

The LM3279 device is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply should be well regulated. If the input supply is located more than a few inches from the LM3279 converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.


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# 10 Layout

## 10.1 Layout Guidelines

PC board layout is critical to successfully designing a DC-DC converter into a product. As much as a 10-dB improvement in RX noise floor can be achieved by carefully following recommended layout practices. A properly planned board layout optimizes the performance of a DC-DC converter and minimizes effects on surrounding circuitry while also addressing manufacturing issues that can have adverse impacts on board quality and final product yield.

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. Erroneous signals could be sent to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance of the converter.

### 10.1.1 PCB

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. Erroneous signals could be sent to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance of the converter.

#### *10.1.1.1 Energy Efficiency*

Minimize resistive losses by using wide traces between the power components and doubling up traces on multiple layers when possible.

#### *10.1.1.2 EMI*

By its very nature, any switching converter generates electrical noise. The circuit board designer’s challenge is to minimize, contain, or attenuate such switcher-generated noise. A high-frequency switching converter, such as the LM3279, switches Ampere level currents within nanoseconds, and the traces interconnecting the associated components can act as radiating antennas. The following guidelines are offered to help to ensure that EMI is maintained within tolerable levels.

To help minimize radiated noise:

- Place the LM3279 switcher, its input capacitor, and output filter inductor and capacitor close together, and make the interconnecting traces as short as possible.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle (buck mode), current flows from the input filter capacitor, through the internal PFET of the LM3279 and the inductor, to the output filter capacitor, then back through ground, forming a current loop. In the second half of each cycle (buck mode), current is pulled up from ground, through the internal synchronous NFET of the LM3279 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- Make the current loop area(s) as small as possible.

To help minimize conducted noise in the ground-plane:

- Reduce the amount of switching current that circulates through the ground plane: Connect the ground bumps of the LM3279 and its input/output filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this copper fill to the system ground-plane (if one is used) by multiple vias. These multiple vias help to minimize ground bounce at the LM3279 by giving it a low-impedance ground connection.

To help minimize coupling to the DC-DC converter's own voltage feedback trace:

- Route noise sensitive traces, such as the voltage feedback path (FB), as directly as possible from the switcher FB pad to the VOUT pad of the output capacitor, but keep it away from noisy traces between the power components. If possible, connect FB bump directly to VOUT bump.

To decouple common power supply lines, series impedances may be used to strategically isolate circuits:

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## Layout Guidelines (continued)

- Take advantage of the inherent inductance of circuit traces to reduce coupling among function blocks, by way of the power supply traces.
- Use star connection for separately routing VBATT to PVIN and VBATT_PA (VCC1).
- Inserting a single ferrite bead in-line with a power supply trace may offer a favorable tradeoff in terms of board area, by allowing the use of fewer bypass capacitors.

Use a star connection from VBATT to LM3279 and VBATT to PA VBATT (VCC1) connection. Do not daisy-chain VBATT connection to LM3279 circuit and then to PA device VBATT connection.

## 10.2 Layout Examples

**Top Layer** (Figure 28)

1. Create a PGND island as shown. PGND pads of C2 (CIN) and C3 (COUT) must be isolated from each other. This PGND island will connect to the dedicated system ground with many vias.
2. Each SW (C3) and (D4) bump will have a via in pad and an additional via next to it, to drop down the SW trace to layer 3.
3. SGND bump (C2) and GND (D1) will have a via in pad, and directly connecting it to the system ground.
4. FB (C2) should connect directly to the VOUT bump (D1).
5. Have PVIN vias next to optional ferrite bead.

**Layer 2** (Figure 29)

6. Digital logic signals may be routed on this layer.
7. PVIN for the LM3279 can be routed on this layer.
8. VCC2 can be routed on this layer.

**Layer 3** (Figure 30)

9. Each SW trace is routed on this layer. The width of each trace should be 15 mils (0.381 mm) for current capabilities. Have two vias bring each SW trace up to the inductor pads.

**Layer 4** (Figure 31)

10. Connect the PGND, SGND, and high Frequency vias from the top layer on this layer.


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## Layout Examples (continued)

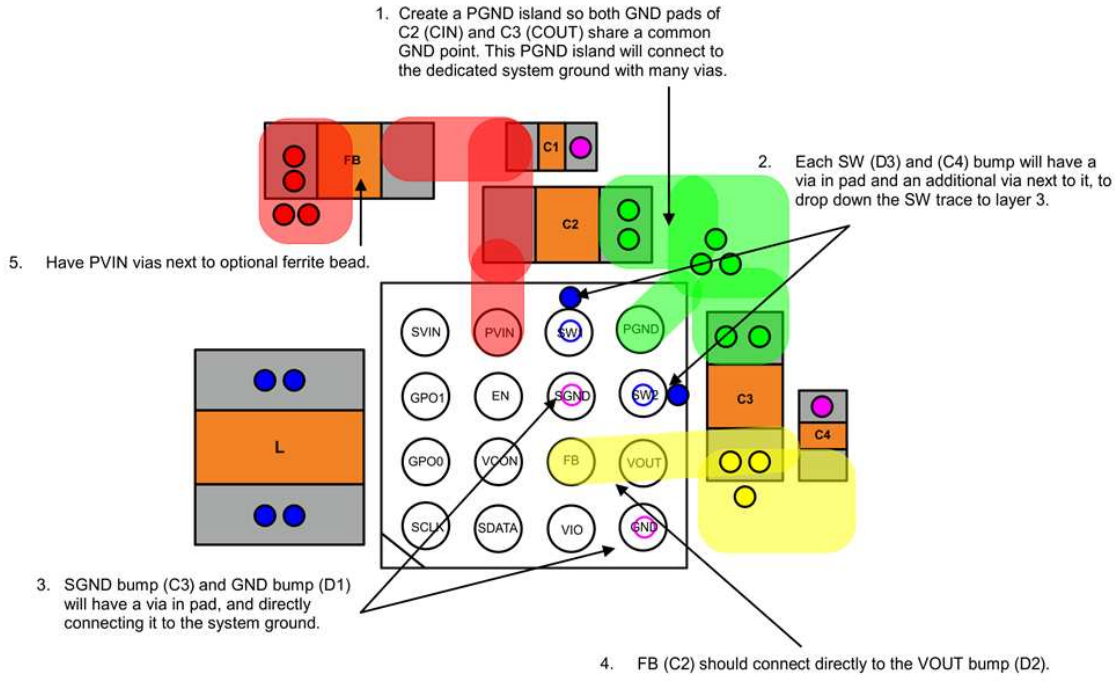



**Figure 28. Top Layer**

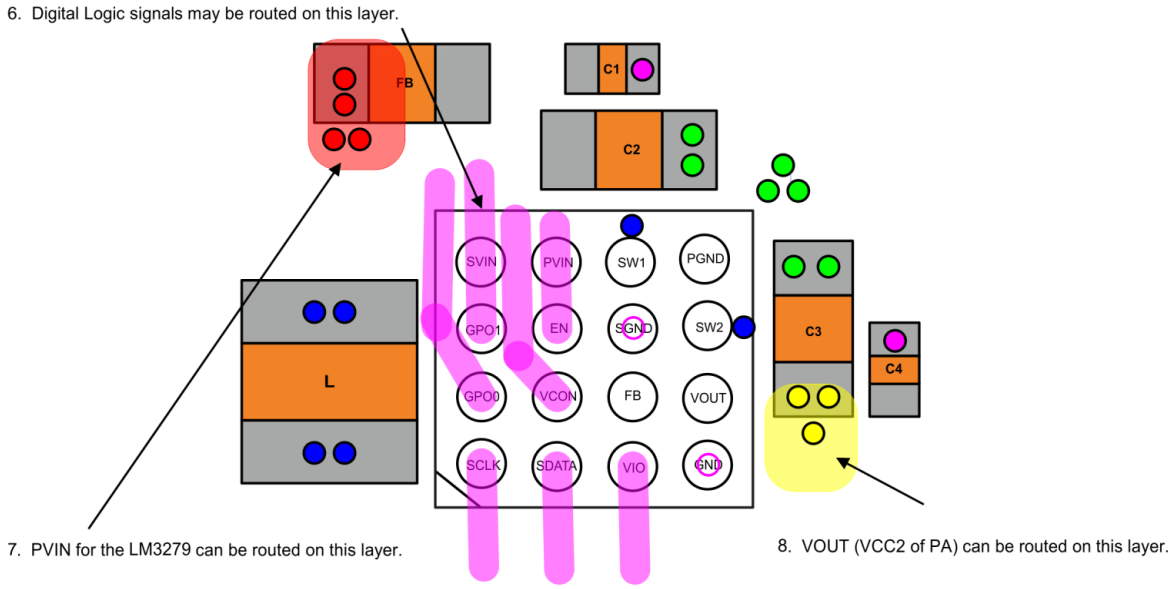



**Figure 29. Board Layer 2 - Logic And PVIN Routing**

## Layout Examples (continued)

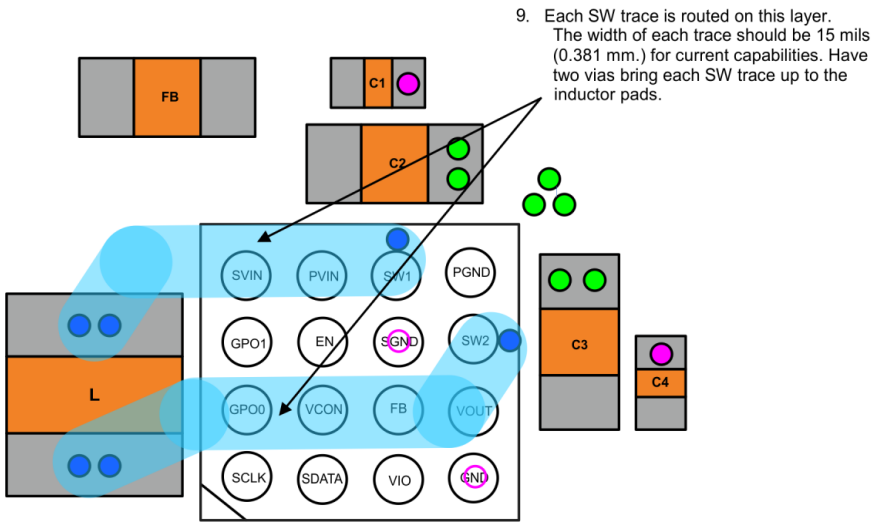



**Figure 30. Board Layer 3 - SW Routing**

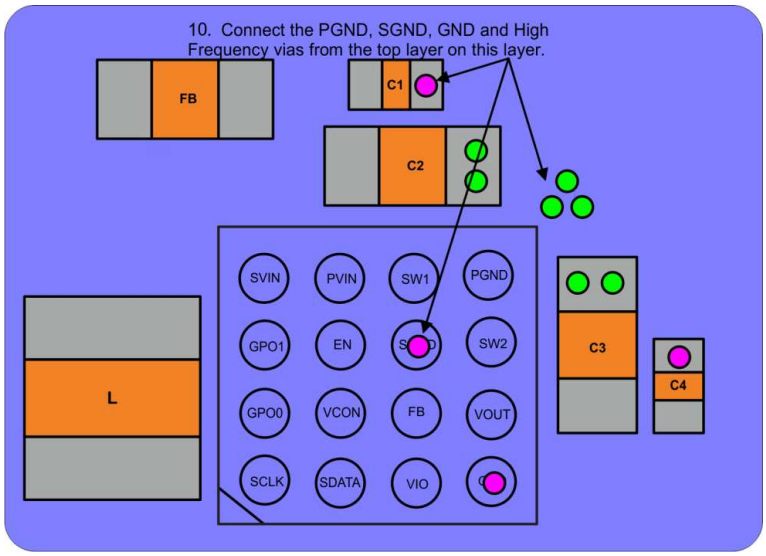



**Figure 31. Board Layer 4 - System GND Plane**


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## Layout Examples (continued)

### 10.2.1 LM3279 RF Evaluation Board

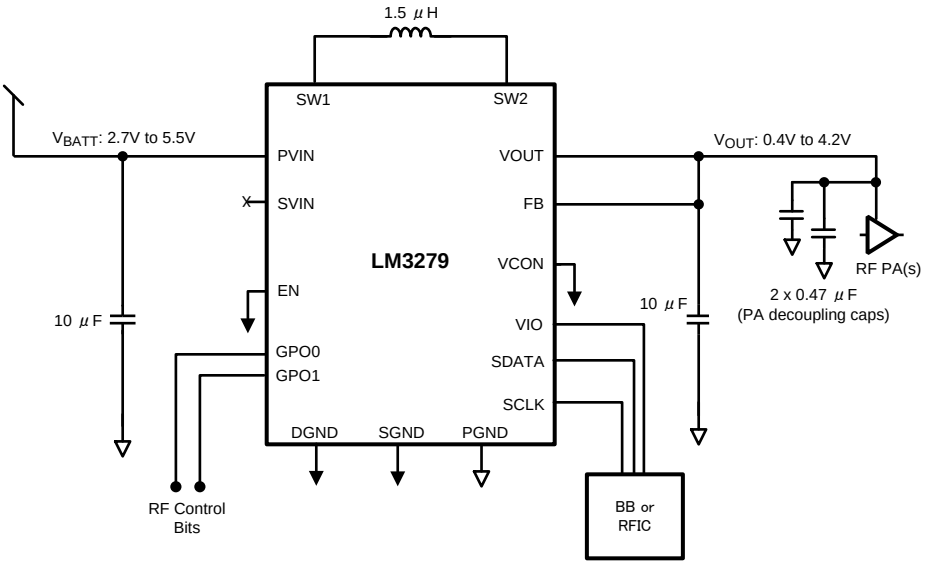



**Figure 32. Simplified LM3279 RF Evaluation Board Schematic**

1. Input Capacitor C2 should be placed closer to LM3279 than C1.
2. Optional to add a 100 nF (C1) on input of LM3279 for high frequency filtering.
3. Bulk Output Capacitor C3 should be placed closer to LM3279 than C4.
4. Optional to add a 100 nF (C4) on output of LM3279 for high frequency filtering.
5. Connect both GND terminals of C1 and C4 directly to System RF GND layer of phone board.
6. Connect bumps SGND (C3) and GND (D1) directly to System GND.
7. TI has seen improvement in high frequency filtering for small bypass caps (C1 and C4) when they are connected to System GND instead of same ground as PGND. These capacitors should be 0201 (0603 metric) case size for minimum footprint and best high frequency characteristics.

### 10.2.2 Component Placement

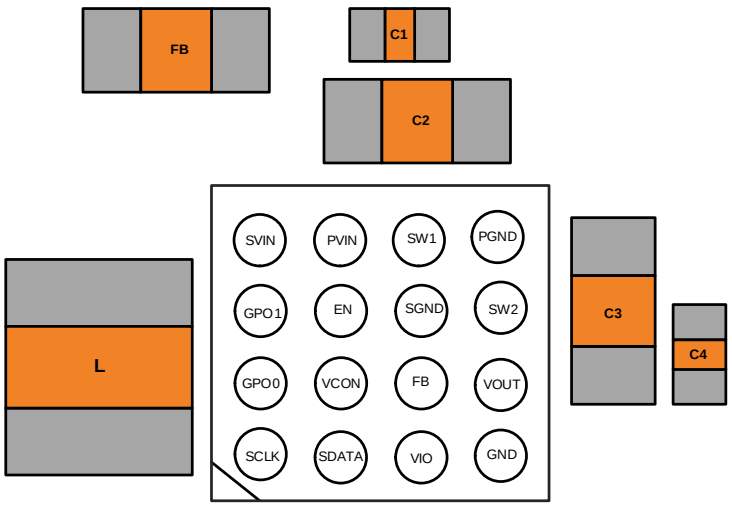



**Figure 33. LM3279 Recommended Parts Placement (Top View)**

## 10.3 DSBGA Package Assembly And Use

Use of the DSBGA package requires specialized board layout, precision mounting, and careful re-flow techniques, as detailed in Texas Instruments Application Note 1112 (SNVA009). Refer to the section *Surface Mount Technology (SMD) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap from holding the device off the surface of the board and interfering with mounting. See SNVA009 for specific instructions how to do this.

The 16-bump package used for the LM3279 has 300 micron solder balls and requires 10.82 mil pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 9 mil wide, for a section approximately 9 mil long, as a thermal relief. Then each trance should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3279 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps B4 and D4. Because PVIN and PGND are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light (in the red and infrared range) shining on the package's exposed die edges.

## 10.4 Manufacturing Considerations

The LM3279 package employs a 16-bump (4x4) array of 300 micron solder balls, with a 0.5-mm pad pitch. A few simple design rules will go a long way to ensuring a good layout.

- Pad size should be 0.265 ± 0.02 mm. Solder mask opening should be 0.375 ± 0.02 mm.
- As a thermal relief, connect to each pad with 9.5 mil wide, 5 mil long traces and incrementally increase each trace to its optimal width. Symmetry is important to ensure the solder bumps re-flow evenly. Refer to TI Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).


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# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Third-Party Products Disclaimer

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## 11.2 Documentation Support

### 11.2.1 Related Documentation

See TI Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009) for general information about the DSBGA package.

## 11.3 Trademarks

MIPI is a registered trademark of Mobil Industry Processor Interface Alliance .
All other trademarks are the property of their respective owners.

## 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3279TLE/NOPB | ACTIVE | DSBGA | YZR | 16 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | SJ4B | Samples |
| LM3279TLX/NOPB | ACTIVE | DSBGA | YZR | 16 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -30 to 85 | SJ4B | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

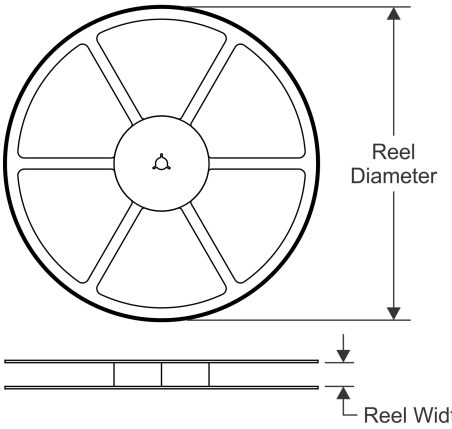
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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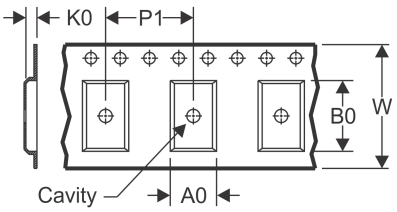
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

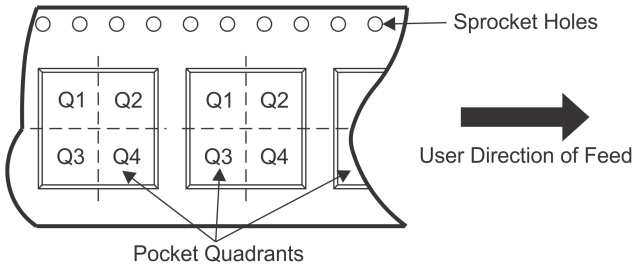



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

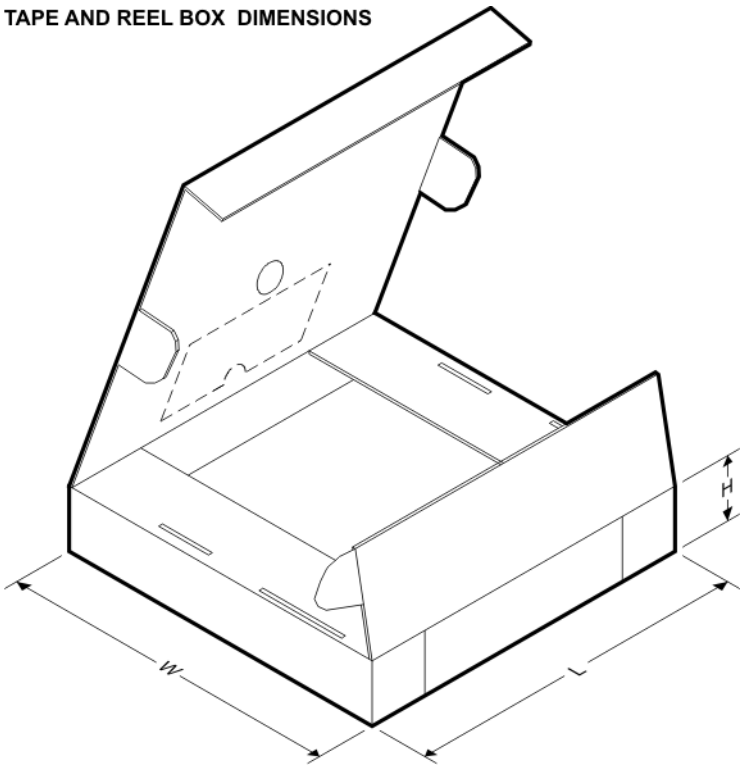
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3279TLE/NOPB | DSBGA | YZR | 16 | 250 | 178.0 | 8.4 | 2.18 | 2.69 | 0.76 | 4.0 | 8.0 | Q1 |
| LM3279TLX/NOPB | DSBGA | YZR | 16 | 3000 | 178.0 | 8.4 | 2.18 | 2.69 | 0.76 | 4.0 | 8.0 | Q1 |

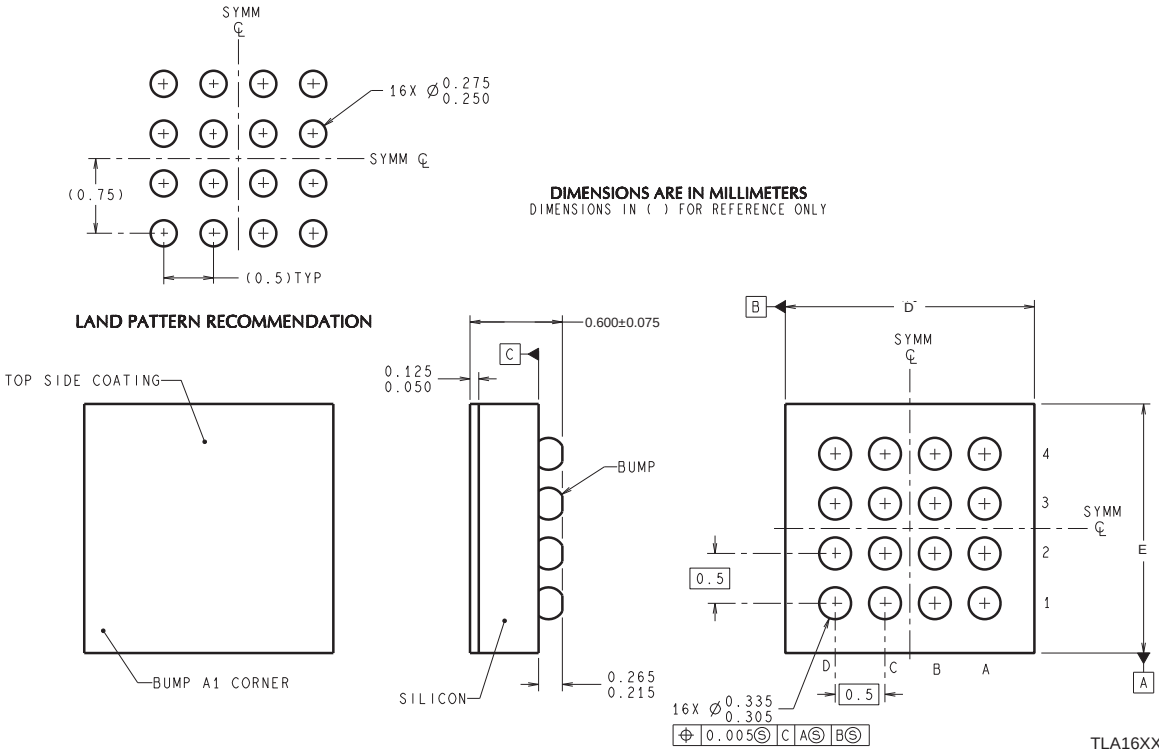
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM3279TLE/NOPB | DSBGA | YZR | 16 | 250 | 210.0 | 185.0 | 35.0 |
| LM3279TLX/NOPB | DSBGA | YZR | 16 | 3000 | 210.0 | 185.0 | 35.0 |

# YZR0016




D: Max = 2.529 mm, Min =2.469 mm

E: Max = 2.146 mm, Min =2.086 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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