- **Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, $I_O = \pm 8$ mA**
- **Very Low Power . . . 200 μW Typ at 5 V**
- **Fast Response Time . . . $t_{PLH}$ = 2.7 μs Typ With 5-mV Overdrive**
- **Single Supply Operation . . . 3 V to 16 V**
  **TLC3704M . . . 4 V to 16 V**
- **On-Chip ESD Protection**

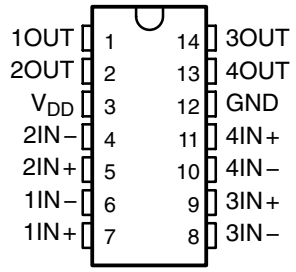
## description

The TLC3704 consists of four independent micropower voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. They are functionally similar to the LM339 but use 1/20th the power for similar response times. The push-pull CMOS output stage drives capacitive loads directly without a power-consuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

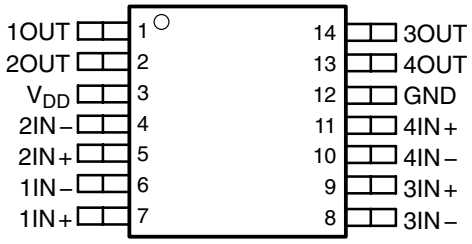
Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS process offers extremely stable input offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.

The TLC3704C is characterized for operation over the commercial temperature range of 0°C to 70°C. The TLC3704I is characterized for operation over the extended industrial temperature range of – 40°C to 85°C. The TLC3704M is characterized for operation over the full military temperature range of – 55°C to 125°C. The TLC3704Q is characterized for operation from – 40°C to 125°C.

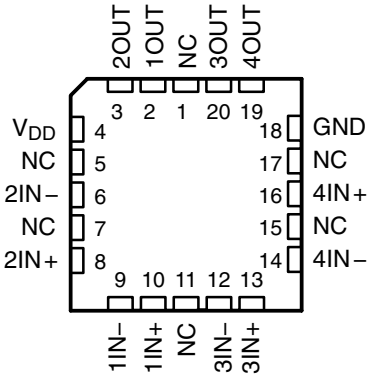
**D, J, OR N PACKAGE**
**(TOP VIEW)**




**PW PACKAGE**
**(TOP VIEW)**

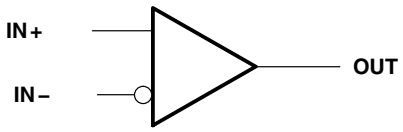



**FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## symbol (each comparator)

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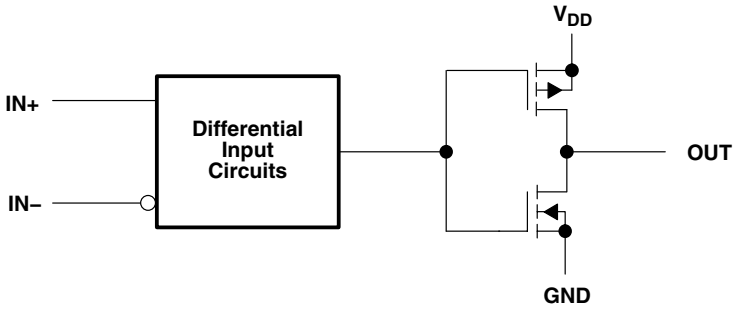
**AVAILABLE OPTIONS**

| $T_A$ | $V_{IO}$max at 25°C | PACKAGE | | | | |
|---|---|---|---|---|---|---|
| | | SMALL OUTLINE (D) | CERAMIC (FK) | CERAMIC DIP (J) | PLASTIC DIP (N) | TSSOP (PW) |
| 0°C to 70°C | 5 mV | TLC3704CD | — | — | TLC3704CN | TLC3704CPW |
| –40°C to 85°C | 5 mV | TLC3704ID | — | — | TLC3704IN | TLC3704IPW |
| –55°C to 125°C | 5 mV | TLC3704MD | TLC3704MFK | TLC3704MJ | — | — |
| –40°C to 125°C | 5 mV | — | — | TLC3704QJ | — | — |

The D and PW packages are available taped and reeled. Add R suffix to the device type (e.g., TLC3704CDR).

## functional block diagram (each comparator)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{DD}$ (see Note 1) . . . . . –0.3 V to 18 V
Differential input voltage, $V_{ID}$ (see Note 2) . . . . . ± 18 V
Input voltage range, $V_I$ . . . . . –0.3 to $V_{DD}$
Output voltage range, $V_O$ . . . . . –0.3 to $V_{DD}$
Input current, $I_I$ . . . . . ±5 mA
Output current, $I_O$ (each output) . . . . . ±20 mA
Total supply current into $V_{DD}$ . . . . . 40 mA
Total current out of GND . . . . . 60 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$: TLC3704C . . . . . 0 to 70°C
TLC3704I . . . . . –40°C to 85°C
TLC3704M . . . . . –55°C to 125°C
TLC3704Q . . . . . –40°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|
| D | 950 mW | 7.6 mW/°C | 608 mW | 494 mW | N/A |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 275 mW |
| J | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 275 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW | N/A |
| PW | 675 mW | 5.4 mW/°C | 432 mW | 351 mW | N/A |

## recommended operating conditions

| | TLC3704C | | | UNIT |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| Supply voltage, $V_{DD}$ | 3 | 5 | 16 | V |
| Common-mode input voltage, $V_{IC}$ | – 0.2 | | $V_{DD}$ – 1.5 | V |
| High-level output current, $I_{OH}$ | | | – 20 | mA |
| Low-level output current, $I_{OL}$ | | | 20 | mA |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | $T_A$ | TLC3704C | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{DD}$ = 5 V to 10 V, $V_{IC} = V_{ICR}$min, | See Note 3 | 25°C | | 1.2 | 5 | mV |
| | | | | 0°C to 70°C | | | 6.5 | |
| $I_{IO}$ | Input offset current | $V_{IC}$ = 2.5 V | | 25°C | | 1 | | pA |
| | | | | 70°C | | | 0.3 | nA |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 2.5 V | | 25°C | | 5 | | pA |
| | | | | 70°C | | | 0.6 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | | 25°C | 0 to $V_{DD}$ – 1 | | | V |
| | | | | 0°C to 70°C | 0 to $V_{DD}$ – 1.5 | | | |
| CMRR | Common-mode rejection ratio | $V_{IC} = V_{ICR}$min | | 25°C | | 84 | | dB |
| | | | | 70°C | | 84 | | |
| | | | | 0°C | | 84 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio | $V_{DD}$ = 5 V to 10 V | | 25°C | | 85 | | dB |
| | | | | 70°C | | 85 | | |
| | | | | 0°C | | 85 | | |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 1 V, | $I_{OH}$ = –4 mA | 25°C | 4.5 | 4.7 | | V |
| | | | | 70°C | 4.3 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = –1 V, | $I_{OH}$ = 4 mA | 25°C | | 210 | 300 | mV |
| | | | | 70°C | | | 375 | |
| $I_{DD}$ | Supply current (all four comparators) | Outputs low, | No load | 25°C | | 35 | 80 | µA |
| | | | | 0°C to 70°C | | | 100 | |

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

## recommended operating conditions

| | TLC3704I | | | UNIT |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| Supply voltage, $V_{DD}$ | 3 | 5 | 16 | V |
| Common-mode input voltage, $V_{IC}$ | – 0.2 | | $V_{DD}$ – 1.5 | V |
| High-level output current, $I_{OH}$ | | | – 20 | mA |
| Low-level output current, $I_{OL}$ | | | 20 | mA |
| Operating free-air temperature, $T_A$ | – 40 | | 85 | °C |

## electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V, $V_{IC}$ = 0 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | TLC3704I | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{DD}$ = 5 V to 10 V, $V_{IC} = V_{ICR}$min, | See Note 3 | 25°C | | 1.2 | 5 | mV |
| | | | | –40°C to 85°C | | | 7 | |
| $I_{IO}$ | Input offset current | $V_{IC}$ = 2.5 V | | 25°C | | 1 | | pA |
| | | | | 85°C | | | 1 | nA |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 2.5 V | | 25°C | | 5 | | pA |
| | | | | 85°C | | | 2 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | | 25°C | 0 to $V_{DD}$ – 1 | | | V |
| | | | | –40°C to 85°C | 0 to $V_{DD}$ – 1.5 | | | |
| CMRR | Common-mode rejection ratio | $V_{IC} = V_{ICR}$min | | 25°C | | 84 | | dB |
| | | | | 85°C | | 84 | | |
| | | | | –40°C | | 83 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio | $V_{DD}$ = 5 V to 10 V | | 25°C | | 85 | | dB |
| | | | | 85°C | | 85 | | |
| | | | | –40°C | | 83 | | |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 1 V, | $I_{OH}$ = –4 mA | 25°C | 4.5 | 4.7 | | V |
| | | | | 85°C | 4.3 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = –1 V, | $I_{OH}$ = 4 mA | 25°C | | 210 | 300 | mV |
| | | | | 85°C | | | 400 | |
| $I_{DD}$ | Supply current (all four comparators) | Outputs low, | No load | 25°C | | 35 | 80 | µA |
| | | | | –40°C to 85°C | | | 125 | |

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

## recommended operating conditions

| | TLC3704M | | | UNIT |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| Supply voltage, $V_{DD}$ | 4 | 5 | 16 | V |
| Common-mode input voltage, $V_{IC}$ | 0 | | $V_{DD}$ – 1.5 | V |
| High-level output current, $I_{OH}$ | | | – 20 | mA |
| Low-level output current, $I_{OL}$ | | | 20 | mA |
| Operating free-air temperature, $T_A$ | – 55 | | 125 | °C |

## electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V, $V_{IC}$ = 0 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ | TLC3704M | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{DD}$ = 5 V to 10 V, $V_{IC} = V_{ICR}$min, | See Note 3 | 25°C | | 1.2 | 5 | mV |
| | | | | –55°C to 125°C | | | 10 | |
| $I_{IO}$ | Input offset current | $V_{IC}$ = 2.5 V | | 25°C | | 1 | | pA |
| | | | | 125°C | | | 15 | nA |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 2.5 V | | 25°C | | 5 | | pA |
| | | | | 125°C | | | 30 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | | 25°C | 0 to $V_{DD}$ – 1 | | | V |
| | | | | –55°C to 125°C | 0 to $V_{DD}$ – 1.5 | | | |
| CMRR | Common-mode rejection ratio | $V_{IC} = V_{ICR}$min | | 25°C | | 84 | | dB |
| | | | | 125°C | | 83 | | |
| | | | | –55°C | | 82 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio | $V_{DD}$ = 5 V to 10 V | | 25°C | | 85 | | dB |
| | | | | 125°C | | 85 | | |
| | | | | –55°C | | 82 | | |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 1 V, | $I_{OH}$ = –4 mA | 25°C | 4.5 | 4.7 | | V |
| | | | | 125°C | 4.2 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = –1 V, | $I_{OH}$ = 4 mA | 25°C | | 210 | 300 | mV |
| | | | | 125°C | | | 500 | |
| $I_{DD}$ | Supply current (all four comparators) | Outputs low, | No load | 25°C | | 35 | 80 | μA |
| | | | | –55°C to 125°C | | | 175 | |

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

## recommended operating conditions

| | TLC3704Q | | | UNIT |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| Supply voltage, $V_{DD}$ | 3 | 5 | 16 | V |
| Common-mode input voltage, $V_{IC}$ | –0.2 | | $V_{DD}$ – 1.5 | V |
| High-level output current, $I_{OH}$ | | | – 20 | mA |
| Low-level output current, $I_{OL}$ | | | 20 | mA |
| Operating free-air temperature, $T_A$ | – 40 | | 125 | °C |

## electrical characteristics at specified operating free-air temperature, $V_{DD}$ = 5 V, $V_{IC}$ = 0 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | TLC3704Q | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_{DD}$ = 5 V to 10 V, $V_{IC} = V_{ICR}$min, See Note 3 | 25°C | | 1.2 | 5 | mV |
| | | | –40°C to 125°C | | | 7 | |
| $I_{IO}$ | Input offset current | $V_{IC}$ = 2.5 V | 25°C | | 1 | | pA |
| | | | 125°C | | | 15 | nA |
| $I_{IB}$ | Input bias current | $V_{IC}$ = 2.5 V | 25°C | | 5 | | pA |
| | | | 125°C | | | 30 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | 25°C | 0 to $V_{DD}$ – 1 | | | V |
| | | | –40°C to 125°C | 0 to $V_{DD}$ – 1.5 | | | |
| CMRR | Common-mode rejection ratio | $V_{IC} = V_{ICR}$min | 25°C | | 84 | | dB |
| | | | 125°C | | 83 | | |
| | | | –40°C | | 83 | | |
| $k_{SVR}$ | Supply-voltage rejection ratio | $V_{DD}$ = 5 V to 10 V | 25°C | | 85 | | dB |
| | | | 125°C | | 85 | | |
| | | | –40°C | | 83 | | |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 1 V, $I_{OH}$ = –4 mA | 25°C | 4.5 | 4.7 | | V |
| | | | 125°C | 4.2 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = –1 V, $I_{OH}$ = 4 mA | 25°C | | 210 | 300 | mV |
| | | | 125°C | | | 500 | |
| $I_{DD}$ | Supply current (all four comparators) | Outputs low, No load | 25°C | | 35 | 80 | µA |
| | | | –40°C to 125°C | | | 175 | |

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

## switching characteristics, $V_{DD}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TLC3704C, TLC3704I TLC3704M, TLC3704Q | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output† | f = 10 kHz, $C_L$ = 50 pF | Overdrive = 2 mV | | 4.5 | | µs |
| | | | Overdrive = 5 mV | | 2.7 | | |
| | | | Overdrive = 10 mV | | 1.9 | | |
| | | | Overdrive = 20 mV | | 1.4 | | |
| | | | Overdrive = 40 mV | | 1.1 | | |
| | | $V_I$ = 1.4-V step at IN+ | | | 1.1 | | |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output† | f = 10 kHz, $C_L$ = 50 pF | Overdrive = 2 mV | | 4 | | µs |
| | | | Overdrive = 5 mV | | 2.3 | | |
| | | | Overdrive = 10 mV | | 1.5 | | |
| | | | Overdrive = 20 mV | | 0.95 | | |
| | | | Overdrive = 40 mV | | 0.65 | | |
| | | $V_I$ = 1.4-V step at IN+ | | | 0.15 | | |
| $t_f$ | Fall time | f = 10 kHz, $C_L$ = 50 pF | Overdrive = 50 mV | | 50 | | ns |
| $t_r$ | Rise time | f = 10 kHz, $C_L$ = 50 pF | Overdrive = 50 mV | | 125 | | ns |

† Simultaneous switching of inputs causes degradation in output response.

## PRINCIPLES OF OPERATION

### LinCMOS process

The LinCMOS process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS products. Direct further questions to the nearest TI field sales office.

### electrostatic discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, e.g., during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages tends to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 1. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD-protection circuit is presented on the next page.

All input and output pins on LinCMOS and Advanced LinCMOS products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a 1500-Ω resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

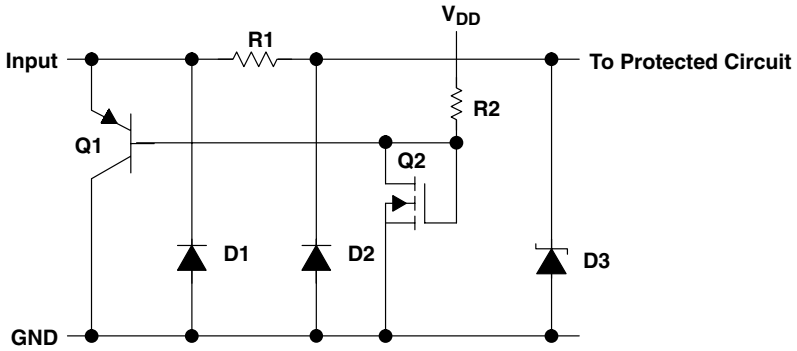



**Figure 1. LinCMOS ESD-Protection Schematic**

## PRINCIPLES OF OPERATION

### input protection circuit operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

### positive ESD transients

Initial positive charged energy is shunted through Q1 to $V_{SS}$. Q1 turns on when the voltage at the input rises above the voltage on the $V_{DD}$ pin by a value equal to the $V_{BE}$ of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level ($V_T$ ~ 22 to 26 V) and turn Q2 on. The shunted input current through Q1 to $V_{SS}$ is now shunted through the n-channel enhancement-type MOSFET Q2 to $V_{SS}$. If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded, and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

### negative ESD transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is – 0.3 V to –1 V (the forward voltage of D1 and D2).

### circuit-design considerations

LinCMOS products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed $V_{ICR}$ and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ±5 mA. Figures 2 and 3 show typical characteristics for input voltage versus input current.

Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limits the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the $V_{DD}$ pin and into the device $I_{DD}$ or the $V_{DD}$ supply through R2 producing the current limiting effects shown in Figure 2. This internal limiting lasts only as long as the input voltage is below the $V_T$ of Q2.

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 4).

## PRINCIPLES OF OPERATION

### circuit-design considerations (continued)

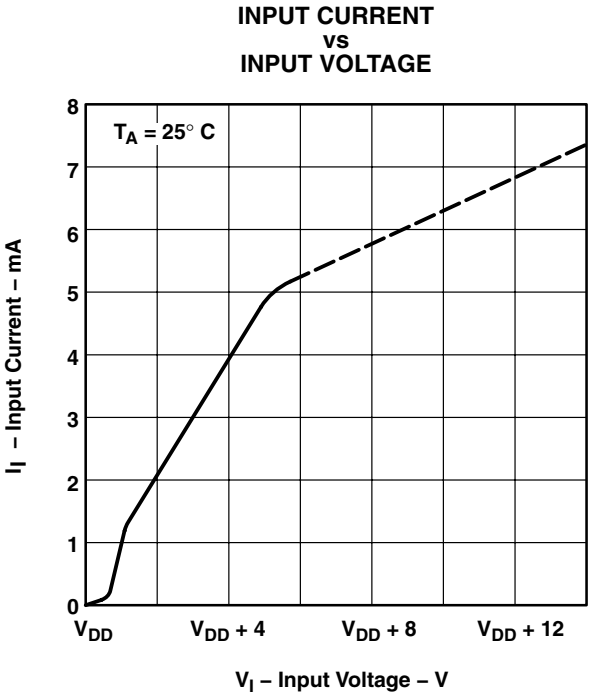



Figure 2

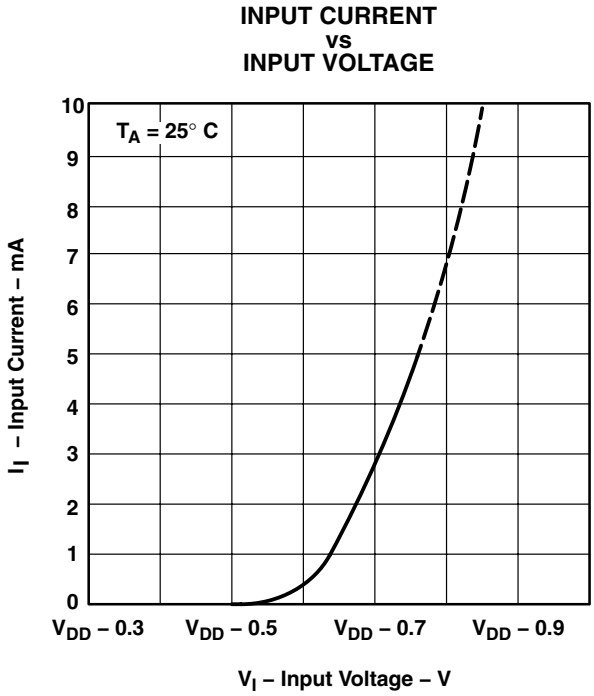
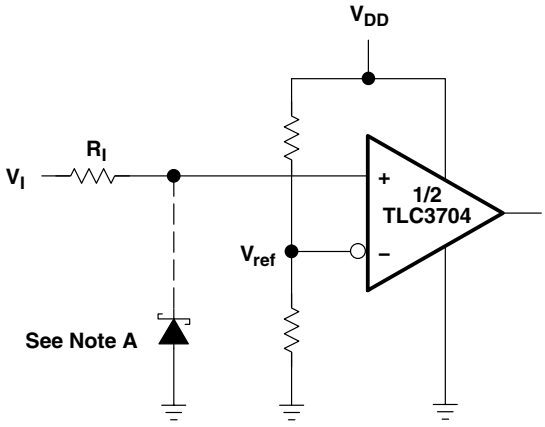



Figure 3




**Positive Voltage Input Current Limit :**

$$R_I = \frac{V_I - V_{DD} - 0.3\ V}{5\ mA}$$

**Negative Voltage Input Current Limit :**

$$R_I = \frac{-V_I - V_{DD} - (-0.3\ V)}{5\ mA}$$

NOTE A: If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required.

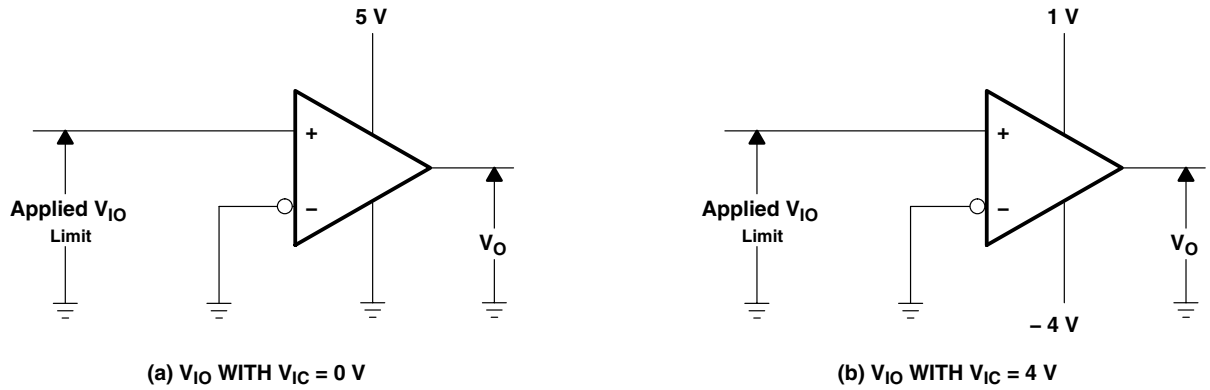
**Figure 4. Typical Input Current-Limiting Configuration for a LinCMOS Comparator**

## PARAMETER MEASUREMENT INFORMATION

The TLC3704 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, we offer the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 5(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 5(b) for the $V_{ICR}$ test, rather than changing the input voltages, to provide greater accuracy.




(a) $V_{IO}$ WITH $V_{IC}$ = 0 V

(b) $V_{IO}$ WITH $V_{IC}$ = 4 V

**Figure 5. Method for Verifying That Input Offset Voltage Is Within Specified Limits**

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 6 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual d.c. offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R8 and R9 provides an increase in the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

## PARAMETER MEASUREMENT INFORMATION

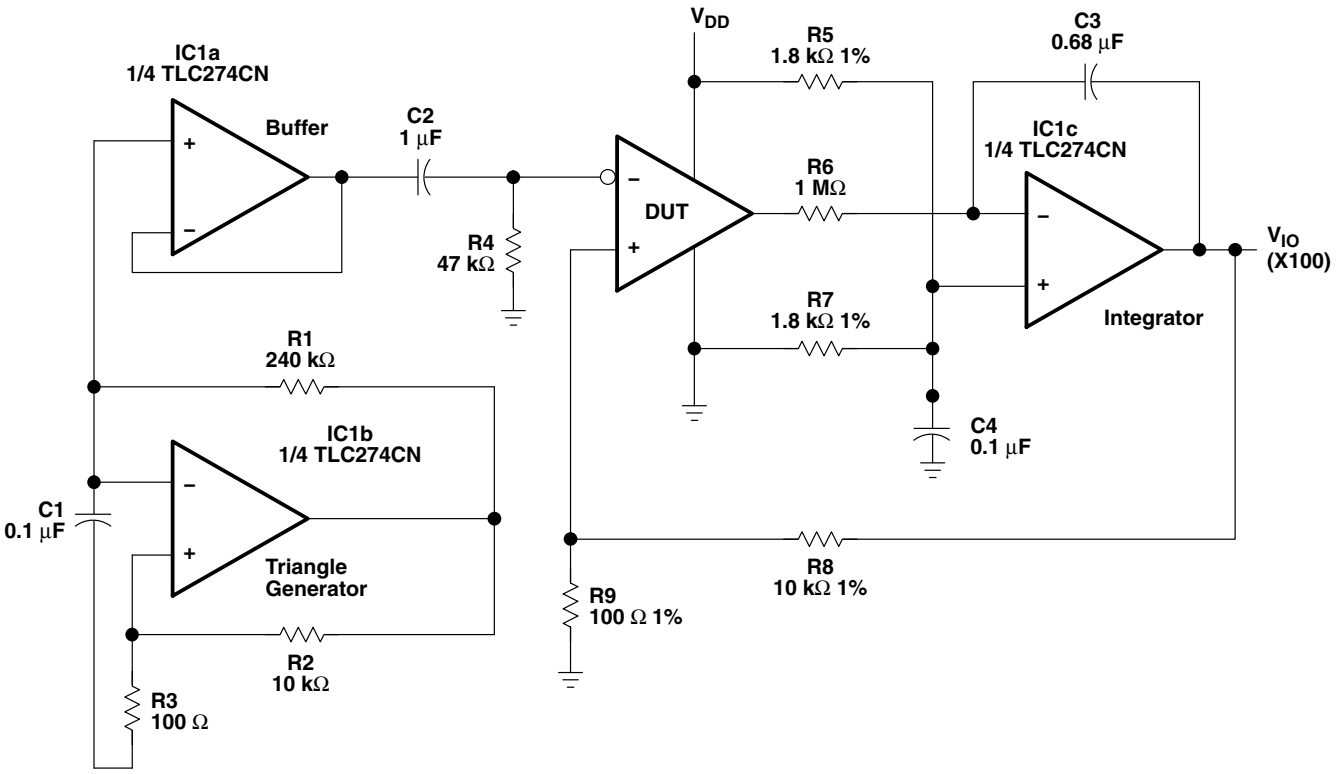
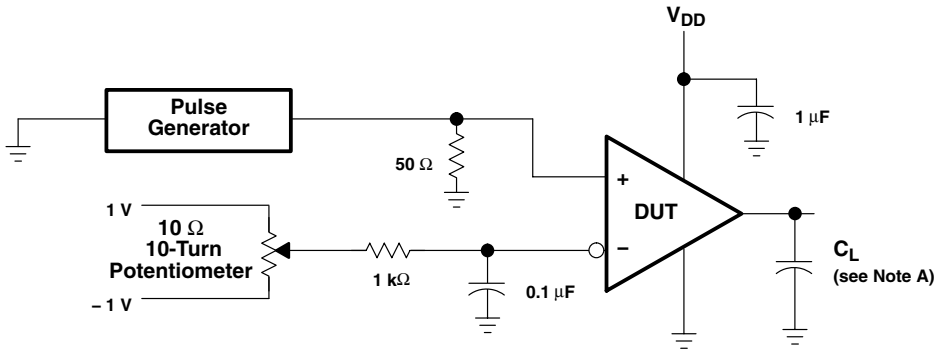


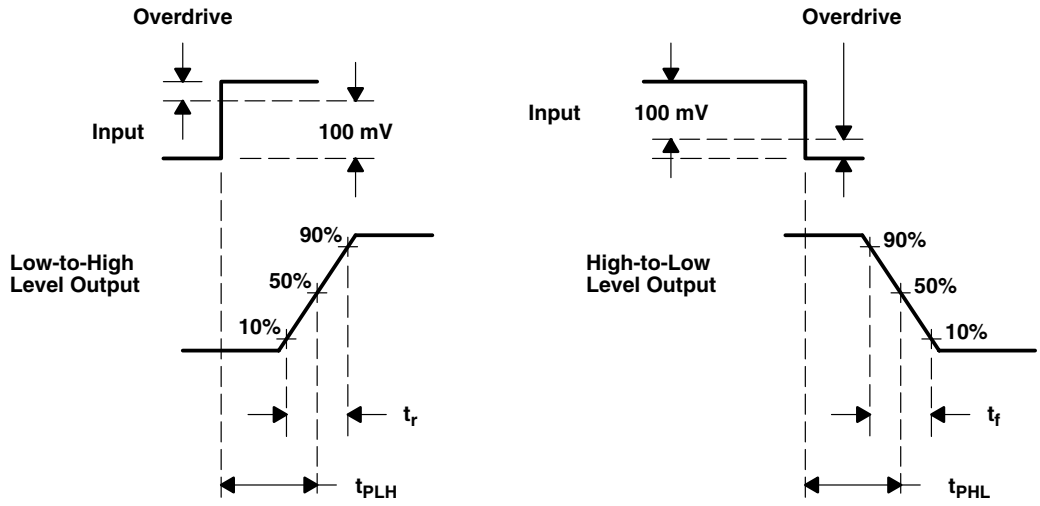

**Figure 6. Circuit for Input Offset Voltage Measurement**

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time for the low-to-high-level output is measured from the leading edge of the input pulse, while response time for the high-to-low-level output is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 7, so that the circuit is just at the transition point. A low signal, for example 105-mV or 5-mV overdrive, causes the output to change state.

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTE A: $C_L$ includes probe and jig capacitance.

**Figure 7. Response, Rise, and Fall Times Circuit and Voltage Waveforms**

## TYPICAL CHARACTERISTICS

### Table of Graphs

| | | | FIGURE |
|---|---|---|---|
| $V_{IO}$ | Input offset voltage | Distribution | 8 |
| $I_{IB}$ | Input bias current | vs Free-air temperature | 9 |
| CMRR | Common-mode rejection ratio | vs Free-air temperature | 10 |
| $k_{SVR}$ | Supply-voltage rejection ratio | vs Free-air temperature | 11 |
| $V_{OH}$ | High-level output current | vs Free-air temperature<br>vs High-level output current | 12<br>13 |
| $V_{OL}$ | Low-level output voltage | vs Low-level output current<br>vs Free-air temperature | 14<br>15 |
| $t_t$ | Output transition time | vs Load capacitance | 16 |
| | Supply current response to an output voltage transition | | 17 |
| | Low-to-high-level output response for various input overdrives | | 18 |
| | High-to-low-level output response for various input overdrives | | 19 |
| $t_{PLH}$ | Low-to-high-level output response time | vs Supply voltage | 20 |
| $t_{PHL}$ | High-to-low-level output response time | vs Supply voltage | 21 |
| $I_{DD}$ | Supply current | vs Frequency<br>vs Supply voltage<br>vs Free-air temperature | 22<br>23<br>24 |

**DISTRIBUTION OF INPUT OFFSET VOLTAGE†**

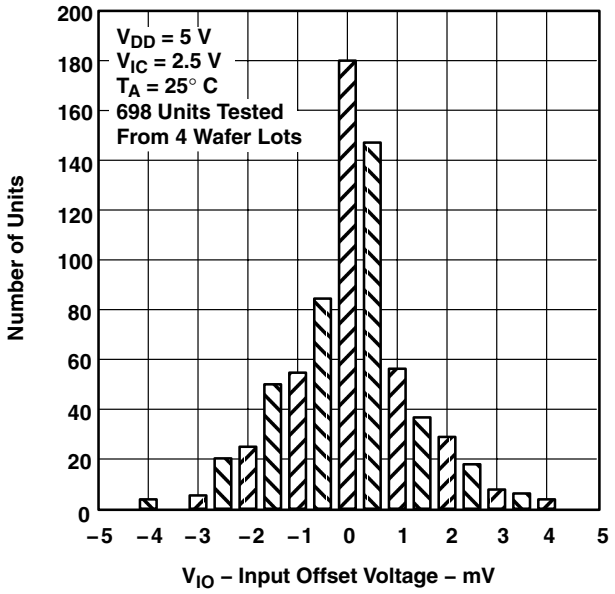



**Figure 8**

**INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE†**

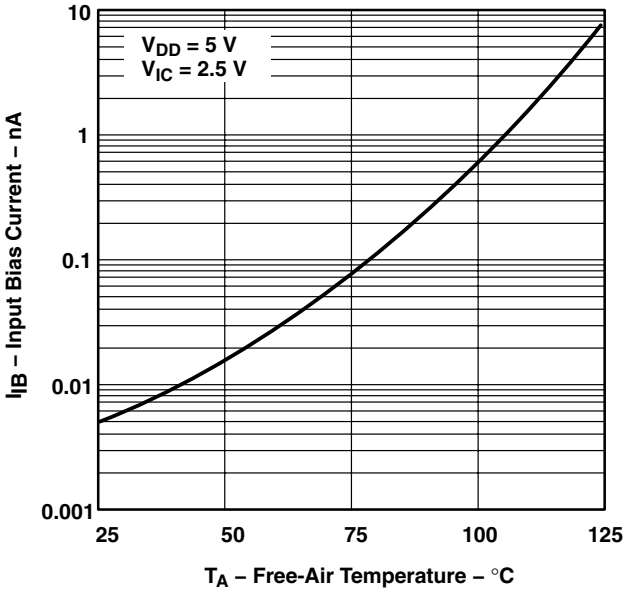



**Figure 9**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS†

**COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE**

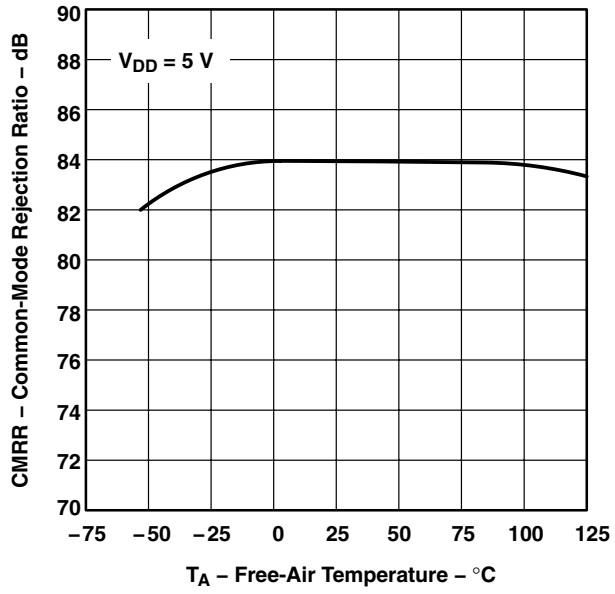



Figure 10

**SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE**

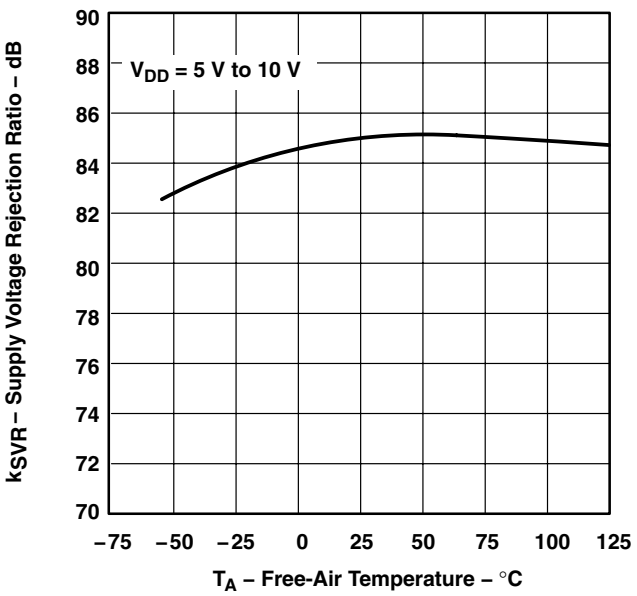



Figure 11

**HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

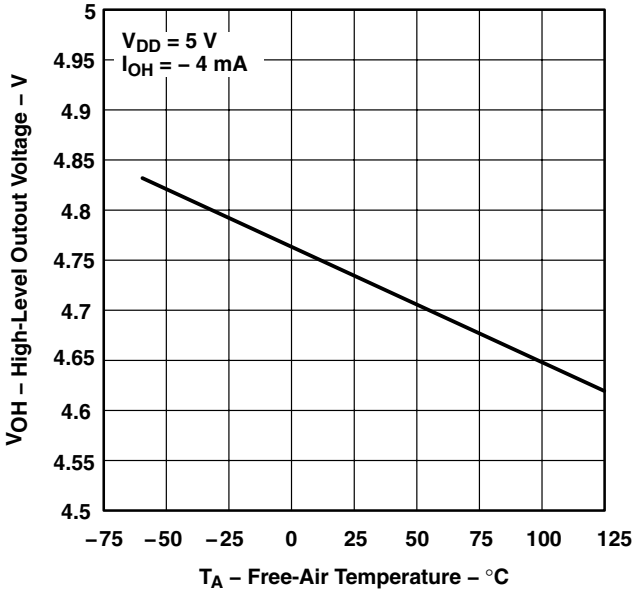



Figure 12

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

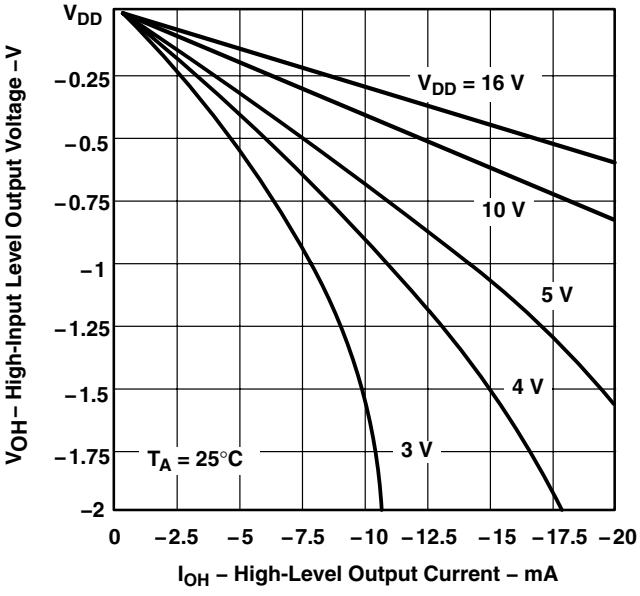



Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS†

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

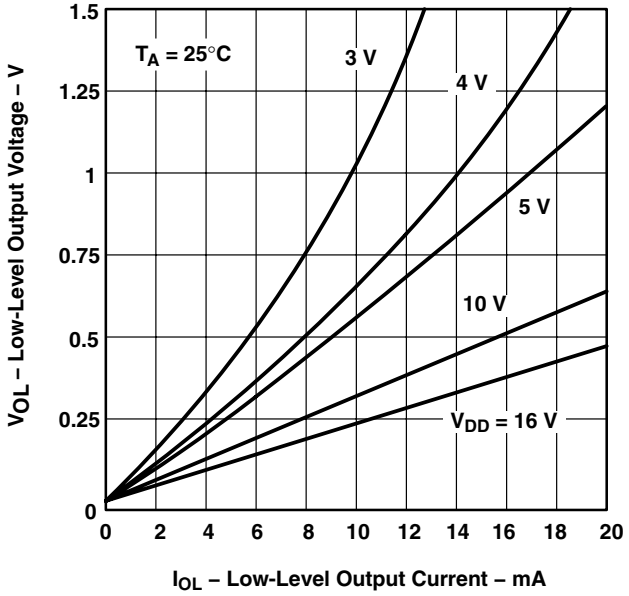



Figure 14

**LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

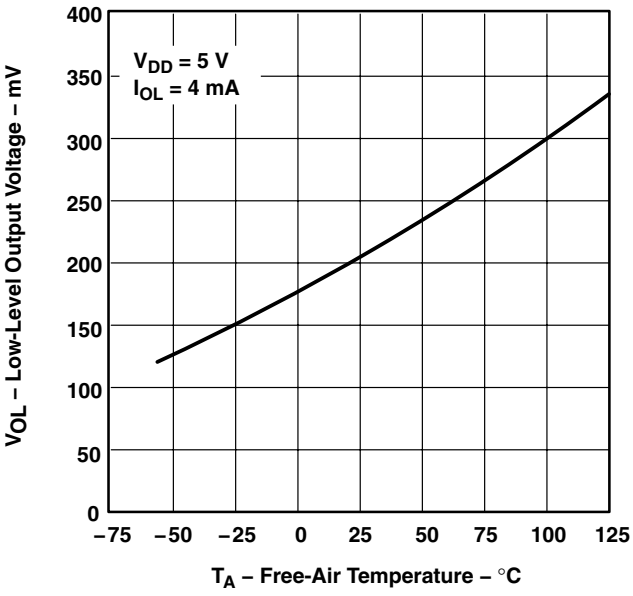



Figure 15

**OUTPUT TRANSITION TIME vs LOAD CAPACITANCE**

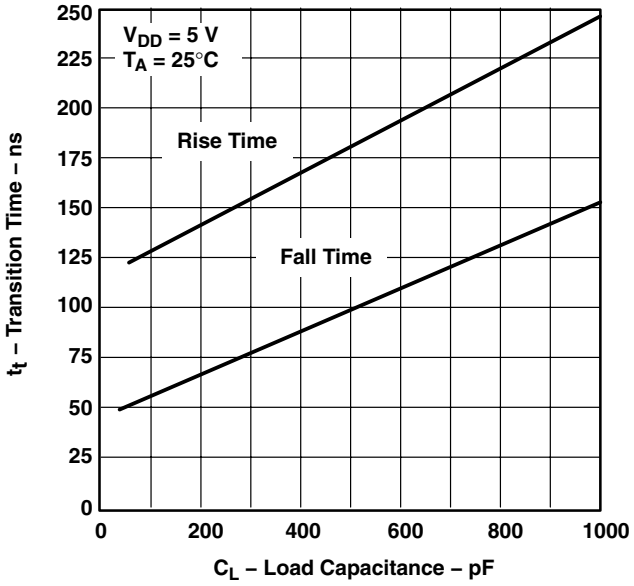



Figure 16

**SUPPLY CURRENT RESPONSE TO AN OUTPUT VOLTAGE TRANSITION**

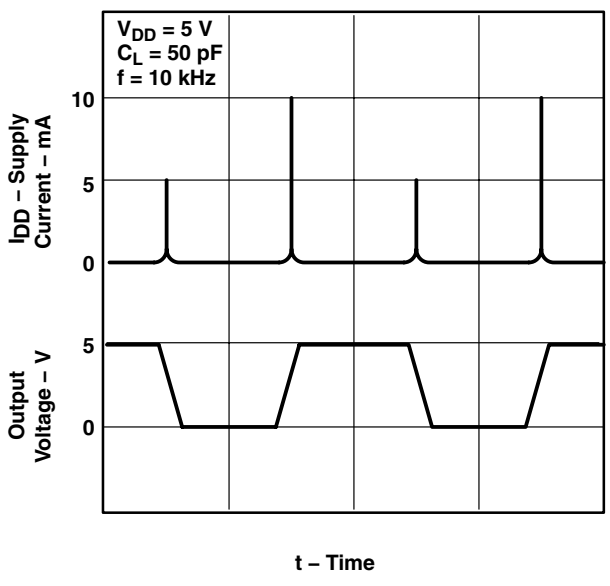



Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

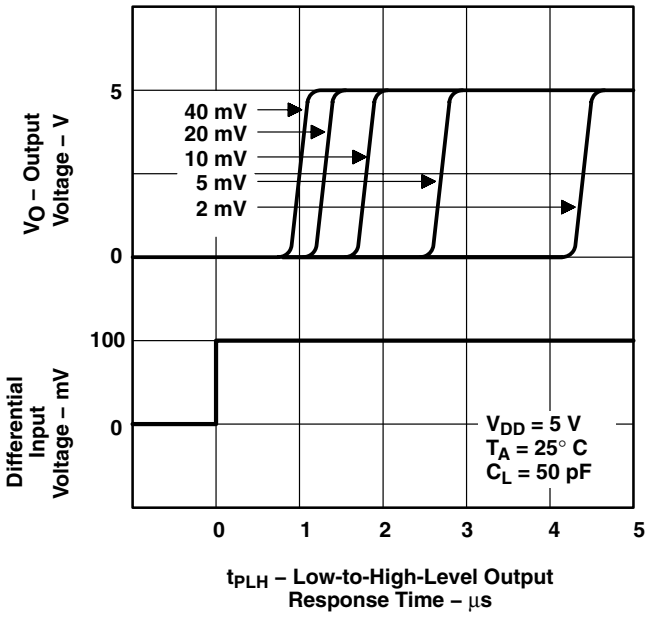



Figure 18

HIGH-TO-LOW-LEVEL OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

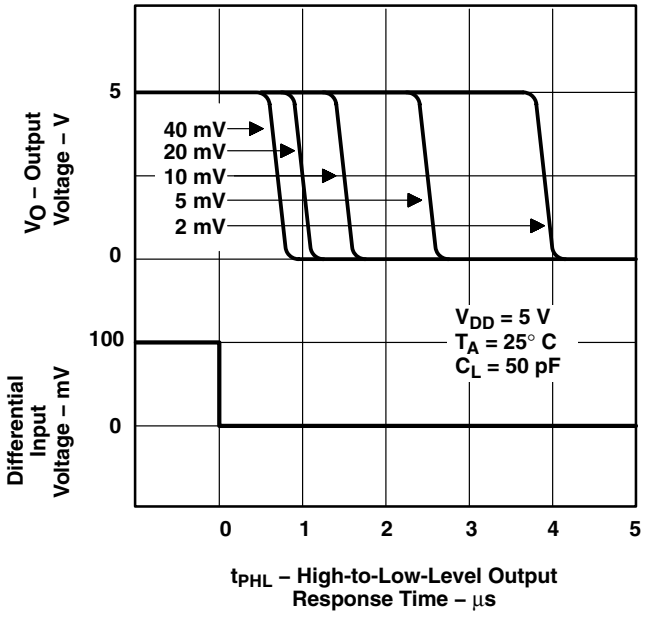



Figure 19

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

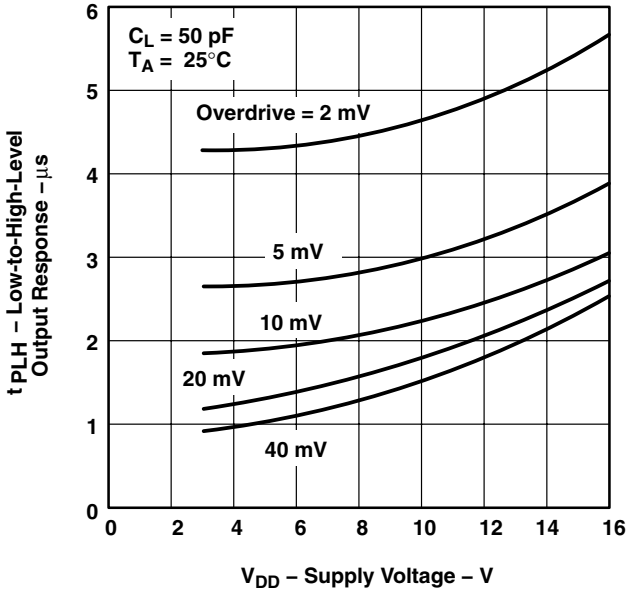



Figure 20

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

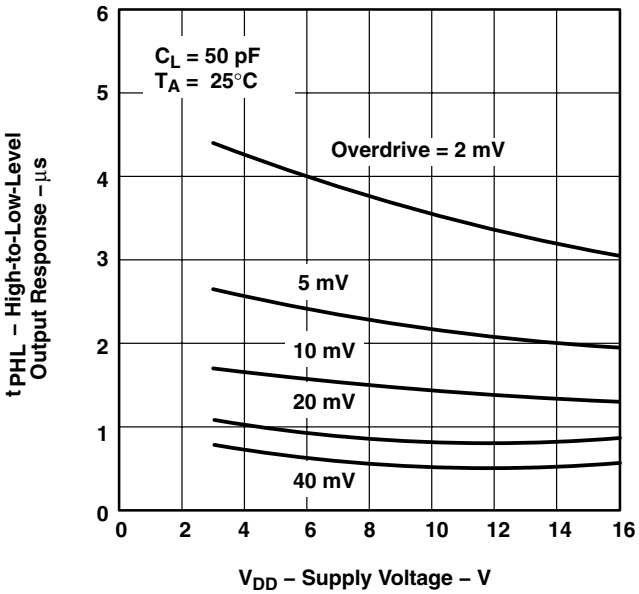



Figure 21

## TYPICAL CHARACTERISTICS†

**AVERAGE SUPPLY CURRENT (PER COMPARATOR) vs FREQUENCY**

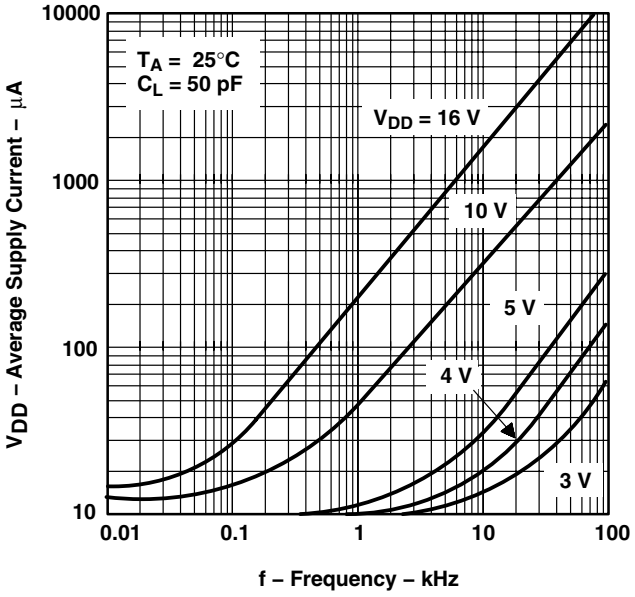



Figure 22

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

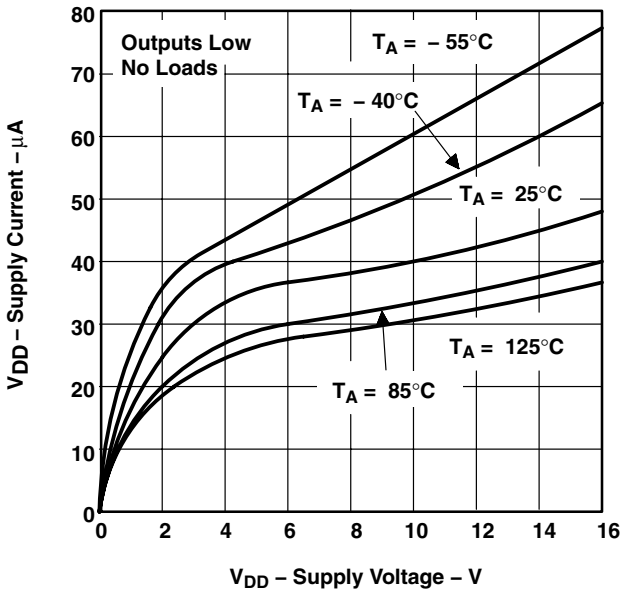



Figure 23

**SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

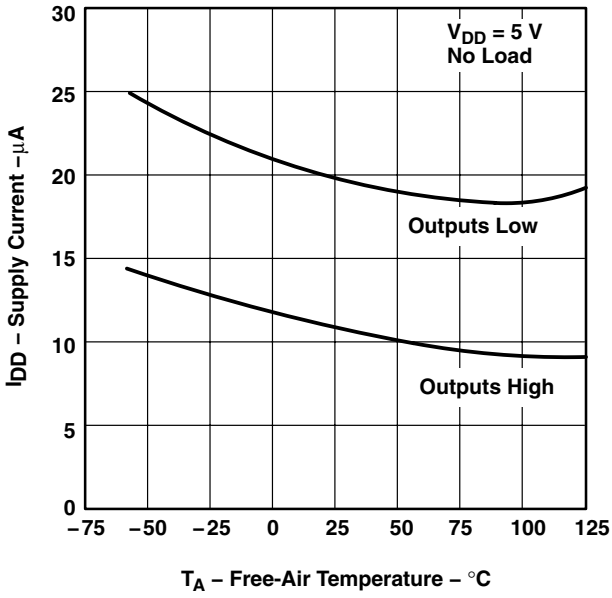



Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

## APPLICATION INFORMATION

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with $V_{DD}$ = 5 V, both inputs must remain between – 0.2 V and 4 V to ensure proper device operation. To ensure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) that is positioned as close to the device as possible.

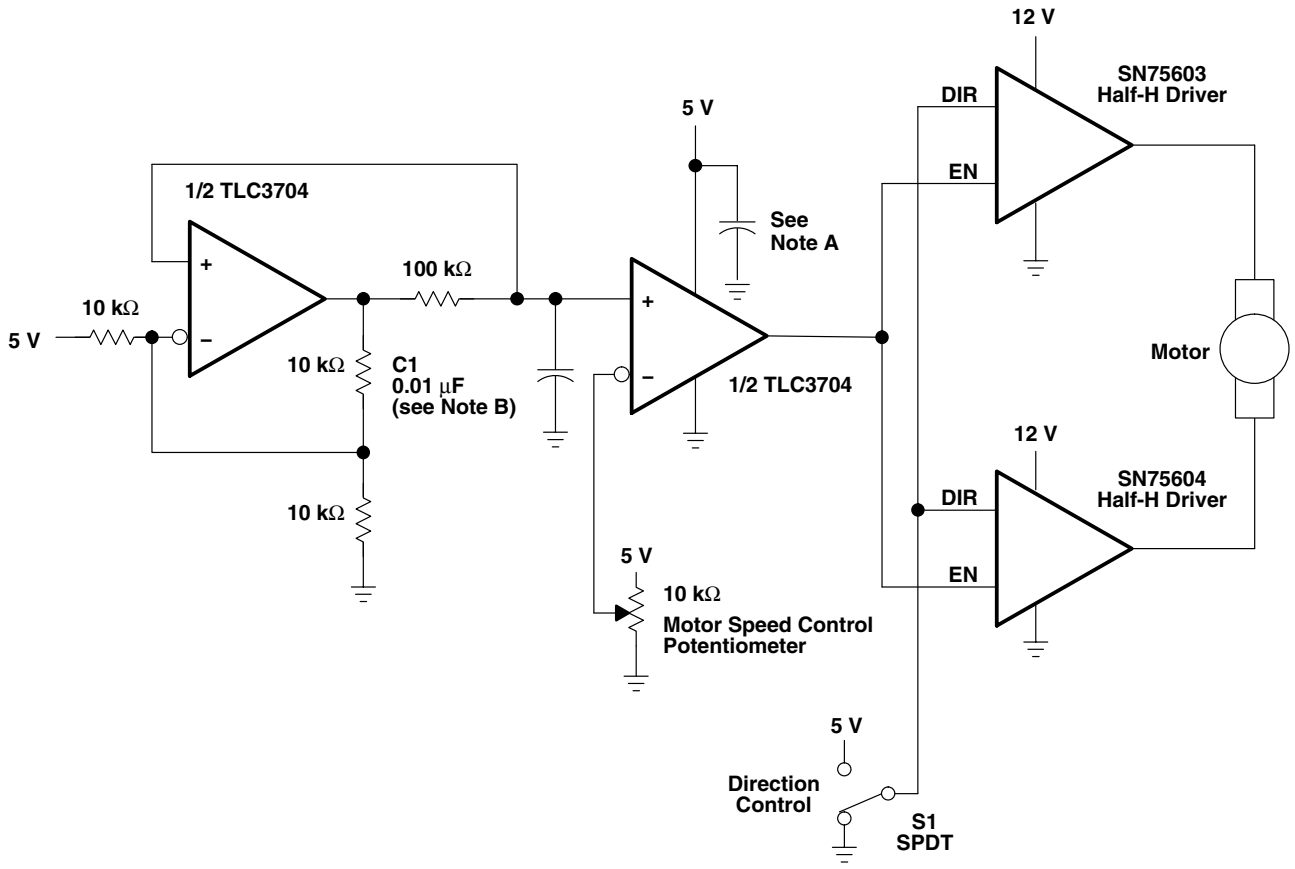
Output and supply current limitations should be watched carefully since the TLC3704 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground can only be an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC3704 has internal ESD-protection circuits that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

**Table of Applications**

| | FIGURE |
|---|---|
| Pulse-width-modulated motor speed controller | 25 |
| Enhanced supply supervisor | 26 |
| Two-phase nonoverlapping clock generator | 27 |
| Micropower switching regulator | 28 |

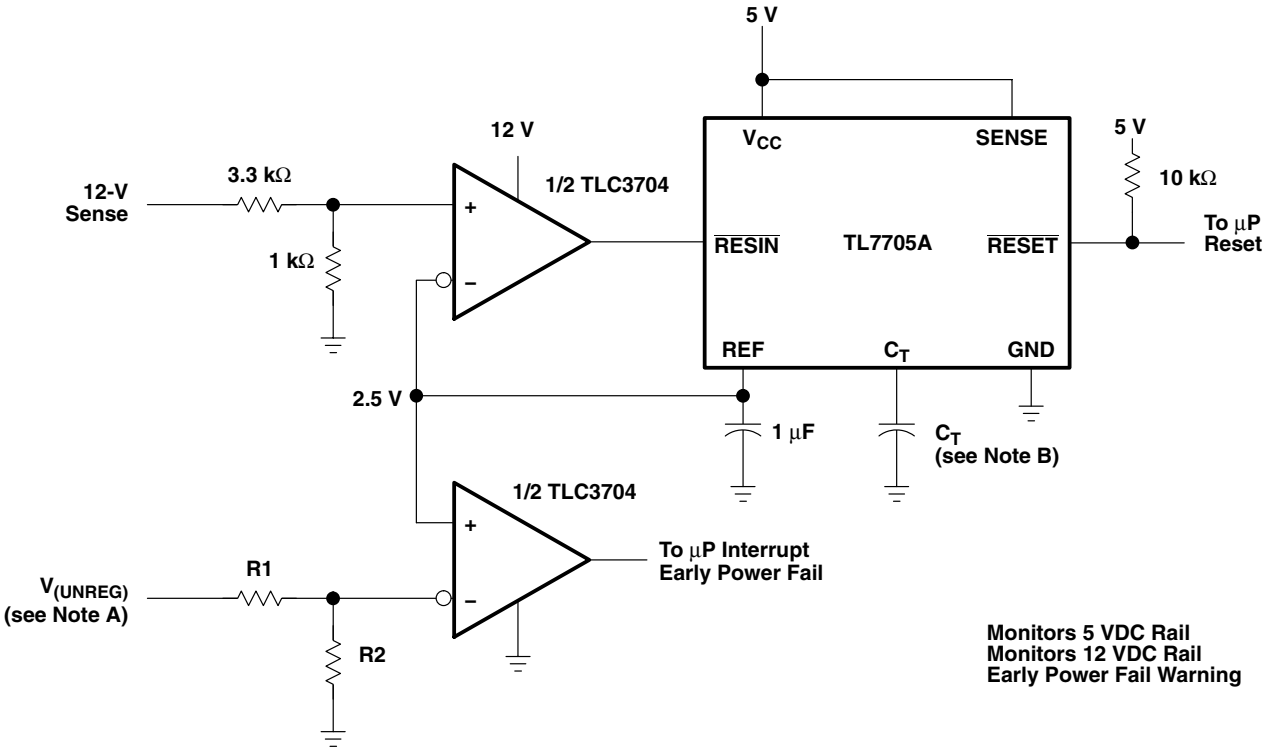
## APPLICATION INFORMATION




NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Adjust C1 for change in oscillator frequency

**Figure 25. Pulse-Width-Modulated Motor Speed Controller**

## APPLICATION INFORMATION

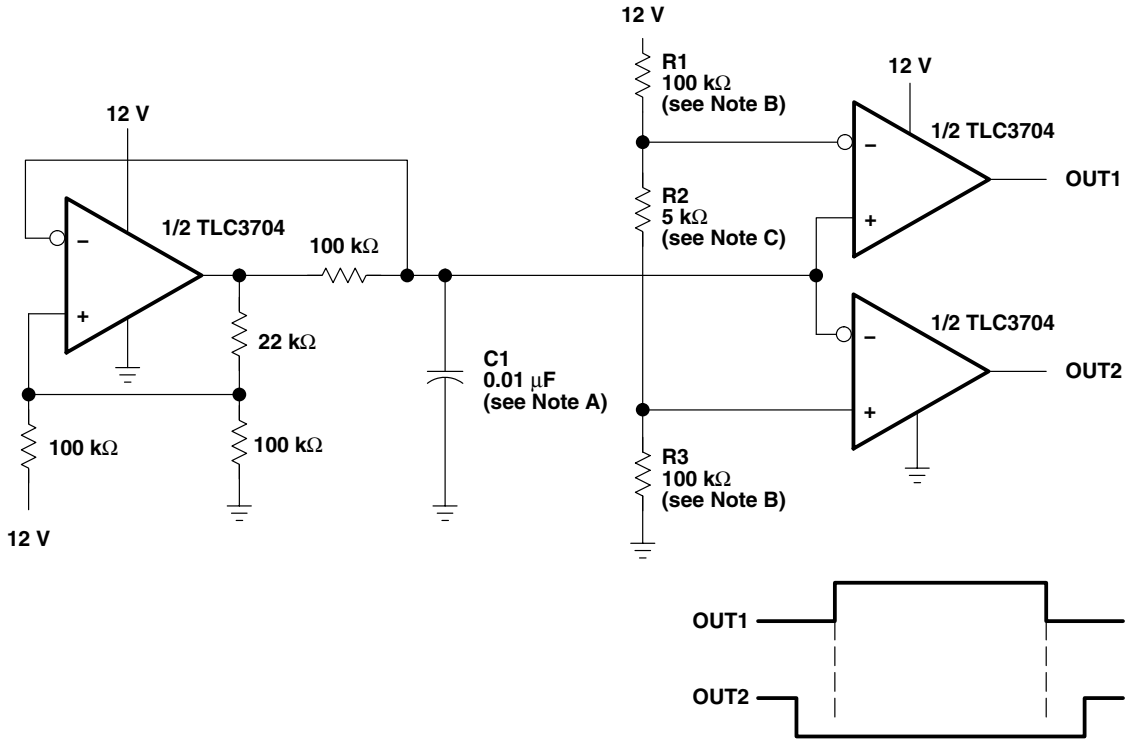



NOTES: A. $V_{(UNREG)} = 2.5\frac{(R1 + R2)}{R2}$

B. The value of $C_T$ determines the time delay of reset.

**Figure 26. Enhanced Supply Supervisor**

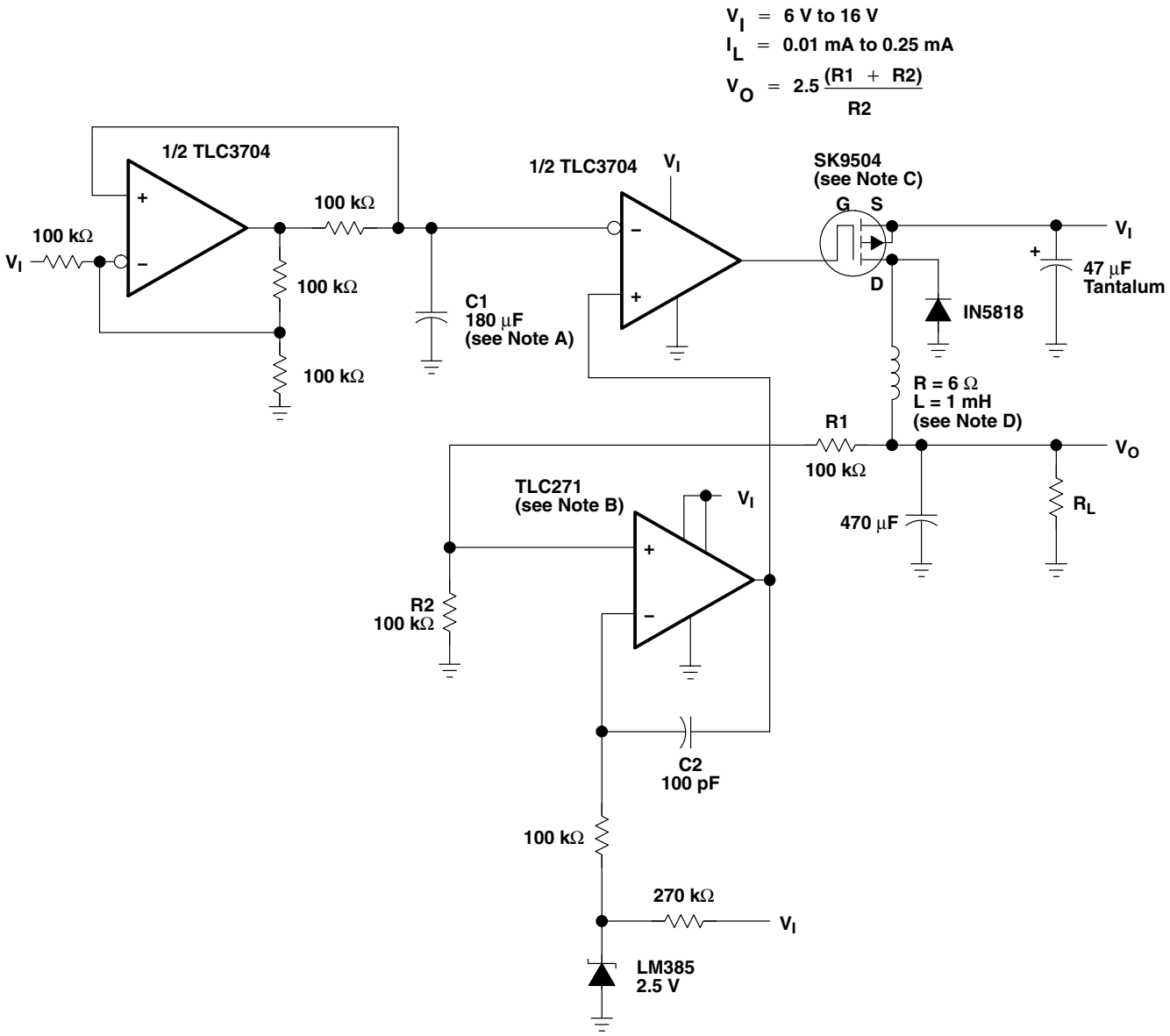
## APPLICATION INFORMATION




NOTES: A. Adjust C1 for a change in oscillator frequency where:
1/f = 1.85(100 kΩ)C1
B. Adjust R1 and R3 to change duty cycle
C. Adjust R2 to change deadtime

**Figure 27. Two-Phase Nonoverlapping Clock Generator**

## APPLICATION INFORMATION




NOTES: A. Adjust C1 for a change in oscillator frequency
B. TLC271 – Tie pin 8 to pin 7 for low bias operation
C. SK9504 – VDS = 40 V
IDS = 1 Awill
D. To achieve microampere current drive, the inductance of the circuit must be increased.

**Figure 28. Micropower Switching Regulator**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9096901M2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9096901M2A TLC3704 MFKB | Samples |
| 5962-9096901MCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9096901MCA TLC3704MJB | Samples |
| TLC3704CD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLC3704C | Samples |
| TLC3704CDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLC3704C | Samples |
| TLC3704CDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLC3704C | Samples |
| TLC3704CN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TLC3704CN | Samples |
| TLC3704CNSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TLC3704 | Samples |
| TLC3704CPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | P3704 | Samples |
| TLC3704CPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | P3704 | Samples |
| TLC3704CPWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | 0 to 70 | | |
| TLC3704CPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | P3704 | Samples |
| TLC3704CPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | P3704 | Samples |
| TLC3704ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLC3704I | Samples |
| TLC3704IDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLC3704I | Samples |
| TLC3704IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLC3704I | Samples |
| TLC3704IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TLC3704I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLC3704IN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TLC3704IN | Samples |
| TLC3704IPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | P3704I | Samples |
| TLC3704IPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | P3704I | Samples |
| TLC3704IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | P3704I | Samples |
| TLC3704IPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | P3704I | Samples |
| TLC3704MD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TLC3704MD | Samples |
| TLC3704MDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | PJ3704M | Samples |
| TLC3704MDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | TLC3704MD | Samples |
| TLC3704MFKB | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9096901M2A TLC3704 MFKB | Samples |
| TLC3704MJB | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9096901MCA TLC3704MJB | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TLC3704, TLC3704M :**

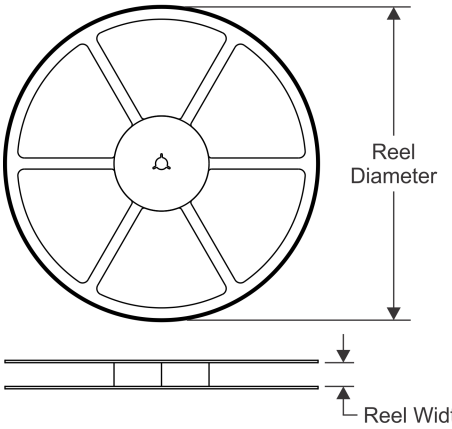
- Catalog: TLC3704
- Automotive: TLC3704-Q1, TLC3704-Q1
- Military: TLC3704M

NOTE: Qualified Version Definitions:

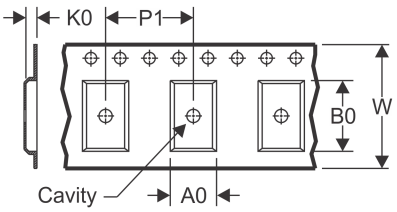
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

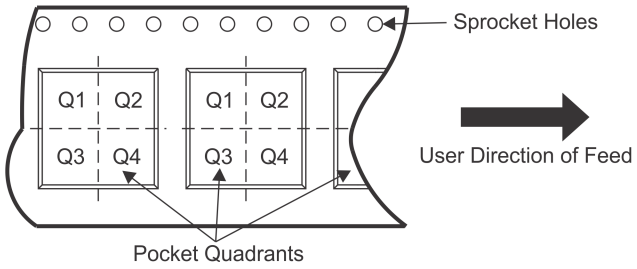



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

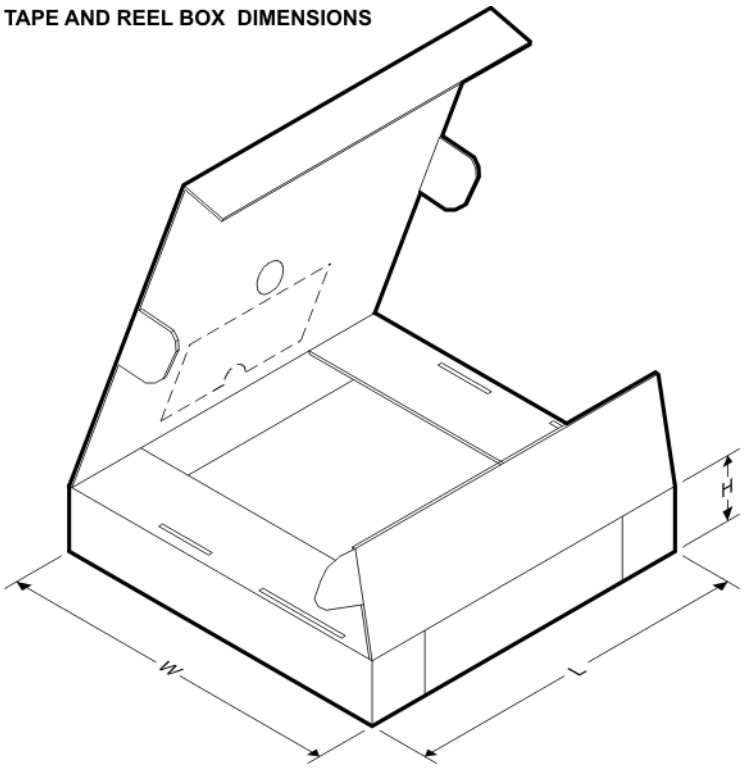
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLC3704CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC3704CNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TLC3704CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC3704IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLC3704IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLC3704MDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



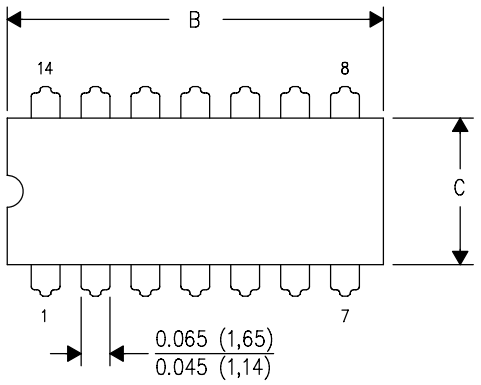

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLC3704CDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLC3704CNSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| TLC3704CPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TLC3704IDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TLC3704IPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TLC3704MDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |

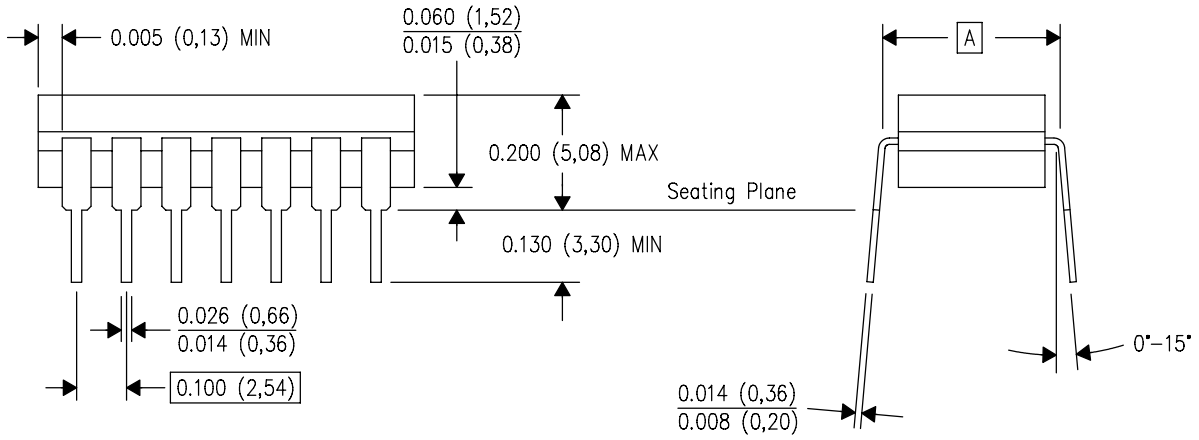
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

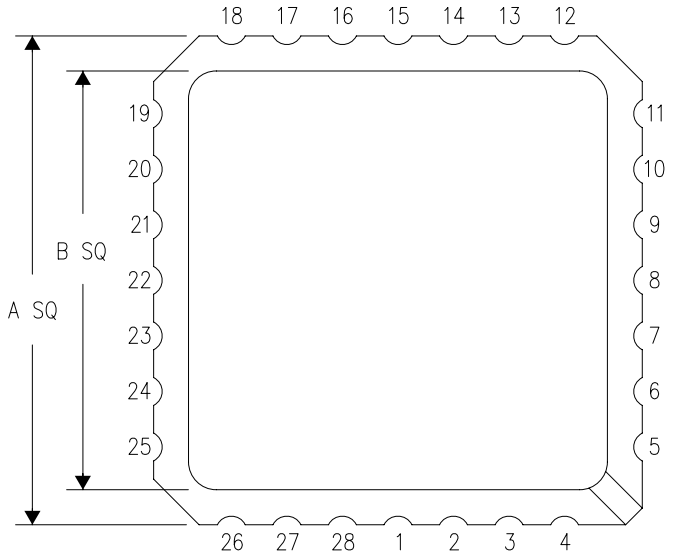



4040083/F 03/03

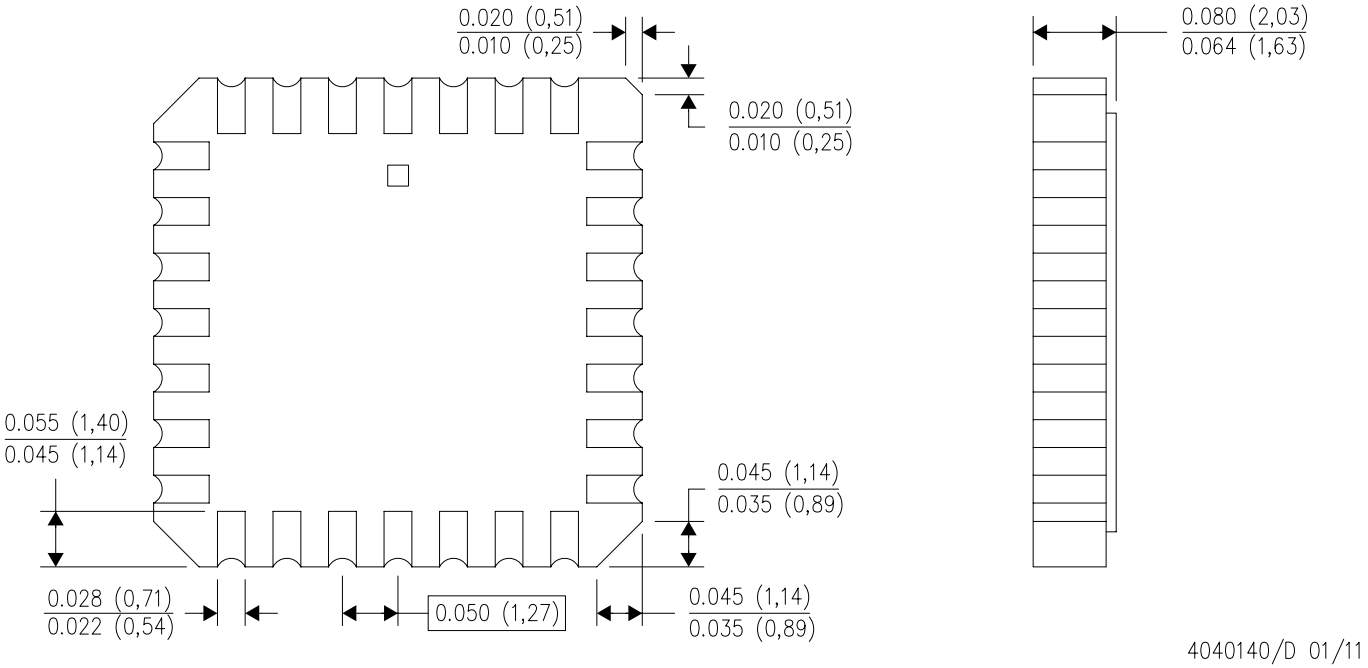
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



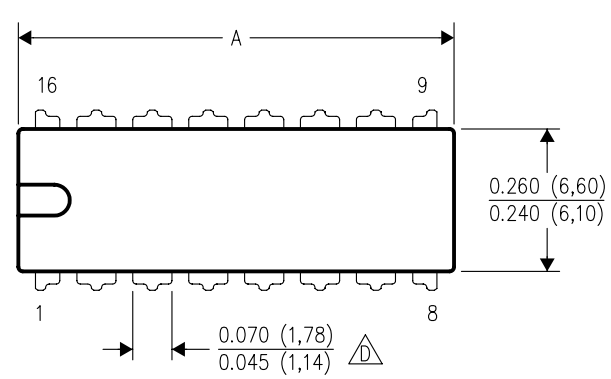

4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

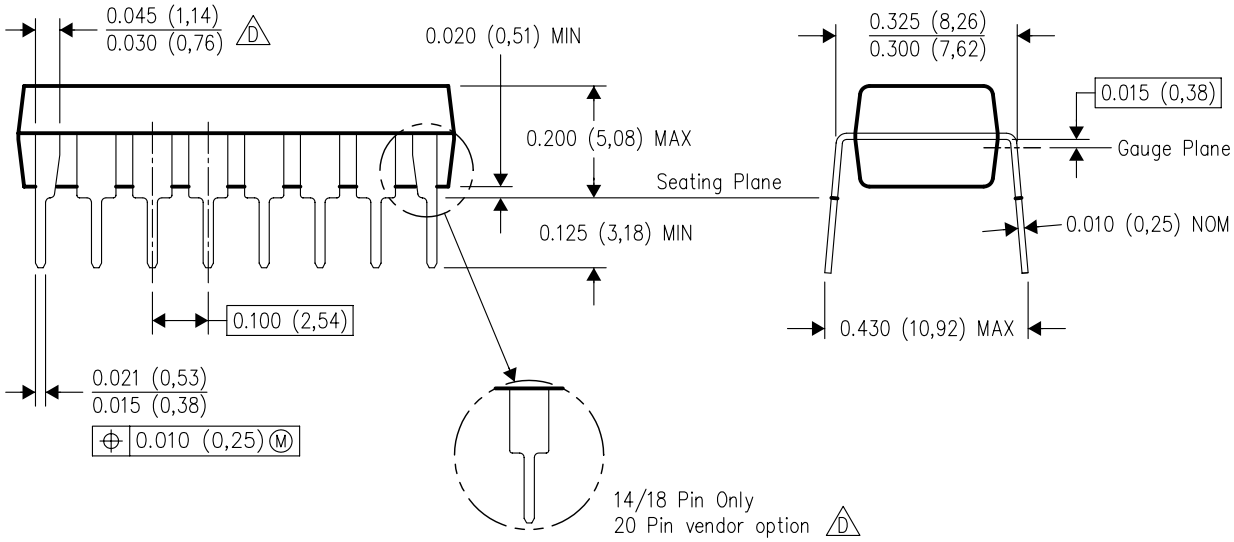
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



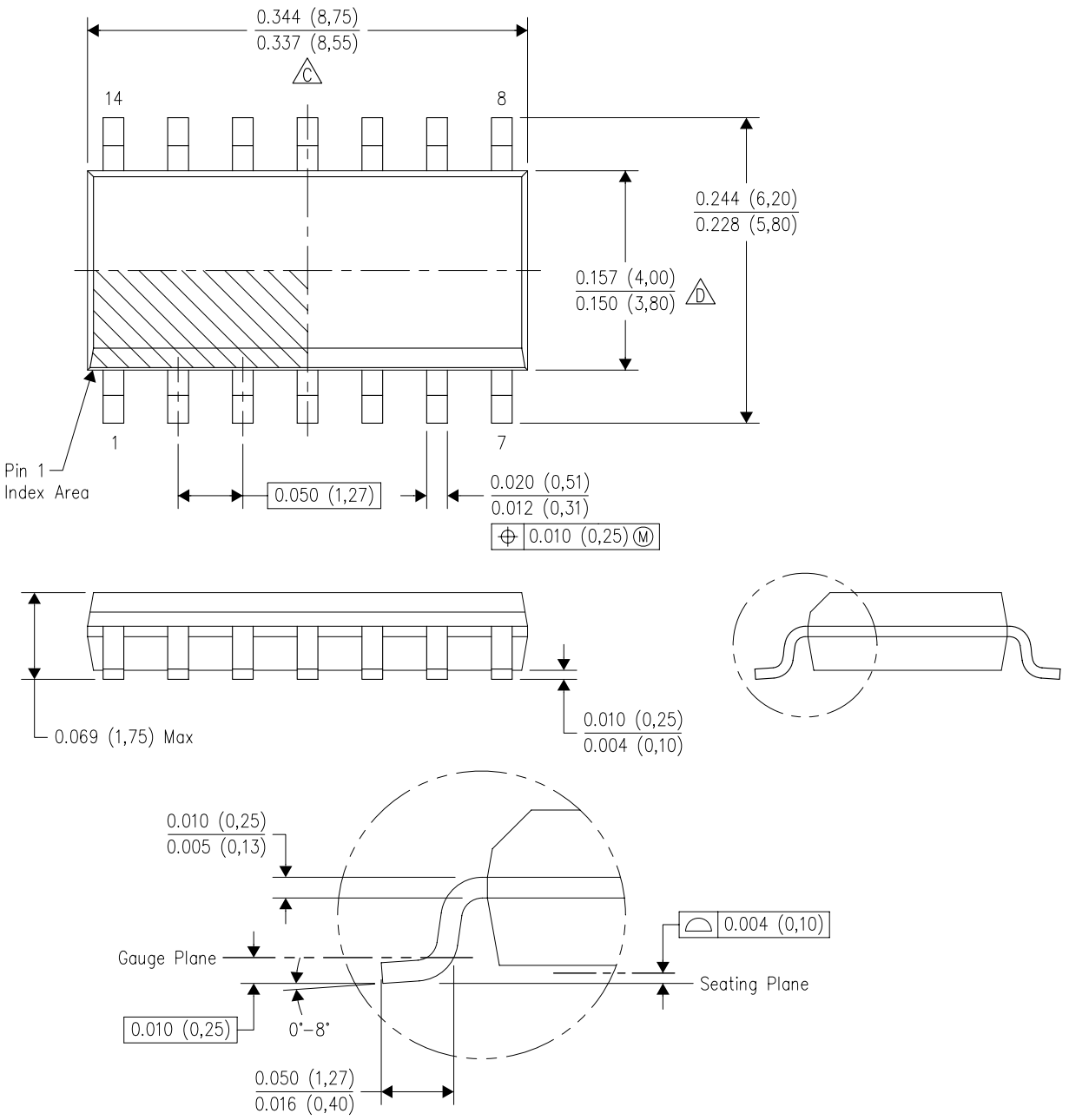

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

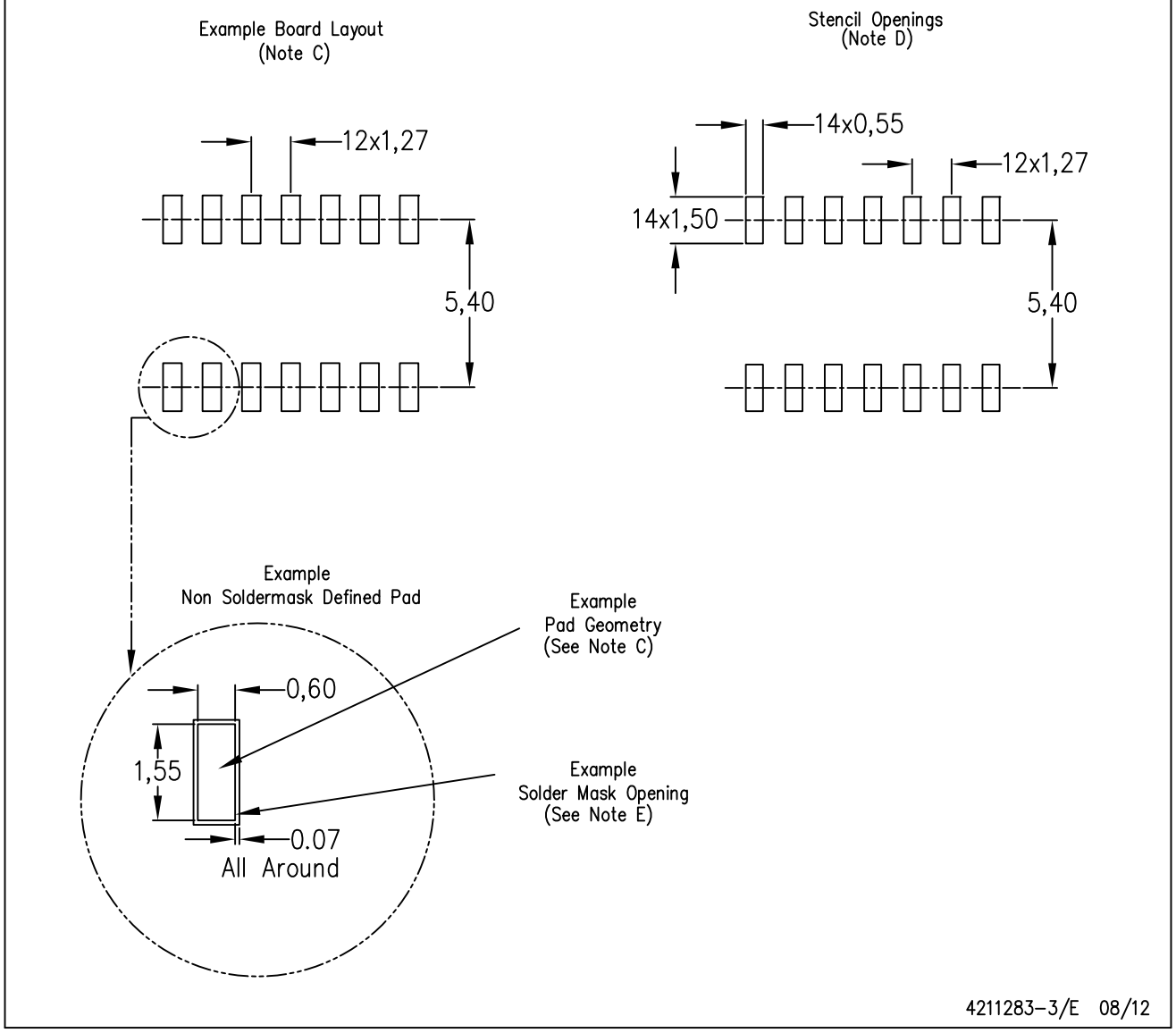
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



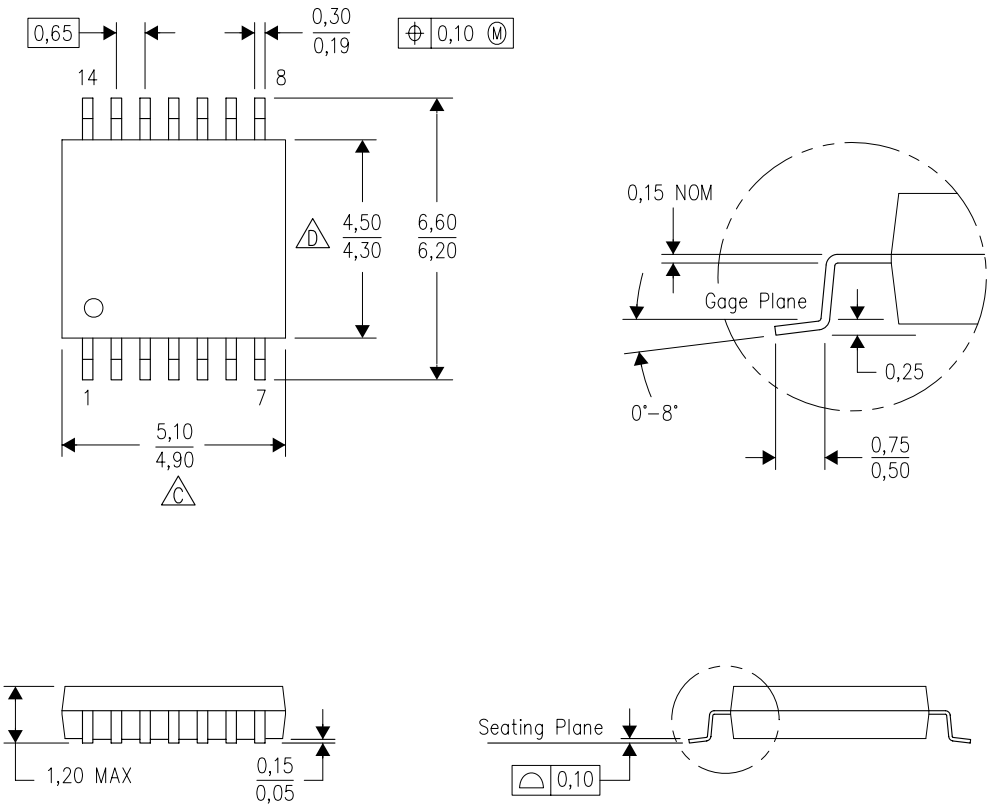

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

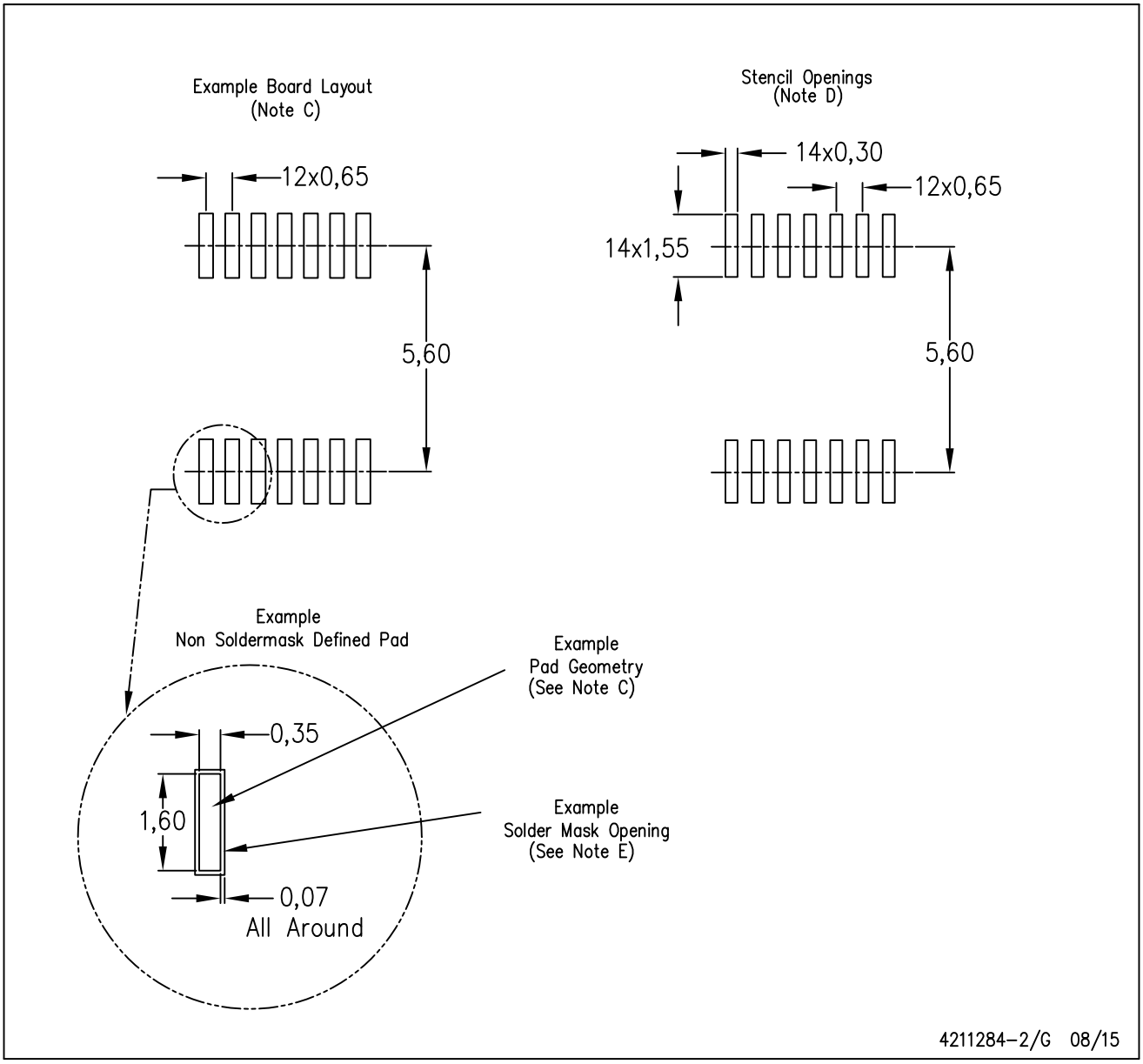
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

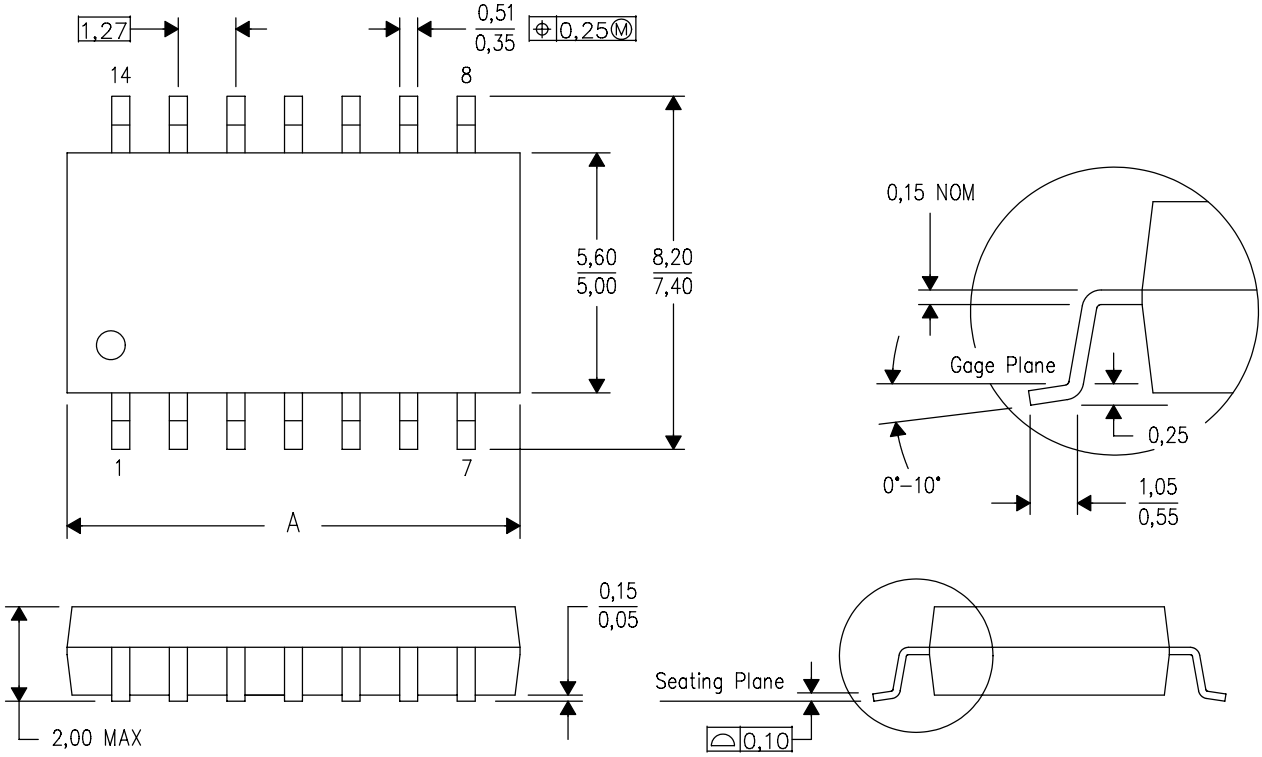



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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