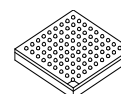




MIMXRT1166CVM5A

MIMXRT1165CVM5A

# i.MX RT1160 Crossover Processors Data Sheet for Industrial Products



## Package Information

Plastic Package

289-pin MAPBGA, 14 x 14 mm, 0.8 mm pitch

## Ordering Information

See [Table 1 on page 6](#)

## 1 i.MX RT1160 introduction

The i.MX RT1160 is a new high-end processor of i.MX RT family, which features NXP's advanced implementation of a high performance Arm Cortex®-M7 core operating at speeds up to 500 MHz and a power efficient Cortex®-M4 core up to 240 MHz.

The i.MX RT1160 processor has 1 MB on-chip RAM in total, including a 768 KB RAM which can be flexibly configured as TCM (512 KB RAM shared with M7 TCM and 256 KB RAM shared with M4 TCM) or general-purpose on-chip RAM. The i.MX RT1160 integrates advanced power management module with DCDC and LDO regulators that reduce complexity of external power supply and simplifies power sequencing. The i.MX RT1160 also provides various memory interfaces, including SDRAM, RAW NAND FLASH, NOR FLASH, SD/eMMC, Quad/Octal SPI, Hyper RAM/Flash, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors. The i.MX RT1160

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also has rich audio and video features, including MIPI CSI/DSI, LCD display, graphic accelerator, camera interface, SPDIF, and I2S audio interface.

The i.MX RT1160 is specifically useful for applications such as:

- Industrial Human Machine Interfaces (HMI)
- Motor Control
- Home Appliance
- High-end Audio Appliance
- Low-end Instrument Cluster
- Point-of-Sale (PoS)

## 1.1 Features

The i.MX RT1160 processors are based on Arm Cortex®-M7 Core™ Platform, which has the following features:

- The Arm Cortex-M7 Core Platform:
  - 32 KB L1 Instruction Cache and 32 KB L1 Data Cache
  - Floating Point Unit (FPU) with single-precision and double-precision support of Armv7-M Architecture FPv5
  - Support the Arm®v7-M Thumb instruction set, defined in the Armv7-M architecture
  - Integrated Memory Protection Unit (MPU), up to 16 individual protection regions
  - Up to 512 KB I-TCM and D-TCM in total
  - Frequency of 500 MHz
  - ECC support for both cache and TCM
  - Frequency of the core, as per [Table 11, "Operating ranges," on page 26](#).
- The Arm Cortex®-M4 Core platform:
  - Cortex-M4 processor with single-precision FPU defined by Armv7-M architecture FPv4-SP
  - Integrated MPU with 8 individual protection regions
  - 16 KB Instruction Cache, 16 KB Data Cache, and 256 KB TCM
  - Frequency of 240 MHz
  - ECC support for TCM and parity check support for cache

The SoC-level memory system consists of the following additional components:

- Boot ROM (256 KB)
- On-chip RAM (1 MB in total)
  - Configurable 512 KB RAM shared with M7 TCM
  - 256 KB RAM shared with M4 TCM
  - Dedicated 256 KB OCRAM
- Secure always-on RAM (4 KB)
- External memory interfaces:

- 8/16/32-bit SDRAM, up to SDRAM-133/SDRAM-166/SDRAM-200
- 8/16-bit SLC NAND FLASH
- SD/eMMC
- SPI NOR/NAND FLASH
- Parallel NOR FLASH with XIP support
- Single/Dual channel Quad SPI FLASH with XIP support
- Hyper RAM/FLASH
- OCT FLASH
- Synchronization mode for all devices
- Timers and PWMs:
  - Six General Programmable Timer (GPT) modules
    - 4-channel generic 32-bit resolution timer for each
    - Each supports standard capture and compare operation
  - Two Periodical Interrupt Timer (PIT) modules
    - Four timers for each module
    - Generic 32-bit resolution timer
    - Periodical interrupt generation
  - Four Quad Timer (QTimer) modules
    - 4-channel generic 16-bit resolution timer for each
    - Each supports standard capture and compare operation
    - Quadrature decoder integrated
  - Four FlexPWMs
    - Up to 8 individual PWM channels for each
    - 16-bit resolution PWM suitable for Motor Control applications
  - Four Quadrature Decoders
  - Four Watch Dog (WDOG) modules

Each i.MX RT1160 processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Display Interface:
  - Parallel RGB LCD interface (eLCDIF)
    - Support 8/16/24-bit interface
    - Support up to WXGA resolution @60fps
    - Support Index color with 256 entry x 24-bit color LUT
  - Parallel RGB LCD Interface Version 2 (LCDIFv2)
    - Enhanced based on LCDIF version
    - Support up to 8 layers of alpha blending
  - MIPI Display Serial Interface (MIPI DSI)

- PHY integrated
  - 2 data lanes interface with up to 1.5 GHz bit rate clock
- Smart LCD Display with 8080 interface through SEMC
- Audio:
  - SPDIF input and output
  - Four Synchronous Audio Interface (SAI) modules supporting I2S, AC97, TDM, and codec/DSP interfaces
  - Medium Quality Sound (MQS) interface via GPIO pads
  - PDM microphone interface with 4 pairs of inputs
  - Asynchronous Sample Rate Converter (ASRC)
- Graphics engine:
  - Generic 2D (PXP)
    - BitBlit
    - Flexible image composition options—alpha, chroma key
    - Porter-duff blending
    - Image rotation (90°, 180°, 270°)
    - Image resize
    - Color space conversion
    - Multiple pixel format support (RGB, YUV444, YUV422, YUV420, YUV400)
    - Standard 2D-DMA operation
  - Vector Graphics Processing
    - Real-time hardware curve tessellation of lines, quadratic, and cubic Bezier curves
    - 16x Line Anti-aliasing
    - OpenVG 1.1 support
    - Vector Drawing
- Camera Interface:
  - Parallel Camera Sensor Interface (CSI)
    - Support 24-bit, 16-bit, and 8-bit input
    - Barcode binarization and histogram statistics
  - MIPI Camera Serial Interface (MIPI CSI)
    - PHY integrated
    - 2 data lanes interface with up to 1.5 GHz bit rate clock
- Connectivity:
  - Two USB 2.0 OTG controllers with integrated PHY interfaces
  - Two Ultra Secure Digital Host Controller (uSDHC) interfaces
    - eMMC 5.0 compliance with HS400 support up to 400 MB/sec
    - SD/SDIO 3.0 compliance with 200 MHz SDR signaling to support up to 100 MB/sec

- Support for SDXC (extended capacity)
- One 10M/100M Ethernet controller with support for IEEE1588
- One Gigabit Ethernet controller with support for AVB
- Twelve universal asynchronous receiver/transmitter (UARTs) modules
- Six I2C modules
- Six SPI modules
- Three FlexCAN (with Flexible Data-rate supported) modules
- Two EMV SIM modules
- Analog:
  - Two Analog-Digital-Converters (ADC), which supports both differential and single-end inputs
  - One Digital-Analog-Converter (DAC)
  - Four Analog Comparators (ACMP)
- GPIO and Pin Multiplexing:
  - General-purpose input/output (GPIO) modules with interrupt capability
  - Input/output multiplexing controller (IOMUXC) to provide centralized pad control
  - Two FlexIO modules
  - 8 x 8 keypad

The i.MX RT1160 processors integrate advanced power management unit and controllers:

- Full PMIC integration, including on-chip DCDC and LDOs
- Temperature sensor with programmable trim points
- Hardware power management controller (GPC)

The i.MX RT1160 processors support the following system debug:

- Arm CoreSight debug and trace architecture
- Trace Port Interface Unit (TPIU) to support off-chip real-time trace
- Cross Triggering Interface (CTI)
- Support for 5-pin (JTAG) and SWD debug interfaces

Security functions are enabled and accelerated by the following hardware:

- High Assurance Boot (HAB)
- Cryptographic Acceleration and Assurance (CAAM) module:
  - Public Key Cryptography Engine (PKHA)
  - Symmetric Engines
  - Cryptographic Hash Engine
  - Random Number Generation (RNG4)
  - Four Job Rings for use by processors
  - Secure Hardware-Only Cryptographic Key Management
  - Encrypted Boot
  - Revision control check based on fuse values

- DEK includes IV
- Side channel attack countermeasures
- 64 KB secure RAM
- Inline Encryption Engine (IEE):
  - External memory encryption/decryption
  - I/O direct encrypted storage and retrieval (Stream Support)
  - FlexSPI decryption only
- On-the-Fly AES Decryption (OTFAD):
  - AES-128 Counter Mode On-the-Fly Decryption
  - Hardware support for unwrapping “key blobs”
  - Functionally acts as a slave sub-module to the FlexSPI
- Secure Non-Volatile Storage (SNVS):
  - Secure real-time clock (SRTC)
  - Zero Master Key (ZMK)
- Secure always-on RAM (4 KB)
- Secure key management and protection
  - Physical Unclonable Function (PUF)
  - UnDocumented Function (UDF)
  - Built-in Manufacturing Protection Hardware
- Secure and trusted access control

#### NOTE

The actual feature set depends on the part numbers as described in [Table 1](#). Functions such as display and camera interfaces, connectivity interfaces, and security features are not offered on all derivatives.

## 1.2 Ordering information

[Table 1](#) provide examples of orderable part numbers covered by this Data Sheet.

**Table 1. Order information**

|                      | <b>MIMXRT1166CVM5A</b>              | <b>MIMXRT1165CVM5A</b>              |
|----------------------|-------------------------------------|-------------------------------------|
| Qualification tier   | Industrial                          | Industrial                          |
| M7 core              | 500 MHz                             | 500 MHz                             |
| M4 core              | 240 MHz                             | 240 MHz                             |
| SRAM                 | 1 MB without ECC or 896 KB with ECC | 1 MB without ECC or 896 KB with ECC |
| Parallel LCD and CSI | Yes                                 | —                                   |
| MIPI DSI and CSI     | Yes                                 | —                                   |
| GPU2D                | Yes                                 | —                                   |

Table 1. Order information (continued)

|                                 | MIMXRT1166CVM5A                        | MIMXRT1165CVM5A                        |
|---------------------------------|----------------------------------------|----------------------------------------|
| PXP                             | Yes                                    | —                                      |
| CAN-FD                          | x3                                     | x3                                     |
| 1 Gb ENET with AVB              | x1                                     | x1                                     |
| 10/100 Mb ENET with 1588        | x1                                     | x1                                     |
| USB OTG                         | x2                                     | x2                                     |
| eMMC 5.0 / SD 3.0               | x2                                     | x2                                     |
| EMV SIM                         | x2                                     | x2                                     |
| SAI                             | x4                                     | x4                                     |
| DMIC                            | x8                                     | x8                                     |
| FlexSPI                         | x2                                     | x2                                     |
| UART                            | x12                                    | x12                                    |
| I2C                             | x6                                     | x6                                     |
| SPI                             | x6                                     | x6                                     |
| GPT                             | x6                                     | x6                                     |
| PIT                             | x2                                     | x2                                     |
| QTimer                          | x4                                     | x4                                     |
| FlexPWM                         | x4                                     | x4                                     |
| Security                        | Yes                                    | Yes                                    |
| Package                         | 289 MAPBGA, 14 mm x14 mm, 0.8 mm pitch | 289 MAPBGA, 14 mm x14 mm, 0.8 mm pitch |
| Junction temperature $T_j$ (°C) | -40 to 105                             | -40 to 105                             |

Figure 1 describes the part number nomenclature so that characteristics of a specific part number can be identified (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX RT1160 Crossover Processors for Industrial Products Data Sheet (IMXRT1160IEC) covers parts listed with a “C (Industrial temp)”

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there are any questions, visit the web page [nxp.com/IMXRT](http://nxp.com/IMXRT) or contact an NXP representative for details.

## i.MX RT1160 introduction

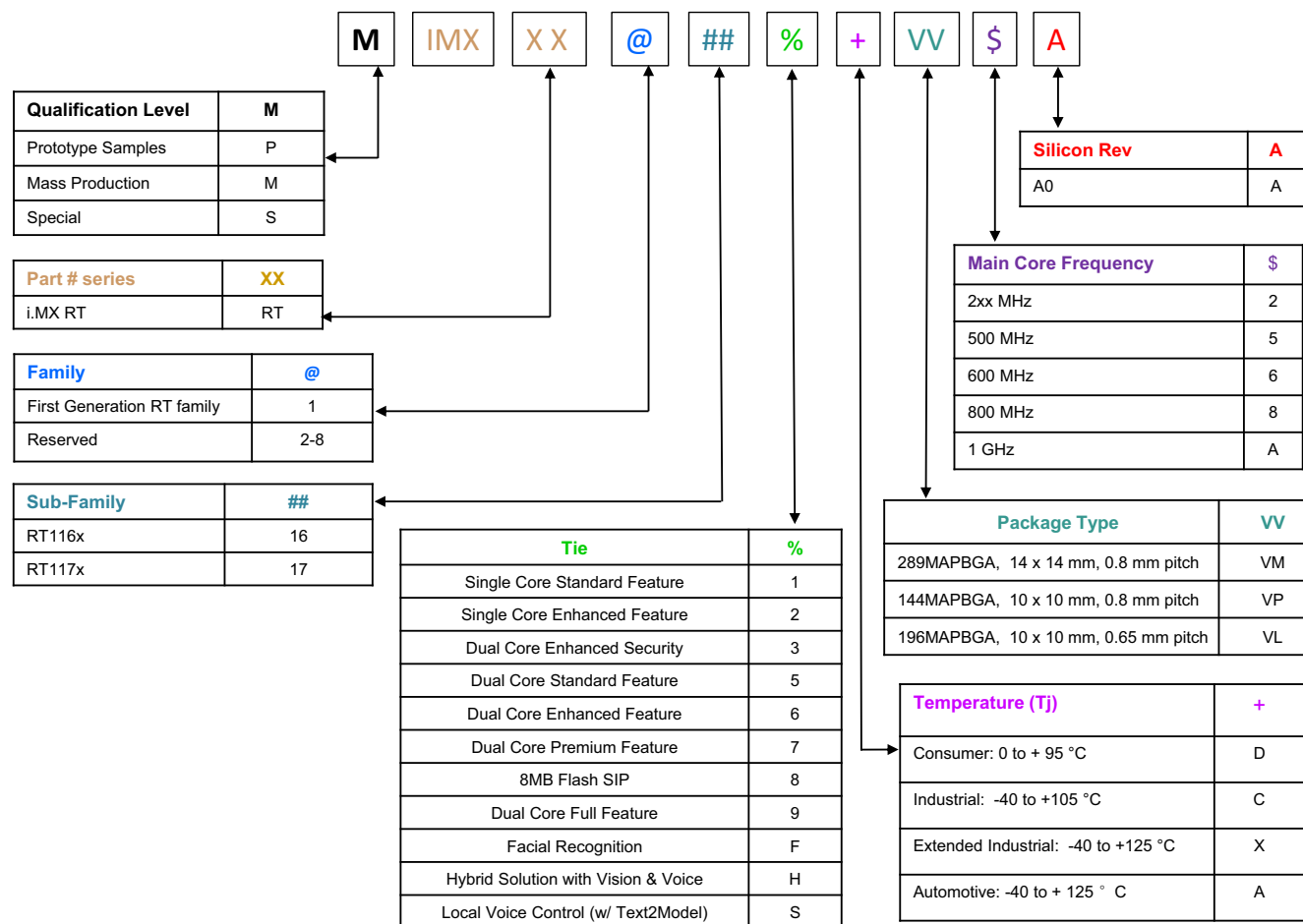


Figure 1. Part number nomenclature—i.MX RT11XX family

```

MATERIAL MARKING ! -----
                  ! !*
FORMAT           ! !
CODE: 3072       ! !      (0)
                  ! !MIMXRT1166CVM5A
                  ! !      MMMMM
                  ! !      AWLYYWWZ
                  ! !
                  ! !
                  ! !
                  ! !
                  ! !

```

- First line: aaaaaaaaaaaaaa
- Second line: mmmmmm
- Third line: xxxyywwx

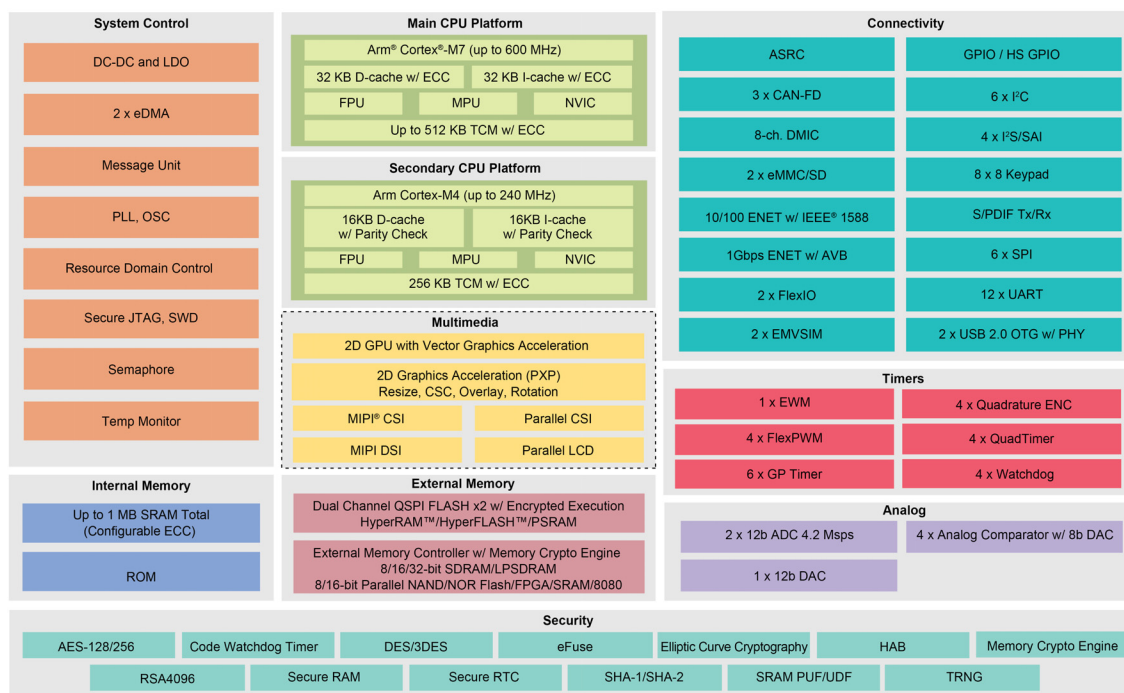
| Identifier | Description                                                                  |
|------------|------------------------------------------------------------------------------|
| a          | Part number code, refer to <a href="#">Section 1.2, Ordering information</a> |
| m          | Mask set                                                                     |
| y          | Year                                                                         |
| w          | Work week                                                                    |
| x          | NXP internal use                                                             |

## 2 Architectural overview

The following subsections provide an architectural overview of the i.MX RT1160 processor system.

### 2.1 Block diagram

Figure 3 shows the functional modules in the i.MX RT1160 processor system<sup>1</sup>.



Available on certain products within the family

**Figure 3. i.MX RT1160 system block diagram**

1. Some modules shown in this block diagram are not offered on all derivatives. See Table 1 for details.

### 3 Modules list

The i.MX RT1160 processors contain a variety of digital and analog modules. [Table 3](#) describes these modules in alphabetical order.

**Table 3. i.MX RT1160 modules list**

| Block Mnemonic                   | Block Name                                                                                                                     | Subsystem                         | Brief Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------------------------------|--------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ACMP1<br>ACMP2<br>ACMP3<br>ACMP4 | Analog Comparator                                                                                                              | Analog                            | The comparator (CMP) provides a circuit for comparing two analog input voltages. The comparator circuit is designed to operate across the full range of the supply voltage (rail-to-rail operation).                                                                                                                                                                                                                                                                                                                                                                                                   |
| ADC_ETC                          | ADC External Trigger Control                                                                                                   | Analog                            | ADC_ETC enables multiple users shares a ADC module in a Time-Division-Multiplexing (TDM).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| ADC1<br>ADC2                     | Analog to Digital Converter                                                                                                    | Analog                            | The ADC is a 12-bit general purpose analog to digital converter.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| AOI                              | And-Or-Inverter                                                                                                                | Cross Trigger                     | The AOI provides a universal boolean function generator using a four-term sum of products expression with each product term containing true or complement values of the four selected inputs (A, B, C, D).                                                                                                                                                                                                                                                                                                                                                                                             |
| Arm                              | Arm Platform                                                                                                                   | Arm                               | The Arm Core Platform includes one Cortex-M7 core. It includes associated sub-blocks, such as Nested Vectored Interrupt Controller (NVIC), Floating-Point Unit (FPU), Memory Protection Unit (MPU), and CoreSight debug modules.<br>The Cortex-M4 platform has following features: <ul style="list-style-type: none"> <li>• Cortex-M4 processor with FPU</li> <li>• Local memory <ul style="list-style-type: none"> <li>– 16 KB instruction cache and 16 KB data cache</li> <li>– 256 KB TCM</li> <li>– TCM memories support ECC</li> <li>– Cache memories support Parity Check</li> </ul> </li> </ul> |
| ASRC                             | Asynchronous Sample Rate Converter                                                                                             | Multimedia Peripherals            | The ASRC can process groups of audio channels with an independent time-based simultaneously.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| CAAM                             | Cryptographic Accelerator and Assurance Module                                                                                 | Security                          | CAAM supports a set of standard hardware accelerators, boot time acceleration of the hashing function, crypto key protection, HDCP 2.x authentication and protected video path support, manufacturing protection and public key cryptographic acceleration, and inter-operate with TrustZone, Resource Domain, and system virtualization access controls.                                                                                                                                                                                                                                              |
| CANFD1<br>CANFD2<br>CANFD3       | Flexible Controller Area Network                                                                                               | Connectivity Peripherals          | The CAN with Flexible Data rate (CAN FD) module is a communication controller implementing the CAN protocol according to the ISO11898-1 and CAN 2.0B protocol specification.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| CCM<br>GPC<br>PGMC<br>PMU<br>SRC | Clock Control Module, General Power Controller, Power Manage Unit, Power Gating and Memory Controller, System Reset Controller | Clocks, Resets, and Power Control | These modules are responsible for clock and reset distribution in the system, and also for the system power management.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

Table 3. i.MX RT1160 modules list (continued)

| Block Mnemonic       | Block Name                                                | Subsystem                  | Brief Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|----------------------|-----------------------------------------------------------|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CSI                  | Parallel CSI                                              | Multimedia Peripherals     | The CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit/24-bit Bayer data input.                                                                                                                                                                                                                          |
| CWT                  | Code Watchdog Timer                                       | Timer peripherals          | The CWT provides mechanisms for detecting side-channel attacks and the execution of unexpected instruction sequences.                                                                                                                                                                                                                                                                                                                                                                       |
| DAC                  | Digital-Analog-Converter                                  | Analog                     | The DAC is a 12-bit general purpose digital to analog converter.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| DAP                  | Debug Access Port                                         | System Control Peripherals | The DAP provides real-time access for the debugger without halting the core to: <ul style="list-style-type: none"> <li>• System memory and peripheral registers</li> <li>• All debug configuration registers</li> </ul> The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-M7 Core Platform.                                                                                                                                               |
| DCDC                 | DCDC Converter                                            | Analog                     | The DCDC module is used for generating power supply for core logic. Main features are: <ul style="list-style-type: none"> <li>• Adjustable high efficiency regulator</li> <li>• Two outputs: 1.0 V and 1.8 V</li> <li>• Over current and over voltage detection</li> </ul>                                                                                                                                                                                                                  |
| eDMA<br>eDMA_LPSR    | enhanced Direct Memory Access                             | System Control Peripherals | There are two enhanced DMAs (eDMA). <ul style="list-style-type: none"> <li>• The eDMA is a 32-channel DMA engine, which is capable of performing complex data transfers with minimal intervention from a host processor.</li> <li>• The DMA_MUX is capable of multiplexing up to 128 DMA request sources to the 32 DMA channels of eDMA.</li> </ul>                                                                                                                                         |
| eLCDIF               | LCD interface                                             | Multimedia Peripherals     | The enhanced LCD controller provides flexible display options and to drive a wide range of display devices varying in size and capability. Major features are: <ul style="list-style-type: none"> <li>• Up to WXGA 60 Hz</li> <li>• 8/16/18/24 bit LCD data bus support available depending on I/O mux options.</li> <li>• Programmable timing and parameters for LCD interfaces to support a wide variety of displays.</li> <li>• Index color with 256 entry x 24-bit color LUT</li> </ul> |
| EMV SIM1<br>EMV SIM2 | Europay, Master and Visa Subscriber Identification Module | Connectivity Peripherals   | EMV SIM is designed to facilitate communication to Smart Cards compatible to the EMV version 4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 standard.                                                                                                                                                                                                                                                                                                                 |

Table 3. i.MX RT1160 modules list (continued)

| Block Mnemonic                               | Block Name                              | Subsystem                          | Brief Description                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------------------|-----------------------------------------|------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ENET                                         | Ethernet Controller                     | Connectivity<br>Peripherals        | The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.                                          |
| ENET 1G                                      | Ethernet Controller                     | Connectivity<br>Peripherals        | One 1G Ethernet is also integrated, which has following features: <ul style="list-style-type: none"> <li>• RGMII/RMII/MII operation</li> <li>• Support IEEE1588</li> <li>• Support AVB</li> </ul>                                                                                                                                                                                                     |
| EWM                                          | External Watchdog<br>Monitor            | Timer Peripherals                  | The EWM modules is designed to monitor external circuits, as well as the software flow. This provides a back-up mechanism to the internal WDOG that can reset the system. The EWM differs from the internal WDOG in that it does not reset the system. The EWM, if allowed to time-out, provides an independent trigger pin that when asserted resets or places an external circuit into a safe mode. |
| FlexIO1<br>FlexIO2                           | Flexible Input/output                   | Connectivity and<br>Communications | The FlexIO is capable of supporting a wide range of protocols including, but not limited to: UART, I2C, SPI, I2S, camera interface, display interface, PWM waveform generation, etc. The module can remain functional when the chip is in a low power mode provided the clock it is using remain active.                                                                                              |
| FlexPWM1<br>FlexPWM2<br>FlexPWM3<br>FlexPWM4 | Pulse Width Modulation                  | Timer Peripherals                  | The pulse-width modulator (PWM) contains four PWM sub-modules, each of which is set up to control a single half-bridge power stage. Fault channel support is provided. The PWM module can generate various switching patterns, including highly sophisticated waveforms.                                                                                                                              |
| FlexRAM                                      | RAM                                     | Memories                           | The i.MX RT1160 has 512 KB of on-chip RAM which could be flexible allocated to I-TCM, D-TCM, and on-chip RAM (OCRAM) in a 32 KB granularity. The FlexRAM is the manager of the 512 KB on-chip RAM array. Major functions of this blocks are: interfacing to I-TCM and D-TCM of CM7 and OCRAM controller; dynamic RAM arrays allocation for I-TCM, D-TCM, and OCRAM.                                   |
| FlexSPI1<br>FlexSPI2                         | Flexible Serial Peripheral<br>Interface | Connectivity and<br>Communications | FlexSPI acts as an interface to one or two external serial memory devices, FlexSPI2 has 8 bi-directional data lines.                                                                                                                                                                                                                                                                                  |

Table 3. i.MX RT1160 modules list (continued)

| Block Mnemonic                                                                                                        | Block Name                  | Subsystem                  | Brief Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------------------------------------------------------------------------------------------------------|-----------------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO1<br>GPIO2<br>GPIO3<br>GPIO4<br>GPIO5<br>GPIO6<br>GPIO7<br>GPIO8<br>GPIO9<br>GPIO10<br>GPIO11<br>GPIO12<br>GPIO13 | General Purpose I/O Modules | System Control Peripherals | Used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.<br><b>Note:</b> GPIO13 register access takes a long time (about 50 $\mu$ s due to clocked by 32 KHz clock source). During the period of registers access, the LPSR domain bus would be on hold.                                                                                                                                                                                                                                                                                                                                                                |
| GPT1<br>GPT2<br>GPT3<br>GPT4<br>GPT5<br>GPT6                                                                          | General Purpose Timer       | Timer Peripherals          | Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock. |
| GPU2D                                                                                                                 | Graphics Processing         | Multimedia Peripherals     | The vector graphics processing supports following features: <ul style="list-style-type: none"> <li>• Real-time hardware curve tessellation of lines, quadratic, and cubic Bezier curves</li> <li>• 16x line anti-aliasing</li> <li>• OpenVG 1.1 support</li> <li>• Vector drawing</li> </ul>                                                                                                                                                                                                                                                                                                                                                                          |
| IOMUXC                                                                                                                | IOMUX Control               | Mux control                | This module enables flexible I/O multiplexing. Each IO pad has a default as well as several alternate functions. The alternate functions are software configurable.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| JTAGC                                                                                                                 | JTAG Controller             | System Control Peripherals | The JTAG interface complies with JTAG TAP standards to internal logic. The i.MX RT1160 processors use JTAG port for production, testing, and system debugging. In addition, the JTAG provides BSR (Boundary Scan Register) standard support, which complies with IEEE 1149.1 and IEEE 1149.6 standards.<br>The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX RT1160 JTAG incorporates two security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.                    |

Table 3. i.MX RT1160 modules list (continued)

| Block Mnemonic                                                                                                                      | Block Name                            | Subsystem                       | Brief Description                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| KPP                                                                                                                                 | Keypad Port                           | Human Machine Interfaces        | The KPP is a 16-bit peripheral that can be used as a keypad matrix interface or as general purpose input/output (I/O). It supports 8 x 8 external key pad matrix. Main features are: <ul style="list-style-type: none"> <li>• Multiple-key detection</li> <li>• Long key-press detection</li> <li>• Standby key-press detection</li> <li>• Supports a 2-point and 3-point contact key matrix</li> </ul> |
| LCDIFv2                                                                                                                             | Parallel RGB LCD interface version 2  | Multimedia Peripherals          | The LCDIFv2 is an enhanced version of LCDIF. Main features are: <ul style="list-style-type: none"> <li>• Eight layers of alpha blending</li> <li>• CRC check for configurable region on the final display output after alpha blending</li> <li>• Write-back channel to save the final output into memory</li> </ul>                                                                                     |
| LPI2C1<br>LPI2C2<br>LPI2C3<br>LPI2C4<br>LPI2C5<br>LPI2C6                                                                            | Low Power Inter-integrated Circuit    | Connectivity and Communications | The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master.<br>The I2C provides a method of communication between a number of external devices. More detailed information, see <a href="#">Section 4.9.2, LPI2C module timing parameters</a> .                                                                                       |
| LPSP11<br>LPSP12<br>LPSP13<br>LPSP14<br>LPSP15<br>LPSP16                                                                            | Low Power Serial Peripheral Interface | Connectivity and Communications | The LPSP1 is a low power Serial Peripheral Interface (SPI) module that support an efficient interface to an SPI bus as a master and/or a slave. <ul style="list-style-type: none"> <li>• It can continue operating while the chip is in stop modes, if an appropriate clock is available</li> <li>• Designed for low CPU overhead, with DMA off loading of FIFO register access</li> </ul>              |
| LPUART1<br>LPUART2<br>LPUART3<br>LPUART4<br>LPUART5<br>LPUART6<br>LPUART7<br>LPUART8<br>LPUART9<br>LPUART10<br>LPUART11<br>LPUART12 | UART Interface                        | Connectivity Peripherals        | Each of the UART modules support the following serial data transmit/receive protocols and configurations: <ul style="list-style-type: none"> <li>• 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none)</li> <li>• Programmable baud rates up to 20 Mbps.</li> </ul>                                                                                                       |
| MECC64                                                                                                                              | Error Correcting Code                 | Memories and Memory Controllers | MECC64 module supports Single Error Correction and Double Error Detection (SECCDED) ECC function to provide reliability for 4 banks On-Chip RAM (OCRAM) access. When ECC function is disabled, ECC OCRM can be also used to store data.                                                                                                                                                                 |

Table 3. i.MX RT1160 modules list (continued)

| Block Mnemonic | Block Name                | Subsystem                       | Brief Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------------|---------------------------|---------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MIPI-CSI       | MIPI CSI Interface        | Multimedia Peripherals          | Key features of MIPI CSI controller are listed as following: <ul style="list-style-type: none"> <li>• Implements all three MIPI CSI-2 layers</li> <li>• Supports CSI-2 Unidirectional Master operation</li> <li>• Virtual Channel support</li> <li>• Flexible pixel-based user interface</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| MIPI-DSI       | MIPI DSI Interface        | Multimedia Peripherals          | Key features of MIPI DSI controller are listed as following: <ul style="list-style-type: none"> <li>• Implements all three DSI layers</li> <li>• Supports Command and Video Modes</li> <li>• Virtual Channel support</li> <li>• Flexible packet based user interface</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| MQS            | Medium Quality Sound      | Multimedia Peripherals          | MQS is used to generate 2-channel medium quality PWM-like audio via two standard digital GPIO pins.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| MU             | Messaging Unit            | System Control                  | The Messaging Unit module enables two processors within the SoC to communicate and coordinate by passing messages (e.g. data, status, and control) through the MU interface.<br>The MU also provides the ability for one processor to signal the other processor using interrupts.                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| OCOTP_CTRL     | OTP Controller            | Security                        | The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (eFUSES). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non volatility. |
| OCRAM          | On-Chip Memory controller | Memories and Memory Controllers | The On-Chip Memory controller (OCRAM) module is designed as an interface between the system's AXI bus and the internal (on-chip) SRAM memory module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| OSC            | Oscillator                | Clock Sources and Control       | Two crystal oscillators: <ul style="list-style-type: none"> <li>• 48 MHz crystal oscillator: it is used as primary clock source for all the PLLs to generate the clock for CPU, BUS, and high-speed interfaces.</li> <li>• 32 kHz crystal oscillator: it is the primary clock source for RTC as well as low speed clock source for CCM/SRC/GPC.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                    |
| PDM            | Pulse Density Modulation  | Multimedia Peripherals          | The PDM supports up to 8-channels (4 lanes) digital MIC inputs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

Table 3. i.MX RT1160 modules list (continued)

| Block Mnemonic                                                           | Block Name                  | Subsystem                       | Brief Description                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|--------------------------------------------------------------------------|-----------------------------|---------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIT1<br>PIT2                                                             | Periodical Interrupt Timer  | Timer Peripherals               | The PIT features 32-bit counter timer, programmable count modules, clock division features, interrupt generation, and a slave mode to synchronize count enable for multiple PITs.                                                                                                                                                                                                                                                                        |
| PXP                                                                      | Pixel Processing Pipeline   | Multimedia Peripherals          | A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, and rotation. The PXP is enhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications.                                                                                     |
| Quadrature DEC1<br>Quadrature DEC2<br>Quadrature DEC3<br>Quadrature DEC4 | Quadrature Decoder          | Timer Peripherals               | The enhanced quadrature decoder module provides interfacing capability to position/speed sensors. There are five input signals: PHASEA, PHASEB, INDEX, TRIGGER, and HOME. This module is used to decode shaft position, revolution count, and speed.                                                                                                                                                                                                     |
| QuadTimer1<br>QuadTimer2<br>QuadTimer3<br>QuadTimer4                     | QuadTimer                   | Timer Peripherals               | The quad-timer provides four time channels with a variety of controls affecting both individual and multi-channel features. Specific features include up/down count, cascading of counters, programmable module, count once/repeated, counter preload, compare registers with preload, shared use of input signals, prescaler controls, independent capture/compare, fault input control, programmable input filters, and multi-channel synchronization. |
| RDC                                                                      | Resource Domain Controller  | Security                        | The RDC provides robust support for the isolation of processing domain to prevent one core from accessing another's peripherals, to control access rights to common memory and provide hardware enforcement of semaphore based locking of shared peripherals. For single system use case, RDC can be disabled and AIPS-TZ/DEXSC can be bypassed. For dual system case, RDC can be configured and locked each core starts their own image.                |
| ROMCP                                                                    | ROM Controller with Patch   | Memories and Memory Controllers | The ROMCP acts as an interface between the Arm advanced high-performance bus and the ROM. The on-chip ROM is only used by the Cortex-M7 core during boot up. Size of the ROM is 256 KB.                                                                                                                                                                                                                                                                  |
| RTC OSC                                                                  | Real Time Clock Oscillator  | Clock Sources and Control       | The RTC OSC provides the clock source for the Real-Time Clock module. The RTC OSC module, in conjunction with an external crystal, generates a 32.768 kHz reference clock for the RTC.                                                                                                                                                                                                                                                                   |
| SAI1<br>SAI2<br>SAI3<br>SAI4                                             | Synchronous Audio Interface | Multimedia Peripherals          | The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.                                                                                                                                                                                                                                                                    |

Table 3. i.MX RT1160 modules list (continued)

| Block Mnemonic | Block Name                               | Subsystem                       | Brief Description                                                                                                                                                                                                                                                                                                      |
|----------------|------------------------------------------|---------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SEMA4          | Semaphores                               | System Control                  | The SEMA4 module implements hardware-enforced semaphores as an IPS-mapped slave peripheral device and provides 16 hardware-enforced gates in a dual-processor configuration.                                                                                                                                           |
| SEMC           | Smart External Memory Controller         | Memory and Memory Controller    | The SEMC is a multi-standard memory controller optimized for both high-performance and low pin-count. It can support multiple external memories in the same application with shared address and data pins. The interface supported includes SDRAM, NOR Flash, SRAM, and NAND Flash, as well as 8080 display interface. |
| SNVS           | Secure Non-Volatile Storage              | Security                        | Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine and Master Key Control.                                                                                                                                                                                                          |
| SPDIF          | Sony Philips Digital Interconnect Format | Multimedia Peripherals          | A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.                                                                                                                                                                            |
| SSARC          | State Save and Restore Controller        | Memories and Memory Controllers | The SSARC saves the registers of functional modules in memory before power down, and restores registers from memory after the module is powered up.                                                                                                                                                                    |
| TEMP SENSE     | Temperature Sensor                       | Analog                          | The temperature sensor implements a temperature sensor/conversion function based on a temperature-dependent voltage to time conversion.                                                                                                                                                                                |
| USB1<br>USB2   | Universal Serial Bus 2.0                 | Connectivity Peripherals        | USB 2.0 OTG modules (USB OTG1 and USB OTG2) contains: <ul style="list-style-type: none"> <li>• Two high-speed OTG 2.0 modules with integrated HS USB PHYs</li> <li>• Support eight Transmit (TX) and eight Receive (Rx) endpoints, including endpoint 0</li> </ul>                                                     |

Table 3. i.MX RT1160 modules list (continued)

| Block Mnemonic                   | Block Name                                                                          | Subsystem                   | Brief Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------------------------------|-------------------------------------------------------------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| uSDHC1<br>uSDHC2                 | SD/MMC and SDXC<br>Enhanced Multi-Media<br>Card / Secure Digital Host<br>Controller | Connectivity<br>Peripherals | <p>i.MX RT1160 specific SoC characteristics:<br/>All four MMC/SD/SDIO controllers are identical and are based on the uSDHC. They are:</p> <ul style="list-style-type: none"> <li>Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification.</li> <li>Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB.</li> <li>Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0</li> </ul> <p>Two ports support:</p> <ul style="list-style-type: none"> <li>1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max)</li> <li>1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)</li> <li>4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)</li> </ul> |
| VIDMUX                           | Video mux                                                                           | Mux control                 | Video mux are mux control for Parallel CSI (IO PADs), MIPI CSI-2, MIPI DSI, Parallel LCDIF (IO PADs) and CSI, LCDIF-V2, eLCDIF control. It also includes the DCIC of MIPI DSI and Parallel DSI.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| WDOG1<br>WDOG2<br>WDOG3<br>WDOG4 | Watch Dog                                                                           | Timer Peripherals           | <p>WDOG1 and WDOG2 Timer support two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the Arm core, and a second point evokes an external event on the WDOG line.</p> <p>WDOG3 and WDOG4 modules are high reliability independent timers that are available for system to use. They provide a safety feature to ensure software is executing as planned and the CPU is not stuck in an infinite loop or executing unintended code. If the WDOG module is not serviced (refreshed) within a certain period, it resets the MCU. Windowed refresh mode is supported as well.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| XBARA<br>XBARB                   | Cross BAR                                                                           | Cross Trigger               | Each crossbar switch is an array of muxes with shared inputs. Each mux output provides one output of the crossbar. The number of inputs and the number of muxes/outputs are user configurable and registers are provided to select which of the shared inputs are routed to each output.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

Table 3. i.MX RT1160 modules list (continued)

| Block Mnemonic | Block Name                          | Subsystem                       | Brief Description                                                                                                                                                                                                                                                                                                                                             |
|----------------|-------------------------------------|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| XECC           | External ECC Controller             | Memories and Memory Controllers | XECC can be used as a gasket module on AXI bus to support ECC function for external memory.                                                                                                                                                                                                                                                                   |
| XRDC           | Extended Resource Domain Controller | Security                        | The XRDC provides an integrated, scalable architectural framework for access control, system memory protection, and peripheral isolation. It allows software to assign chip resources including processor cores, non-core bus masters, memory regions, and slave peripherals to processing domains to support enforcement of robust operational environments. |

### 3.1 Special signal considerations

Table 4 lists special signal considerations for the i.MX RT1160 processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in [Section 6, Package information and contact assignments.](#) Signal descriptions are provided in the *i.MX RT1160 Reference Manual* (IMXRT1160RM).

Table 4. Special signal considerations

| Signal Name         | Remarks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK1_P/CLK1_N       | This differential output is reserved for NXP internal use. For users, this output must be a no connect.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| DCDC_PSWITCH        | PAD is in DCDC_IN domain and connected to ground to bypass DCDC.<br>To enable DCDC function, assert DCDC_IN with at least 1ms delay for DCDC_IN rising edge.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| RTC_XTALI/RTC_XTALO | To hit the exact oscillation frequency, the board capacitors must be reduced to account for the board and chip parasitics. The integrated oscillation amplifier is self-biasing, but relatively weak. Care must be taken to limit the parasitic leakage from RTC_XTALI and RTC_XTALO to either the power or the ground (> 100 M). This de-biases the amplifier and reduces the start-up margin. If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level of this forcing clock must not exceed the VDD_SNVS_DIG level and the frequency shall be < 100 kHz under the typical conditions.<br>It is recommended to tie RTC_XTALI to GND if external crystal is not used. When a high-accuracy real-time clock is not required, the system may use the on-chip 32 kHz oscillator. The tolerance is $\pm 10\%$ . The ring oscillator starts faster than the external crystal and is used until the external crystal reaches a stable oscillation. The ring oscillator also starts automatically if no clock is detected at RTC_XTALI. |
| XTALI/XTALO         | The SDK software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, refer to section of Bypass Configuration (24 MHz) from the reference manual. There are three configurations that can be utilized, but configuration 2 is recommended.<br>The logic level of this forcing clock must not exceed the VDD_LPSR_ANA level.<br>If this clock is used as a reference clock for USB, then there are strict frequency tolerance and jitter requirements. See <a href="#">Section 4.2.6, On-chip oscillators</a> and relevant interface specifications chapters for details.                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

**Table 4. Special signal considerations (continued)**

| Signal Name | Remarks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| JTAG_####   | <p>External resistors can be used with all JTAG signals except for JTAG_TDO, but they are not required. See <a href="#">Table 5</a> for a summary of the JTAG interface.</p> <p>JTAG_TDO is configured with an on-chip keeper circuit, such that the floating condition is actively eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental. See <a href="#">Table 5</a> for a summary of the JTAG interface.</p> <p>When JTAG_MOD is low, the JTAG interface is configured for a common software debug, adding all the system TAPs to the chain.<br/>When JTAG_MOD is high, the JTAG interface is configured to a mode compliant with the IEEE 1149.1 standard.</p>                                                                                                                                                                                                                                                                                    |
| NC          | These signals are No Connect (NC) and should not be connected by the user.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| POR_B       | <p>See the System Boot chapter in the reference manual for the correct boot configuration. Note that an incorrect setting may result from an improper boot sequence.</p> <p>POR_B signal has internal 100 k<math>\Omega</math> pull up to SNVS domain, should pull up to VDD_SNVS_ANA if need to add external pull up resistor, otherwise it will cause additional leakage during SNVS mode. It is recommended to add the external reset IC to the circuit to guarantee POR_B is properly processed during power up/down, please refer to the EVK design for details.</p> <p>Note:</p> <ul style="list-style-type: none"> <li>As the Low DCDC_IN detection threshold is 2.6 V, the reset IC's reset threshold must be higher than 2.6 V, then the whole chip is reset before the internal DCDC module reset to guarantee the chip safety during power down.</li> <li>For power on reset, on any conditions ones need to make sure the voltage on DCDC_PSWITCH pin is below 0.5 V before power up.</li> </ul> |
| ONOFF       | A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). Approximately five seconds (or more) to GND causes a forced OFF. Both boot mode inputs can be disconnected.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| TEST_MODE   | This input is reserved for NXP manufacturing use. The user must tie this pin directly to GND.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| WAKEUP      | A GPIO powered by SNVS domain power supply which can be configured as wakeup source in SNVS mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 5. JTAG controller interface summary**

| JTAG       | I/O Type       | On-chip Termination        |
|------------|----------------|----------------------------|
| JTAG_TCK   | Input          | 20–50 k $\Omega$ pull-down |
| JTAG_TMS   | Input          | 20–50 k $\Omega$ pull-up   |
| JTAG_TDI   | Input          | 20–50 k $\Omega$ pull-up   |
| JTAG_TDO   | 3-state output | High-impedance             |
| JTAG_TRSTB | Input          | 20–50 k $\Omega$ pull-up   |
| JTAG_MOD   | Input          | 20–50 k $\Omega$ pull-down |

## 3.2 Recommended connections for unused analog interfaces

[Table 6](#) shows the recommended connections for unused analog interfaces.

**Table 6. Recommended connections for unused analog interfaces**

| Module     | Pad Name                                                                           | Recommendations if Unused                                                                           |
|------------|------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|
| 32 kHz OSC | RTC_XTALI, RTC_XTALO                                                               | Not connected<br>It is recommended that RTC_XTALI ties to GND if external crystal is not connected. |
| ADC        | ADC_VREFH                                                                          | 10 K $\Omega$ resistor to ground                                                                    |
|            | VDDA_ADC_1P8                                                                       | 10 K $\Omega$ resistor to ground                                                                    |
|            | VDDA_ADC_3P3                                                                       | 10 K $\Omega$ resistor to ground                                                                    |
| CCM        | CLK1_N, CLK1_P                                                                     | Not connected                                                                                       |
| DAC        | DAC_OUT                                                                            | Not connected                                                                                       |
| MIPI       | VDD_MIPI_1P0                                                                       | 10 K $\Omega$ resistor to ground                                                                    |
|            | VDD_MIPI_1P8                                                                       | 10 K $\Omega$ resistor to ground                                                                    |
|            | MIPI_DSI_CKN, MIPI_DSI_CKP, MIPI_DSI_DN0, MIPI_DSI_DP0, MIPI_DSI_DN1, MIPI_DSI_DP1 | Not connected                                                                                       |
|            | MIPI_CSI_CKN, MIPI_CSI_CKP, MIPI_CSI_DN0, MIPI_CSI_DP0, MIPI_CSI_DN1, MIPI_CSI_DP1 | Not connected                                                                                       |
| DCDC       | DCDC_IN, DCDC_IN_Q, DCDC_DIG, DCDC_ANA                                             | Not connected                                                                                       |
|            | DCDC_DIG_SENSE, DCDC_ANA_SENSE, DCDC_LP, DCDC_LN                                   | Not connected                                                                                       |
|            | DCDC_PSWITCH, DCDC_MODE                                                            | To ground                                                                                           |
| USB        | USB1_DN, USB1_DP, USB1_VBUS, USB2_DN, USB2_DP, USB2_VBUS                           | Not connected                                                                                       |
|            | VDD_USB_1P8                                                                        | Powered with 1.8 V                                                                                  |
|            | VDD_USB_3P3                                                                        | Powered with 3.3 V                                                                                  |
| SYS OSC    | XTALI, XTALO                                                                       | Not connected                                                                                       |

## 4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX RT1160 processors.

### 4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See [Table 7](#) for a quick reference to the individual tables and sections.

**Table 7. i.MX RT1160 chip-Level conditions**

| For these characteristics                          | Topic appears              |
|----------------------------------------------------|----------------------------|
| <a href="#">Absolute maximum ratings</a>           | <a href="#">on page 23</a> |
| <a href="#">Thermal characteristics</a>            | <a href="#">on page 25</a> |
| <a href="#">Operating ranges</a>                   | <a href="#">on page 25</a> |
| <a href="#">Maximum supply currents</a>            | <a href="#">on page 28</a> |
| <a href="#">Typical power mode supply currents</a> | <a href="#">on page 29</a> |
| <a href="#">System power and clocks</a>            | <a href="#">on page 32</a> |

#### 4.1.1 Absolute maximum ratings

#### CAUTION

Stress beyond those listed under [Table 8](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[Table 8](#) shows the absolute maximum operating ratings.

**Table 8. Absolute maximum ratings**

| Parameter Description                                                   | Symbol                 | Min  | Max  | Unit |
|-------------------------------------------------------------------------|------------------------|------|------|------|
| Core supplies input voltage                                             | VDD_SOC_IN             | -0.3 | 1.2  | V    |
| Power for LPSR domain                                                   | VDD_LPSR_IN            | -0.3 | 3.96 | V    |
| Power for DCDC                                                          | DCDC_IN                | -0.3 | 3.96 | V    |
| Power for PLL, OSC, and LDOs                                            | VDDA_1P8_IN            | -0.3 | 1.98 | V    |
| Supply input voltage to Secure Non-Volatile Storage and Real Time Clock | VDD_SNVS_IN            | -0.3 | 3.96 | V    |
| USB VBUS supply                                                         | USB1_VBUS<br>USB2_VBUS | -0.3 | 5.6  | V    |

Table 8. Absolute maximum ratings (continued)

|                                                |                  |      |                |    |
|------------------------------------------------|------------------|------|----------------|----|
| Power for USB OTG PHYs                         | VDD_USB_1P8      | -0.3 | 1.98           | V  |
|                                                | VDD_USB_3P3      | -0.3 | 3.96           | V  |
| Power for ADC, DAC, and ACMP                   | VDDA_ADC_1P8     | -0.3 | 1.98           | V  |
|                                                | VDDA_ADC_3P3     | -0.3 | 3.96           | V  |
| Power for MIPI CSI/DSI PHY                     | VDD_MIPI_1P8     | -0.3 | 1.98           | V  |
|                                                | VDD_MIPI_1P0     | -0.3 | 1.2            | V  |
| IO supply for GPIO in SDIO1 bank (3.3 V mode)  | NVCC_SD1         | -0.3 | 3.96           | V  |
| IO supply for GPIO in SDIO1 bank (1.8 V mode)  |                  | -0.3 | 1.98           | V  |
| IO supply for GPIO in SDIO2 bank (3.3 V mode)  | NVCC_SD2         | -0.3 | 3.96           | V  |
| IO supply for GPIO in SDIO2 bank (1.8 V mode)  |                  | -0.3 | 1.98           | V  |
| IO supply for GPIO in EMC bank1 (3.3 V mode)   | NVCC_EMC1        | -0.3 | 3.96           | V  |
| IO supply for GPIO in EMC bank1 (1.8 V mode)   |                  | -0.3 | 1.98           | V  |
| IO supply for GPIO in EMC bank2 (3.3 V mode)   | NVCC_EMC2        | -0.3 | 3.96           | V  |
| IO supply for GPIO in EMC bank2 (1.8 V mode)   |                  | -0.3 | 1.98           | V  |
| IO power for GPIO in GPIO AD bank (3.3 V mode) | NVCC_GPIO        | -0.3 | 3.96           | V  |
| IO power for GPIO in GPIO AD bank (1.8 V mode) |                  | -0.3 | 1.98           | V  |
| IO supply for GPIO in DISP1 bank (3.3 V mode)  | NVCC_DISP1       | -0.3 | 3.96           | V  |
| IO supply for GPIO in DISP1 bank1 (1.8 V mode) |                  | -0.3 | 1.98           | V  |
| IO supply for GPIO in DISP2 bank (3.3 V mode)  | NVCC_DISP2       | -0.3 | 3.96           | V  |
| IO supply for GPIO in DISP2 bank1 (1.8 V mode) |                  | -0.3 | 1.98           | V  |
| IO power for GPIO in LPSR bank (3.3 V mode)    | NVCC_LPSR        | -0.3 | 3.96           | V  |
| IO power for GPIO in LPSR bank (1.8 V mode)    |                  | -0.3 | 1.98           | V  |
| IO power for GPIO in SNVS bank (1.8 V mode)    | NVCC_SNVS        | -0.3 | 1.98           | V  |
| Input/Output Voltage range                     | $V_{in}/V_{out}$ | -0.5 | $NVCC + 0.3^1$ | V  |
| Storage Temperature range                      | $T_{STORAGE}$    | -40  | 150            | °C |

<sup>1</sup> NVCC is the I/O supply voltage.

Table 9. Electrostatic discharge and latch-up characteristics

| Symbol    | Description                                       | Min   | Max   | Unit | Notes        |
|-----------|---------------------------------------------------|-------|-------|------|--------------|
| $V_{HBM}$ | Electrostatic discharge voltage, human body model | -2000 | +2000 | V    | <sup>1</sup> |

**Table 9. Electrostatic discharge and latch-up characteristics (continued)**

| Symbol           | Description                                              | Min  | Max  | Unit | Notes |
|------------------|----------------------------------------------------------|------|------|------|-------|
| V <sub>ESD</sub> | Electrostatic discharge voltage, charged-device model    |      |      |      |       |
|                  | All pins except the corner pins                          | -500 | +500 | V    | 2     |
|                  | Corner pins only                                         | -750 | +750 | V    |       |
| I <sub>LAT</sub> | Immunity level<br>• Class II @105 °C ambient temperature | 100  | 100  | mA   | 3     |

<sup>1</sup> Determined according to JEDEC Standard JS001, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

<sup>2</sup> Determined according to JEDEC Standard JS002, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

<sup>3</sup> Determined according to JEDEC Standard JESD78, *IC Latch-up Test*.

## 4.1.2 Thermal characteristics

Table 10 displays the 14 x 14 mm package thermal characteristics.

**Table 10. 14 x 14 mm thermal characteristics**

| Rating                                                                     | Board Type <sup>1</sup> | Symbol                        | Value | Unit |
|----------------------------------------------------------------------------|-------------------------|-------------------------------|-------|------|
| Junction to Ambient Thermal Resistance <sup>2</sup>                        | JESD51-9, 2s2p          | R <sub>θJA</sub> <sup>3</sup> | 31.6  | °C/W |
| Junction to Top of Package Thermal Characterization Parameter <sup>2</sup> | JESD51-9, 2s2p          | Ψ <sub>JT</sub> <sup>4</sup>  | 1.4   | °C/W |
| Junction to Case Thermal Resistance <sup>5</sup>                           | JESD51-9, 1s            | R <sub>θJC</sub> <sup>6</sup> | 10    | °C/W |

<sup>1</sup> Thermal test board meets JEDEC specification for this package (JESD51-9).

<sup>2</sup> Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.

<sup>3</sup>  $R_{\theta JA} = (T_j - T_a)/P$  [unit: °C/W], where  $T_j$  = junction temperature,  $T_a$  = ambient temperature,  $P$  = device power.

<sup>4</sup>  $\Psi_{JT} = (T_j - T_t)/P$  [unit: °C/W], where  $T_j$  = junction temperature,  $T_t$  = temperature at top of package,  $P$  = device power.

<sup>5</sup> Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature is taken at the package top side centre surface temperature.

<sup>6</sup>  $R_{\theta JC} = (T_j - T_c)/P$  [unit: °C/W], where  $T_j$  = junction temperature,  $T_c$  = case temperature,  $P$  = device power.

## 4.1.3 Operating ranges

Table 11 provides the operating ranges of the i.MX RT1160 processors. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX RT1160 Reference Manual (IMXRT1160RM)*.

Table 11. Operating ranges

| Parameter Description        | Symbol       | Operating Conditions | Min  | Max <sup>1</sup> | Unit | Comment |
|------------------------------|--------------|----------------------|------|------------------|------|---------|
| Run Mode                     | VDD_SOC_IN   | M7 core at 500 MHz   | 1.0  | 1.15             | V    | —       |
|                              |              | M7 core at 240 MHz   | 0.9  | 1.15             | V    | —       |
|                              | VDD_LPSR_DIG | M4 core at 240 MHz   | 1.0  | 1.15             | V    | —       |
|                              |              | M4 core at 120 MHz   | 0.9  | 1.15             | V    | —       |
| STANDBY Mode                 | VDD_SOC_IN   | M7 core              | 0.8  | 1.15             | V    | —       |
|                              | VDD_LPSR_DIG | M4 core              | 0.8  | 1.15             | V    | —       |
| Power for DCDC               | DCDC_IN      | —                    | 3.0  | 3.6              | V    | —       |
| Power for PLL, OSC, and LDOs | VDDA_1P8_IN  | —                    | 1.71 | 1.89             | V    | —       |
| Power for LPSR domain        | VDD_LPSR_IN  | —                    | 3.0  | 3.6              | V    | —       |
| Power for SNVS and RTC       | VDD_SNVS_IN  | —                    | 2.4  | 3.6              | V    | —       |
| Power for USB OTG PHYs       | VDD_USB_1P8  | —                    | 1.65 | 1.95             | V    | —       |
|                              | VDD_USB_3P3  | —                    | 3.0  | 3.6              | V    | —       |
| Power for ADC, DAC, and ACMP | VDDA_ADC_1P8 | —                    | 1.65 | 1.95             | V    | —       |
|                              | VDDA_ADC_3P3 | —                    | 3.0  | 3.6              | V    | —       |
|                              | ADC_VREFH    | —                    | 1.0  | 1.89             | V    | —       |
| Power for MIPI CSI/DSI PHY   | VDD_MIPI_1P8 | —                    | 1.65 | 1.95             | V    | —       |
|                              | VDD_MIPI_1P0 | —                    | 0.9  | 1.1              | V    | —       |

Table 11. Operating ranges (continued)

|                              |                |                     |      |      |    |                                                                                                                                                 |
|------------------------------|----------------|---------------------|------|------|----|-------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO supplies                | NVCC_SD1       | —                   | 3.0  | 3.6  | V  | IO power for GPIO in SDIO1 bank (3.3 V mode)                                                                                                    |
|                              |                | —                   | 1.65 | 1.95 | V  | IO power for GPIO in SDIO1 bank (1.8 V mode)                                                                                                    |
|                              | NVCC_SD2       | —                   | 3.0  | 3.6  | V  | IO power for GPIO in SDIO2 bank (3.3 V mode)                                                                                                    |
|                              |                | —                   | 1.65 | 1.95 | V  | IO power for GPIO in SDIO2 bank (1.8 V mode)                                                                                                    |
|                              | NVCC_EMC1      | —                   | 3.0  | 3.6  | V  | IO power for GPIO in EMC bank1 (3.3 V mode)                                                                                                     |
|                              |                | —                   | 1.65 | 1.95 | V  | IO power for GPIO in EMC bank1 (1.8 V mode)                                                                                                     |
|                              | NVCC_EMC2      | —                   | 3.0  | 3.6  | V  | IO power for GPIO in EMC bank2 (3.3 V mode)                                                                                                     |
|                              |                | —                   | 1.65 | 1.95 | V  | IO power for GPIO in EMC bank2 (1.8 V mode)                                                                                                     |
|                              | NVCC_GPIO      | —                   | 3.0  | 3.6  | V  | IO power for GPIO in GPIO AD bank (3.3 V mode)                                                                                                  |
|                              |                | —                   | 1.65 | 1.95 | V  | IO power for GPIO in GPIO AD bank (1.8 V mode)                                                                                                  |
|                              | NVCC_DISP1     | —                   | 3.0  | 3.6  | V  | IO power for GPIO in DISP1 bank (3.3 V mode)                                                                                                    |
|                              |                | —                   | 1.65 | 1.95 | V  | IO power for GPIO in DISP1 bank (1.8 V mode)                                                                                                    |
|                              | NVCC_DISP2     | —                   | 3.0  | 3.6  | V  | IO power for GPIO in DISP2 bank (3.3 V mode)                                                                                                    |
|                              |                | —                   | 1.65 | 1.95 | V  | IO power for GPIO in DISP2 bank (1.8 V mode)                                                                                                    |
|                              | NVCC_LPSR      | —                   | 3.0  | 3.6  | V  | IO power for GPIO in LPSR bank (3.3 V mode)                                                                                                     |
|                              |                | —                   | 1.65 | 1.95 | V  | IO power for GPIO in LPSR bank (1.8 V mode)                                                                                                     |
|                              | NVCC_SNVS      | —                   | 1.65 | 1.95 | V  | IO power for GPIO in SNVS bank (1.8 V mode)                                                                                                     |
| Temperature Operating Ranges |                |                     |      |      |    |                                                                                                                                                 |
| Junction temperature         | T <sub>j</sub> | Standard Industrial | -40  | 105  | °C | See the application note, i.MX RT1160 Product Lifetime Usage Estimates for information on product lifetime (power-on years) for this processor. |

<sup>1</sup> Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = ( $V_{\min}$  + the supply tolerance). This results in an optimized power/speed ratio.

#### 4.1.4 Maximum supply currents

The data shown in [Table 12](#) represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention were to specifically show the worst case power consumption.

**Table 12. Maximum supply currents**

| Power Rail                                                                                                        | Comments                                                                                                                                                                                                                                                                                                                             | Max Current | Unit |
|-------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------|
| DCDC_IN                                                                                                           | Max power for chip at 105 °C                                                                                                                                                                                                                                                                                                         | 500         | mA   |
| VDDA_1P8_IN                                                                                                       | 1.8 V power supply for PLL, OSC, and LDOs                                                                                                                                                                                                                                                                                            | 100         | mA   |
| VDD_SOC_IN                                                                                                        | Power supply for digital logic                                                                                                                                                                                                                                                                                                       | 850         | mA   |
| VDD_LPSR_IN                                                                                                       | 3.3 V power supply for LPSR domain                                                                                                                                                                                                                                                                                                   | 75          | mA   |
| VDD_SNVS_IN                                                                                                       | Power supply for SNVS domain                                                                                                                                                                                                                                                                                                         | 1           | mA   |
| VDD_USB_1P8                                                                                                       | 1.8 V power supply for USB OTG PHYs                                                                                                                                                                                                                                                                                                  | 50          | mA   |
| VDD_USB_3P3                                                                                                       | 3.3 V power supply for USB OTG PHYs                                                                                                                                                                                                                                                                                                  | 60          | mA   |
| VDDA_ADC_1P8                                                                                                      | 1.8 V power supply for ADC, DAC, and ACMP                                                                                                                                                                                                                                                                                            | 10          | mA   |
| VDDA_ADC_3P3<br>ADC_VREFH                                                                                         | 3.3 V power supply for ADC, DAC, and ACMP                                                                                                                                                                                                                                                                                            | 2           | mA   |
| VDD_MIPI_1P8                                                                                                      | 1.8 V power supply for MIPI CSI/DSI PHY                                                                                                                                                                                                                                                                                              | 100         | mA   |
| VDD_MIPI_1P0                                                                                                      | 1.0 V power supply for MIPI CSI/DSI PHY                                                                                                                                                                                                                                                                                              | 30          | mA   |
| NVCC_SD1<br>NVCC_SD2<br>NVCC_EMC1<br>NVCC_EMC2<br>NVCC_GPIO<br>NVCC_DISP1<br>NVCC_DISP2<br>NVCC_LPSR<br>NVCC_SNVS | $I_{max} = N \times C \times V \times (0.5 \times F)$<br>Where:<br>N—Number of IO pins supplied by the power line<br>C—Equivalent external capacitive load<br>V—IO voltage<br>(0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F)<br>In this equation, I <sub>max</sub> is in Amps, C in Farads, V in Volts, and F in Hertz. |             |      |

### 4.1.5 Typical power mode supply currents

Table 13 shows the current and power consumption (not including I/O) of i.MX RT1160 processors in selected power modes.

**Table 13. Typical power modes current and power consumption (Dual core)**

| Modes                  | Test conditions                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Power supplies at 3.3 V (Typical) <sup>1</sup> |          |           | Units |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|----------|-----------|-------|
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                | 25 °C Tj | 105 °C Tj |       |
| Set Point #0<br>Active | <ul style="list-style-type: none"> <li>CM7 runs at 500 MHz, drive voltage to 1.0 V; CM4 runs at 240 MHz, drive voltage to 1.0 V</li> <li>CM7 domain bus frequency at 200 MHz; CM4 domain bus frequency at 120 MHz</li> <li>Enables ECC for cache, TCM, and OCRAM</li> <li>LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed</li> <li>16 MHz, 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled</li> <li>All PLLs are enabled</li> <li>All peripherals are enabled and run at their maximum clock root frequency under normal drive mode</li> </ul> | DCDC_IN                                        | 83.4     | 137.6     | mA    |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VDD_LPSR_IN                                    | 28.1     | 30.8      | μA    |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VDD_SNVIS_IN                                   | 4        | 12        | μA    |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Total                                          | 275.326  | 454.221   | mW    |
| Set Point #5<br>Active | <ul style="list-style-type: none"> <li>CM7 runs at 240 MHz, lower voltage to 0.9 V; CM4 runs at 120 MHz, lower voltage to 0.9 V</li> <li>CM7 domain bus frequency at 100 MHz; CM4 domain bus frequency at 60 MHz</li> <li>Enables ECC for cache, TCM, and OCRAM</li> <li>LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed</li> <li>16 MHz, 400 MHz, external 24 MHz crystal, and external 32 kHz crystal are enabled</li> <li>All PLLs are enabled</li> <li>All peripherals are enabled and run at their maximum clock root frequency under underdrive mode</li> </ul>    | DCDC_IN                                        | 43.3     | 74.1      | mA    |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VDD_LPSR_IN                                    | 28.1     | 30.5      | μA    |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VDD_SNVIS_IN                                   | 3.9      | 11.4      | μA    |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Total                                          | 142.996  | 244.668   | mW    |
| Set Point #7<br>Active | <ul style="list-style-type: none"> <li>CM7 runs at 200 MHz, lower voltage to 0.9 V; CM4 is clock gated, lower voltage to 0.9 V</li> <li>CM7 domain bus frequency at 100 MHz</li> <li>Enables ECC for cache, TCM, and OCRAM</li> <li>LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed</li> <li>16 MHz, 400 MHz, and external 32 kHz crystal are enabled</li> <li>All PLLs are power gated</li> <li>All peripherals controlled by CM4 core are clock gated, but remain powered</li> </ul>                                                                                   | DCDC_IN                                        | 24.9     | 52.6      | mA    |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VDD_LPSR_IN                                    | 28.1     | 30.3      | μA    |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | VDD_SNVIS_IN                                   | 3.9      | 11.1      | μA    |
|                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Total                                          | 82.276   | 173.717   | mW    |

**Table 13. Typical power modes current and power consumption (Dual core) (continued)**

|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |             |         |         |    |
|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------|---------|----|
| Set Point #9<br>Active             | <ul style="list-style-type: none"> <li>CM7 is clock gated, lower voltage to 0.9 V; CM4 runs at 100 MHz, lower voltage to 0.9 V</li> <li>CM4 domain bus frequency at 50 MHz</li> <li>Enables ECC for cache, TCM, and OCRAM</li> <li>LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed</li> <li>16 MHz, 400 MHz, and external 32 kHz crystal are enabled</li> <li>All PLLs are power gated</li> <li>All peripherals controlled by CM7 core are clock gated, but remain powered</li> </ul>                                       | DCDC_IN     | 14.5    | 39.5    | mA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD_LPSR_IN | 28.2    | 30.2    | μA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD_SNVS_IN | 3.9     | 11      | μA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Total       | 47.956  | 130.486 | mW |
| Set Point #11<br>Active            | <ul style="list-style-type: none"> <li>CM7 is power off; CM4 runs at 200 MHz, drive voltage to 1.0 V</li> <li>CM4 domain bus frequency at 100 MHz</li> <li>Enables ECC for CM4 TCM and OCRAM</li> <li>DCDC is off, LDO_LPSR_ANA and LDO_LPSR_DIG are active</li> <li>16 MHz, 400 MHz, and external 32 kHz crystal are enabled</li> <li>All PLLs are power gated</li> <li>The WAKEUPMIX domain, MEGAMIX domain, and DISPLAYMIX domain are power gated</li> <li>All peripherals in LPSRMIX domain are clocked</li> </ul> | DCDC_IN     | 26.5    | 41.8    | μA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD_LPSR_IN | 38.2    | 46.9    | mA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD_SNVS_IN | 3.9     | 11.3    | μA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Total       | 126.160 | 154.945 | mW |
| Set Point #12<br>Active            | <ul style="list-style-type: none"> <li>CM7 is power off; CM4 runs at 100 MHz, lower voltage to 0.9 V</li> <li>CM4 domain bus frequency at 50 MHz</li> <li>Enables ECC for CM4 TCM and OCRAM</li> <li>DCDC is off, LDO_LPSR_ANA and LDO_LPSR_DIG are active</li> <li>16 MHz, 400 MHz, and external 32 kHz crystal are enabled</li> <li>All PLLs are power gated</li> <li>The WAKEUPMIX domain, MEGAMIX domain, and DISPLAYMIX domain are power gated</li> <li>All peripherals in LPSRMIX domain are clocked</li> </ul>  | DCDC_IN     | 26.2    | 41.1    | μA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD_LPSR_IN | 22.9    | 28.9    | mA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD_SNVS_IN | 3.9     | 11      | μA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Total       | 75.669  | 95.542  | mW |
| Set Point #0<br>Standby<br>Suspend | <ul style="list-style-type: none"> <li>System is on STANDBY mode</li> <li>Both CM7 and CM4 are on SUSPEND mode</li> <li>TCM with ECC is on retention</li> <li>LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed</li> <li>All clock sources are turned off except for 32 kHz RTC</li> <li>All PLLs are power gated</li> <li>All peripherals are clock gated, but remain powered</li> </ul>                                                                                                                                     | DCDC_IN     | 3       | 19.4    | mA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD_LPSR_IN | 29.9    | 41.1    | μA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | VDD_SNVS_IN | 3.9     | 10.8    | μA |
|                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Total       | 10.012  | 64.191  | mW |

**Table 13. Typical power modes current and power consumption (Dual core) (continued)**

|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |              |       |        |    |
|-------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------|--------|----|
| Set Point #5<br>Standby<br>Suspend  | <ul style="list-style-type: none"> <li>System is on STANDBY mode</li> <li>Both CM7 and CM4 are on SUSPEND mode</li> <li>TCM with ECC is on retention</li> <li>LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed</li> <li>All clock sources are turned off except for 32 kHz RTC</li> <li>All PLLs are power gated</li> <li>All peripherals are clock gated, but remain powered</li> </ul>                                                                                                                           | DCDC_IN      | 2.3   | 14.6   | mA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | VDD_LPSR_IN  | 29.8  | 41.3   | μA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | VDD_SNVIS_IN | 3.8   | 10.7   | μA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Total        | 7.701 | 48.352 | mW |
| Set Point #7<br>Standby<br>Suspend  | <ul style="list-style-type: none"> <li>System is on STANDBY mode</li> <li>Both CM7 and CM4 are on SUSPEND mode</li> <li>TCM with ECC is on retention</li> <li>LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed</li> <li>All clock sources are turned off except for 32 kHz RTC</li> <li>All PLLs are power gated</li> <li>All peripherals are clock gated, but remain powered</li> </ul>                                                                                                                           | DCDC_IN      | 2.3   | 14.6   | mA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | VDD_LPSR_IN  | 29.8  | 41.3   | μA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | VDD_SNVIS_IN | 3.8   | 10.7   | μA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Total        | 7.701 | 48.352 | mW |
| Set Point #10<br>Standby<br>Suspend | <ul style="list-style-type: none"> <li>Lower voltage to 0.8 V with RBB mode for both SOC and LPSR domains</li> <li>System is on STANDBY mode</li> <li>Both CM7 and CM4 are on SUSPEND mode</li> <li>TCM with ECC is on retention</li> <li>LDO_LPSR_ANA and LDO_LPSR_DIG are bypassed</li> <li>All clock sources are turned off except for 32 kHz RTC</li> <li>All PLLs are power gated</li> <li>All peripherals are clock gated, but remain powered</li> </ul>                                               | DCDC_IN      | 1.8   | 11     | mA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | VDD_LPSR_IN  | 29.7  | 41.2   | μA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | VDD_SNVIS_IN | 3.8   | 10.7   | μA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Total        | 6.051 | 36.471 | mW |
| Set Point #11<br>Standby<br>Suspend | <ul style="list-style-type: none"> <li>System is on STANDBY mode</li> <li>CM7 is power off, CM4 is on SUSPEND mode</li> <li>CM4 TCM with ECC is on retention</li> <li>DCDC is off, LDO_LPSR_ANA and LDO_LPSR_DIG are active</li> <li>All clock sources are turned off except for 32 kHz RTC</li> <li>All PLLs are power gated</li> <li>The WAKEUPMIX domain, MEGAMIX domain, and DISPLAYMIX domain are power gated</li> <li>All peripherals in LPSRMIX domain are clock gated, but remain powered</li> </ul> | DCDC_IN      | 26.1  | 40.8   | μA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | VDD_LPSR_IN  | 0.893 | 7.1    | mA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | VDD_SNVIS_IN | 3.8   | 10.6   | μA |
|                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Total        | 3.046 | 23.600 | mW |

**Table 13. Typical power modes current and power consumption (Dual core) (continued)**

|                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |             |       |        |    |
|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------|--------|----|
| Set Point #15 Standby Suspend | <ul style="list-style-type: none"> <li>Lower voltage to 0.8 V with RBB mode for LPSR domain</li> <li>System is on STANDBY mode</li> <li>CM7 is power off, CM4 is on SUSPEND mode</li> <li>CM4 TCM with ECC is on retention</li> <li>DCDC is off, LDO_LPSR_ANA and LDO_LPSR_DIG are active</li> <li>All clock sources are turned off except for 32 kHz RTC</li> <li>All PLLs are power gated</li> <li>The WAKEUPMIX domain, MEGAMIX domain, and DISPLAYMIX domain are power gated</li> <li>All peripherals in LPSRMIX domain are clock gated, but remain powered</li> </ul> | DCDC_IN     | 26.1  | 40.6   | μA |
|                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | VDD_LPSR_IN | 0.503 | 4.6    | mA |
|                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | VDD_SNVS_IN | 3.8   | 10.6   | μA |
|                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Total       | 1.759 | 15.349 | mW |
| SNVS                          | <ul style="list-style-type: none"> <li>Only SNVS domain is powered</li> <li>32 kHz RTC is alive</li> <li>DCDC_IN and VDD_LPSR_IN are power gated</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                | DCDC_IN     | 0     | 0      | μA |
|                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | VDD_LPSR_IN | 0     | 0      | μA |
|                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | VDD_SNVS_IN | 3.8   | 10.7   | μA |
|                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Total       | 12.54 | 35.31  | μW |

<sup>1</sup> Code runs in the ITCM; typical values are the average values on typical process wafers.

Table 14 shows the typical wakeup time.

**Table 14. Typical wakeup time<sup>1</sup>**

| Description                                                         | Typical wakeup time | Unit |
|---------------------------------------------------------------------|---------------------|------|
| From Set Point #0 Standby Suspend to Set Point #0 normal drive RUN  | 4.13                | ms   |
| From Set Point #5 Standby Suspend to Set Point #0 normal drive RUN  | 4.79                | ms   |
| From Set Point #10 Standby Suspend to Set Point #0 normal drive RUN | 5.47                | ms   |
| From Set Point #15 Standby Stop to Set Point #0 normal drive RUN    | 7.6                 | ms   |
| From SNVS mode to ROM exit                                          | 8.54                | ms   |

<sup>1</sup> Please refer to Table 13 for Set Point modes definition, and the only difference between Set Point #15 Standby Suspend mode and Set Point #15 Standby Stop mode is the Suspend mode versus Stop mode on CM4 core.

## 4.2 System power and clocks

This section provides the information about the system power and clocks.

### 4.2.1 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting

- Irreversible damage to the processor (worst-case scenario)

Figure 4 shows the power sequence.

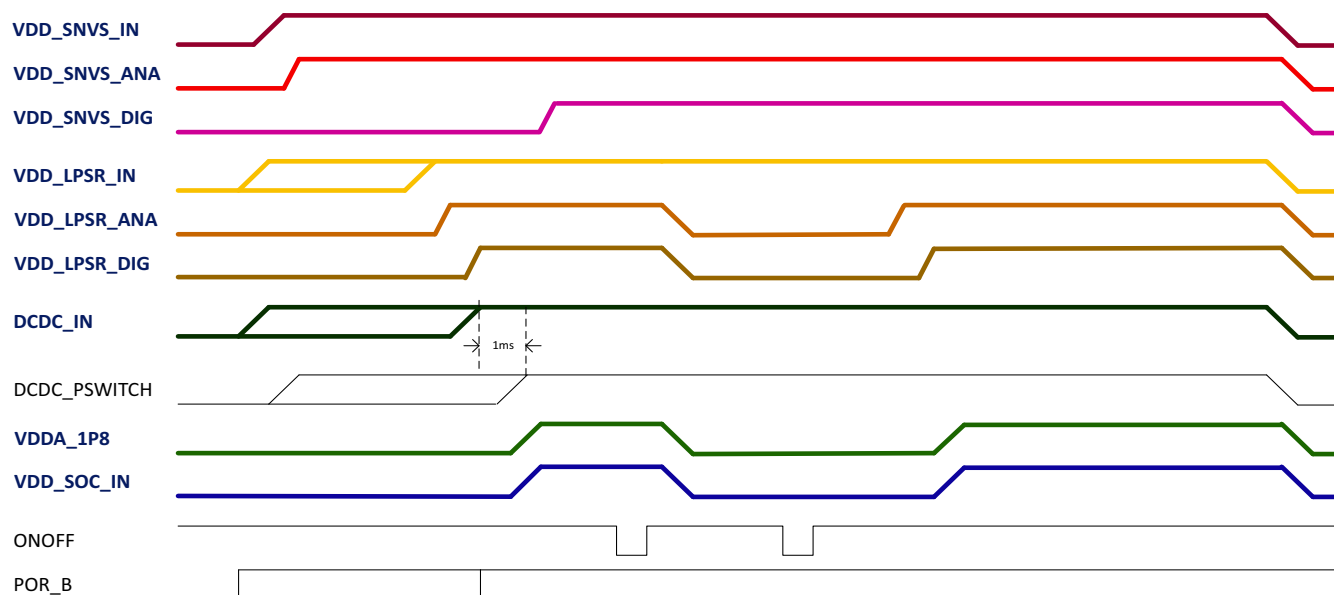


Figure 4. Power sequence

#### 4.2.1.1 Power-up sequence

The below restrictions must be followed:

- VDD\_SNVS\_IN supply must be turned on before any other power supply or be connected (shorted) with VDD\_LPSR\_IN and DCDC\_IN supply.
- If a coin cell is used to power VDD\_SNVS\_IN, then ensure that it is connected before any other supply is switched on.
- When internal DCDC is enabled, external delay circuit is required to delay the “DCDC\_PSWITCH” signal at least 1 ms after DCDC\_IN is stable.
- Need to ensure DCDC\_IN ramps to 3.0 V within  $0.2 \times RC$ , RC is from external delay circuit used for DCDC\_PSWITCH and must be longer than 1 ms.
- POR\_B (if used) must be held low during the entire power up sequence.

#### NOTE

The POR\_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR\_B input, the internal POR module takes control. See the *i.MX RT1160 Reference Manual* ([IMXRT1160RM](#)) for further details and to ensure that all necessary requirements are being met.

**NOTE**

The voltage on DCDC\_PSWITCH pin should be below 0.5 V before ramping up the voltage on DCDC\_PSWITCH.

**NOTE**

The power rail VDD\_SNVS\_DIG is controlled by software.

**NOTE**

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

**NOTE**

USB1\_VBUS, USB2\_VBUS, and VDDA\_ADC\_3P3 are not part of the power supply sequence and may be powered at any time.

#### 4.2.1.2 Power-down sequence

The following restrictions must be followed:

- VDD\_SNVS\_IN supply must be turned off after any other power supply or be connected (shorted) with VDD\_LPSR\_IN and DCDC\_IN supply.
- If a coin cell is used to power VDD\_SNVS\_IN, then ensure that it is removed after any other supply is switched off.

#### 4.2.1.3 Power supplies usage

I/O pins should not be externally driven while the I/O power supply for the pin (NVCC\_XXXX) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of [Section 6, Package information and contact assignments](#).”

### 4.2.2 Internal POR and power detect

Internal detector monitors VDD\_SOC\_IN and VDD\_LPSR\_DIG. Internal POR will be asserted whenever VDD\_SOC\_IN or VDD\_LPSR\_DIG are lower than the valid voltage values shown in the [Table 15](#).

**Table 15. Internal POR and power detect**

| Symbol                    | Description             | Value | Unit |
|---------------------------|-------------------------|-------|------|
| V <sub>detlpsr1p0_H</sub> | 1.0 V supply valid      | 0.75  | V    |
| V <sub>detloc1p0_H</sub>  | 1.0 V supply valid      | 0.75  | V    |
| Hyst <sub>det1p0</sub>    | The detector hysteresis | 100   | mV   |

### 4.2.3 Integrated LDO voltage regulator parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. The on-chip LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX RT1160 Reference Manual (IMXRT1160RM)* for details on the power tree scheme.

#### 4.2.3.1 LDO\_SNVS\_ANA

Table 16 shows the parameters of LDO\_SNVS\_ANA.

Table 16. LDO\_SNVS\_ANA specification

| Specification                 | Min  | Typ  | Max  | Unit |
|-------------------------------|------|------|------|------|
| VDD_SNVS_IN                   | 2.4  | 3    | 3.6  | V    |
| VDD_SNVS_ANA                  | 1.65 | 1.75 | 1.95 | V    |
| I <sub>out</sub>              | —    | —    | 1    | mA   |
| External decoupling capacitor | —    | 2.2  | —    | μF   |

#### 4.2.3.2 LDO\_SNVS\_DIG

Table 17 shows the parameters of LDO\_SNVS\_DIG.

Table 17. LDO\_SNVS\_DIG specification

| Specification                 | Min  | Typ  | Max  | Unit |
|-------------------------------|------|------|------|------|
| VDD_SNVS_ANA                  | 1.65 | 1.75 | 1.95 | V    |
| VDD_SNVS_DIG                  | 0.65 | 0.85 | 0.95 | V    |
| I <sub>out</sub>              | —    | —    | 1    | mA   |
| External decoupling capacitor | —    | 0.22 | —    | μF   |

#### 4.2.3.3 LDO\_PLL

Table 18 shows the parameters of LDO\_PLL.

Table 18. LDO\_PLL specification

| Specification                 | Min  | Typ | Max  | Unit |
|-------------------------------|------|-----|------|------|
| VDDA_1P8_IN                   | 1.71 | 1.8 | 1.89 | V    |
| VDDA_1P0                      | 0.9  | 1   | 1.2  | V    |
| I <sub>out</sub>              | —    | —   | 70   | mA   |
| External decoupling capacitor | —    | 2.2 | —    | μF   |

#### 4.2.3.4 LPSR\_LDO\_DIG

LPSR\_LDO\_DIG provides 1.0 V power source (VDD\_LPSR\_DIG) from 1.8V power domain (VDD\_LPSR\_ANA). The trim voltage range of LDO output is from 0.7 V to 1.15 V. There are two work

## Electrical characteristics

modes: Low Power mode and High Power mode. In typical PVT case, the static current consumption is less than 3  $\mu$ A in Low Power mode. The maximum drive strength of this LDO regulator is 50 mA in High Power mode.

**Table 19. LPSR\_LDO\_DIG specification**

| Specification                 | Min  | Typ | Max  | Unit    |
|-------------------------------|------|-----|------|---------|
| VDD_LPSR_ANA                  | 1.71 | 1.8 | 1.89 | V       |
| VDD_LPSR_DIG                  | 0.7  | 1   | 1.15 | V       |
| I <sub>out</sub>              | —    | —   | 50   | mA      |
| External decoupling capacitor | —    | 2.2 | —    | $\mu$ F |

### 4.2.3.5 LPSR\_LDO\_ANA

LPSR\_LDO\_ANA provides 1.8 V power source (VDD\_LPSR\_ANA) from 3.3 V power domain (VDD\_LPSR\_IN). Its default output value is 1.8 V. Two work modes are supported by this LDO: Low Power mode and High Power mode. In Low Power mode, the LDO provides 2 mA (maximum value) by consuming only 4  $\mu$ A current. In High Power mode, the LDO provides 75 mA current capacity with 40  $\mu$ A static power dissipation.

**Table 20. LPSR\_LDO\_ANA specification**

| Specification                 | Min | Typ | Max | Unit    |
|-------------------------------|-----|-----|-----|---------|
| VDD_LPSR_IN                   | 3   | 3.3 | 3.6 | V       |
| VDD_LPSR_ANA                  | —   | 1.8 | —   | V       |
| I <sub>out</sub>              | —   | —   | 75  | mA      |
| External decoupling capacitor | —   | 4.7 | —   | $\mu$ F |

### 4.2.4 DCDC

DCDC can be configured to operate on power-save mode when the load current is less than 50 mA. During the power-save mode, the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency.

DCDC can detect the peak current in the P-channel switch. When the peak current exceeds the threshold, DCDC will give an alert signal, and the threshold can be configured. By this way, DCDC can roughly detect the current loading.

DCDC also includes the following protection functions:

- Over current protection. In run mode, DCDC shuts down when detecting abnormal large current in the P-type power switch.
- Over voltage protection. DCDC shuts down when detecting the output voltage is too high.
- Low voltage detection. DCDC shuts down when detecting the input voltage is too low.

Table 21 shows DCDC characteristics.

Table 21. DCDC characteristics

| Description             | Min   | Typ                                  | Max   | Unit    | Comments                                                                |
|-------------------------|-------|--------------------------------------|-------|---------|-------------------------------------------------------------------------|
| Input voltage           | 3     | 3.3                                  | 3.6   | V       | —                                                                       |
| Output voltage          |       |                                      |       |         |                                                                         |
| • 1.0 V output          | 0.6   | 1                                    | 1.375 | V       | 25 mV per step                                                          |
| • 1.8 V output          | 1.5   | 1.8                                  | 2.275 | V       | 25 mV per step                                                          |
| Loading                 |       |                                      |       |         |                                                                         |
| • 1.0 V output          | —     | 150                                  | 850   | mA      | —                                                                       |
| • 1.8 V output          | —     | 80                                   | 150   | mA      | —                                                                       |
| Efficiency              |       |                                      |       |         |                                                                         |
| • DCDC run mode         | —     | 80%                                  | —     | —       | 150 mA@vdd1p0<br>80 mA@vdd1p8                                           |
| • DCDC low power mode   | —     | 80%                                  | —     | —       | 300 $\mu$ A@vdd1p0<br>300 $\mu$ A@vdd1p8                                |
| Output voltage accuracy |       |                                      |       |         |                                                                         |
| • DCDC Run mode         | -2.5% | —                                    | 2.5%  | —       | Maximum 50 mV<br>Vp-p@vdd1p0                                            |
| • DCDC Low power mode   | -6%   | —                                    | 6%    | —       | —                                                                       |
| Over current detection  | —     | 1.5                                  | —     | A       | The typical value can be<br>configured as 1.5 A and<br>2 A by register. |
| Over voltage detection  |       |                                      |       |         |                                                                         |
| • Output 1.8 V          | —     | 2.5                                  | 2.75  | V       | —                                                                       |
| • Output 1.0 V          | —     | 1.5                                  | 1.65  | V       | —                                                                       |
| • Low DCDC_IN detection | —     | 2.6                                  | 2.8   | V       | —                                                                       |
| Leakage current         | —     | 3                                    | —     | $\mu$ A | DCDC off                                                                |
| Quiescent current       |       |                                      |       |         |                                                                         |
| • DCDC Run mode         | —     | 150                                  | —     | $\mu$ A | —                                                                       |
| • DCDC Low power mode   | —     | 5                                    | —     | $\mu$ A | —                                                                       |
| Capacitor value         | —     | 33<br>(DCDC_ANA)<br>66<br>(DCDC_DIG) | —     | $\mu$ F | High frequency<br>capacitor are also<br>required.                       |
| Inductor value          | —     | 4.7                                  | —     | $\mu$ H | —                                                                       |
| • Saturation current    | —     | 1                                    | —     | A       | —                                                                       |

For additional information, see the *i.MX RT1160 Reference Manual* ([IMXRT1160RM](#)).

## 4.2.5 PLL's electrical characteristics

This section provides PLL electrical characteristics.

### 4.2.5.1 Audio/Video PLL's electrical parameters

**Table 22. Audio/Video PLL's electrical parameters**

| Parameter           | Min  | Typ | Max   | Unit             |
|---------------------|------|-----|-------|------------------|
| Clock output range  | 650  | —   | 1300  | MHz              |
| Reference clock     | —    | 24  | —     | MHz              |
| Lock time           | —    | —   | 11250 | reference cycles |
| Period jitter (p2p) | —    | 50  | —     | ps               |
| Duty cycle          | 48.5 | —   | 51.5  | %                |

### 4.2.5.2 528 MHz PLL

**Table 23. 528 MHz PLL's electrical parameters**

| Parameter               | Min | Typ | Max   | Unit             |
|-------------------------|-----|-----|-------|------------------|
| Clock output range      | —   | —   | 528   | MHz              |
| Reference clock         | —   | 24  | —     | MHz              |
| Lock time               | —   | —   | 11250 | reference cycles |
| Period jitter (p2p)     | —   | 50  | —     | ps               |
| PFD period jitter (p2p) | —   | 100 | —     | ps               |
| Duty cycle              | 45  | —   | 55    | %                |

### 4.2.5.3 Ethernet PLL

**Table 24. Ethernet PLL's electrical parameters**

| Parameter           | Min  | Typ | Max   | Unit             |
|---------------------|------|-----|-------|------------------|
| Clock output range  | —    | —   | 1000  | MHz              |
| Reference clock     | —    | 24  | —     | MHz              |
| Lock time           | —    | —   | 11250 | reference cycles |
| Period jitter (p2p) | —    | 50  | —     | ps               |
| Duty cycle          | 47.5 | —   | 52.5  | %                |

#### 4.2.5.4 480 MHz PLL

Table 25. 480 MHz PLL's electrical parameters

| Parameter               | Min | Typ | Max | Unit             |
|-------------------------|-----|-----|-----|------------------|
| Clock output range      | —   | —   | 480 | MHz              |
| Reference clock         | —   | 24  | —   | MHz              |
| Lock time               | —   | —   | 383 | reference cycles |
| Period jitter (p2p)     | —   | 40  | —   | ps               |
| PFD period jitter (p2p) | —   | 125 | —   | ps               |
| Duty cycle              | 45  | —   | 55  | %                |

#### 4.2.5.5 Arm PLL

Table 26. Arm PLL's electrical parameters

| Parameter           | Min | Typ | Max  | Unit             |
|---------------------|-----|-----|------|------------------|
| Clock output range  | 648 | —   | 1296 | MHz              |
| Reference clock     | —   | 24  | —    | MHz              |
| Lock time           | —   | —   | 2250 | reference cycles |
| Period jitter (p2p) | —   | 15  | —    | ps               |
| Duty cycle          | 45  | —   | 55   | %                |

#### 4.2.6 On-chip oscillators

The system oscillator (SYS OSC) is a crystal oscillator. The SYS OSC, in conjunction with an external crystal or resonator, generates a reference clock for this chip. It also provides the option for an external input clock to XTALI signal directly.

Table 27. System oscillator frequency specifications

| Symbol                      | Parameter                                    | Conditions                                            | Min     | Typ | Max | Unit |
|-----------------------------|----------------------------------------------|-------------------------------------------------------|---------|-----|-----|------|
| $I_{VDDA}$ (Low power mode) | Analog supply current                        | 24 MHz                                                | —       | 0.5 | —   | mA   |
| $I_{VDDA}$ (High gain mode) | Analog supply current                        | 24 MHz                                                | —       | 1.3 | —   | mA   |
| $R_F$                       | Feedback resistor                            | Low-power mode                                        | No need |     |     |      |
|                             |                                              | High-gain mode                                        | —       | 1   | —   | MΩ   |
| $R_S$                       | Series resistor <sup>1</sup>                 | —                                                     | —       | 0   | —   | kΩ   |
| $C_X C_Y$                   | XTALI/XTALO load capacitance                 | See crystal or resonator manufacture's recommendation |         |     |     |      |
| $C_{para}$                  | Parasitically capacitance of XTALI and XTALO | —                                                     | —       | 1.5 | 2.0 | pF   |

Table 27. System oscillator frequency specifications (continued)

| Symbol             | Parameter                                 | Conditions            | Min                  | Typ                  | Max | Unit    |
|--------------------|-------------------------------------------|-----------------------|----------------------|----------------------|-----|---------|
| Clock output       |                                           |                       |                      |                      |     |         |
| $F_{OSC}$          | Oscillator crystal or resonator frequency | —                     | —                    | 24                   | —   | MHz     |
| $t_{dcy}$          | Duty-cycle of the output clock            | —                     | 40                   | 50                   | 60  | %       |
| Dynamic parameters |                                           |                       |                      |                      |     |         |
| $V_{PP}$           | Peak-peak amplitude of oscillation        | Low-power mode        | —                    | 0.8                  | —   | V       |
|                    |                                           | High gain mode        | 0.75x<br>VDDA_1P8_IN | 0.8 x<br>VDDA_1P8_IN | —   | V       |
| $t_{start}$        | Start-up time                             | 24 MHz low-power mode | —                    | 250                  | —   | $\mu$ s |
|                    |                                           | 24 MHz high-gain mode | —                    | 250                  | —   | $\mu$ s |

<sup>1</sup> Depends on the drive level of external crystal device

Each i.MX RT1160 processor has two external input system clocks: a low frequency (RTC\_XTALI) and a high frequency (XTALI).

The RTC\_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can be used instead of the RTC\_XTALI if accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 28. 32 kHz oscillator DC electrical specifications

| Symbol            | Description                                          | Min | Typ    | Max          | Unit | Note           |
|-------------------|------------------------------------------------------|-----|--------|--------------|------|----------------|
| $C_{para}$        | Parasitically capacitance of RTC_XTALI and RTC_XTALO | —   | 1.5    | 2.0          | pF   | —              |
| $V_{pp}$          | Peak-to-peak amplitude of oscillator                 | —   | 0.6    | —            | V    | <sup>1</sup>   |
| $f_{osc\_lo}$     | Oscillator crystal                                   | —   | 32.768 | —            | kHz  | —              |
| $t_{start}$       | Crystal startup time                                 | —   | 500    | —            | ms   | <sup>1</sup>   |
| $V_{ec\_extal32}$ | Externally provided input clock amplitude            | 0.7 | —      | VDD_SNVS_ANA | V    | <sup>2,3</sup> |

<sup>1</sup> Proper PCB layout procedures must be followed to achieve specifications.

<sup>2</sup> This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.

<sup>3</sup> The parameter specified is a peak-to-peak value and  $V_{IH}$  and  $V_{IL}$  specifications do not apply. The voltage of the applied clock must be within the range of  $V_{SS}$  to VDD\_SNVS\_ANA.

The RTC OSC module provides the clock source for the Real-Time Clock module. The RTC OSC module, in conjunction with an external crystal, generates a 32.768 kHz reference clock for the RTC.

**Table 29. RC oscillator with 16 MHz internal reference frequency**

| Symbol                  | Parameter                    | Condition | Min  | Typ | Max  | Unit |
|-------------------------|------------------------------|-----------|------|-----|------|------|
| Clock output            |                              |           |      |     |      |      |
| F <sub>clkout_16M</sub> | Clock frequency              | —         | 15.1 | 16  | 16.9 | MHz  |
| Dynamic parameters      |                              |           |      |     |      |      |
| T <sub>start_16M</sub>  | Start-up time                | —         | —    | 50  | —    | μs   |
| Power-down mode         |                              |           |      |     |      |      |
| I <sub>VDDA</sub>       | Supply current in power-down | —         | 1    | 2   | 95   | nA   |

**Table 30. RC oscillator with 48 MHz internal reference frequency**

| Symbol              | Parameter             | Condition | Min | Typ | Max | Unit |
|---------------------|-----------------------|-----------|-----|-----|-----|------|
| General             |                       |           |     |     |     |      |
| I <sub>VDDA</sub>   | Analog supply current | —         | —   | 350 | 500 | μA   |
| Clock output        |                       |           |     |     |     |      |
| F <sub>clkout</sub> | Clock frequency       | —         | —   | 48  | —   | MHz  |
| Dynamic parameters  |                       |           |     |     |     |      |
| T <sub>start</sub>  | Start-up time         | —         | —   | 2.5 | —   | μs   |
| Accuracy            |                       |           |     |     |     |      |
| T <sub>target</sub> | Trimmed               | —         | -2  | —   | 2   | %    |

**Table 31. RC oscillator with 400 MHz internal reference frequency**

| Symbol                   | Parameter                    | Condition | Min | Typ | Max | Unit |
|--------------------------|------------------------------|-----------|-----|-----|-----|------|
| General                  |                              |           |     |     |     |      |
| I <sub>VDD_1P8V_ON</sub> | Analog supply current        | —         | —   | 60  | —   | μA   |
| I <sub>VDD_ON</sub>      | Digital supply current       | —         | —   | 80  | —   | μA   |
| Clock output             |                              |           |     |     |     |      |
| F <sub>tuned</sub>       | Tuned clock frequency        | —         | —   | 400 | —   | MHz  |
| ΔF/F                     | Frequency error after tuning | —         | —   | 0.1 | —   | %    |
| Dynamic parameters       |                              |           |     |     |     |      |
| J <sub>PP-CC</sub>       | Peak-peak, period jitter     | —         | —   | 50  | —   | ns   |
| t <sub>start</sub>       | Start-up time                | —         | —   | 1   | —   | μs   |
| t <sub>tune</sub>        | Tuning time                  | —         | 1   | —   | 256 | μs   |

Table 32. RC oscillator with 32 kHz internal reference frequency

| Symbol              | Description                   | Min  | Typ | Max | Unit           | Note |
|---------------------|-------------------------------|------|-----|-----|----------------|------|
| $f_{irc32k}$        | Internal reference frequency  | —    | 32  | —   | kHz            | —    |
| $\Delta f_{irc32k}$ | Deviation of IRC32K frequency | -25% | —   | 25% | % $f_{irc32k}$ | —    |

## 4.3 I/O parameters

This section provides parameters on I/O interfaces.

### 4.3.1 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- XTALI and RTC\_XTALI (Clock Inputs) DC Parameters
- General Purpose I/O (GPIO)

#### NOTE

The term 'NVCC\_XXXX' in this section refers to the associated supply rail of an input or output.

#### NOTE

When enable the open drain for I/O pad, the external pull-up voltage cannot exceed the associated supply rail.

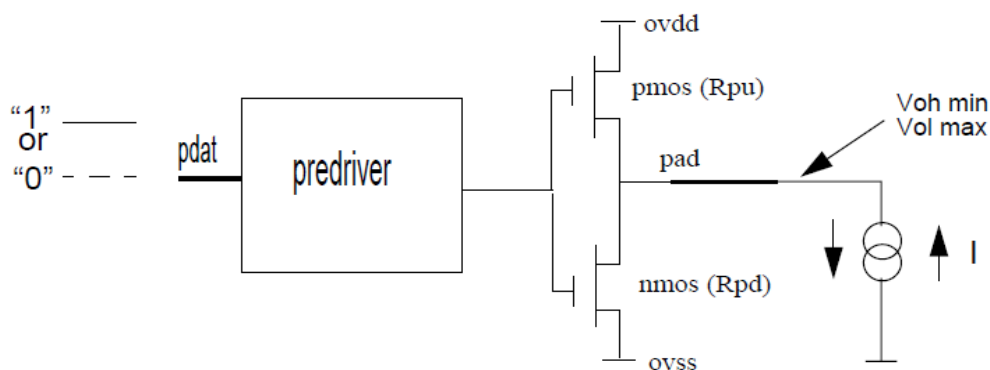


Figure 5. Circuit for parameters Voh and Vol for I/O cells

### 4.3.1.1 XTALI and RTC\_XTALI (clock inputs) DC parameters

Table 33 shows the DC parameters for the clock inputs.

**Table 33. XTALI and RTC\_XTALI DC parameters<sup>1</sup>**

| Parameter                             | Symbol          | Test Conditions | Min                | Max          | Unit |
|---------------------------------------|-----------------|-----------------|--------------------|--------------|------|
| XTALI high-level DC input voltage     | V <sub>Ih</sub> | —               | VDDA_1P8_IN - 0.5  | VDDA_1P8_IN  | V    |
| XTALI low-level DC input voltage      | V <sub>Il</sub> | —               | 0                  | 0.5          | V    |
| RTC_XTALI high-level DC input voltage | V <sub>Ih</sub> | —               | VDD_SNVS_ANA - 0.5 | VDD_SNVS_ANA | V    |
| RTC_XTALI low-level DC input voltage  | V <sub>Il</sub> | —               | 0                  | 0.5          | V    |

<sup>1</sup> The DC parameters are for external clock input only.

### 4.3.1.2 General purpose I/O (GPIO) DC parameters

Following section introduces the GPIO DC parameters, respectively, for GPIO pads. These parameters are guaranteed per the operating ranges in Table 11 unless otherwise noted.

**Table 34. DC specification for GPIO\_EMC\_B1/GPIO\_EMC\_B2/GPIO\_SD\_B1/GPIO\_SD\_B2/GPIO\_DISP\_B1 bank**

| Parameter                                               | Symbol            | Value        |     |             | Unit | Condition                           |
|---------------------------------------------------------|-------------------|--------------|-----|-------------|------|-------------------------------------|
|                                                         |                   | Min          | Typ | Max         |      |                                     |
| Receiver 3.3 V                                          |                   |              |     |             |      |                                     |
| High level input voltage                                | V <sub>IH</sub>   | 0.625 x NVCC | —   | NVCC + 0.3  | V    | —                                   |
| Low level input voltage                                 | V <sub>IL</sub>   | -0.3         | —   | 0.25 x NVCC | V    | —                                   |
| Receiver 1.8 V                                          |                   |              |     |             |      |                                     |
| High level input voltage                                | V <sub>IH</sub>   | 0.65 x NVCC  | —   | NVCC + 0.3  | V    | —                                   |
| Low level input voltage                                 | V <sub>IL</sub>   | -0.3         | —   | 0.35 x NVCC | V    | —                                   |
| Driver 3.3 V and driver 1.8 V for PDRV = L and PDRV = H |                   |              |     |             |      |                                     |
| Output high current                                     | I <sub>OH</sub>   | -6           | —   | —           | mA   | V <sub>OH</sub> = 0.8 x NVCC        |
| Output low current                                      | I <sub>OL</sub>   | 6            | —   | —           | mA   | V <sub>OL</sub> = 0.2 x NVCC        |
| Output low/high current total for each IO bank          | I <sub>OCT</sub>  | —            | —   | 100         | mA   | —                                   |
| Weak pull-up and pull-down                              |                   |              |     |             |      |                                     |
| Pull-up / pull-down resistance                          | R <sub>High</sub> | 10           | —   | 100         | kΩ   | High voltage range (2.7 V - 3.6 V)  |
| Pull-up / pull-down resistance                          | R <sub>Low</sub>  | 20           | —   | 50          | kΩ   | Low voltage range (1.65 V - 1.95 V) |

Table 35. DC specification for GPIO\_SNVS bank

| Parameter                                      | Symbol     | Min                     | Typ  | Max                     | Unit     | Condition                   |
|------------------------------------------------|------------|-------------------------|------|-------------------------|----------|-----------------------------|
| High level input voltage                       | $V_{IH}$   | $0.7 \times NVCC\_SNVS$ | —    | $NVCC\_SNVS + 0.1$      | V        | —                           |
| Low level input voltage                        | $V_{IL}$   | -0.3                    | —    | $0.3 \times NVCC\_SNVS$ | V        | —                           |
| Output high current                            | $I_{OH}$   | 170                     | —    | —                       | $\mu A$  | $V_{OH} = NVCC\_SNVS - 0.3$ |
| Output low current                             | $I_{OL}$   | 270                     | —    | —                       | $\mu A$  | $V_{OL} = 0.3$              |
| Output low/high current total for each IO bank | $I_{OCT}$  | —                       | —    | 100                     | mA       | —                           |
| Weak pull-up and pull-down                     |            |                         |      |                         |          |                             |
| Pull-up resistance                             | $R_{High}$ | —                       | 1000 | 3500                    | $\Omega$ | —                           |
| Pull-down resistance                           | $R_{Low}$  | —                       | 850  | 3500                    | $\Omega$ | —                           |

Table 36. DC specification for GPIO\_AD/GPIO\_LPSR/GPIO\_DISP\_B2 bank

| NO. | Characteristics                             | Test Conditions                                    | Min                | Max                | Units |
|-----|---------------------------------------------|----------------------------------------------------|--------------------|--------------------|-------|
| 1   | Input high voltage ( $V_{IH}$ )             | Normal voltage range                               | $0.7 \times NVCC$  | $NVCC + 0.1$       | V     |
|     |                                             | Derated voltage range                              | $0.75 \times NVCC$ | $NVCC + 0.1$       | V     |
|     |                                             | Derated2 voltage range                             | $0.75 \times NVCC$ | $NVCC + 0.1$       | V     |
|     |                                             | Low voltage range                                  | $0.7 \times NVCC$  | $NVCC + 0.1$       | V     |
|     |                                             | High voltage range                                 | $0.7 \times NVCC$  | $NVCC + 0.1$       | V     |
| 2   | Input low voltage ( $V_{IL}$ )              | Normal voltage range                               | - 0.3              | $0.3 \times NVCC$  | V     |
|     |                                             | Derated voltage range                              | - 0.3              | $0.25 \times NVCC$ | V     |
|     |                                             | Derated2 voltage range                             | - 0.3              | $0.25 \times NVCC$ | V     |
|     |                                             | Low voltage range                                  | - 0.3              | $0.3 \times NVCC$  | V     |
|     |                                             | High voltage range                                 | - 0.3              | $0.3 \times NVCC$  | V     |
| 3   | Input Hysteresis ( $V_{HYSN}$ )             | All voltage range                                  | $0.06 \times NVCC$ | —                  | V     |
| 4   | Output high voltage ( $V_{OH}$ )<br>DSE = 1 | Normal voltage range<br>$I_{OH} = -10 \text{ mA}$  | $NVCC - 0.5$       | —                  | V     |
|     |                                             | Derated voltage range<br>$I_{OH} = -6 \text{ mA}$  | $NVCC - 0.5$       | —                  | V     |
|     |                                             | Derated2 voltage range<br>$I_{OH} = -5 \text{ mA}$ | $NVCC - 0.5$       | —                  | V     |
|     |                                             | Low voltage range<br>$I_{OH} = -10 \text{ mA}$     | $NVCC - 0.5$       | —                  | V     |
|     |                                             | High voltage range<br>$I_{OH} = -10 \text{ mA}$    | $NVCC - 0.5$       | —                  | V     |

Table 36. DC specification for GPIO\_AD/GPIO\_LPSR/GPIO\_DISP\_B2 bank (continued)

| NO. | Characteristics                                             | Test Conditions                              | Min        | Max  | Units      |
|-----|-------------------------------------------------------------|----------------------------------------------|------------|------|------------|
| 5   | Output high voltage ( $V_{OH}$ )<br>DSE = 0                 | Normal voltage range<br>$I_{OH} = -5$ mA     | NVCC - 0.5 | —    | V          |
|     |                                                             | Derated voltage range<br>$I_{OH} = -3$ mA    | NVCC - 0.5 | —    | V          |
|     |                                                             | Derated2 voltage range<br>$I_{OH} = -2.5$ mA | NVCC - 0.5 | —    | V          |
|     |                                                             | Low voltage range<br>$I_{OH} = -5$ mA        | NVCC - 0.5 | —    | V          |
|     |                                                             | High voltage range<br>$I_{OH} = -5$ mA       | NVCC - 0.5 | —    | V          |
| 6   | Output low voltage ( $V_{OL}$ )<br>DSE = 1                  | Normal voltage range<br>$I_{OL} = 10$ mA     | —          | 0.5  | V          |
|     |                                                             | Derated voltage range<br>$I_{OL} = 6$ mA     | —          | 0.5  | V          |
|     |                                                             | Derated2 voltage range<br>$I_{OL} = 5$ mA    | —          | 0.5  | V          |
|     |                                                             | Low voltage range<br>$I_{OL} = 10$ mA        | —          | 0.5  | V          |
|     |                                                             | High voltage range<br>$I_{OL} = 10$ mA       | —          | 0.5  | V          |
| 7   | Output low voltage ( $V_{OL}$ )<br>DSE = 0                  | Normal voltage range<br>$I_{OL} = 5$ mA      | —          | 0.5  | V          |
|     |                                                             | Derated voltage range<br>$I_{OL} = 3$ mA     | —          | 0.5  | V          |
|     |                                                             | Derated2 voltage range<br>$I_{OL} = 2.5$ mA  | —          | 0.5  | V          |
|     |                                                             | Low voltage range<br>$I_{OL} = 5$ mA         | —          | 0.5  | V          |
|     |                                                             | High voltage range<br>$I_{OL} = 5$ mA        | —          | 0.5  | V          |
| 8   | NVCC                                                        | Normal voltage range                         | 2.7        | 3.6  | V          |
|     |                                                             | Derated voltage range                        | 1.98       | 2.7  | V          |
|     |                                                             | Derated2 voltage range                       | 1.71       | 1.98 | V          |
|     |                                                             | Low voltage range                            | 1.71       | 1.98 | V          |
|     |                                                             | High voltage range                           | 3          | 3.6  | V          |
| 11  | Pull-up resistor range ( $R_{PU}$ )<br>Measure @ $V_{DD}$   | All voltage range                            | 25         | 50   | k $\Omega$ |
| 12  | Pull-down resistor range ( $R_{PD}$ )<br>Measure @ $V_{SS}$ | All voltage range                            | 25         | 50   | k $\Omega$ |

Table 36. DC specification for GPIO\_AD/GPIO\_LPSR/GPIO\_DISP\_B2 bank (continued)

| NO. | Characteristics                                                    | Test Conditions   | Min | Max | Units |
|-----|--------------------------------------------------------------------|-------------------|-----|-----|-------|
| 13  | Input leakage current                                              | All voltage range | —   | 400 | nA    |
| 14  | Output capacitance (CL)                                            | All voltage range | —   | 15  | pF    |
| 15  | Input capacitance (Cin)                                            | All voltage range | —   | 5   | pF    |
| 16  | Output low/high current total for each IO bank (I <sub>OCT</sub> ) | All voltage range | —   | 100 | mA    |

### 4.3.2 I/O AC parameters

The GPIO and DDR I/O load circuit and output transition time waveform are shown in Figure 6 and Figure 7.

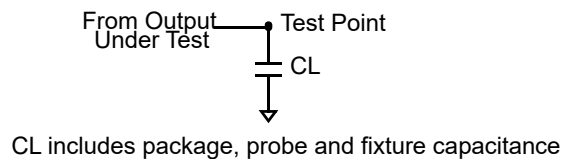


Figure 6. Load circuit for output

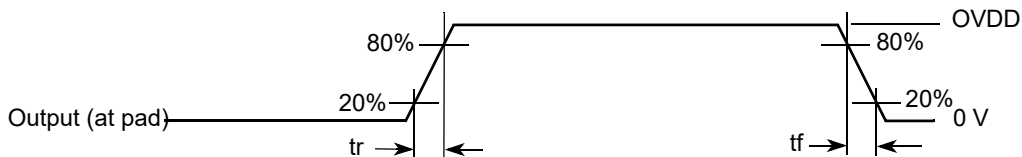


Figure 7. Output transition time waveform

#### 4.3.2.1 General purpose I/O (GPIO) AC parameters

The I/O AC parameters for GPIO are presented in the Table 37 and Table 38, respectively.

Table 37. AC specification for GPIO\_EMC\_B1/GPIO\_EMC\_B2/GPIO\_SD\_B1/GPIO\_SD\_B2/GPIO\_DISP\_B1 bank

| Symbol                          | Parameter         | Test Condition                                       | Min | Typ | Max  | Unit |
|---------------------------------|-------------------|------------------------------------------------------|-----|-----|------|------|
| <b>Driver 1.8 V application</b> |                   |                                                      |     |     |      |      |
| f <sub>max</sub>                | Maximum frequency | Load = 21 pF (PDRV = L, high drive, 33 Ω)            | —   | —   | 208  | MHz  |
|                                 |                   | Load = 15 pF (PDRV = H, low drive, 50 Ω)             |     |     |      |      |
| tr                              | Rise time         | Measured between V <sub>OL</sub> and V <sub>OH</sub> | 0.4 | —   | 1.32 | ns   |
| tf                              | Fall time         | Measured between V <sub>OH</sub> and V <sub>OL</sub> | 0.4 | —   | 1.32 | ns   |
| <b>Driver 3.3 V application</b> |                   |                                                      |     |     |      |      |

**Table 37. AC specification for GPIO\_EMC\_B1/GPIO\_EMC\_B2/GPIO\_SD\_B1/GPIO\_SD\_B2/GPIO\_DISP\_B1 bank (continued)**

| Symbol     | Parameter         | Test Condition                         | Min | Typ | Max | Unit |
|------------|-------------------|----------------------------------------|-----|-----|-----|------|
| $f_{\max}$ | Maximum frequency | Load = 20 pF                           | —   | —   | 200 | MHz  |
| $t_r$      | Rise time         | Measured between $V_{OL}$ and $V_{OH}$ | —   | —   | 3   | ns   |
| $t_f$      | Fall time         | Measured between $V_{OH}$ and $V_{OL}$ | —   | —   | 3   | ns   |

**Table 38. Dynamic input characteristics for GPIO\_EMC\_B1/GPIO\_EMC\_B2/GPIO\_SD\_B1/GPIO\_SD\_B2/GPIO\_DISP\_B1 bank**

| Symbol                                                     | Parameter                    | Test Condition <sup>1, 2</sup>               | Min | Max | Unit |
|------------------------------------------------------------|------------------------------|----------------------------------------------|-----|-----|------|
| <b>Dynamic Input Characteristics for 3.3 V Application</b> |                              |                                              |     |     |      |
| $f_{op}$                                                   | Input frequency of operation | —                                            | —   | 200 | MHz  |
| INPSL                                                      | Slope of input signal at I/O | Measured between 10% to 90% of the I/O swing | —   | 3.5 | ns   |
| <b>Dynamic Input Characteristics for 1.8 V Application</b> |                              |                                              |     |     |      |
| $f_{op}$                                                   | Input frequency of operation | —                                            | —   | 208 | MHz  |
| INPSL                                                      | Slope of input signal at I/O | Measured between 10% to 90% of the I/O swing | —   | 1.5 | ns   |

<sup>1</sup> For all supply ranges of operation.<sup>2</sup> The dynamic input characteristic specifications are applicable for the digital bidirectional cells.**Table 39. AC specifications for GPIO\_AD/GPIO\_LPSR/GPIO\_DISP\_B2 bank**

| NO. | Characteristic                        | Condition                                 |   | Max | Unit |
|-----|---------------------------------------|-------------------------------------------|---|-----|------|
| 1   | Pad rise/fall time (DSE = 0, SRE = 0) | Normal voltage range<br>(Cload = 15 pF)   | — | 3   | ns   |
|     |                                       | Derated voltage range<br>(Cload = 15 pF)  | — | 5   | ns   |
|     |                                       | Derated2 voltage range<br>(Cload = 15 pF) | — | 6   | ns   |
|     |                                       | Low voltage range<br>(Cload = 15 pF)      | — | 3   | ns   |
|     |                                       | High voltage range<br>(Cload = 15 pF)     | — | 3   | ns   |

Table 39. AC specifications for GPIO\_AD/GPIO\_LPSR/GPIO\_DISP\_B2 bank (continued)

| NO. | Characteristic                                         | Condition                                 |   | Max | Unit |
|-----|--------------------------------------------------------|-------------------------------------------|---|-----|------|
| 2   | Pad rise/fall time (DSE = 0, SRE = 1)                  | Normal voltage range<br>(Cload = 15 pF)   | — | 6   | ns   |
|     |                                                        | Derated voltage range<br>(Cload = 15 pF)  | — | 10  | ns   |
|     |                                                        | Derated2 voltage range<br>(Cload = 15 pF) | — | 12  | ns   |
|     |                                                        | Low voltage range<br>(Cload = 15 pF)      | — | 6   | ns   |
|     |                                                        | High voltage range<br>(Cload = 15 pF)     | — | 6   | ns   |
| 3   | Pad rise/fall time (DSE = 1, SRE = 0)                  | Normal voltage range<br>(Cload = 15 pF)   | — | 2.5 | ns   |
|     |                                                        | Derated voltage range<br>(Cload = 15 pF)  | — | 4.5 | ns   |
|     |                                                        | Derated2 voltage range<br>(Cload = 15 pF) | — | 5   | ns   |
|     |                                                        | Low voltage range<br>(Cload = 15 pF)      | — | 2.5 | ns   |
|     |                                                        | High voltage range<br>(Cload = 15 pF)     | — | 2.5 | ns   |
| 4   | Pad rise/fall time (DSE = 1, SRE = 1)                  | Normal voltage range<br>(Cload = 15 pF)   | — | 5   | ns   |
|     |                                                        | Derated voltage range<br>(Cload = 15 pF)  | — | 9   | ns   |
|     |                                                        | Derated2 voltage range<br>(Cload = 15 pF) | — | 10  | ns   |
|     |                                                        | Low voltage range<br>(Cload = 15 pF)      | — | 5   | ns   |
|     |                                                        | High voltage range<br>(Cload = 15 pF)     | — | 5   | ns   |
| 5   | IPP_DO to pad propagation delay:<br>(DSE = 0, SRE = 0) | Normal voltage range<br>(Cload = 15 pF)   | — | 2.5 | ns   |
|     |                                                        | Derated voltage range<br>(Cload = 15 pF)  | — | 4.5 | ns   |
|     |                                                        | Derated2 voltage range<br>(Cload = 15 pF) | — | 5   | ns   |
|     |                                                        | Low voltage range<br>(Cload = 15 pF)      | — | 2.5 | ns   |
|     |                                                        | High voltage range<br>(Cload = 15 pF)     | — | 4   | ns   |

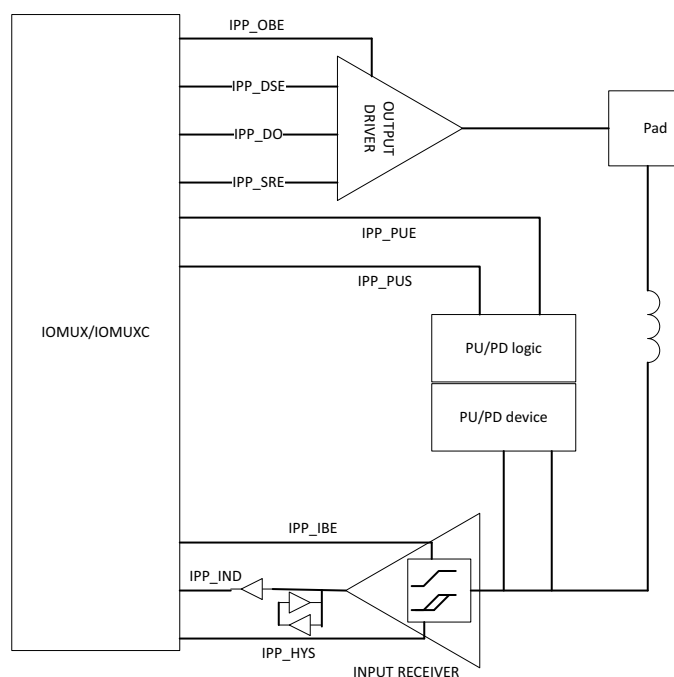
Table 39. AC specifications for GPIO\_AD/GPIO\_LPSR/GPIO\_DISP\_B2 bank (continued)

| NO. | Characteristic                                         | Condition                                         |   | Max | Unit |
|-----|--------------------------------------------------------|---------------------------------------------------|---|-----|------|
| 6   | IPP_DO to pad propagation delay:<br>(DSE = 0, SRE = 1) | Normal voltage range<br>(Cload = 15 pF)           | — | 7   | ns   |
|     |                                                        | Derated voltage range<br>(Cload = 15 pF)          | — | 12  | ns   |
|     |                                                        | Derated2 voltage range<br>(Cload = 15 pF)         | — | 14  | ns   |
|     |                                                        | Low voltage range<br>(Cload = 15 pF)              | — | 7   | ns   |
|     |                                                        | High voltage range<br>(Cload = 15 pF)             | — | 8.5 | ns   |
| 7   | IPP_DO to pad propagation delay:<br>(DSE = 1, SRE = 0) | Normal voltage range<br>(Cload = 15 pF)           | — | 2   | ns   |
|     |                                                        | Derated voltage range<br>(Cload = 15 pF)          | — | 3.6 | ns   |
|     |                                                        | Derated2 voltage range<br>(Cload = 15 pF)         | — | 4   | ns   |
|     |                                                        | Low voltage range<br>(Cload = 15 pF)              | — | 2   | ns   |
|     |                                                        | High voltage range<br>(Cload = 15 pF)             | — | 4   | ns   |
| 8   | IPP_DO to pad propagation delay:<br>(DSE = 1, SRE = 1) | Normal voltage range<br>(Cload = 15 pF)           | — | 6   | ns   |
|     |                                                        | Derated voltage range<br>(Cload = 15 pF)          | — | 11  | ns   |
|     |                                                        | Derated2 voltage range<br>(Cload = 15 pF)         | — | 12  | ns   |
|     |                                                        | Low voltage range<br>(Cload = 15 pF)              | — | 6   | ns   |
|     |                                                        | High voltage range<br>(Cload = 15 pF)             | — | 7.5 | ns   |
| 9   | Pad to IPP_IND propagation delay                       | Normal voltage range<br>(100 F load on IPP_IND)   | — | 2   | ns   |
|     |                                                        | Derated voltage range<br>(100 F load on IPP_IND)  | — | 3.5 | ns   |
|     |                                                        | Derated2 voltage range<br>(100 F load on IPP_IND) | — | 4   | ns   |
|     |                                                        | Low voltage range<br>(100 F load on IPP_IND)      | — | 4   | ns   |
|     |                                                        | High voltage range<br>(100 F load on IPP_IND)     | — | 2   | ns   |

**Table 39. AC specifications for GPIO\_AD/GPIO\_LPSR/GPIO\_DISP\_B2 bank (continued)**

| NO. | Characteristic         | Condition                                         |   | Max | Unit |
|-----|------------------------|---------------------------------------------------|---|-----|------|
| 10  | IPP_IND rise/fall time | Normal voltage range<br>(100 F load on IPP_IND)   | — | 0.3 | ns   |
|     |                        | Derated voltage range<br>(100 F load on IPP_IND)  | — | 0.4 | ns   |
|     |                        | Derated2 voltage range<br>(100 F load on IPP_IND) | — | 0.5 | ns   |
|     |                        | Low voltage range<br>(100 F load on IPP_IND)      | — | 0.3 | ns   |
|     |                        | High voltage range<br>(100 F load on IPP_IND)     | — | 0.3 | ns   |

Figure 8 is the GPIO block diagram.



**Figure 8. GPIO block diagram**

## 4.4 System modules

This section contains the timing and electrical parameters for the modules in the i.MX RT1160 processor.

### 4.4.1 Reset timing parameters

Figure 9 shows the POR reset timing and Table 40 lists the timing parameters.

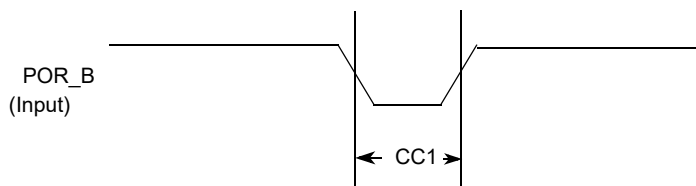


Figure 9. POR reset timing diagram

Table 40. POR reset timing parameters

| ID  | Parameter                                   | Min | Max | Unit            |
|-----|---------------------------------------------|-----|-----|-----------------|
| CC1 | Duration of POR_B to be qualified as valid. | 1   | —   | RTC_XTALI cycle |

### 4.4.2 WDOG reset timing parameters

Figure 10 shows the WDOG reset timing and Table 41 lists the timing parameters.

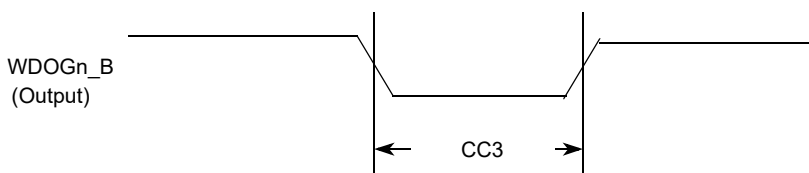


Figure 10. WDOGn\_B timing diagram

Table 41. WDOGn\_B timing parameters

| ID  | Parameter                     | Min | Max | Unit            |
|-----|-------------------------------|-----|-----|-----------------|
| CC3 | Duration of WDOGn_B Assertion | 1   | —   | RTC_XTALI cycle |

#### NOTE

RTC\_XTALI is approximately 32 kHz. RTC\_XTALI cycle is one period or approximately 30  $\mu$ s.

#### NOTE

WDOGn\_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

### 4.4.3 JTAG Controller timing parameters

Figure 11 depicts the JTAG controller timing. Figure 12 depicts the JTAG TRST\_B timing.

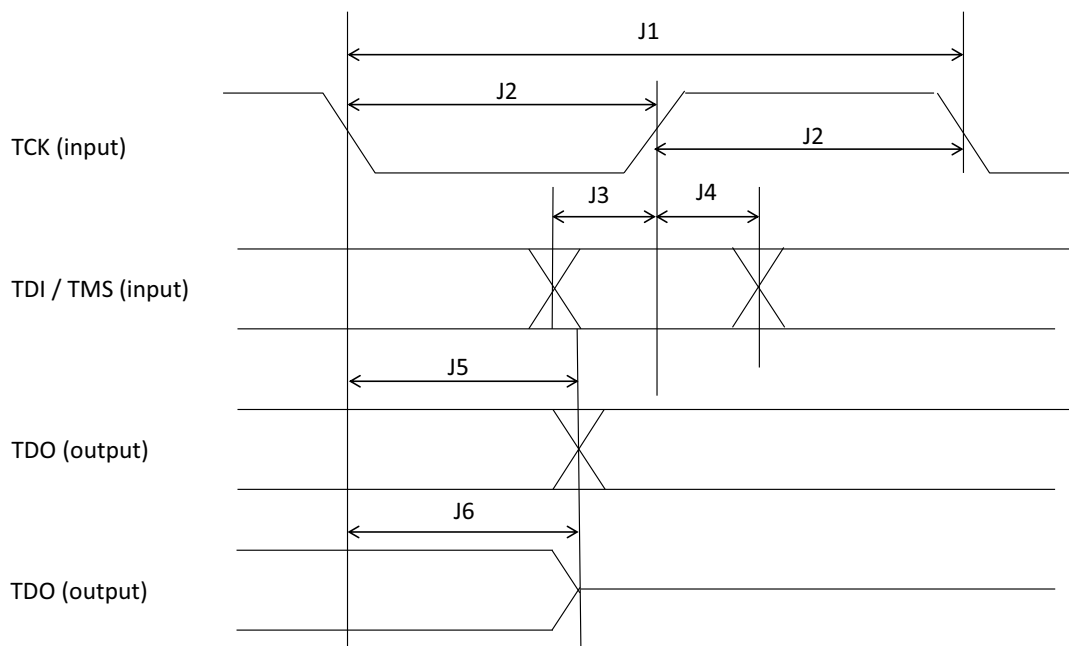


Figure 11. JTAG controller timing

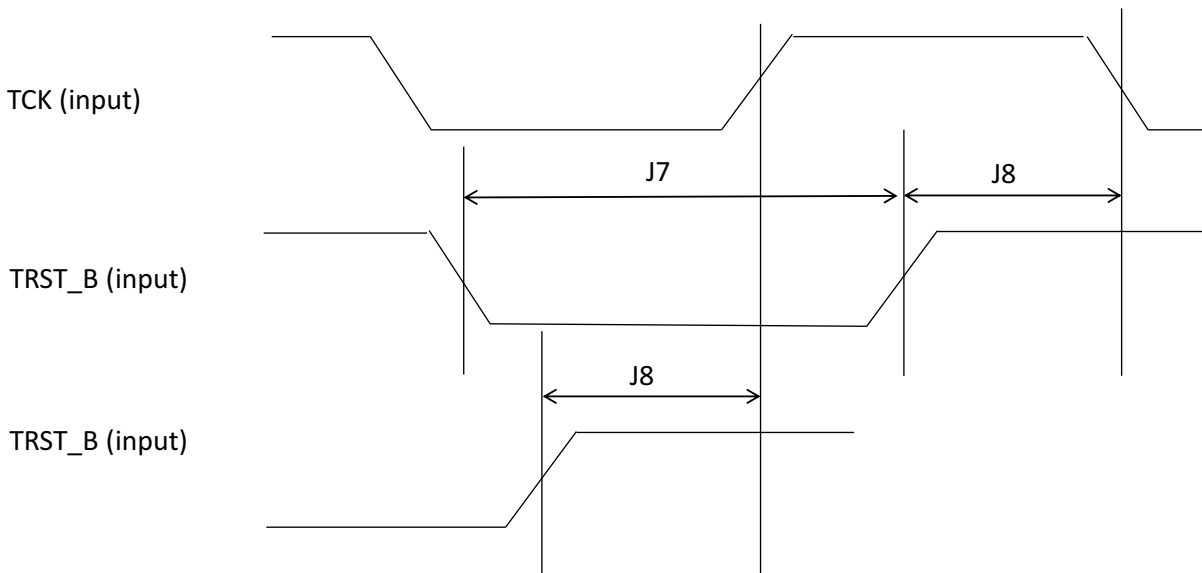


Figure 12. JTAG\_TRST\_B timing

Table 42. JTAG timing parameters

| ID | Parameter                     | Value |      | Unit |
|----|-------------------------------|-------|------|------|
|    |                               | Min   | Max  |      |
| J0 | TCK frequency                 | —     | 25   | MHz  |
| J1 | TCK cycle time                | 40    | —    | ns   |
| J2 | TCK pulse width               | 20    | —    | ns   |
| J3 | Input data setup time         | 5     | —    | ns   |
| J4 | Input data hold time          | 5     | —    | ns   |
| J5 | Output data valid time        | —     | 15.2 | ns   |
| J6 | Output high impedance time    | —     | 15.2 | ns   |
| J7 | TRST_B assert time            | 100   | —    | ns   |
| J8 | TRST_B setup time to TCK edge | 18    | —    | ns   |

#### 4.4.4 SWD timing parameters

Figure 13 depicts the SWD timing.

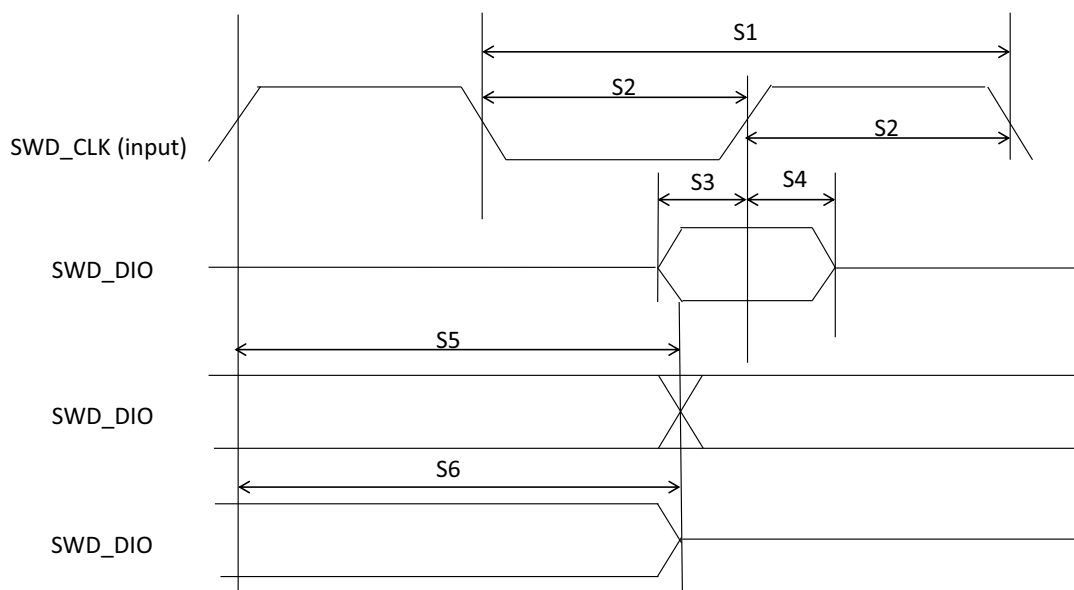


Figure 13. SWD timing

Table 43. SWD timing parameters

| Symbol | Description                | Min | Max  | Unit |
|--------|----------------------------|-----|------|------|
| S0     | SWD_CLK frequency          | —   | 50   | MHz  |
| S1     | SWD_CLK cycle time         | 20  | —    | ns   |
| S2     | SWD_CLK pulse width        | 10  | —    | ns   |
| S3     | Input data setup time      | 5   | —    | ns   |
| S4     | Input data hold time       | 1   | —    | ns   |
| S5     | Output data valid time     | —   | 14.4 | ns   |
| S6     | Output high impedance time | —   | 14.4 | ns   |

#### 4.4.5 Trace timing parameters

Figure 14 depicts the trace timing.

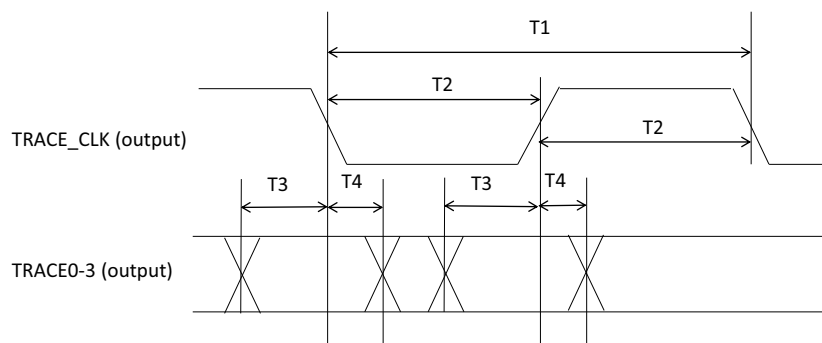


Figure 14. Trace timing

Table 44. Trace timing parameters

| Symbol | Description           | Min  | Max | Unit |
|--------|-----------------------|------|-----|------|
| T0     | TRACE_CLK frequency   | —    | 70  | MHz  |
| T1     | TRACE_CLK cycle time  | 1/T0 | —   | ns   |
| T2     | TRACE_CLK pulse width | 6    | —   | ns   |
| T3     | TRACE data setup time | 2    | —   | ns   |
| T4     | TRACE data hold time  | 0.7  | —   | ns   |

### 4.5 External memory interface

The following sections provide information about external memory interfaces.

## 4.5.1 SEMC specifications

The following sections provide information on SEMC interface.

Measurements are with a load of 15 pf and an input slew rate of 1 V/ns.

### 4.5.1.1 SEMC output timing

There are ASYNC and SYNC modes for SEMC output timing.

#### 4.5.1.1.1 SEMC output timing in ASYNC mode

Table 45 shows SEMC output timing in ASYNC mode.

**Table 45. SEMC output timing in ASYNC mode**

| Symbol     | Parameter                 | Min.             | Max. | Unit | Comment                                                                                                                                          |
|------------|---------------------------|------------------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------|
|            | Frequency of operation    | —                | 200  | MHz  |                                                                                                                                                  |
| $T_{CK}$   | Internal clock period     | 5                | —    | ns   |                                                                                                                                                  |
| $T_{AVO}$  | Address output valid time | —                | 2    | ns   | These timing parameters apply to Address and ADV# for NOR/PSRAM in ASYNC mode.                                                                   |
| $T_{AHO}$  | Address output hold time  | $(T_{CK} - 2)^1$ | —    | ns   |                                                                                                                                                  |
| $T_{ADVL}$ | Active low time           | $(T_{CK} - 1)^2$ |      |      |                                                                                                                                                  |
| $T_{DVO}$  | Data output valid time    | —                | 2    | ns   | These timing parameters apply to Data/CLE/ALE and WE# for NAND, apply to Data/DM/CRE for NOR/PSRAM, apply to Data/DCX and WRX for DBI interface. |
| $T_{DHO}$  | Data output hold time     | $(T_{CK} - 2)^3$ | —    | ns   |                                                                                                                                                  |
| $T_{WEL}$  | WE# low time              | $(T_{CK} - 1)^4$ |      | ns   |                                                                                                                                                  |

<sup>1</sup> Address output hold time is configurable by SEMC\_CR0.AH. AH field setting value is 0x0 in above table. When AH is set with value N,  $T_{AHO}$  min time should be  $((N + 1) \times T_{CK})$ . See the *i.MX RT1160 Reference Manual (IMXRT1160RM)* for more detail about SEMC\_CR0.AH register field.

<sup>2</sup> ADV# low time is configurable by SEMC\_CR0.AS. AS field setting value is 0x0 in above table. When AS is set with value N,  $T_{ADL}$  min time should be  $((N + 1) \times T_{CK} - 1)$ . See the *i.MX RT1160 Reference Manual (IMXRT1160RM)* for more detail about SEMC\_CR0.AS register field.

<sup>3</sup> Data output hold time is configurable by SEMC\_CR0.WEH. WEH field setting value is 0x0 in above table. When WEH is set with value N,  $T_{DHO}$  min time should be  $((N + 1) \times T_{CK})$ . See the *i.MX RT1160 Reference Manual (IMXRT1160RM)* for more detail about SEMC\_CR0.WEH register field.

<sup>4</sup> WE# low time is configurable by SEMC\_CR0.WEL. WEL field setting value is 0x0 in above table. When WEL is set with value N,  $T_{WEL}$  min time should be  $((N + 1) \times T_{CK} - 1)$ . See the *i.MX RT1160 Reference Manual (IMXRT1160RM)* for more detail about SEMC\_CR0.WEL register field.

Figure 15 shows the output timing in ASYNC mode.

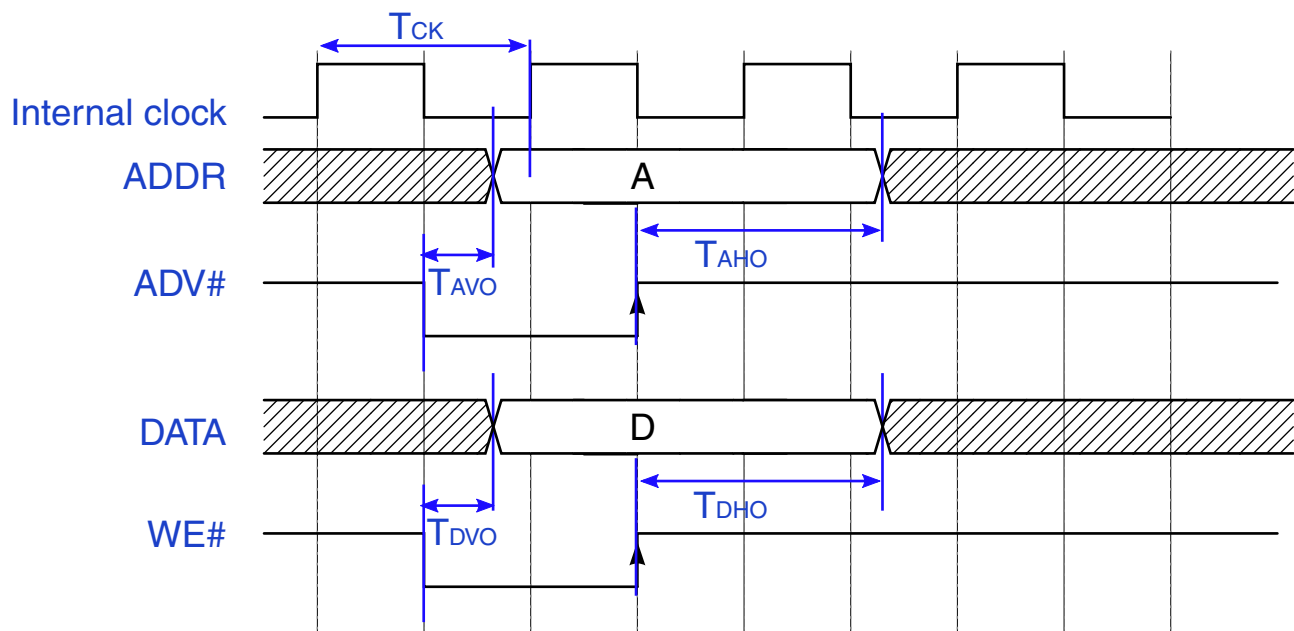


Figure 15. SEMC output timing in ASYNC mode

4.5.1.1.2 SEMC output timing in SYNC mode

Table 46 shows SEMC output timing in SYNC mode.

Table 46. SEMC output timing in SYNC mode

| Symbol    | Parameter              | Min. | Max. | Unit | Comment                                                                                       |
|-----------|------------------------|------|------|------|-----------------------------------------------------------------------------------------------|
|           | Frequency of operation | —    | 200  | MHz  | —                                                                                             |
| $T_{CK}$  | Internal clock period  | 5    | —    | ns   | —                                                                                             |
| $T_{DVO}$ | Data output valid time | —    | 0.6  | ns   | These timing parameters apply to Address/Data/DM/CKE/control signals with SEMC_CLK for SDRAM. |
| $T_{DHO}$ | Data output hold time  | -0.7 | —    | ns   |                                                                                               |

Figure 16 shows the output timing in SYNC mode.

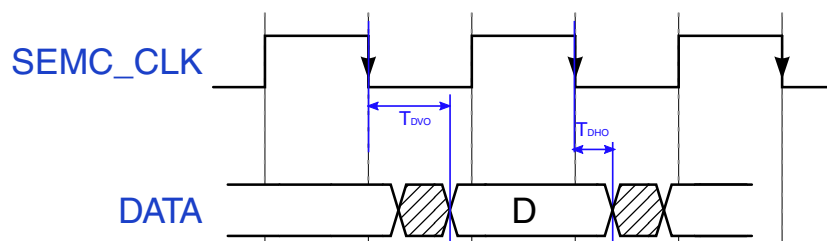


Figure 16. SEMC output timing in SYNC mode

#### 4.5.1.2 SEMC input timing

There are ASYNC and SYNC modes for SEMC input timing.

##### 4.5.1.2.1 SEMC input timing in ASYNC mode

Table 47 shows SEMC input timing in ASYNC mode.

Table 47. SEMC input timing in ASYNC mode

| Symbol   | Parameter        | Min. | Max. | Unit | Comment                                                                     |
|----------|------------------|------|------|------|-----------------------------------------------------------------------------|
| $T_{IS}$ | Data input setup | 7.1  | —    | ns   | For NAND/NOR/PSRAM/DBI, these timing parameters apply to RE# and Read Data. |
| $T_{IH}$ | Data input hold  | 0    | —    | ns   |                                                                             |

Figure 17 shows the input timing in ASYNC mode.

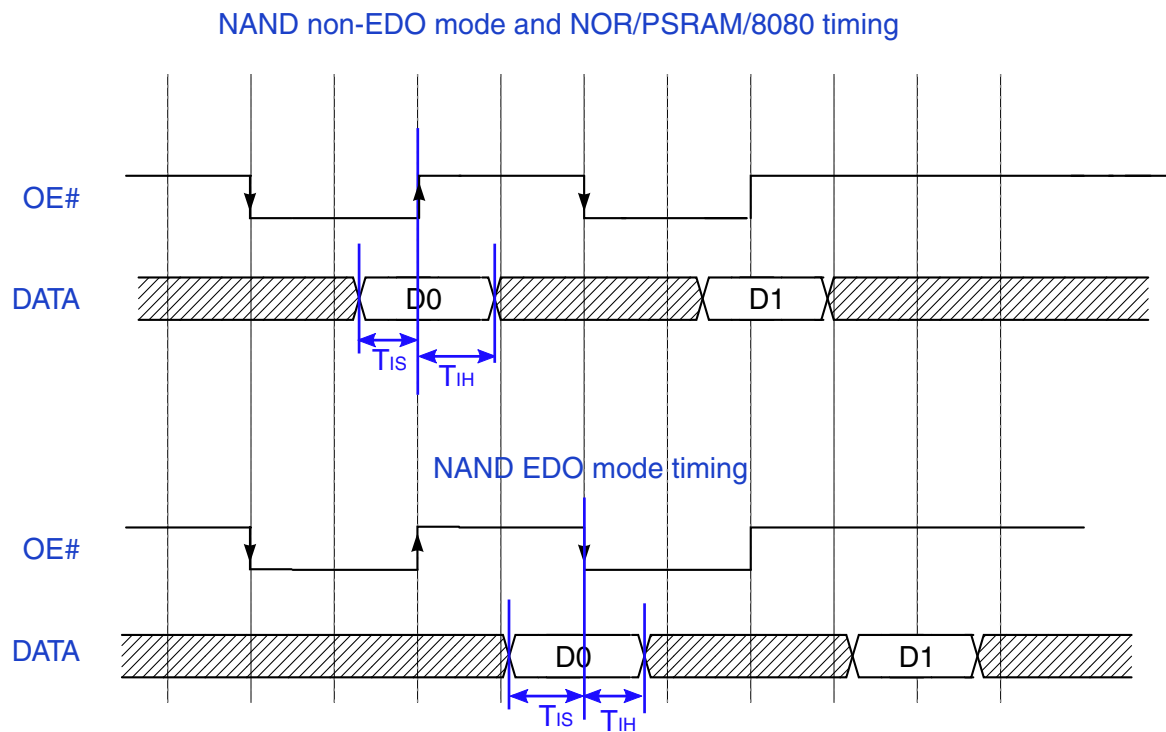


Figure 17. SEMC input timing in ASYNC mode

#### 4.5.1.2.2 SEMC input timing in SYNC mode

Table 48 and Table 49 show SEMC input timing in SYNC mode.

Table 48. SEMC input timing in SYNC mode (SEMC\_MCR.DQSMD = 0x0)

| Symbol   | Parameter        | Min. | Max. | Unit | Comment |
|----------|------------------|------|------|------|---------|
| $T_{IS}$ | Data input setup | 8.67 | —    | ns   | —       |
| $T_{IH}$ | Data input hold  | 0    | —    | ns   |         |

Table 49. SEMC input timing in SYNC mode (SEMC\_MCR.DQSMD = 0x1)

| Symbol   | Parameter        | Min. | Max. | Unit | Comment |
|----------|------------------|------|------|------|---------|
| $T_{IS}$ | Data input setup | 2    | —    | ns   | —       |
| $T_{IH}$ | Data input hold  | 1    | —    | ns   |         |

Figure 18 shows the input timing in SYNC mode.

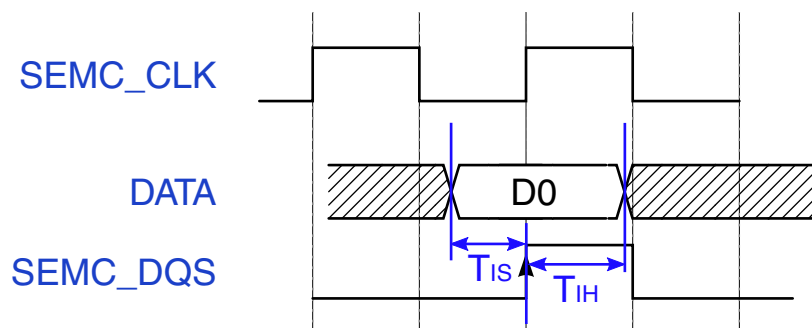


Figure 18. SEMC input timing in SYNC mode

## 4.5.2 FlexSPI parameters

Measurements are with a load 15 pF and input slew rate of 1 V/ns.

### 4.5.2.1 FlexSPI input/read timing

There are three sources for the internal sample clock for FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x1)
- Read strobe provided by memory device and input from DQS pad (FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x3)

The following sections describe input signal timing for each of these three internal sample clock sources.

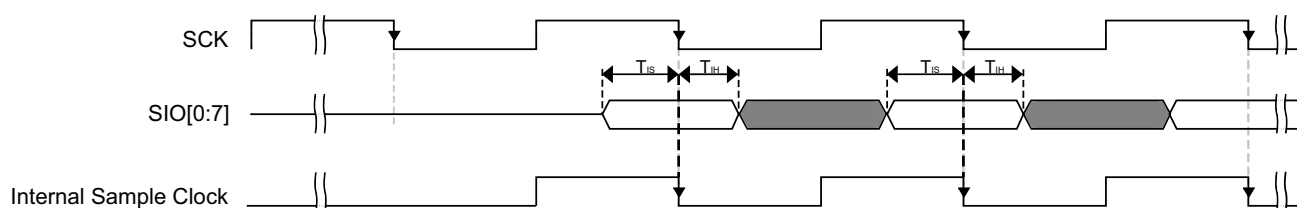
#### 4.5.2.1.1 SDR mode with FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x0, 0x1

Table 50. FlexSPI input timing in SDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0X0

| Symbol          | Parameter                    | Min  | Max | Unit |
|-----------------|------------------------------|------|-----|------|
|                 | Frequency of operation       | —    | 60  | MHz  |
| T <sub>IS</sub> | Setup time for incoming data | 8.67 | —   | ns   |
| T <sub>IH</sub> | Hold time for incoming data  | 0    | —   | ns   |

Table 51. FlexSPI input timing in SDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0X1

| Symbol          | Parameter                    | Min | Max | Unit |
|-----------------|------------------------------|-----|-----|------|
|                 | Frequency of operation       | —   | 133 | MHz  |
| T <sub>IS</sub> | Setup time for incoming data | 2   | —   | ns   |
| T <sub>IH</sub> | Hold time for incoming data  | 1   | —   | ns   |



**Figure 19. FlexSPI input timing in SDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0X0, 0X1**

#### NOTE

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

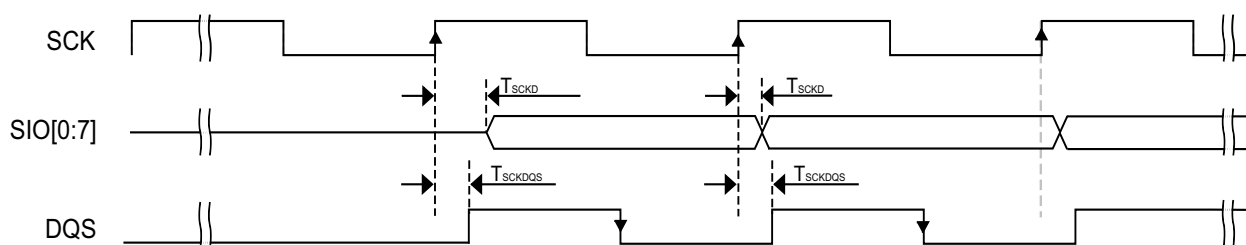
#### 4.5.2.1.2 SDR mode with FlexSPIn\_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in SDR mode:

- A1—Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2—Memory generates read data on SCK falling edge and generates read strobe on SCK rising edge

**Table 52. FlexSPI input timing in SDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0x3 (case A1)**

| Symbol                  | Parameter                                      | Value |     | Unit |
|-------------------------|------------------------------------------------|-------|-----|------|
|                         |                                                | Min   | Max |      |
|                         | Frequency of operation                         | —     | 166 | MHz  |
| $T_{SCKD} - T_{SCKDQS}$ | Time delta between $T_{SCKD}$ and $T_{SCKDQS}$ | -2    | 2   | ns   |



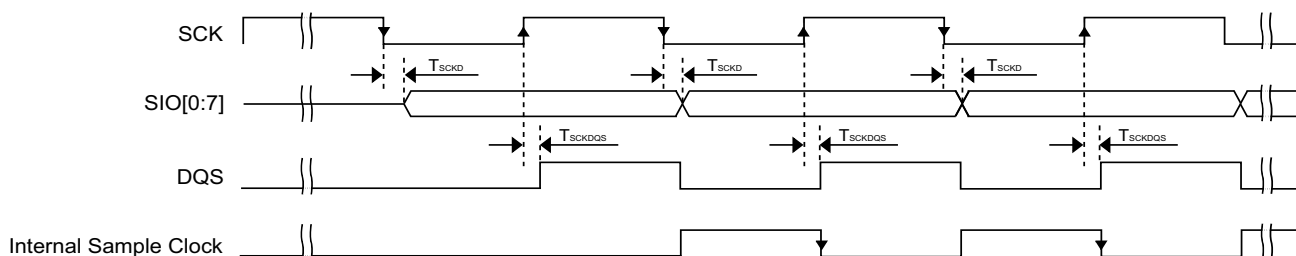
**Figure 20. FlexSPI input timing in SDR mode where FlexSPIn\_MCR0[RXCLKSRC] = 0X3 (case A1)**

**NOTE**

Timing shown is based on the memory generating read data and read strobe on the SCK rising edge. The FlexSPI controller samples read data on the DQS falling edge.

**Table 53. FlexSPI input timing in SDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x3 (case A2)**

| Symbol                  | Parameter                                      | Value |     | Unit |
|-------------------------|------------------------------------------------|-------|-----|------|
|                         |                                                | Min   | Max |      |
|                         | Frequency of operation                         | —     | 166 | MHz  |
| $T_{SCKD} - T_{SCKDQS}$ | Time delta between $T_{SCKD}$ and $T_{SCKDQS}$ | -2    | 2   | ns   |



**Figure 21. FlexSPI input timing in SDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x3 (case A2)**

**NOTE**

Timing shown is based on the memory generating read data on the SCK falling edge and read strobe on the SCK rising edge. The FlexSPI controller samples read data on a half cycle delayed DQS falling edge.

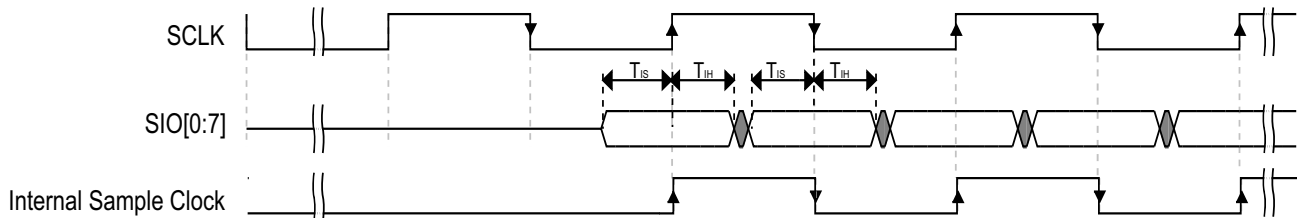
#### 4.5.2.1.3 DDR mode with FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x0, 0x1

**Table 54. FlexSPI input timing in DDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x0**

| Symbol   | Parameter                    | Min  | Max | Unit |
|----------|------------------------------|------|-----|------|
|          | Frequency of operation       | —    | 30  | MHz  |
| $T_{IS}$ | Setup time for incoming data | 8.67 | —   | ns   |
| $T_{IH}$ | Hold time for incoming data  | 0    | —   | ns   |

**Table 55. FlexSPI input timing in DDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x1**

| Symbol   | Parameter                    | Min | Max | Unit |
|----------|------------------------------|-----|-----|------|
|          | Frequency of operation       | —   | 66  | MHz  |
| $T_{IS}$ | Setup time for incoming data | 2   | —   | ns   |
| $T_{IH}$ | Hold time for incoming data  | 1   | —   | ns   |

**Figure 22. FlexSPI input timing in DDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x0, 0x1**

#### 4.5.2.1.4 DDR mode with FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in DDR mode:

- B1—Memory generates both read data and read strobe on SCK edges
- B2—Memory generates read data on SCK edges and generates read strobe on SCK2 edges

**Table 56. FlexSPI input timing in DDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x3 (case B1)**

| Symbol                  | Parameter                                      | Min | Max | Unit |
|-------------------------|------------------------------------------------|-----|-----|------|
|                         | Frequency of operation                         | —   | 166 | MHz  |
| $T_{SCKD} - T_{SCKDQS}$ | Time delta between $T_{SCKD}$ and $T_{SCKDQS}$ | -1  | 1   | ns   |

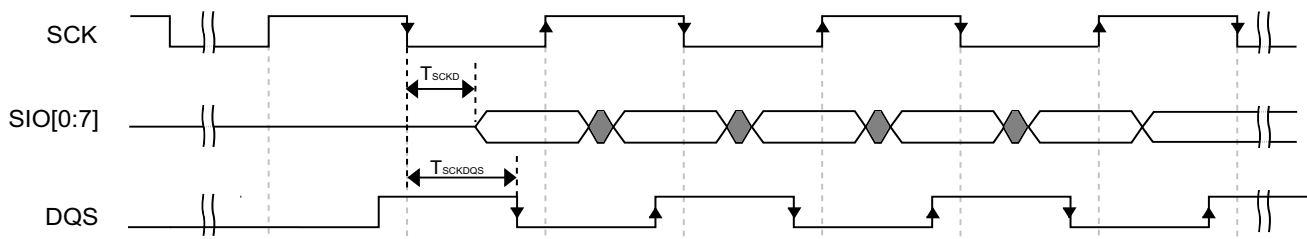
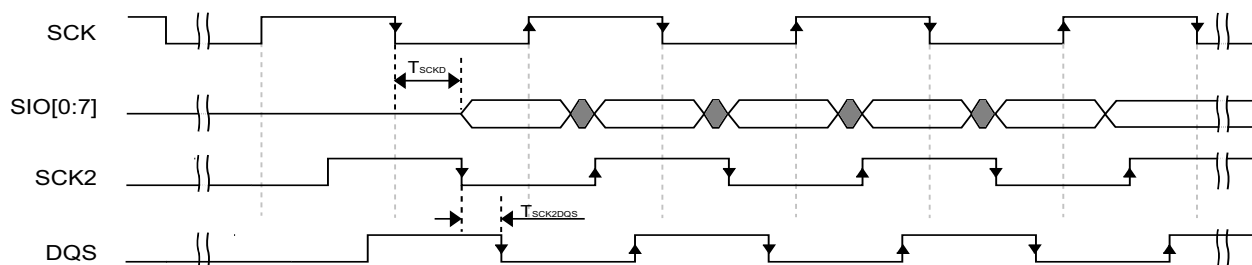
**Figure 23. FlexSPI input timing in DDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x3 (case B1)**

Table 57. FlexSPI input timing in DDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x3 (case B2)

| Symbol                  | Parameter                                      | Min | Max | Unit |
|-------------------------|------------------------------------------------|-----|-----|------|
|                         | Frequency of operation                         | —   | 166 | MHz  |
| $T_{SCKD} - T_{SCKDQS}$ | Time delta between $T_{SCKD}$ and $T_{SCKDQS}$ | -1  | 1   | ns   |

Figure 24. FlexSPI input timing in DDR mode where FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] = 0x3 (case B2)

#### 4.5.2.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

##### 4.5.2.2.1 SDR mode

Table 58. FlexSPI output timing in SDR mode

| Symbol    | Parameter                     | Min                   | Max              | Unit |
|-----------|-------------------------------|-----------------------|------------------|------|
|           | Frequency of operation        | —                     | 166 <sup>1</sup> | MHz  |
| $T_{ck}$  | SCK clock period              | 6.0                   | —                | ns   |
| $T_{DVO}$ | Output data valid time        | —                     | 1                | ns   |
| $T_{DHO}$ | Output data hold time         | 1                     | —                | ns   |
| $T_{CSS}$ | Chip select output setup time | $3 \times T_{CK} - 1$ | —                | ns   |
| $T_{CSH}$ | Chip select output hold time  | $3 \times T_{CK} + 2$ | —                | ns   |

<sup>1</sup> The actual maximum frequency supported is limited by the FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI SDR input timing specifications.

#### NOTE

$T_{CSS}$  and  $T_{CSH}$  are configured by the FlexSPI<sub>n</sub>\_FLSHAxCR1 register, the default values are shown above. Please refer to the *i.MXRT1160 Reference Manual* ([IMXRT1160RM](#)) for more details.

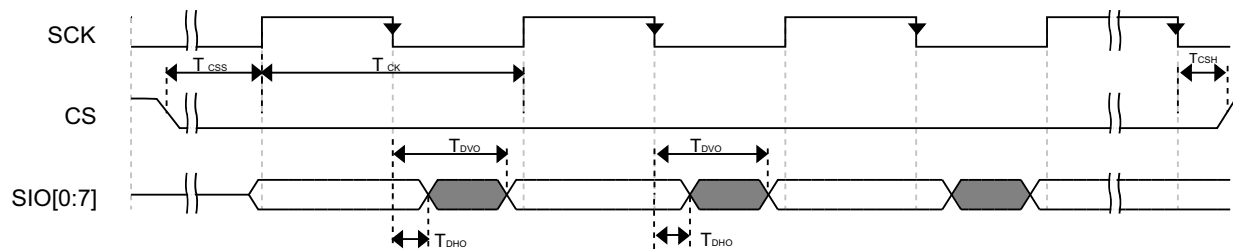


Figure 25. FlexSPI output timing in SDR mode

#### 4.5.2.2.2 DDR mode

Table 59. FlexSPI output timing in DDR mode

| Symbol    | Parameter                                                     | Min                         | Max | Unit |
|-----------|---------------------------------------------------------------|-----------------------------|-----|------|
|           | Frequency of operation <sup>1</sup>                           | —                           | 166 | MHz  |
| $T_{ck}$  | SCK clock period (FlexSPI <sub>n</sub> _MCR0[RXCLKSRC] = 0x0) | 6.0                         | —   | ns   |
| $T_{DVO}$ | Output data valid time                                        | —                           | 2.2 | ns   |
| $T_{DHO}$ | Output data hold time                                         | 0.8                         | —   | ns   |
| $T_{CSS}$ | Chip select output setup time                                 | $3 \times T_{CK} / 2 - 0.7$ | —   | ns   |
| $T_{CSH}$ | Chip select output hold time                                  | $3 \times T_{CK} / 2 + 0.8$ | —   | ns   |

<sup>1</sup> The actual maximum frequency supported is limited by the FlexSPI<sub>n</sub>\_MCR0[RXCLKSRC] configuration used. Please refer to the FlexSPI SDR input timing specifications.

#### NOTE

$T_{CSS}$  and  $T_{CSH}$  are configured by the FlexSPI<sub>n</sub>\_FLSHAxCR1 register, the default values are shown above. Please refer to the *i.MXRT1160 Reference Manual* ([IMXRT1160RM](#)) for more details.

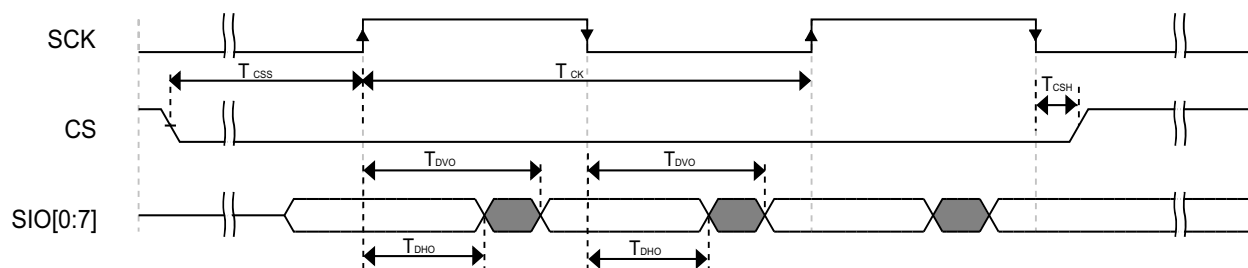


Figure 26. FlexSPI output timing in DDR mode

## 4.6 Display and graphics

The following sections provide information about display and graphic interfaces.

## 4.6.1 MIPI D-PHY electrical characteristics

The i.MX RT1160 conforms to the MIPI CSI-2 and D-PHY standards for protocol and electrical specifications.

Compliant with standards:

- *MIPI Alliance Specification for Display Serial Interface Version 1.1* (MIPI DSI controller)
- *MIPI Standard 1.1 for D-PHY* (MIPI DSI D-PHY)
- Compatible with *MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.1*

### 4.6.1.1 MIPI HS-TX specifications

**Table 60. MIPI high-speed transmitter DC specifications**

| Symbol                      | Parameter                                                           | Min | Typ | Max  | Unit     |
|-----------------------------|---------------------------------------------------------------------|-----|-----|------|----------|
| $V_{CMTX}^1$                | High Speed Transmit Static Common Mode Voltage                      | 150 | 200 | 250  | mV       |
| $ \Delta V_{CMTX} _{(1,0)}$ | $V_{CMTX}$ mismatch when Output is Differential-1 or Differential-0 | —   | —   | 5    | mV       |
| $ V_{OD} ^1$                | High Speed Transmit Differential Voltage                            | 140 | 200 | 270  | mV       |
| $ \Delta V_{OD} $           | $V_{OD}$ mismatch when Output is Differential-1 or Differential-0   | —   | —   | 14   | mV       |
| $V_{OHHS}^1$                | High Speed Output High Voltage                                      | —   | —   | 360  | mV       |
| $Z_{OS}$                    | Single Ended Output Impedance                                       | 40  | 50  | 62.5 | $\Omega$ |
| $\Delta Z_{OS}$             | Single Ended Output Impedance Mismatch                              | —   | —   | 10   | %        |

<sup>1</sup> Value when driving into load impedance anywhere in the  $Z_{ID}$  (Differential input impedance) range.

**Table 61. MIPI high-speed transmitter AC specifications**

| Symbol                | Parameter                                 | Min | Typ | Max      | Unit               |
|-----------------------|-------------------------------------------|-----|-----|----------|--------------------|
| $\Delta V_{CMTX(HF)}$ | Common-level variations above 450 MHz     | —   | —   | 15       | mV <sub>RMS</sub>  |
| $\Delta V_{CMTX(LF)}$ | Common-level variation between 50-450 MHz | —   | —   | 25       | mV <sub>PEAK</sub> |
| $t_R$ and $t_F^1$     | Rise Time and Fall Time (20% to 80%)      | 150 | —   | 0.3 x UI | ps                 |

<sup>1</sup> UI is the long-term average unit interval.

### 4.6.1.2 MIPI LP-TX specifications

**Table 62. MIPI low-power transmitter DC specifications**

| Symbol      | Parameter                                 | Min | Typ | Max | Unit     |
|-------------|-------------------------------------------|-----|-----|-----|----------|
| $V_{OH}^1$  | Thevenin Output High Level                | 1.1 | 1.2 | 1.3 | V        |
| $V_{OL}$    | Thevenin Output Low Level                 | -50 | —   | 50  | mV       |
| $Z_{OLP}^2$ | Output Impedance of Low Power Transmitter | 110 | —   | —   | $\Omega$ |

<sup>1</sup> This specification can only be met when limiting the core supply variation from 1.1 V to 1.3 V.

## Electrical characteristics

- <sup>2</sup> Though there is no specified maximum for  $Z_{OLP}$ , the LP transmitter output impedance ensures the  $T_{RLP}/T_{FLP}$  specification is met.

**Table 63. MIPI low-power transmitter AC specifications**

| Symbol                                      | Parameter                                                                                                                    | Min | Typ | Max | Unit  |
|---------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-------|
| $T_{RLP}/T_{FLP}$ <sup>1</sup>              | 15% to 85% Rise Time and Fall Time                                                                                           | —   | —   | 25  | ns    |
| $T_{REOT}$ <sup>1,2,3</sup>                 | 30% to 85% Rise Time and Fall Time                                                                                           | —   | —   | 35  | ns    |
| $T_{LP-PULSE-TX}$ <sup>4</sup>              | Pulse width of the LP exclusive-OR clock: First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state | 40  | —   | —   | ns    |
|                                             | Pulse width of the LP exclusive-OR clock: All other pulses                                                                   | 20  | —   | —   | ns    |
| $T_{LP-PER-TX}$                             | Period of the LP exclusive-OR clock                                                                                          | 90  | —   | —   | ns    |
| $\delta V/\delta t_{SR}$ <sup>1,5,6,7</sup> | Slew Rate @ $C_{LOAD} = 0$ pF                                                                                                | 30  | —   | 500 | mV/ns |
|                                             | Slew Rate @ $C_{LOAD} = 5$ pF                                                                                                | 30  | —   | 200 | mV/ns |
|                                             | Slew Rate @ $C_{LOAD} = 20$ pF                                                                                               | 30  | —   | 150 | mV/ns |
|                                             | Slew Rate @ $C_{LOAD} = 70$ pF                                                                                               | 30  | —   | 100 | mV/ns |
| $C_{LOAD}$ <sup>1</sup>                     | Load Capacitance                                                                                                             | 0   | —   | 70  | pF    |

<sup>1</sup>  $C_{LOAD}$  includes the low equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2 ns delay.

<sup>2</sup> The rise-time of  $T_{REOT}$  starts from the HS common-level at the moment of the differential amplitude drops below 70 mV, due to stopping of the differential drive.

<sup>3</sup> With an additional load capacitance  $C_{CM}$  between 0 to 60 pF on the termination center tap at RX side of the lane.

<sup>4</sup> This parameter value can be lower than  $T_{LPX}$  (MIPI D-PHY low power states), due to differences in rise vs. fall signal slopes, trip levels, and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in Low-Power Receiver section.

<sup>5</sup> When the output voltage is between 15% and 85% of the fully settled LP signal levels.

<sup>6</sup> Measured as average across any 50 mV segment of the output signal transition.

<sup>7</sup> This value represents a corner point in a piecewise linear curve.

### 4.6.1.3 MIPI LP-RX specifications

**Table 64. MIPI low power receiver DC specifications**

| Symbol        | Parameter                               | Min | Typ | Max  | Unit |
|---------------|-----------------------------------------|-----|-----|------|------|
| $V_{IH}$      | Logic 1 input voltage                   | 880 | —   | 1300 | mV   |
| $V_{IL}$      | Logic 0 input voltage, not in ULP state | —   | —   | 550  | mV   |
| $V_{IL-ULPS}$ | Logic 0 input voltage, ULP state        | —   | —   | 300  | mV   |
| $V_{HYST}$    | Input hysteresis                        | 25  | —   | —    | mV   |

**Table 65. MIPI low power receiver AC specifications**

| Symbol                     | Parameter             | Min | Typ | Max | Unit |
|----------------------------|-----------------------|-----|-----|-----|------|
| $e_{SPIKE}$ <sup>1,2</sup> | Input pulse rejection | —   | —   | 300 | V.ps |

**Table 65. MIPI low power receiver AC specifications (continued)**

|                       |                              |     |   |     |     |
|-----------------------|------------------------------|-----|---|-----|-----|
| $T_{\text{MIN-RX}}^3$ | Minimum pulse width response | 20  | — | —   | ns  |
| $V_{\text{INT}}$      | Peak Interference amplitude  | —   | — | 200 | mV  |
| $f_{\text{INT}}$      | Interference frequency       | 450 | — | —   | MHz |

<sup>1</sup> Time-voltage integration of a spike above  $V_{\text{IL}}$  when being in LP-0 state or below  $V_{\text{IH}}$  when being in LP-1 state.

<sup>2</sup> An impulse below this value will not change the receiver state.

<sup>3</sup> An input pulse greater than this value will toggle the output.

#### 4.6.1.4 MIPI LP-CD specifications

**Table 66. MIPI contention detector DC specifications**

| Symbol            | Parameter                    | Min | Typ | Max | Unit |
|-------------------|------------------------------|-----|-----|-----|------|
| $V_{\text{IHCD}}$ | Logic 1 contention threshold | 450 | —   | —   | mV   |
| $V_{\text{ILCD}}$ | Logic 0 contention threshold | —   | —   | 200 | mV   |

#### 4.6.1.5 MIPI DC specifications

**Table 67. MIPI input characteristics DC specifications**

| Symbol                      | Parameter                                                                         | Min   | Typ | Max  | Unit          |
|-----------------------------|-----------------------------------------------------------------------------------|-------|-----|------|---------------|
| $V_{\text{PIN}}$            | Pad signal voltage range                                                          | -50   | —   | 1350 | mV            |
| $I_{\text{LEAK}}^1$         | Pin leakage current                                                               | -10   | —   | 10   | $\mu\text{A}$ |
| $V_{\text{GNDSH}}$          | Ground shift                                                                      | -50   | —   | 50   | mV            |
| $V_{\text{PIN(absmax)}}^2$  | Maximum pin voltage level                                                         | -0.15 | —   | 1.45 | V             |
| $T_{\text{VPIN(absmax)}}^3$ | Maximum transient time above $V_{\text{PIN(max)}}$ or below $V_{\text{PIN(min)}}$ | —     | —   | 20   | ns            |

<sup>1</sup> When the pad voltage is within the signal voltage range between  $V_{\text{GNDSH(min)}}$  to  $V_{\text{OH}} + V_{\text{GNDSH(max)}}$  and the Lane Module is in LP receive mode.

<sup>2</sup> This value includes ground shift.

<sup>3</sup> The voltage overshoot and undershoot beyond the  $V_{\text{PIN}}$  is only allowed during a single 20 ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the  $V_{\text{PIN}}$  range.

### 4.6.2 CMOS Sensor Interface (CSI) timing parameters

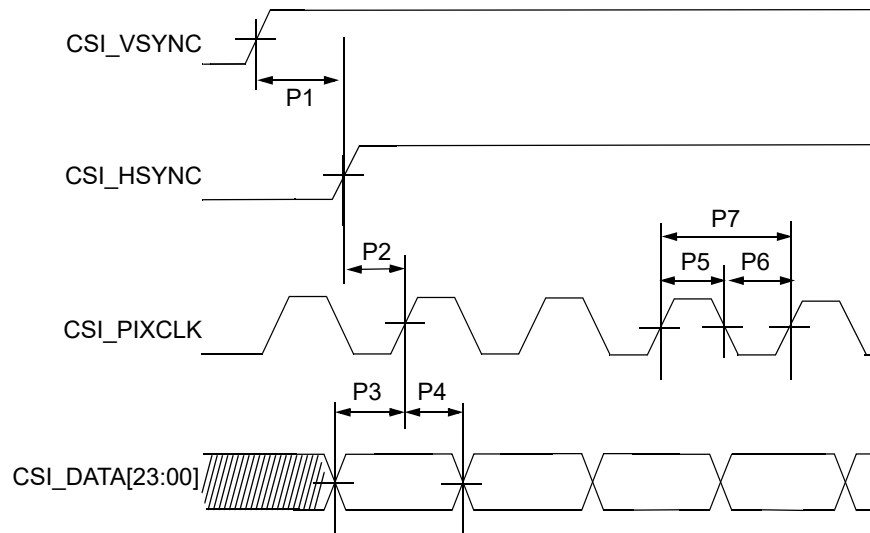
The following sections describe the CSI timing in gated and ungated clock modes.

#### 4.6.2.1 Gated clock mode timing

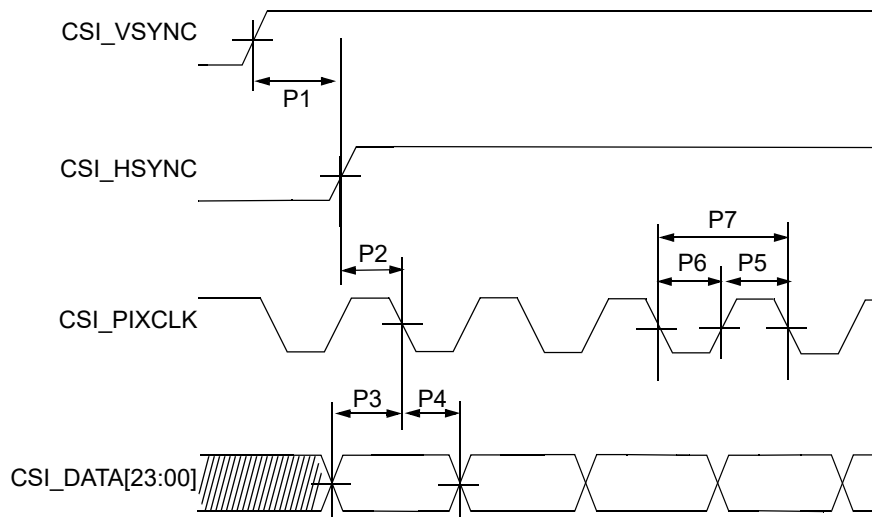
Figure 27 and Figure 28 shows the gated clock mode timings for CSI, and Table 68 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on CSI\_VSYNC

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(VSYNC), then CSI\_HSYNC (HSYNC) is asserted and holds for the entire line. The pixel clock, CSI\_PIXCLK (PIXCLK), is valid as long as HSYNC is asserted.



**Figure 27. CSI Gated clock mode—sensor data at falling edge, latch data at rising edge**



**Figure 28. CSI Gated clock mode—sensor data at rising edge, latch data at falling edge**

**Table 68. CSI gated clock mode timing parameters**

| ID | Parameter                   | Symbol | Min. | Max. | Units |
|----|-----------------------------|--------|------|------|-------|
| P1 | CSI_VSYNC to CSI_HSYNC time | tV2H   | 33.5 | —    | ns    |
| P2 | CSI_HSYNC setup time        | tHsu   | 2.6  | —    | ns    |
| P3 | CSI DATA setup time         | tDsu   | 2.6  | —    | ns    |

Table 68. CSI gated clock mode timing parameters (continued)

| ID | Parameter                 | Symbol | Min. | Max. | Units |
|----|---------------------------|--------|------|------|-------|
| P4 | CSI DATA hold time        | tDh    | 0    | —    | ns    |
| P5 | CSI pixel clock high time | tCLKh  | 3.75 | —    | ns    |
| P6 | CSI pixel clock low time  | tCLKl  | 3.75 | —    | ns    |
| P7 | CSI pixel clock frequency | fCLK   | —    | 80   | MHz   |

#### 4.6.2.2 Ungated clock mode timing

Figure 29 shows the ungated clock mode timings of CSI, and Table 69 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI\_VSYNC and CSI\_PIXCLK signals are used, and the CSI\_HSYNC signal is ignored.

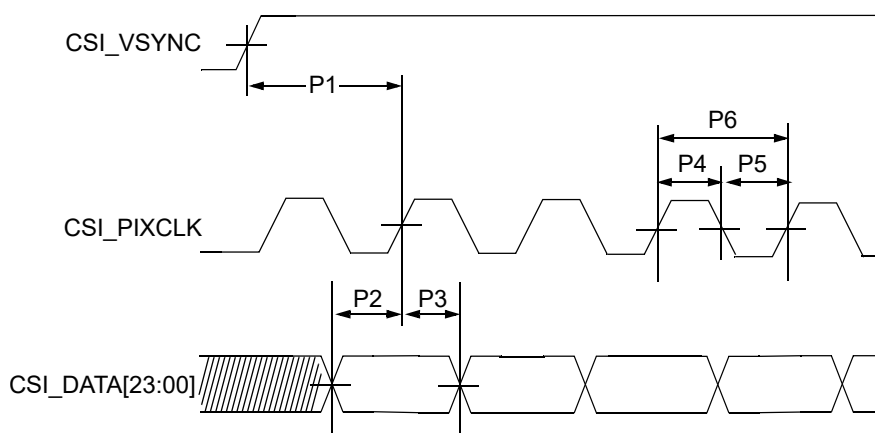


Figure 29. CSI ungated clock mode—sensor data at falling edge, latch data at rising edge

Table 69. CSI ungated clock mode timing parameters

| ID | Parameter                     | Symbol | Min. | Max. | Units |
|----|-------------------------------|--------|------|------|-------|
| P1 | CSI_VSYNC to pixel clock time | tVSYNC | 33.5 | —    | ns    |
| P2 | CSI DATA setup time           | tDsu   | 2.6  | —    | ns    |
| P3 | CSI DATA hold time            | tDh    | 0    | —    | ns    |
| P4 | CSI pixel clock high time     | tCLKh  | 3.75 | —    | ns    |
| P5 | CSI pixel clock low time      | tCLKl  | 3.75 | —    | ns    |
| P6 | CSI pixel clock frequency     | fCLK   | —    | 80   | MHz   |

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

### 4.6.3 LCD Controller timing parameters

Figure 30 shows the LCD timing and Table 70 lists the timing parameters.

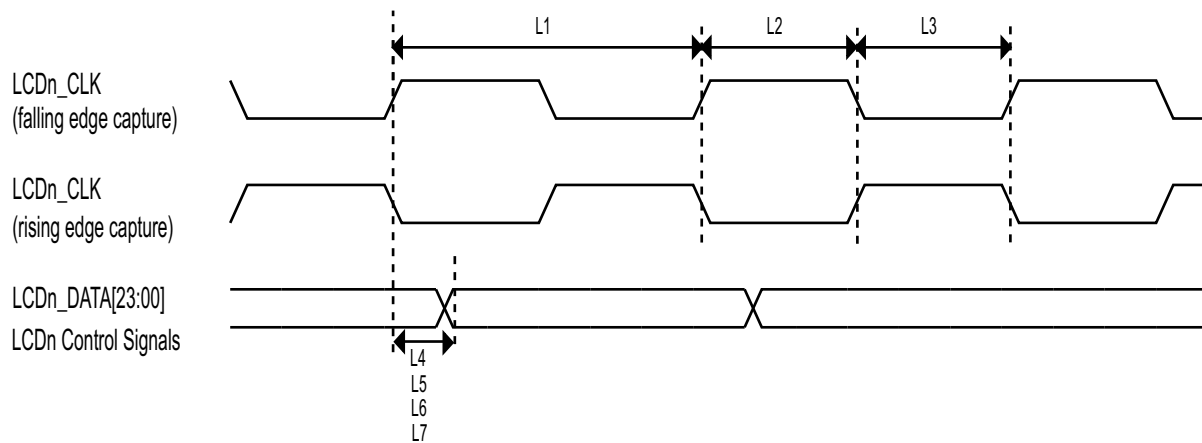


Figure 30. LCD timing

Table 70. LCD timing parameters

| ID | Parameter                                                           | Symbol         | Min | Max                 | Unit |
|----|---------------------------------------------------------------------|----------------|-----|---------------------|------|
| L1 | LCD pixel clock frequency                                           | tCLK(LCD)      | —   | 75/150 <sup>1</sup> | MHz  |
| L2 | LCD pixel clock high (falling edge capture)                         | tCLKH(LCD)     | 3   | —                   | ns   |
| L3 | LCD pixel clock low (rising edge capture)                           | tCLKL(LCD)     | 3   | —                   | ns   |
| L4 | LCD pixel clock high to data valid (falling edge capture)           | td(CLKH-DV)    | -1  | 1                   | ns   |
| L5 | LCD pixel clock low to data valid (rising edge capture)             | td(CLKL-DV)    | -1  | 1                   | ns   |
| L6 | LCD pixel clock high to control signal valid (falling edge capture) | td(CLKH-CTRLV) | -1  | 1                   | ns   |
| L7 | LCD pixel clock low to control signal valid (rising edge capture)   | td(CLKL-CTRLV) | -1  | 1                   | ns   |

<sup>1</sup> For eLCDIF or LCDIFv2, the maximum pixel clock frequency of parallel IO interface is 75 MHz, while it is 150 MHz for MIPI DSI interface.

## 4.7 Audio

This section provides information about SAI/I2S.

### 4.7.1 SAI/I2S switching specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave (clocks input) modes. All timings are given for non-inverted serial clock polarity (SAI\_TCR[TSCKP] = 0, SAI\_RCR[RSCKP] = 0) and non-inverted frame sync (SAI\_TCR[TFSI] = 0, SAI\_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI\_BCLK) and/or the frame sync (SAI\_FS) shown in the figures below.

Table 71. Master mode SAI timing

| Num | Characteristic                             | Min | Max | Unit        |
|-----|--------------------------------------------|-----|-----|-------------|
| S1  | SAI_MCLK cycle time                        | 15  | —   | ns          |
| S2  | SAI_MCLK pulse width high/low              | 40% | 60% | MCLK period |
| S3  | SAI_BCLK cycle time                        | 40  | —   | ns          |
| S4  | SAI_BCLK pulse width high/low              | 40% | 60% | BCLK period |
| S5  | SAI_BCLK to SAI_FS output valid            | —   | 8.4 | ns          |
| S6  | SAI_BCLK to SAI_FS output invalid          | 0   | —   | ns          |
| S7  | SAI_BCLK to SAI_TXD valid                  | —   | 10  | ns          |
| S8  | SAI_BCLK to SAI_TXD invalid                | 1   | —   | ns          |
| S9  | SAI_RXD/SAI_FS input setup before SAI_BCLK | 14  | —   | ns          |
| S10 | SAI_RXD/SAI_FS input hold after SAI_BCLK   | 0   | —   | ns          |

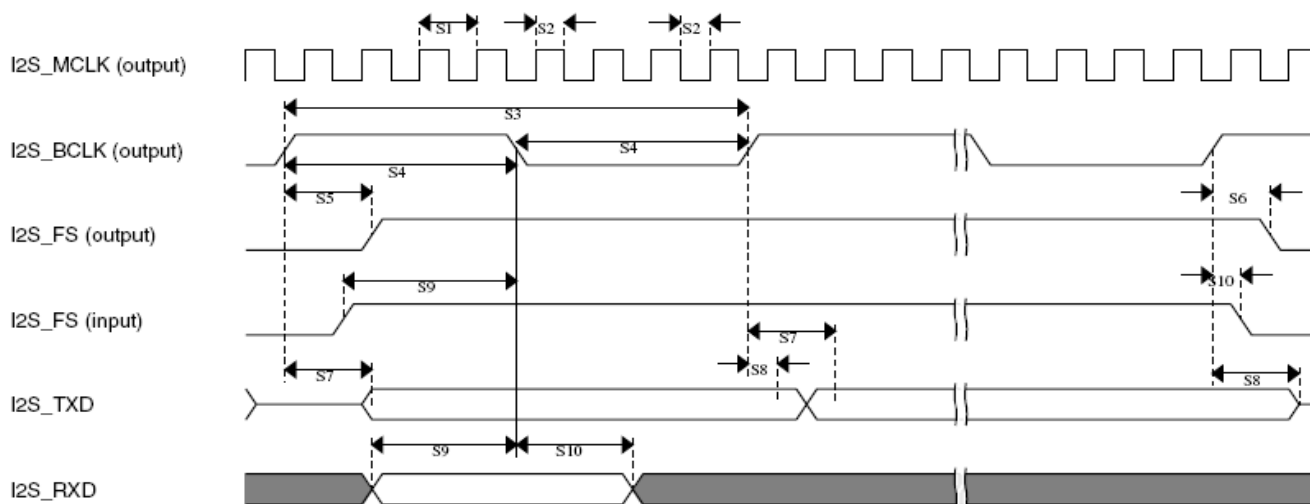


Figure 31. SAI timing—Master modes

Table 72. Slave mode SAI timing

| Num | Characteristic                            | Min  | Max | Unit        |
|-----|-------------------------------------------|------|-----|-------------|
| S11 | SAI_BCLK cycle time (input)               | 40   | —   | ns          |
| S12 | SAI_BCLK pulse width high/low (input)     | 40%  | 60% | BCLK period |
| S13 | SAI_FS input setup before SAI_BCLK        | 6    | —   | ns          |
| S14 | SAI_FA input hold after SAI_BCLK          | 2    | —   | ns          |
| S15 | SAI_BCLK to SAI_TXD/SAI_FS output valid   | —    | 20  | ns          |
| S16 | SAI_BCLK to SAI_TXD/SAI_FS output invalid | -1.5 | —   | ns          |

Table 72. Slave mode SAI timing

| Num | Characteristic                | Min | Max | Unit |
|-----|-------------------------------|-----|-----|------|
| S17 | SAI_RXD setup before SAI_BCLK | 6   | —   | ns   |
| S18 | SAI_RXD hold after SAI_BCLK   | 2   | —   | ns   |

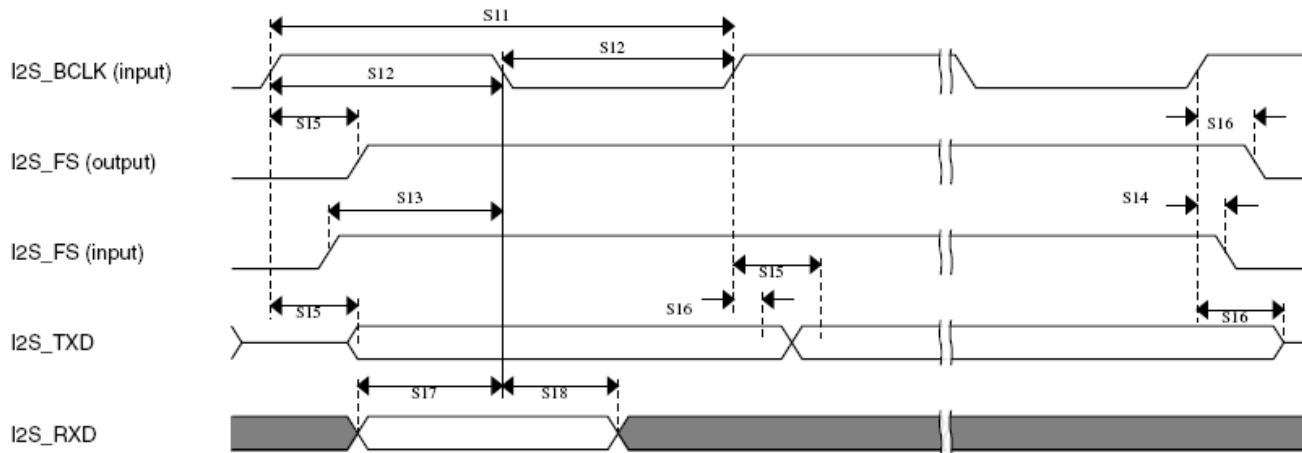


Figure 32. SAI timing—Slave mode

## 4.8 Analog

The following sections provide information about analog interfaces.

### 4.8.1 12-bit ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

**Table 73. ADC electrical specifications ( $V_{REFH} = V_{DD\_ANA\_18}^1$  and  $V_{ADIN_{max}} \leq V_{REFH}$ )**

| Symbol           | Description                     | Min                                         | Typ  | Max        | Unit      | Notes |
|------------------|---------------------------------|---------------------------------------------|------|------------|-----------|-------|
| $V_{ADIN}$       | Input voltage                   | $V_{REFL}$                                  | —    | $V_{REFH}$ | V         | —     |
| $V_{REFH}$       | ADC high reference supply input | 1.0                                         | 1.8  | 1.89       | V         | —     |
| $C_{ADIN}$       | Input capacitance               | —                                           | 4.5  | —          | pF        | —     |
| $R_{ADIN}$       | Input resistance                | —                                           | 500  | —          | $\Omega$  | —     |
| $R_{AS}$         | Analog source resistance        | —                                           | —    | 5          | $K\Omega$ | 2     |
| $f_{ADCK}$       | ADC conversion clock frequency  | 8                                           | —    | 88         | MHz       | —     |
| $C_{sample}$     | Sample cycles                   | 3.5                                         | —    | 131.5      | Cycles    | 3     |
| $C_{compare}$    | Fixed compare cycles            | —                                           | 17.5 | —          | Cycles    | —     |
| $C_{conversion}$ | Conversion cycles               | $C_{conversion} = C_{sample} + C_{compare}$ |      |            | Cycles    | —     |

**Table 73. ADC electrical specifications (VREFH = VDD\_ANA\_18<sup>1</sup> and VADIN<sub>max</sub> ≤ VREFH) (continued)**

| Symbol                | Description                      | Min                                         | Typ       | Max | Unit | Notes |
|-----------------------|----------------------------------|---------------------------------------------|-----------|-----|------|-------|
| TUE                   | Total unadjusted Error           | —                                           | -14 to -2 | —   | LSB  | 4     |
| DNL                   | Differential nonlinearity        | —                                           | ±1.2      | —   | LSB  | 4,5   |
| INL                   | Integral nonlinearity            | —                                           | ±1.2      | —   | LSB  | 4,5   |
| ENOB                  | Effective number of bits         |                                             |           |     |      | 6     |
|                       | Single-ended mode                |                                             |           |     |      |       |
|                       | Avg = 1                          | —                                           | 10.3      | —   | —    |       |
|                       | Avg = 2                          | —                                           | 10.6      | —   | —    |       |
|                       | Avg = 16                         | —                                           | 11.3      | —   | —    |       |
|                       | Differential mode                |                                             |           |     |      |       |
|                       | Avg = 1                          | —                                           | 11.2      | —   | —    |       |
|                       | Avg = 2                          | —                                           | —         | —   | —    |       |
|                       | Avg = 16                         | —                                           | —         | —   | —    |       |
| SINAD                 | Signal to noise plus distortion  | SINAD = 6.02 x ENOB + 1.76                  |           |     | dB   | —     |
| EFS                   | Full-scale error                 | —                                           | -4        | —   | LSB  | 4     |
| EZS                   | Zero-scale error                 | —                                           | 0.05      | —   | LSB  | 4     |
| lin_ext_leak          | External channel leakage current | —                                           | 30        | 500 | nA   | —     |
| EIL                   | Input leakage error              | R <sub>AS</sub> * I <sub>lin_ext_leak</sub> |           |     | mV   | —     |
| t <sub>ADCSETUP</sub> | Setup time                       | —                                           | 5         | —   | μs   | —     |

<sup>1</sup> The range is from 1.71 V to 1.89 V.

<sup>2</sup> This resistance is external to the SoC. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The R<sub>AS</sub> and C<sub>AS</sub> time constant should be kept to < 1 ns.

<sup>3</sup> See [Figure 33, "Sample time VS. RAS"](#).

<sup>4</sup> 1 LSB = (VREFH - VREFL) / 2<sup>N</sup>, N = 12

<sup>5</sup> ADC conversion clock at max frequency and using linear histogram.

<sup>6</sup> Input data used for test is 1 kHz sine wave.

**Table 74. ADC electrical specifications (VREFH = 1.68 V and VADIN<sub>max</sub> ≤ NVCC\_GPIO<sub>max</sub>)**

| Symbol            | Description                     | Min               | Typ <sup>1</sup> | Max                      | Unit | Notes        |
|-------------------|---------------------------------|-------------------|------------------|--------------------------|------|--------------|
| V <sub>ADIN</sub> | Input voltage                   | V <sub>REFL</sub> | —                | NVCC_GPIO <sub>max</sub> | V    | —            |
| V <sub>REFH</sub> | ADC high reference supply input | 1.0               | 1.8              | 1.89                     | V    | —            |
| C <sub>ADIN</sub> | Input capacitance               | —                 | 4.5              | —                        | pF   | —            |
| R <sub>ADIN</sub> | Input resistance                | —                 | 1                | —                        | KΩ   | —            |
| R <sub>AS</sub>   | Analog source resistance        | —                 | —                | 5                        | KΩ   | <sup>2</sup> |

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**Table 74. ADC electrical specifications (VREFH = 1.68 V and VADIN<sub>max</sub> ≤ NVCC\_GPIO<sub>max</sub>) (continued)**

| Symbol                   | Description                      | Min                                                                  | Typ <sup>1</sup> | Max   | Unit   | Notes |
|--------------------------|----------------------------------|----------------------------------------------------------------------|------------------|-------|--------|-------|
| f <sub>ADCK</sub>        | ADC conversion clock frequency   | 8                                                                    | —                | 88    | MHz    | —     |
| C <sub>sample</sub>      | Sample cycles                    | 3.5                                                                  | —                | 131.5 | Cycles | 3     |
| C <sub>compare</sub>     | Fixed compare cycles             | —                                                                    | 17.5             | —     | Cycles | —     |
| C <sub>conversion</sub>  | Conversion cycles                | C <sub>conversion</sub> = C <sub>sample</sub> + C <sub>compare</sub> |                  |       | Cycles | —     |
| TUE                      | Total unadjusted Error           | —                                                                    | -14 to -2        | —     | LSB    | 4     |
| DNL                      | Differential nonlinearity        | —                                                                    | ±1.2             | —     | LSB    | 4,5   |
| INL                      | Integral nonlinearity            | —                                                                    | ±1.2             | —     | LSB    | 4,5   |
| ENOB                     | Effective number of bits         |                                                                      |                  |       |        | 6     |
|                          | Single-ended mode                |                                                                      |                  |       |        |       |
|                          | Avg = 1                          | —                                                                    | 10.3             | —     | —      |       |
|                          | Avg = 2                          | —                                                                    | 10.6             | —     | —      |       |
|                          | Avg = 16                         | —                                                                    | 11.3             | —     | —      |       |
|                          | Differential mode                |                                                                      |                  |       |        |       |
|                          | Avg = 1                          | —                                                                    | 11.2             | —     | —      |       |
|                          | Avg = 2                          | —                                                                    | —                | —     | —      |       |
|                          | Avg = 16                         | —                                                                    | —                | —     | —      |       |
| SINAD                    | Signal to noise plus distortion  | SINAD = 6.02 x ENOB + 1.76                                           |                  |       | dB     | —     |
| EFS                      | Full-scale error                 | —                                                                    | -4               | —     | LSB    | 4     |
| EZS                      | Zero-scale error                 | —                                                                    | 0.05             | —     | LSB    | 4     |
| I <sub>in_ext_leak</sub> | External channel leakage current | —                                                                    | 30               | 500   | nA     | —     |
| EIL                      | Input leakage error              | R <sub>AS</sub> * I <sub>in_ext_leak</sub>                           |                  |       | mV     | —     |
| t <sub>ADCSETUP</sub>    | Setup time                       | —                                                                    | 5                | —     | μs     | —     |

<sup>1</sup> Typical values assume Temp = 25 °C and f<sub>ADCK</sub> = Max, unless otherwise stated. Typical values are for reference only, and are not tested in production.

<sup>2</sup> This resistance is external to the SoC. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 15 Ω analog source resistance. The R<sub>AS</sub> and C<sub>AS</sub> time constant should be kept to < 1 ns.

<sup>3</sup> See [Figure 33, "Sample time VS. RAS"](#).

<sup>4</sup> 1 LSB = (VREFH - VREFL) / 2<sup>N</sup>, N = 12

<sup>5</sup> ADC conversion clock at max frequency and using linear histogram.

<sup>6</sup> Input data used for test is 1 kHz sine wave.

**Table 75. ADC electrical specifications ( $1\text{ V} \leq V_{\text{REFH}} < V_{\text{DD\_ANA\_18}}_{\text{min}}$ <sup>1</sup> and  $V_{\text{ADIN}}_{\text{max}} \leq V_{\text{REFH}}$ )<sup>2</sup>**

| Symbol                   | Description                      | Min                                                                  | Typ <sup>3</sup> | Max               | Unit   | Notes |
|--------------------------|----------------------------------|----------------------------------------------------------------------|------------------|-------------------|--------|-------|
| V <sub>ADIN</sub>        | Input voltage                    | V <sub>REFL</sub>                                                    | —                | V <sub>REFH</sub> | V      | —     |
| V <sub>REFH</sub>        | ADC high reference supply input  | 1.0                                                                  | 1.8              | 1.89              | V      | —     |
| C <sub>ADIN</sub>        | Input capacitance                | —                                                                    | 4.5              | —                 | pF     | —     |
| R <sub>ADIN</sub>        | Input resistance                 | —                                                                    | 500              | —                 | Ω      | —     |
| R <sub>AS</sub>          | Analog source resistance         | —                                                                    | —                | 5                 | KΩ     | 4     |
| f <sub>ADCK</sub>        | ADC conversion clock frequency   | 8                                                                    | —                | 88                | MHz    | —     |
| C <sub>sample</sub>      | Sample cycles                    | 3.5                                                                  | —                | 131.5             | Cycles | 5     |
| C <sub>compare</sub>     | Fixed compare cycles             | —                                                                    | 17.5             | —                 | Cycles | —     |
| C <sub>conversion</sub>  | Conversion cycles                | C <sub>conversion</sub> = C <sub>sample</sub> + C <sub>compare</sub> |                  |                   | Cycles | —     |
| TUE                      | Total unadjusted Error           | —                                                                    | -14 to -2        | —                 | LSB    | 6     |
| DNL                      | Differential nonlinearity        | —                                                                    | ±1.2             | —                 | LSB    | 6,7   |
| INL                      | Integral nonlinearity            | —                                                                    | ±1.2             | —                 | LSB    | 6,7   |
| ENOB                     | Effective number of bits         |                                                                      |                  |                   |        | 8     |
|                          | Single-ended mode                |                                                                      |                  |                   |        |       |
|                          | Avg = 1                          | —                                                                    | 10.3             | —                 | —      |       |
|                          | Avg = 2                          | —                                                                    | 10.6             | —                 | —      |       |
|                          | Avg = 16                         | —                                                                    | 11.3             | —                 | —      |       |
|                          | Differential mode                |                                                                      |                  |                   |        |       |
|                          | Avg = 1                          | —                                                                    | 11.2             | —                 | —      |       |
|                          | Avg = 2                          | —                                                                    | —                | —                 | —      |       |
|                          | Avg = 16                         | —                                                                    | —                | —                 | —      |       |
| SINAD                    | Signal to noise plus distortion  | SINAD = 6.02 x ENOB + 1.76                                           |                  |                   | dB     | —     |
| EFS                      | Full-scale error                 | —                                                                    | -4               | —                 | LSB    | 6     |
| EZS                      | Zero-scale error                 | —                                                                    | 0.05             | —                 | LSB    | 6     |
| I <sub>in_ext_leak</sub> | External channel leakage current | —                                                                    | 30               | 500               | nA     | —     |
| EIL                      | Input leakage error              | R <sub>AS</sub> * I <sub>in_ext_leak</sub>                           |                  |                   | mV     | —     |
| t <sub>ADCSETUP</sub>    | Setup time                       | —                                                                    | 5                | —                 | μs     | —     |

<sup>1</sup>  $V_{\text{DD\_ANA\_18}}_{\text{min}} = 1.71\text{ V}$ <sup>2</sup> Values in this table are based on design simulations.<sup>3</sup> Typical values assume Temp = 25 °C and  $f_{\text{ACLK}} = \text{Max}$ , unless otherwise stated. Typical values are for reference only, and are not tested in production.

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- <sup>4</sup> This resistance is external to the SoC. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had  $< 15\ \Omega$  analog source resistance. The  $R_{AS}$  and  $C_{AS}$  time constant should be kept to  $< 1\ \text{ns}$ .
- <sup>5</sup> See Figure 33, "Sample time VS.  $R_{AS}$ ".
- <sup>6</sup>  $1\ \text{LSB} = (V_{REFH} - V_{REFL}) / 2^N$ ,  $N = 12$
- <sup>7</sup> ADC conversion clock at max frequency and using linear histogram.
- <sup>8</sup> Input data used for test is 1 kHz sine wave.

The following figure shows a plot of the ADC sample time versus  $R_{AS}$ .

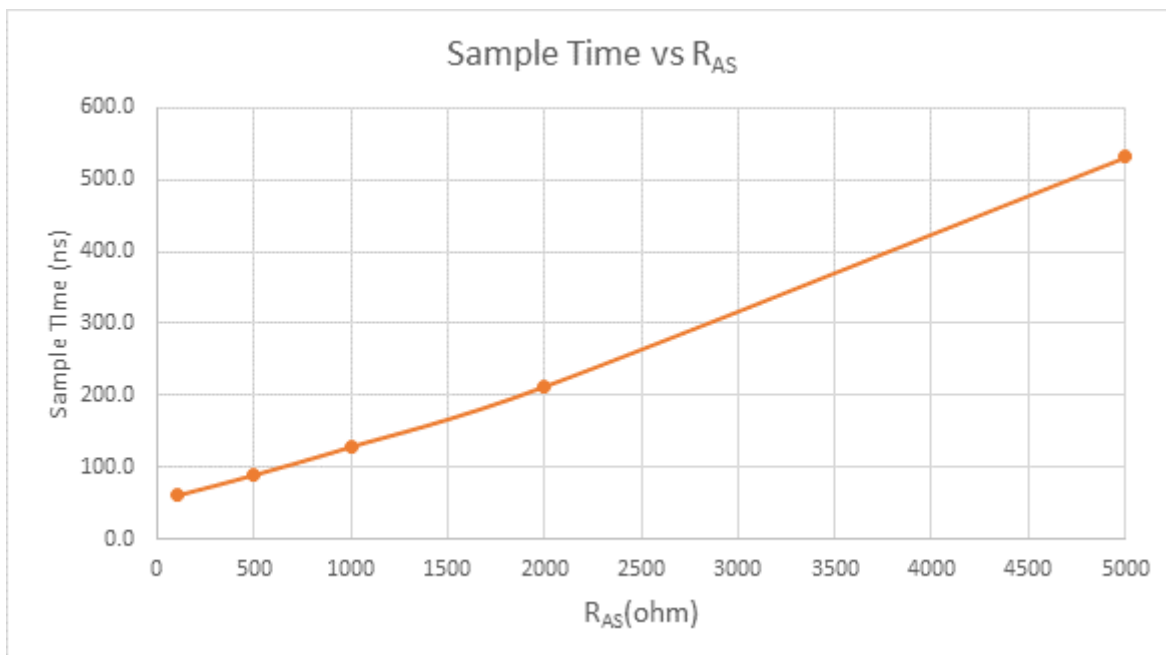


Figure 33. Sample time VS.  $R_{AS}$

### 4.8.1.1 12-bit ADC input impedance equivalent circuit diagram

The following figure shows 12-bit ADC input impedance equivalent circuit diagram.

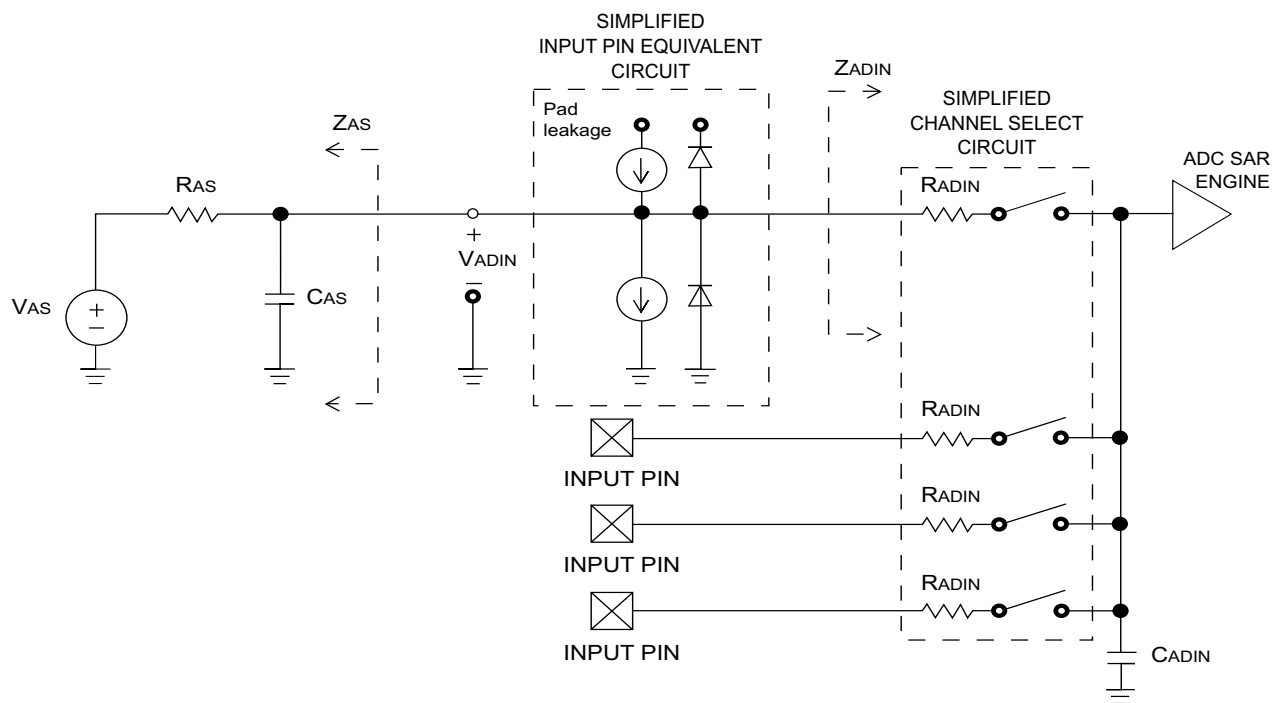


Figure 34. ADC input impedance equivalent circuit diagram

## 4.8.2 12-bit DAC electrical characteristics

### 4.8.2.1 12-bit DAC operating requirements

Table 76. 12-bit DAC operating conditions

| Symbol | Description             | Min | Typ | Max | Unit | Notes |
|--------|-------------------------|-----|-----|-----|------|-------|
| $C_L$  | Output load capacitance | —   | 50  | 100 | pF   | 1     |
| $I_L$  | Output load current     | —   | —   | 1   | mA   | 2     |

<sup>1</sup> The DAC output can drive R and C loading. The user should consider both DC and dynamic application requirements. 50 pF  $C_L$  provides the best dynamic performance, while 100 pF provides the best DC performance.

<sup>2</sup> Sink or source current ability.

Table 77. DAC characteristics

| Symbol   | Description                     | Test Conditions                                     | Min                        | Typ  | Max              | Unit | Notes |
|----------|---------------------------------|-----------------------------------------------------|----------------------------|------|------------------|------|-------|
| VDACOUTL | DAC low level output voltage    | ADC_VREFH selected,<br>Rload = 18 kΩ, Cload = 50 pF | VSS                        | —    | 0.15             | V    | 1     |
| VDACOUTH | DAC high level output voltage   |                                                     | VDDA_AD<br>C_1P8 -<br>0.15 | —    | VDDA_AD<br>C_1P8 | V    |       |
| DNL      | Differential nonlinearity error | Code 100h — F00h best fit curve                     | —                          | ±0.5 | ±1               | LSB  | —     |

Table 77. DAC characteristics (continued)

| Symbol | Description                          | Test Conditions                 | Min | Typ  | Max | Unit                    | Notes        |
|--------|--------------------------------------|---------------------------------|-----|------|-----|-------------------------|--------------|
| INL    | Integral nonlinearity error          | Code 100h — F00h best fit curve | —   | ±1   | —   | LSB                     | <sup>2</sup> |
|        |                                      |                                 | —   | ±2   | —   | LSB                     | <sup>3</sup> |
| EO     | Offset error                         | Code 100h                       | —   | ±0.6 | —   | %FSR (Full-scale range) | —            |
| TEO    | Offset error temperature coefficient | Code 100h                       | —   | ±30  | —   | μV/°C                   | —            |
| EG     | Gain error                           | Code F00h                       | —   | ±0.4 | —   | %FSR                    | —            |
| TEG    | Gain error temperature coefficient   | Code F00h                       | —   | ±10  | —   | ppm of FSR/°C           | —            |

Table 77. DAC characteristics (continued)

| Symbol | Description                                    | Test Conditions                               | Min | Typ | Max | Unit    | Notes |
|--------|------------------------------------------------|-----------------------------------------------|-----|-----|-----|---------|-------|
| TFS_LS | Full scale setting time in Low Speed mode      | Code 100h — F00h or F00h — 100h @ZTC current  | —   | 5   | —   | $\mu$ s | 4     |
|        |                                                | Code 100h — F00h or F00h — 100h @PTAT current | —   | 5   | —   |         |       |
| TFS_MS | Full scale setting time in Middle Speed mode   | Code 100h — F00h or F00h — 100h @ZTC current  | —   | 1   | —   |         |       |
|        |                                                | Code 100h — F00h or F00h — 100h @PTAT current | —   | 1   | —   |         |       |
| TFS_HS | Full scale setting time in High Speed mode     | Code 100h — F00h or F00h — 100h @ZTC current  | —   | 0.5 | —   |         |       |
|        |                                                | Code 100h — F00h or F00h — 100h @PTAT current | —   | 0.5 | —   |         |       |
| TCC_LS | Code to code setting time in Low Speed mode    | Code 7F7h — 807h or 807h — 7F7h @ZTC current  | —   | 1   | —   |         |       |
|        |                                                | Code 7F7h — 807h or 807h — 7F7h @PTAT current | —   | 1   | —   |         |       |
| TCC_MS | Code to code setting time in Middle Speed mode | Code 7F7h — 807h or 807h — 7F7h @ZTC current  | —   | 0.5 | —   |         |       |
|        |                                                | Code 7F7h — 807h or 807h — 7F7h @PTAT current | —   | 0.5 | —   |         |       |
| TCC_HS | Code to code setting time in Middle Speed mode | Code 7F7h — 807h or 807h — 7F7h @ZTC current  | —   | 0.3 | —   |         |       |
|        |                                                | Code 7F7h — 807h or 807h — 7F7h @PTAT current | —   | 0.3 | —   |         |       |

Table 77. DAC characteristics (continued)

| Symbol | Description                    | Test Conditions                                               | Min | Typ  | Max | Unit       | Notes |
|--------|--------------------------------|---------------------------------------------------------------|-----|------|-----|------------|-------|
| SR_LS  | Slew rate in Low Speed mode    | Code 100h — F00h or F00h — 100h @ZTC current                  | —   | 0.24 | —   | V/ $\mu$ s | 5     |
|        |                                | Code 100h — F00h or F00h — 100h @PTAT current                 | —   | 0.24 | —   |            |       |
| SR_MS  | Slew rate in Middle Speed mode | Code 100h — F00h or F00h — 100h @ZTC current                  | —   | 1.2  | —   |            |       |
|        |                                | Code 100h — F00h or F00h — 100h @PTAT current                 | —   | 1.2  | —   |            |       |
| SR_HS  | Slew rate in High Speed mode   | Code 100h — F00h or F00h — 100h @ZTC current                  | —   | 2.4  | —   |            |       |
|        |                                | Code 100h — F00h or F00h — 100h @PTAT current                 | —   | 2.4  | —   |            |       |
| PSRR   | Power supply rejection ratio   | Code 800h, $\Delta VDD\_ANA18 = 100$ mV, VREFH_ANA12 selected | —   | 70   | —   | dB         | 6     |
| Glitch | Glitch energy                  | Code 100h — F00h — 100h                                       | —   | 30   | —   | nV-s       | —     |
|        |                                | Code 7FFh — 800h — 7FFh                                       | —   | 30   | —   |            |       |
| CT     | Channel to channel crosstalk   | —                                                             | —   | —    | -80 | dB         | 7     |
| ROP    | Output resistance              | Code 100h — F00h and Rload = 18 k $\Omega$                    | —   | 200  | —   | $\Omega$   | 8     |

<sup>1</sup> It is recommended to operate the DAC in the output voltage range between 0.15 V and (VDDA\_ADC\_1P8 - 0.15 V) for best accuracy. Linearity of the output voltage outside this range will be affected as current load increases.

<sup>2</sup> When ADC\_VREFH is selected as the reference (DAC\_CR[DACRFS] = 0b).

<sup>3</sup> When the internal 1.2 V source is selected as the reference (DAC\_CR[DACRFS] = 1b).

<sup>4</sup> The DAC output remains within  $\pm 0.5$  LSB of the final measured value for digital input code change. Noise on the power supply can cause this performance to degrade to  $\pm 1$  LSB. This parameter represents both rising edge and falling edge settling time.

<sup>5</sup> Time for the DAC output to transition from 10% to 90% signal amplitude (rising edge or falling edge).

<sup>6</sup>  $PSRR = 20 \times \log\{\Delta VDD\_ANA18 / \Delta VDAC\_OUT\}$

<sup>7</sup> If two DACs are used and sharing the same VREFH.

<sup>8</sup> Based on design simulation.

### 4.8.3 ACMP electrical specifications

**Table 78. ACMP operating conditions**

| Symbol                 | Description                | Min | Typ | Max  | Unit |
|------------------------|----------------------------|-----|-----|------|------|
| VREFH_EXT              | External reference voltage | 1   | —   | 1.98 | V    |
| VREFH_INT <sup>1</sup> | Internal reference voltage | —   | 1.3 | —    | V    |

<sup>1</sup> This is an internal reference voltage generated by PMCO.

**Table 79. ACMP characteristics**

| Symbol | Description                            | Condition        | Min | Typ | Max                    | Unit |
|--------|----------------------------------------|------------------|-----|-----|------------------------|------|
| VAIN   | Analog input voltage                   | —                | 0   | —   | NVCC_GPIO <sup>1</sup> | V    |
| VAIO   | Analog input offset voltage            | —                | —   | —   | 20                     | mV   |
| VH     | Analog comparator hysteresis           | Hystrl[1:0] = 00 | —   | 5   | —                      | mV   |
|        |                                        | Hystrl[1:0] = 01 | —   | 10  | —                      | mV   |
|        |                                        | Hystrl[1:0] = 10 | —   | 20  | —                      | mV   |
|        |                                        | Hystrl[1:0] = 11 | —   | 30  | —                      | mV   |
| TDHS   | Propagation delay, high-speed mode     | Normal supply    | —   | —   | 50                     | ns   |
| TDHS   | Propagation delay, low-speed mode      | —                | —   | —   | 5                      | μs   |
| —      | Analog comparator initialization delay | —                | —   | —   | 20                     | μs   |
| INL    | 8-bit DAC integral non-linearity       | —                | -1  | —   | 1                      | LSB  |
| DNL    | 8-bit DAC differential non-linearity   | —                | -1  | —   | 1                      | LSB  |

<sup>1</sup> The maximum input voltage for CMP analog inputs associated with GPIO\_AD bank is NVCC\_GPIO.

### 4.8.4 Temperature sensor

Table 80 lists the parameters of temperature sensor.

**Table 80. Temperature sensor parameters**

| Parameter                      | Min | Max | Unit |
|--------------------------------|-----|-----|------|
| Temperature range <sup>1</sup> | -40 | 125 | °C   |

<sup>1</sup> Accuracy of measurement: ± 5°C for 25°C and above, while ± 10°C for below 25°C.

## 4.9 Communication interfaces

The following sections provide the information about communication interfaces.

### 4.9.1 LPSPI timing parameters

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

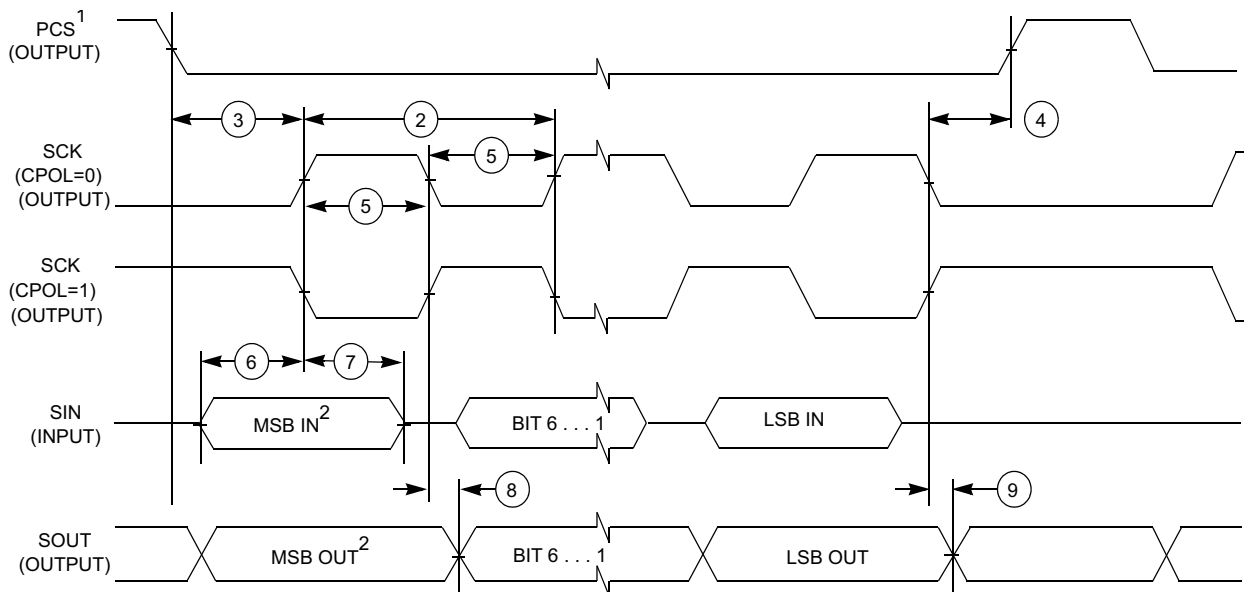
All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

**Table 81. LPSPI Master mode timing**

| Number | Symbol     | Description                  | Min.                  | Max.             | Units        | Note         |
|--------|------------|------------------------------|-----------------------|------------------|--------------|--------------|
| 1      | $f_{SCK}$  | Frequency of operation       | —                     | $f_{periph} / 2$ | MHz          | <sup>1</sup> |
| 2      | $t_{SCK}$  | SCK period                   | $2 \times t_{periph}$ | —                | ns           | <sup>2</sup> |
| 3      | $t_{Lead}$ | Enable lead time             | 1                     | —                | $t_{periph}$ | —            |
| 4      | $t_{Lag}$  | Enable lag time              | 1                     | —                | $t_{periph}$ | —            |
| 5      | $t_{WSCK}$ | Clock (SCK) high or low time | $t_{SCK} / 2 - 3$     | —                | ns           | —            |
| 6      | $t_{SU}$   | Data setup time (inputs)     | 10                    | —                | ns           | —            |
| 7      | $t_{HI}$   | Data hold time (inputs)      | 2                     | —                | ns           | —            |
| 8      | $t_V$      | Data valid (after SCK edge)  | —                     | 8                | ns           | —            |
| 9      | $t_{HO}$   | Data hold time (outputs)     | 0                     | —                | ns           | —            |

<sup>1</sup> Absolute maximum frequency of operation (fop) is 30 MHz. The clock driver in the LPSPI module for  $f_{periph}$  must guaranteed this limit is not exceeded.

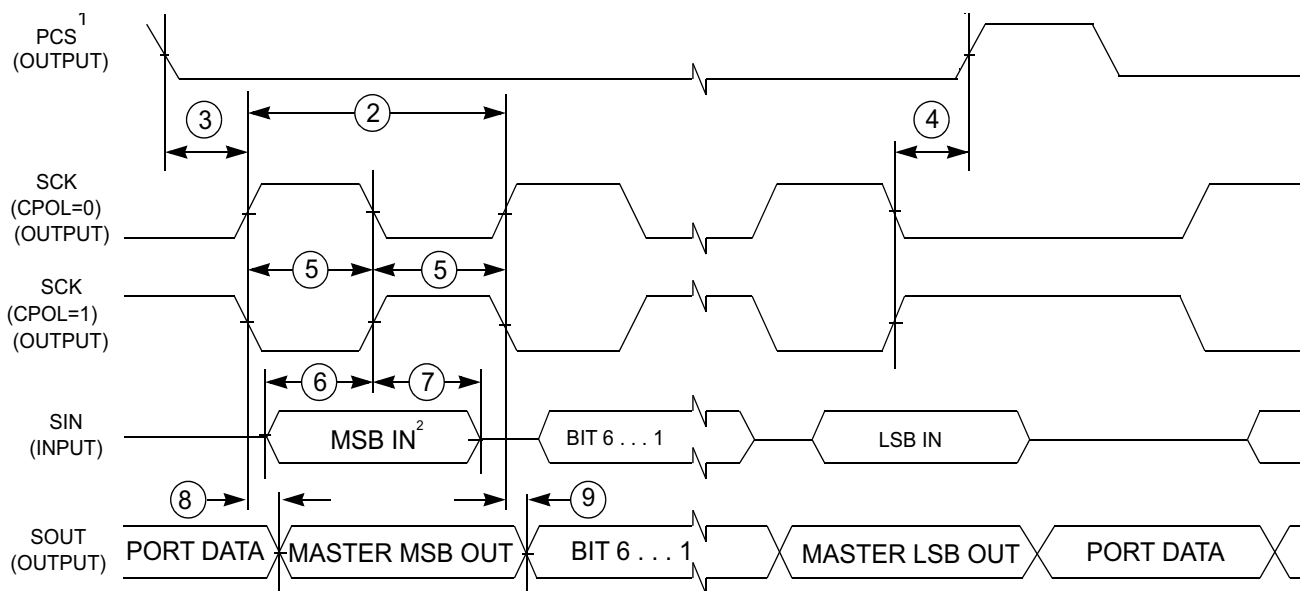
<sup>2</sup>  $t_{periph} = 1000 / f_{periph}$



1. If configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 35. LPSPI Master mode timing (CPHA = 0)**



1. If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 36. LPSPI Master mode timing (CPHA = 1)**

**Table 82. LPSPI Slave mode timing**

| Number | Symbol     | Description                  | Min.                  | Max.             | Units        | Note |
|--------|------------|------------------------------|-----------------------|------------------|--------------|------|
| 1      | $f_{SCK}$  | Frequency of operation       | 0                     | $f_{periph} / 2$ | MHz          | 1    |
| 2      | $t_{SCK}$  | SCK period                   | $2 \times t_{periph}$ | —                | ns           | 2    |
| 3      | $t_{Lead}$ | Enable lead time             | 1                     | —                | $t_{periph}$ | —    |
| 4      | $t_{Lag}$  | Enable lag time              | 1                     | —                | $t_{periph}$ | —    |
| 5      | $t_{WSCK}$ | Clock (SCK) high or low time | $t_{SCK} / 2 - 5$     | —                | ns           | —    |
| 6      | $t_{SU}$   | Data setup time (inputs)     | 2.7                   | —                | ns           | —    |
| 7      | $t_{HI}$   | Data hold time (inputs)      | 3.8                   | —                | ns           | —    |
| 8      | $t_a$      | Slave access time            | —                     | $t_{periph}$     | ns           | 3    |
| 9      | $t_{dis}$  | Slave MISO disable time      | —                     | $t_{periph}$     | ns           | 4    |
| 10     | $t_V$      | Data valid (after SCK edge)  | —                     | 14.5             | ns           | —    |
| 11     | $t_{HO}$   | Data hold time (outputs)     | 0                     | —                | ns           | —    |

<sup>1</sup> Absolute maximum frequency of operation ( $f_{op}$ ) is 30 MHz. The clock driver in the LPSPI module for  $f_{periph}$  must be guaranteed this limit is not exceeded.

<sup>2</sup>  $t_{periph} = 1000 / f_{periph}$

<sup>3</sup> Time to data active from high-impedance state

<sup>4</sup> Hold time to high-impedance state

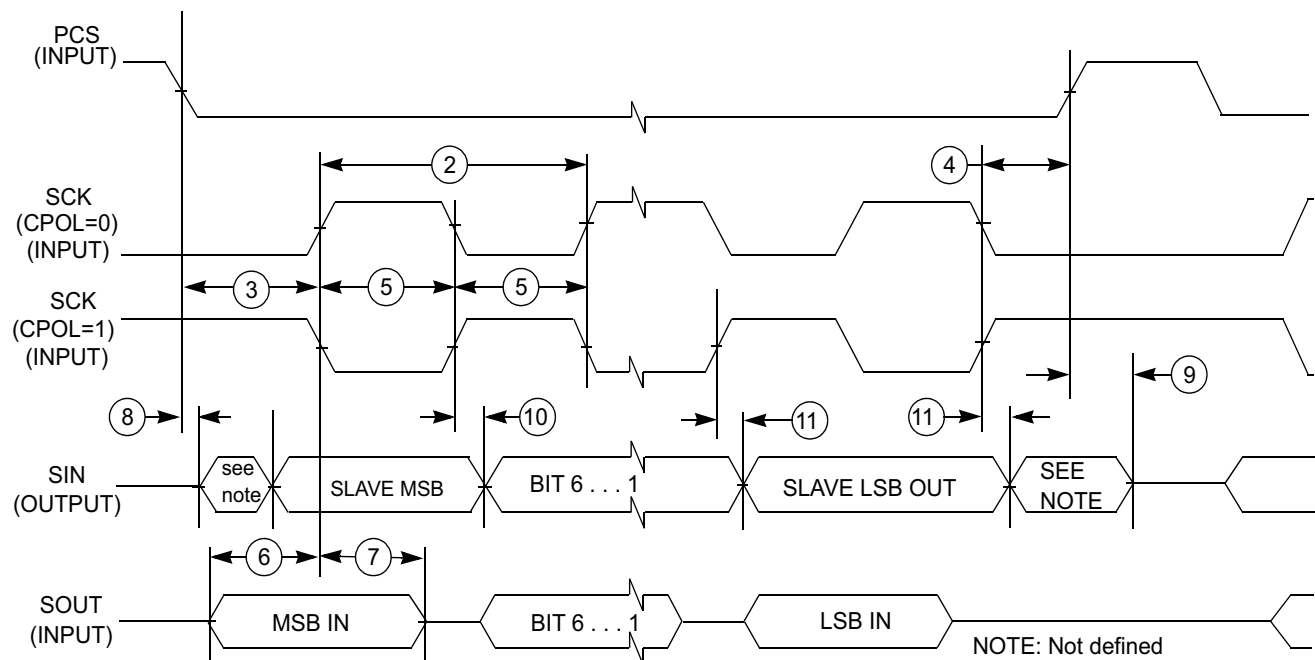


Figure 37. LPSPI Slave mode timing (CPHA = 0)

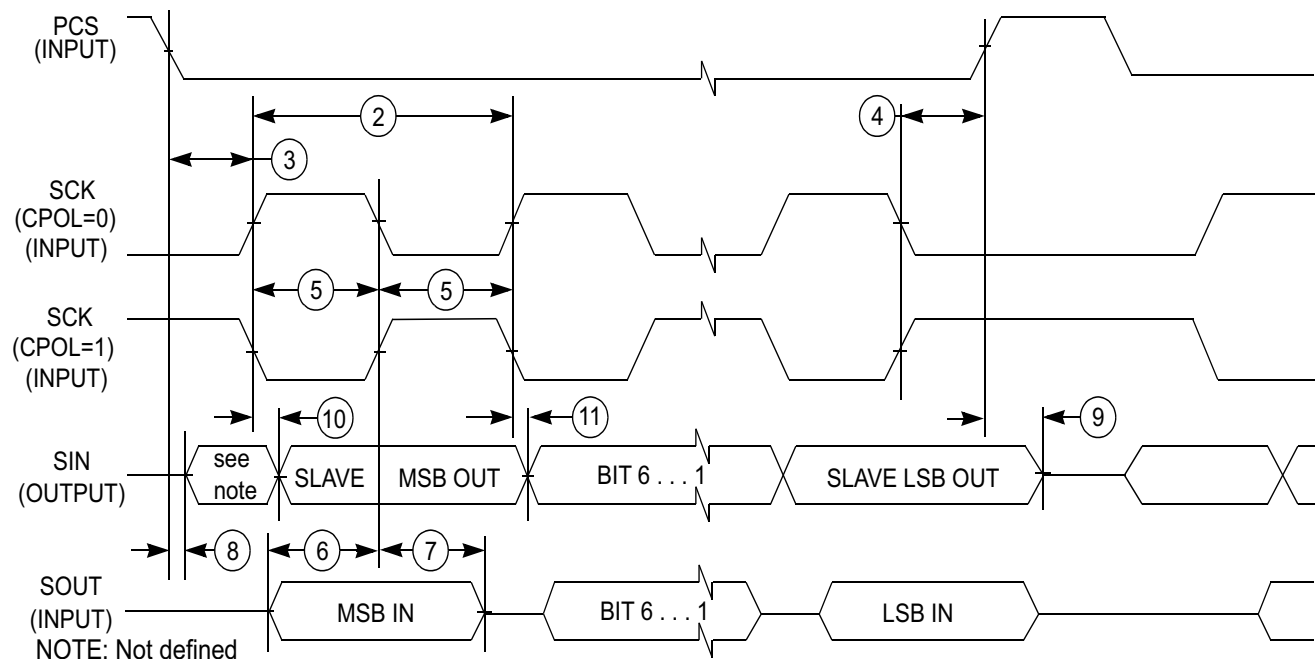


Figure 38. LPSPI Slave mode timing (CPHA = 1)

## 4.9.2 LPI2C module timing parameters

This section describes the timing parameters of the LPI2C module.

**Table 83. LPI2C module timing parameters**

| Symbol    | Description         |                           | Min | Max  | Unit | Notes |
|-----------|---------------------|---------------------------|-----|------|------|-------|
| $f_{SCL}$ | SCL clock frequency | Standard mode (Sm)        | 0   | 100  | kHz  | 1     |
|           |                     | Fast mode (Fm)            | 0   | 400  |      |       |
|           |                     | Fast mode Plus (Fm+)      | 0   | 1000 |      |       |
|           |                     | High speed mode (Hs-mode) | 0   | 3400 |      |       |
|           |                     | Ultra Fast mode (UFm)     | 0   | 5000 |      |       |

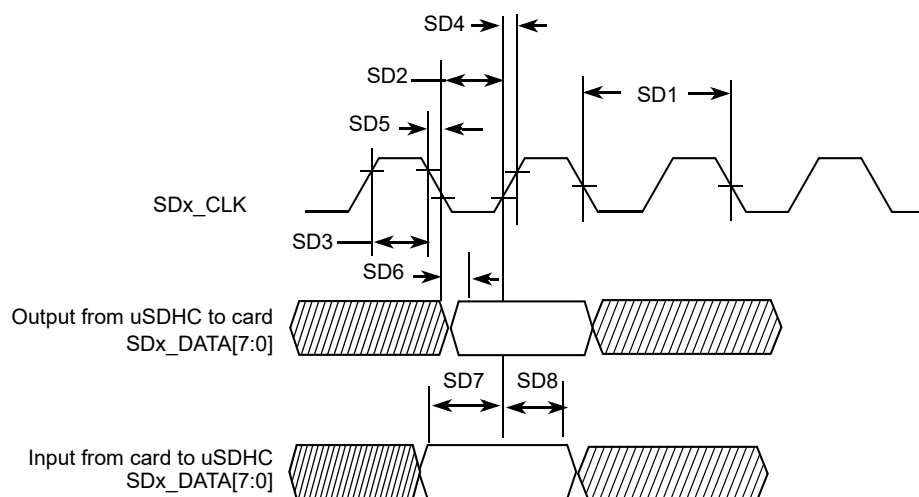
<sup>1</sup> Hs-mode and Ultra Fast mode are supported in slave mode.

## 4.9.3 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD3.0 (Single Data Rate) timing and eMMC5.0 (up to 200 MHz) timing.

### 4.9.3.1 SD3.0/eMMC4.3 (Single Data Rate) specifications

Figure 39 depicts the timing of SD3.0/eMMC4.3, and Table 84 lists the SD/eMMC4.3 timing characteristics.



**Figure 39. SD/eMMC4.3 timing**

Table 84. SD/eMMC4.3 interface timing specification

| ID                                                                   | Parameter                                       | Symbols    | Min  | Max   | Unit |
|----------------------------------------------------------------------|-------------------------------------------------|------------|------|-------|------|
| <b>Card Input Clock</b>                                              |                                                 |            |      |       |      |
| SD1                                                                  | Clock Frequency (Low Speed)                     | $f_{PP}^1$ | 0    | 400   | kHz  |
|                                                                      | Clock Frequency (SD/SDIO Full Speed/High Speed) | $f_{PP}^2$ | 0    | 25/50 | MHz  |
|                                                                      | Clock Frequency (MMC Full Speed/High Speed)     | $f_{PP}^3$ | 0    | 20/52 | MHz  |
|                                                                      | Clock Frequency (Identification Mode)           | $f_{OD}$   | 100  | 400   | kHz  |
| SD2                                                                  | Clock Low Time                                  | $t_{WL}$   | 7    | —     | ns   |
| SD3                                                                  | Clock High Time                                 | $t_{WH}$   | 7    | —     | ns   |
| SD4                                                                  | Clock Rise Time                                 | $t_{TLH}$  | —    | 3     | ns   |
| SD5                                                                  | Clock Fall Time                                 | $t_{THL}$  | —    | 3     | ns   |
| <b>uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)</b> |                                                 |            |      |       |      |
| SD6                                                                  | uSDHC Output Delay                              | $t_{OD}$   | -6.6 | 3.6   | ns   |
| <b>uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)</b> |                                                 |            |      |       |      |
| SD7                                                                  | uSDHC Input Setup Time                          | $t_{ISU}$  | 2.5  | —     | ns   |
| SD8                                                                  | uSDHC Input Hold Time <sup>4</sup>              | $t_{IH}$   | 1.5  | —     | ns   |

<sup>1</sup> In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

<sup>2</sup> In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

<sup>3</sup> In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

<sup>4</sup> To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

#### 4.9.3.2 eMMC4.4/4.41/SD3.0 (Dual Data Rate) AC timing

Figure 40 depicts the timing of eMMC4.4/4.41/SD3.0. Table 85 lists the eMMC4.4/4.41/SD3.0 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

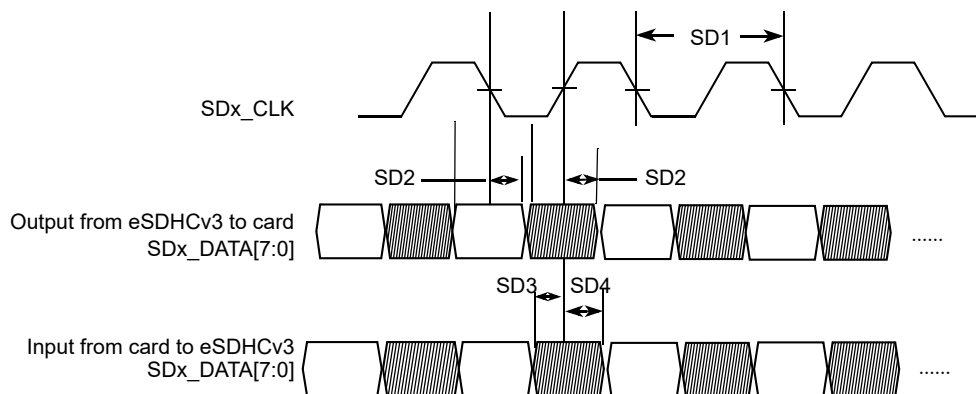


Figure 40. eMMC4.4/4.41/SD3.0 timing

Table 85. eMMC4.4/4.41/SD3.0 interface timing specification

| ID                                                              | Parameter                          | Symbols   | Min | Max | Unit |
|-----------------------------------------------------------------|------------------------------------|-----------|-----|-----|------|
| Card Input Clock                                                |                                    |           |     |     |      |
| SD1                                                             | Clock Frequency (eMMC4.4/4.41 DDR) | $f_{PP}$  | 0   | 52  | MHz  |
| SD1                                                             | Clock Frequency (SD3.0 DDR)        | $f_{PP}$  | 0   | 50  | MHz  |
| uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK) |                                    |           |     |     |      |
| SD2                                                             | uSDHC Output Delay                 | $t_{OD}$  | 2.8 | 6.8 | ns   |
| uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK) |                                    |           |     |     |      |
| SD3                                                             | uSDHC Input Setup Time             | $t_{ISU}$ | 2.4 | —   | ns   |
| SD4                                                             | uSDHC Input Hold Time              | $t_{IH}$  | 1.2 | —   | ns   |

#### 4.9.3.3 SDR50/SDR104 AC timing

Figure 41 depicts the timing of SDR50/SDR104, and Table 86 lists the SDR50/SDR104 timing characteristics.

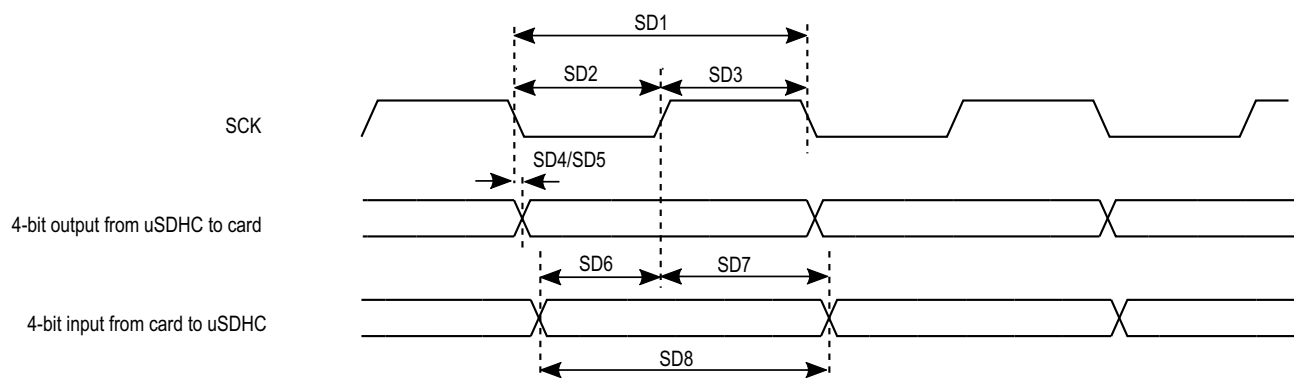


Figure 41. SDR50/SDR104 timing

Table 86. SDR50/SDR104 interface timing specification

| ID                                                                                         | Parameter               | Symbols   | Min                   | Max                   | Unit |
|--------------------------------------------------------------------------------------------|-------------------------|-----------|-----------------------|-----------------------|------|
| <b>Card Input Clock</b>                                                                    |                         |           |                       |                       |      |
| SD1                                                                                        | Clock Frequency Period  | $t_{CLK}$ | 5.0                   | —                     | ns   |
| SD2                                                                                        | Clock Low Time          | $t_{CL}$  | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns   |
| SD3                                                                                        | Clock High Time         | $t_{CH}$  | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns   |
| <b>uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)</b>              |                         |           |                       |                       |      |
| SD4                                                                                        | uSDHC Output Delay      | $t_{OD}$  | −3                    | 1                     | ns   |
| <b>uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)</b>             |                         |           |                       |                       |      |
| SD5                                                                                        | uSDHC Output Delay      | $t_{OD}$  | −1.6                  | 1                     | ns   |
| <b>uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)</b>              |                         |           |                       |                       |      |
| SD6                                                                                        | uSDHC Input Setup Time  | $t_{ISU}$ | 2.5                   | —                     | ns   |
| SD7                                                                                        | uSDHC Input Hold Time   | $t_{IH}$  | 1.5                   | —                     | ns   |
| <b>uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)<sup>1</sup></b> |                         |           |                       |                       |      |
| SD8                                                                                        | Card Output Data Window | $t_{ODW}$ | $0.5 \times t_{CLK}$  | —                     | ns   |

<sup>1</sup>Data window in SDR104 mode is variable.

#### 4.9.3.4 HS200 mode timing

Figure 42 depicts the timing of HS200 mode, and Table 87 lists the HS200 timing characteristics.

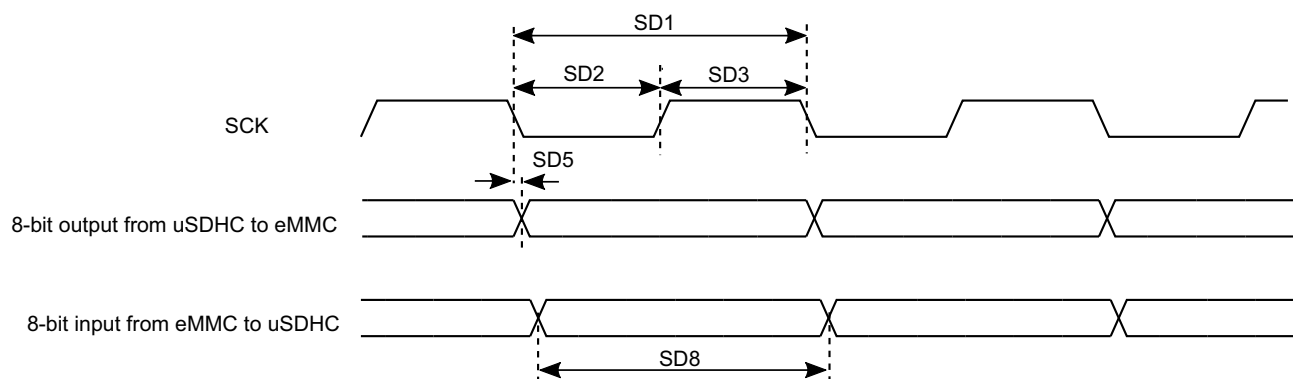


Figure 42. HS200 mode timing

**Table 87. HS200 interface timing specification**

| ID                                                                                        | Parameter               | Symbols   | Min                   | Max                   | Unit |
|-------------------------------------------------------------------------------------------|-------------------------|-----------|-----------------------|-----------------------|------|
| <b>Card Input Clock</b>                                                                   |                         |           |                       |                       |      |
| SD1                                                                                       | Clock Frequency Period  | $t_{CLK}$ | 5.0                   | —                     | ns   |
| SD2                                                                                       | Clock Low Time          | $t_{CL}$  | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns   |
| SD3                                                                                       | Clock High Time         | $t_{CH}$  | $0.46 \times t_{CLK}$ | $0.54 \times t_{CLK}$ | ns   |
| <b>uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)</b>             |                         |           |                       |                       |      |
| SD5                                                                                       | uSDHC Output Delay      | $t_{OD}$  | -1.6                  | 0.74                  | ns   |
| <b>uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)<sup>1</sup></b> |                         |           |                       |                       |      |
| SD8                                                                                       | Card Output Data Window | $t_{ODW}$ | $0.5 \times t_{CLK}$  | —                     | ns   |

<sup>1</sup>HS200 is for 8 bits while SDR104 is for 4 bits.

#### 4.9.3.5 HS400 specifications - eMMC 5.0 only

Be aware that only data are sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for HS200 mode. Check SD5 and SD8 parameters in the HS200 interface timing specifications table for CMD input/output timing of HS400 mode.

Table 87 lists the HS400 timing characteristics.

**Table 88. HS400 interface timing specification**

| Symbol                                                                     | Description                          | Min               | Max               | Unit |
|----------------------------------------------------------------------------|--------------------------------------|-------------------|-------------------|------|
|                                                                            | Operating voltage                    | 1.71              | 1.95              | V    |
| <b>Card input clock</b>                                                    |                                      |                   |                   |      |
|                                                                            | Clock frequency                      | 0                 | 200               | MHz  |
| SD1                                                                        | Clock period                         | 5.0               | —                 | ns   |
| SD2                                                                        | Clock Low time                       | $0.46 \times SD1$ | $0.54 \times SD1$ | ns   |
| SD3                                                                        | Clock High time                      | $0.46 \times SD1$ | $0.54 \times SD1$ | ns   |
| <b>SDHC output / card Inputs SDHC_CMD, SDHC_Dn (reference to SDHC_CLK)</b> |                                      |                   |                   |      |
| SD4                                                                        | Output skew from data to edge of SCK | 0.45              | —                 | ns   |
| SD5                                                                        | Output skew from edge of SCK to data | 0.45              | —                 | ns   |
| <b>SDHC input / card outputs (reference to strobe)</b>                     |                                      |                   |                   |      |
| SD6                                                                        | SDHC input skew                      | —                 | 0.45              | ns   |
| SD7                                                                        | SDHC hold skew                       | —                 | 0.45              | ns   |

Figure 42 depicts the timing of HS400.

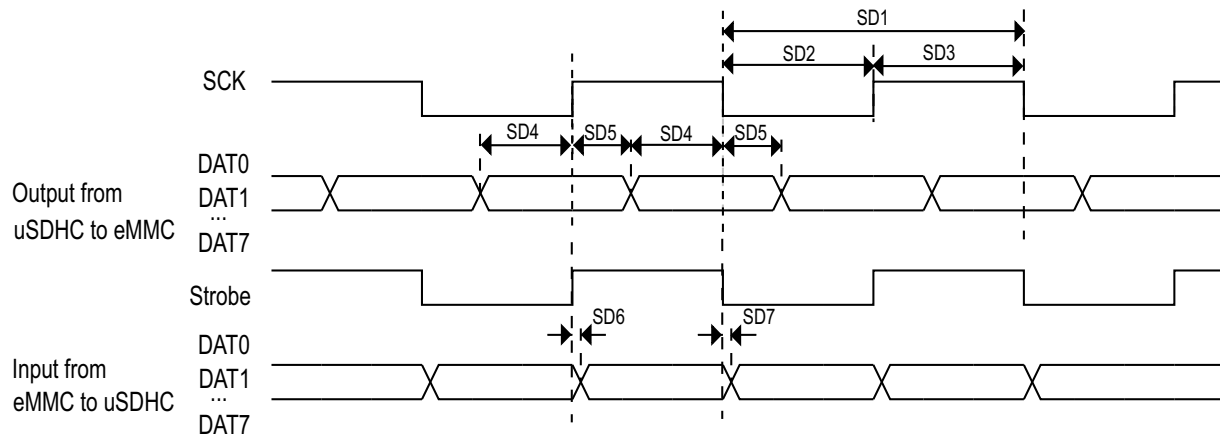


Figure 43. HS400 timing

#### 4.9.3.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.3 and eMMC4.4/4.41 modes is 3.3 V. Signaling level of SDR104/SDR50/HS200/HS400 mode is 1.8 V.

### 4.9.4 Ethernet controller (ENET) AC electrical specifications

#### 4.9.4.1 ENET MII mode timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

##### 4.9.4.1.1 MII receive signal timing (ENET\_RX\_DATA3,2,1,0, ENET\_RX\_EN, ENET\_RX\_ER, and ENET\_RX\_CLK)

The receiver functions correctly up to an ENET\_RX\_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET\_RX\_CLK frequency.

Figure 44 shows MII receive signal timings. Table 89 describes the timing parameters (M1–M4) shown in the figure.

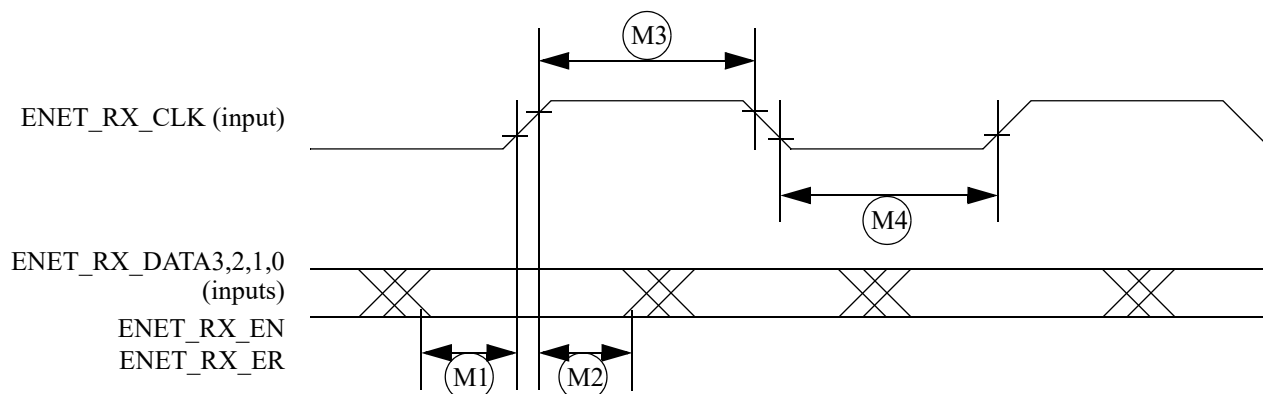


Figure 44. MII receive signal timing diagram

Table 89. MII receive signal timing

| ID | Characteristic <sup>1</sup>                                      | Min. | Max. | Unit               |
|----|------------------------------------------------------------------|------|------|--------------------|
| M1 | ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup | 5    | —    | ns                 |
| M2 | ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold  | 5    | —    | ns                 |
| M3 | ENET_RX_CLK pulse width high                                     | 35%  | 65%  | ENET_RX_CLK period |
| M4 | ENET_RX_CLK pulse width low                                      | 35%  | 65%  | ENET_RX_CLK period |

<sup>1</sup> ENET\_RX\_EN, ENET\_RX\_CLK, and ENET0\_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

#### 4.9.4.1.2 MII transmit signal timing (ENET\_TX\_DATA3,2,1,0, ENET\_TX\_EN, ENET\_TX\_ER, and ENET\_TX\_CLK)

The transmitter functions correctly up to an ENET\_TX\_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET\_TX\_CLK frequency.

## Electrical characteristics

Figure 45 shows MII transmit signal timings. Table 90 describes the timing parameters (M5–M8) shown in the figure.

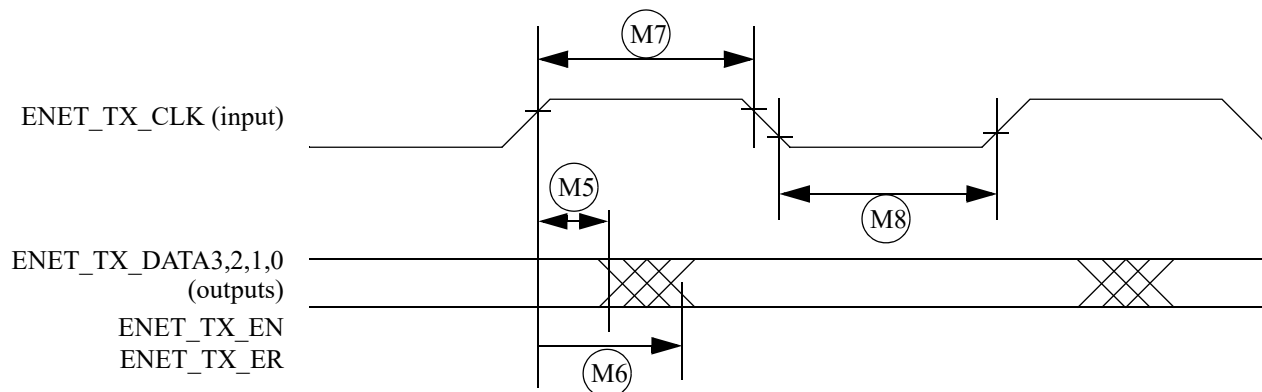


Figure 45. MII transmit signal timing diagram

Table 90. MII transmit signal timing

| ID | Characteristic <sup>1</sup>                                        | Min. | Max. | Unit               |
|----|--------------------------------------------------------------------|------|------|--------------------|
| M5 | ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid | 5    | —    | ns                 |
| M6 | ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid   | —    | 20   | ns                 |
| M7 | ENET_TX_CLK pulse width high                                       | 35%  | 65%  | ENET_TX_CLK period |
| M8 | ENET_TX_CLK pulse width low                                        | 35%  | 65%  | ENET_TX_CLK period |

<sup>1</sup> ENET\_TX\_EN, ENET\_TX\_CLK, and ENET0\_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

### 4.9.4.1.3 MII asynchronous inputs signal timing (ENET\_CRS and ENET\_COL)

Figure 46 shows MII asynchronous input timings. Table 91 describes the timing parameter (M9) shown in the figure.

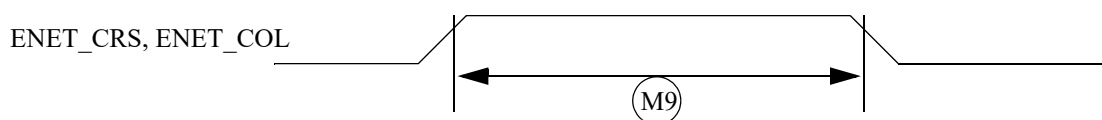


Figure 46. MII asynchronous inputs timing diagram

Table 91. MII asynchronous inputs signal timing

| ID              | Characteristic                           | Min. | Max. | Unit               |
|-----------------|------------------------------------------|------|------|--------------------|
| M9 <sup>1</sup> | ENET_CRS to ENET_COL minimum pulse width | 1.5  | —    | ENET_TX_CLK period |

<sup>1</sup> ENET\_COL has the same timing in 10-Mbit 7-wire interface mode.

#### 4.9.4.1.4 MII serial management channel timing (ENET\_MDIO and ENET\_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 47 shows MII asynchronous input timings. Table 92 describes the timing parameters (M10–M15) shown in the figure.

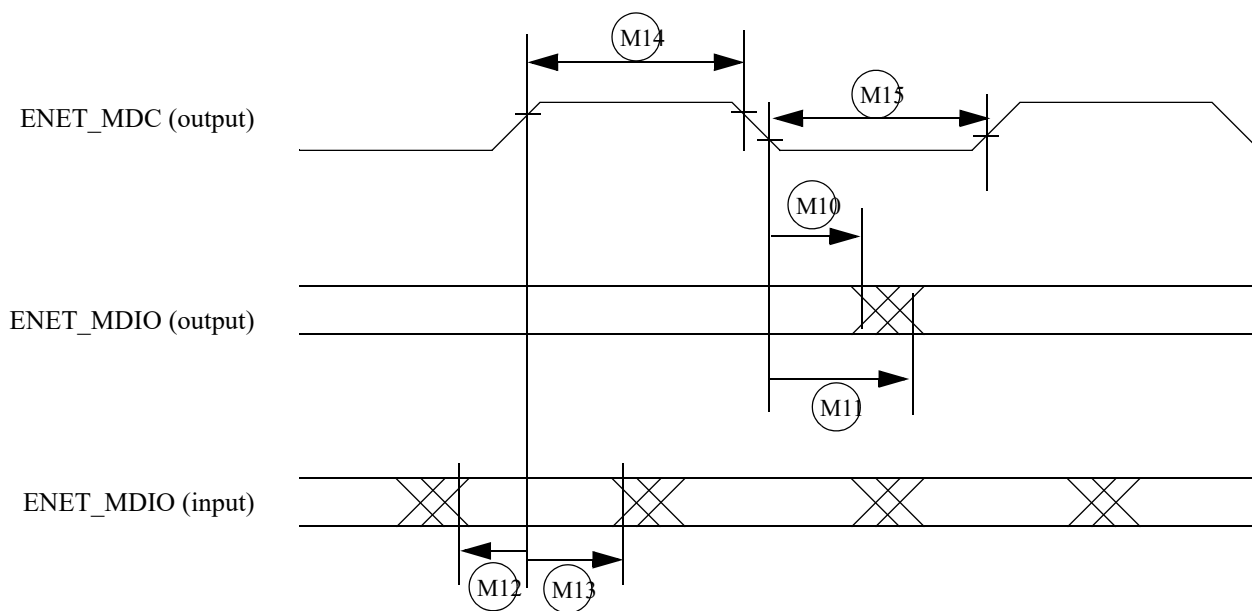


Figure 47. MII serial management channel timing diagram

Table 92. MII serial management channel timing

| ID  | Characteristic                                                             | Min. | Max. | Unit            |
|-----|----------------------------------------------------------------------------|------|------|-----------------|
| M10 | ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay) | 0    | —    | ns              |
| M11 | ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)   | —    | 5    | ns              |
| M12 | ENET_MDIO (input) to ENET_MDC rising edge setup                            | 18   | —    | ns              |
| M13 | ENET_MDIO (input) to ENET_MDC rising edge hold                             | 0    | —    | ns              |
| M14 | ENET_MDC pulse width high                                                  | 40%  | 60%  | ENET_MDC period |
| M15 | ENET_MDC pulse width low                                                   | 40%  | 60%  | ENET_MDC period |

#### 4.9.4.2 RMII mode timing

In RMII mode, ENET\_CLK is used as the REF\_CLK, which is a 50 MHz  $\pm$  50 ppm continuous reference clock.

Figure 48 shows RMII mode timings. Table 93 describes the timing parameters (M16–M21) shown in the figure.

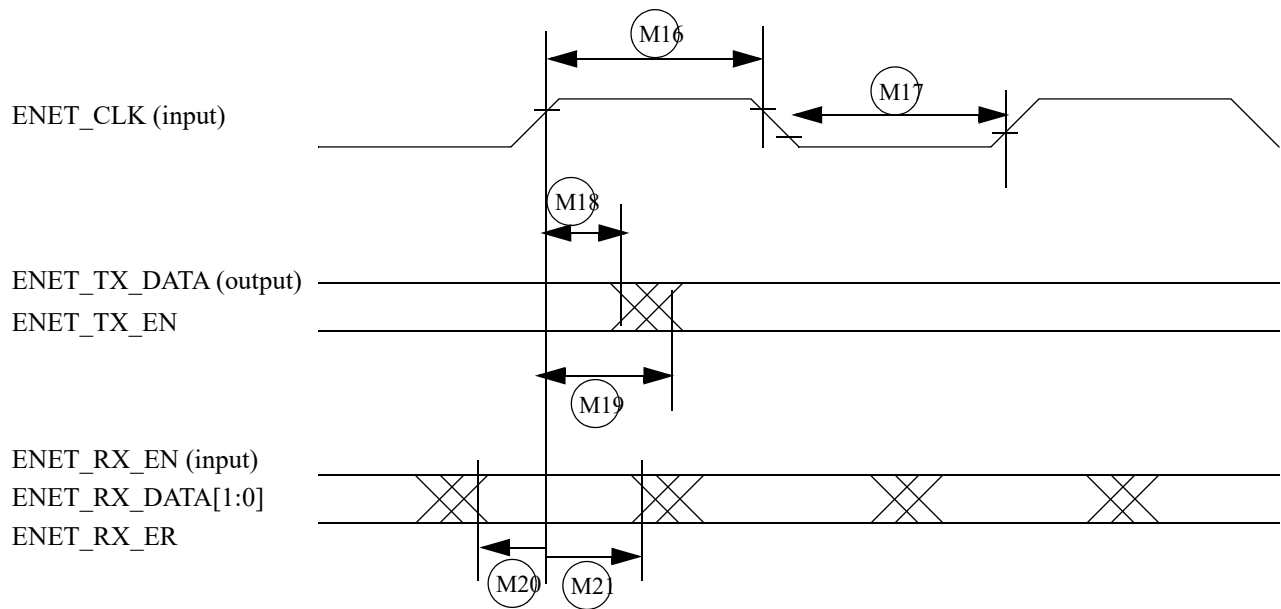


Figure 48. RMII mode signal timing diagram

Table 93. RMII signal timing

| ID  | Characteristic                                                          | Min. | Max. | Unit            |
|-----|-------------------------------------------------------------------------|------|------|-----------------|
| M16 | ENET_CLK pulse width high                                               | 35%  | 65%  | ENET_CLK period |
| M17 | ENET_CLK pulse width low                                                | 35%  | 65%  | ENET_CLK period |
| M18 | ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA invalid                        | 4    | —    | ns              |
| M19 | ENET_CLK to ENET0_TXD[1:0], ENET_TX_DATA valid                          | —    | 13   | ns              |
| M20 | ENET_RX_DATA[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup | 2    | —    | ns              |
| M21 | ENET_CLK to ENET_RX_DATA[1:0], ENET_RX_EN, ENET_RX_ER hold              | 2    | —    | ns              |

#### 4.9.4.3 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 94. RGMII signal switching specifications<sup>1</sup>

| Symbol        | Description                              | Min. | Max. | Unit |
|---------------|------------------------------------------|------|------|------|
| $T_{cyc}^2$   | Clock cycle duration                     | 7.2  | 8.8  | ns   |
| $T_{skewT}^3$ | Data to clock output skew at transmitter | -500 | 500  | ps   |

Table 94. RGMII signal switching specifications<sup>1</sup> (continued)

| Symbol               | Description                          | Min. | Max. | Unit |
|----------------------|--------------------------------------|------|------|------|
| $T_{\text{skewR}}^3$ | Data to clock input skew at receiver | 1    | 2.6  | ns   |
| Duty_G <sup>4</sup>  | Duty cycle for Gigabit               | 45   | 85   | %    |
| Duty_T <sup>4</sup>  | Duty cycle for 10/100T               | 40   | 90   | %    |
| Tr/Tf                | Rise/fall time (20–80%)              | —    | 0.98 | ns   |

<sup>1</sup> The timings assume the following configuration:

DDR\_SEL = (11)b

DSE (drive-strength) = (111)b

<sup>2</sup> For 10 Mbps and 100 Mbps,  $T_{\text{cyc}}$  will scale to 400 ns  $\pm$  40 ns and 40 ns  $\pm$  4 ns respectively.

<sup>3</sup> For all versions of RGMII prior to 2.0; this implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

<sup>4</sup> Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three  $T_{\text{cyc}}$  of the lowest speed transitioned between.

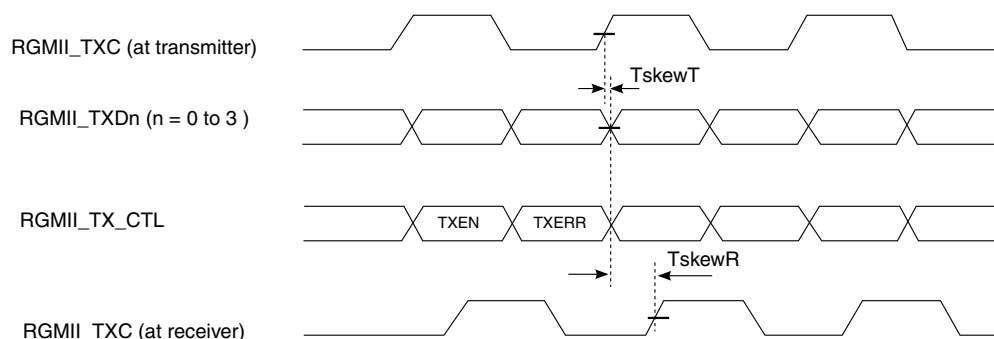


Figure 49. RGMII transmit signal timing diagram

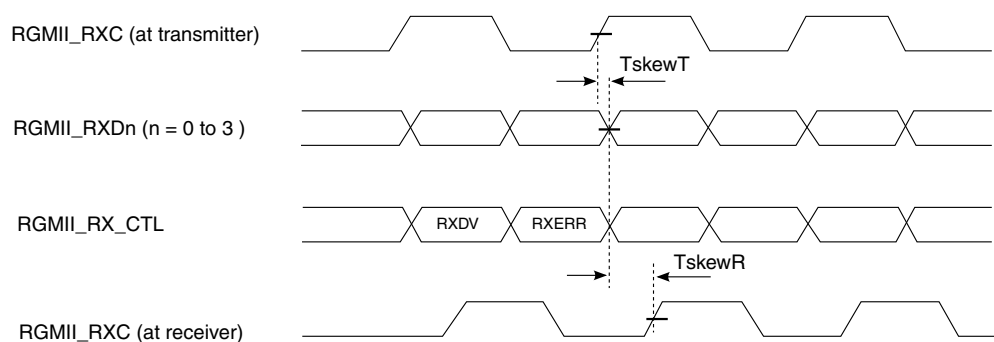


Figure 50. RGMII receive signal timing diagram

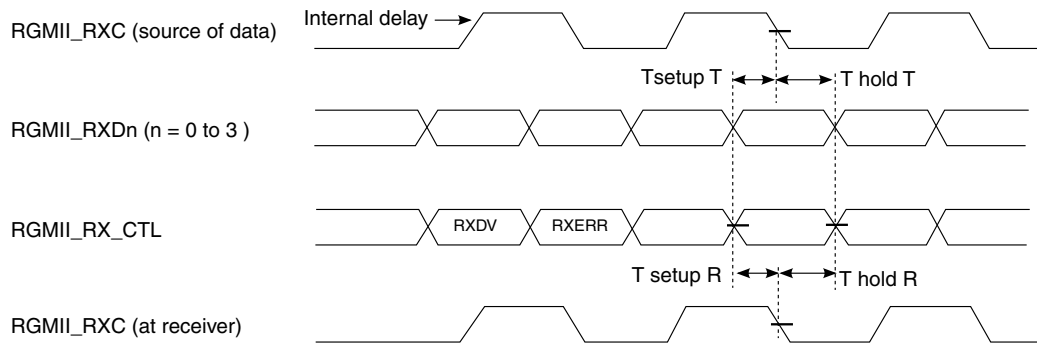


Figure 51. RGMII receive signal timing diagram with internal delay

### 4.9.5 Controller Area Network (CAN) AC electrical specifications

The Controller Area Network (CAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor has three CAN modules available. Tx and Rx ports are multiplexed with other I/O pins. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named CAN\_TX and CAN\_RX, respectively.

Please refer to [Section 4.3.2.1, General purpose I/O \(GPIO\) AC parameters](#).

### 4.9.6 LPUART electrical specifications

Please refer to [Section 4.3.2.1, General purpose I/O \(GPIO\) AC parameters](#).

### 4.9.7 USB PHY parameters

This section describes the USB-OTG PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG with the following amendments.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE

- Title: USB 2.0 Phase Locked SOFs
- Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only

## 4.10 Timers

This section provides information on timers.

### 4.10.1 Pulse Width Modulator (PWM) characteristics

This section describes the electrical information of the PWM.

**Table 95. PWM timing parameters**

| Parameter           | Symbol | Typ | Max | Unit |
|---------------------|--------|-----|-----|------|
| PWM Clock Frequency | —      | —   | 240 | MHz  |
| Output skew         | —      | —   | 2   | ns   |

### 4.10.2 Quad timer timing

[Table 96](#) lists the quad timer parameters.

Table 96. Quad timer timing

| Characteristic               | Symbo       | Min <sup>1</sup> | Max | Unit | See Figure |
|------------------------------|-------------|------------------|-----|------|------------|
| Timer input period           | $T_{IN}$    | $2T + 6$         | —   | ns   |            |
| Timer input high/low period  | $T_{INHL}$  | $1T + 3$         | —   | ns   |            |
| Timer output period          | $T_{OUT}$   | 33               | —   | ns   |            |
| Timer output high/low period | $T_{OUTHL}$ | 16.7             | —   | ns   |            |

<sup>1</sup> T = clock cycle. For 60 MHz operation, T = 16.7 ns.

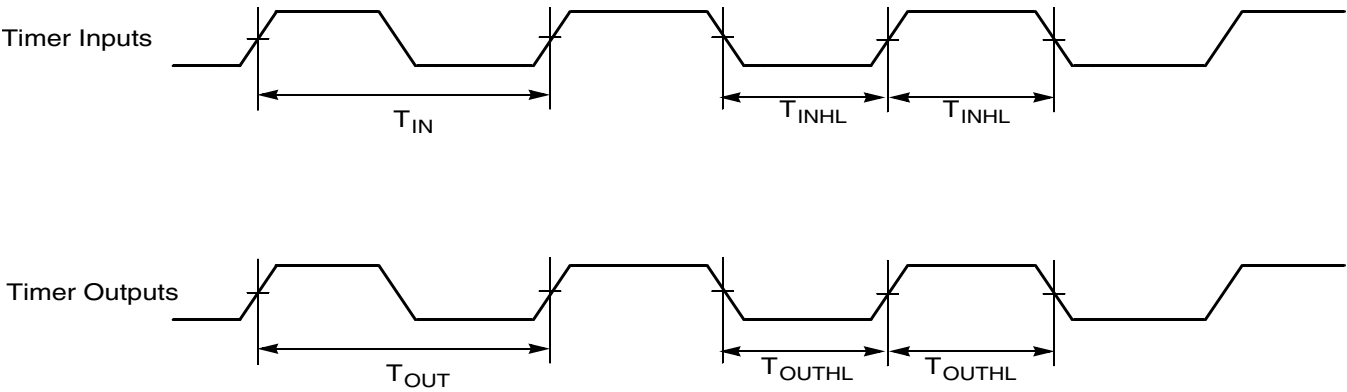


Figure 52. Quad timer timing

## 5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

### 5.1 Boot mode configuration pins

**Table 97** provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT\_FUSE\_SEL fuse. The boot option pins are in effect when BT\_FUSE\_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX RT1160 Fuse Map and the System Boot chapter in *i.MX RT1160 Reference Manual (IMXRT1160RM)*.

**Table 97. Fuses and associated pins used for boot**

| Pad             | Default setting on reset | eFuse name   | Details                                                                                                                                                                                                                                                                                          |
|-----------------|--------------------------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO_LPSR_02    | 35 K pull-down           | BOOT_MODE[0] | Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses. |
| GPIO_LPSR_03    | 35 K pull-down           | BOOT_MODE[1] |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B1_06 | HighZ                    | BT_CFG[0]    |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B1_07 | HighZ                    | BT_CFG[1]    |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B1_08 | HighZ                    | BT_CFG[2]    |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B1_09 | HighZ                    | BT_CFG[3]    |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B1_10 | HighZ                    | BT_CFG[4]    |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B1_11 | HighZ                    | BT_CFG[5]    |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B2_00 | HighZ                    | BT_CFG[6]    |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B2_01 | HighZ                    | BT_CFG[7]    |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B2_02 | HighZ                    | BT_CFG[8]    |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B2_03 | HighZ                    | BT_CFG[9]    |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B2_04 | HighZ                    | BT_CFG[10]   |                                                                                                                                                                                                                                                                                                  |
| GPIO_DISP_B2_05 | HighZ                    | BT_CFG[11]   |                                                                                                                                                                                                                                                                                                  |

### 5.2 Boot device interface allocation

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

**Table 98. Boot through NAND**

| PAD Name       | IO Function  | ALT   | Comments |
|----------------|--------------|-------|----------|
| GPIO_EMC_B1_00 | semc.DATA[0] | ALT 0 | —        |
| GPIO_EMC_B1_01 | semc.DATA[1] | ALT 0 | —        |
| GPIO_EMC_B2_02 | semc.DATA[2] | ALT 0 | —        |

**Table 98. Boot through NAND**

|                |               |       |   |
|----------------|---------------|-------|---|
| GPIO_EMC_B1_03 | semc.DATA[3]  | ALT 0 | — |
| GPIO_EMC_B1_04 | semc.DATA[4]  | ALT 0 | — |
| GPIO_EMC_B1_05 | semc.DATA[5]  | ALT 0 | — |
| GPIO_EMC_B1_06 | semc.DATA[6]  | ALT 0 | — |
| GPIO_EMC_B1_07 | semc.DATA[7]  | ALT 0 | — |
| GPIO_EMC_B1_30 | semc.DATA[8]  | ALT 0 | — |
| GPIO_EMC_B1_31 | semc.DATA[9]  | ALT 0 | — |
| GPIO_EMC_B1_32 | semc.DATA[10] | ALT 0 | — |
| GPIO_EMC_B1_33 | semc.DATA[11] | ALT 0 | — |
| GPIO_EMC_B1_34 | semc.DATA[12] | ALT 0 | — |
| GPIO_EMC_B1_35 | semc.DATA[13] | ALT 0 | — |
| GPIO_EMC_B1_36 | semc.DATA[14] | ALT 0 | — |
| GPIO_EMC_B1_37 | semc.DATA[15] | ALT 0 | — |
| GPIO_EMC_B1_18 | semc.ADDR[9]  | ALT 0 | — |
| GPIO_EMC_B1_19 | semc.ADDR[11] | ALT 0 | — |
| GPIO_EMC_B1_20 | semc.ADDR[12] | ALT 0 | — |
| GPIO_EMC_B1_22 | semc.BA1      | ALT 0 | — |
| GPIO_EMC_B1_41 | semc.CSX[0]   | ALT 0 | — |

**Table 99. Boot through FlexSPI1**

| PAD Name       | IO Function        | Mux Mode | Comments                 |
|----------------|--------------------|----------|--------------------------|
| GPIO_SD_B2_00  | flexspi1.B_DATA[3] | ALT 1    | —                        |
| GPIO_SD_B2_01  | flexspi1.B_DATA[2] | ALT 1    | —                        |
| GPIO_SD_B2_02  | flexspi1.B_DATA[1] | ALT 1    | —                        |
| GPIO_SD_B2_03  | flexspi1.B_DATA[0] | ALT 1    | —                        |
| GPIO_SD_B2_04  | flexspi1.B_SCLK    | ALT 1    | —                        |
| GPIO_SD_B1_05  | flexspi1.B_DQS     | ALT 8    | —                        |
| GPIO_SD_B1_04  | flexspi1.B_SS0_B   | ALT 8    | —                        |
| GPIO_SD_B1_03  | flexspi1.B_SS1_B   | ALT 9    | —                        |
| GPIO_SD_B2_05  | flexspi1.A_DQS     | ALT 1    | —                        |
| GPIO_EMC_B2_18 | flexspi1.A_DQS     | ALT 6    | Secondary option for DQS |
| GPIO_SD_B2_06  | flexspi1.A_SS0_B   | ALT 1    | —                        |
| GPIO_SD_B1_02  | flexspi1.A_SS1_B   | ALT 9    | —                        |

Table 99. Boot through FlexSPI1 (continued)

| PAD Name      | IO Function        | Mux Mode | Comments |
|---------------|--------------------|----------|----------|
| GPIO_SD_B2_07 | flexspi1.A_SCLK    | ALT 1    | —        |
| GPIO_SD_B2_08 | flexspi1.A_DATA[0] | ALT 1    | —        |
| GPIO_SD_B2_09 | flexspi1.A_DATA[1] | ALT 1    | —        |
| GPIO_SD_B2_10 | flexspi1.A_DATA[2] | ALT 1    | —        |
| GPIO_SD_B2_11 | flexspi1.A_DATA[3] | ALT 1    | —        |

Table 100. Boot through FlexSPI2 (QSPI/HyperFLASH)

| PAD Name       | IO Function        | ALT   | Comments |
|----------------|--------------------|-------|----------|
| GPIO_EMC_B1_41 | flexspi2.B_DATA[7] | ALT 4 | —        |
| GPIO_EMC_B2_00 | flexspi2.B_DATA[6] | ALT 4 | —        |
| GPIO_EMC_B2_01 | flexspi2.B_DATA[5] | ALT 4 | —        |
| GPIO_EMC_B2_02 | flexspi2.B_DATA[4] | ALT 4 | —        |
| GPIO_EMC_B2_03 | flexspi2.B_DATA[3] | ALT 4 | —        |
| GPIO_EMC_B2_04 | flexspi2.B_DATA[2] | ALT 4 | —        |
| GPIO_EMC_B2_05 | flexspi2.B_DATA[1] | ALT 4 | —        |
| GPIO_EMC_B2_06 | flexspi2.B_DATA[0] | ALT 4 | —        |
| GPIO_EMC_B2_07 | flexspi2.B_DQS     | ALT 4 | —        |
| GPIO_EMC_B2_08 | flexspi2.B_SS0_B   | ALT 4 | —        |
| GPIO_EMC_B2_09 | flexspi2.B_SCLK    | ALT 4 | —        |
| GPIO_EMC_B2_10 | flexspi2.A_SCLK    | ALT 4 | —        |
| GPIO_EMC_B2_11 | flexspi2.A_SS0_B   | ALT 4 | —        |
| GPIO_EMC_B2_12 | flexspi2.A_DQS     | ALT 4 | —        |
| GPIO_EMC_B2_13 | flexspi2.A_DATA[0] | ALT 4 | —        |
| GPIO_EMC_B2_14 | flexspi2.A_DATA[1] | ALT 4 | —        |
| GPIO_EMC_B2_15 | flexspi2.A_DATA[2] | ALT 4 | —        |
| GPIO_EMC_B2_16 | flexspi2.A_DATA[3] | ALT 4 | —        |
| GPIO_EMC_B2_17 | flexspi2.A_DATA[4] | ALT 4 | —        |
| GPIO_EMC_B2_18 | flexspi2.A_DATA[5] | ALT 4 | —        |
| GPIO_EMC_B2_19 | flexspi2.A_DATA[6] | ALT 4 | —        |
| GPIO_EMC_B2_20 | flexspi2.A_DATA[7] | ALT 4 | —        |

**Table 101. FlexSPI reset**

| PAD Name       | IO Function     | Mux Mode | Comments         |
|----------------|-----------------|----------|------------------|
| GPIO_SD_B1_00  | gpio_mux4.IO[3] | ALT 5    | —                |
| GPIO_EMC_B1_40 | gpio_mux2.IO[8] | ALT 5    | Secondary option |

**Table 102. Boot through SAI1**

| PAD Name   | IO Function     | Mux Mode | Comments |
|------------|-----------------|----------|----------|
| GPIO_AD_17 | sai1.MCLK       | ALT 0    | —        |
| GPIO_AD_18 | sai1.RX_SYNC    | ALT 0    | —        |
| GPIO_AD_19 | sai1.RX_BCLK    | ALT 0    | —        |
| GPIO_AD_20 | sai1.RX_DATA[0] | ALT 0    | —        |
| GPIO_AD_21 | sai1.TX_DATA[0] | ALT 0    | —        |
| GPIO_AD_22 | sai1.TX_BCLK    | ALT 0    | —        |
| GPIO_AD_23 | sai1.TX_SYNC    | ALT 0    | —        |

**Table 103. Boot through SD1**

| PAD Name      | IO Function    | Mux Mode | Comments |
|---------------|----------------|----------|----------|
| GPIO_AD_32    | usdhc1.CD_B    | ALT 4    | —        |
| GPIO_AD_33    | usdhc1.WP      | ALT 4    | —        |
| GPIO_AD_34    | usdhc1.VSELECT | ALT 4    | —        |
| GPIO_AD_35    | usdhc1.RESET_B | ALT 4    | —        |
| GPIO_SD_B1_00 | usdhc1.CMD     | ALT 0    | —        |
| GPIO_SD_B1_01 | usdhc1.CLK     | ALT 0    | —        |
| GPIO_SD_B1_02 | usdhc1.DATA0   | ALT 0    | —        |
| GPIO_SD_B1_03 | usdhc1.DATA1   | ALT 0    | —        |
| GPIO_SD_B1_04 | usdhc1.DATA2   | ALT 0    | —        |
| GPIO_SD_B1_05 | usdhc1.DATA3   | ALT 0    | —        |

**Table 104. Boot through SD2**

| PAD Name      | IO Function    | Mux Mode | Comments |
|---------------|----------------|----------|----------|
| GPIO_AD_26    | usdhc2.CD_B    | ALT 11   | —        |
| GPIO_AD_27    | usdhc2.WP      | ALT 11   | —        |
| GPIO_AD_28    | usdhc2.VSELECT | ALT 11   | —        |
| GPIO_SD_B2_00 | usdhc2.DATA3   | ALT 0    | —        |
| GPIO_SD_B2_01 | usdhc2.DATA2   | ALT 0    | —        |

**Table 104. Boot through SD2 (continued)**

| PAD Name      | IO Function    | Mux Mode | Comments |
|---------------|----------------|----------|----------|
| GPIO_SD_B2_02 | usdhc2.DATA1   | ALT 0    | —        |
| GPIO_SD_B2_03 | usdhc2.DATA0   | ALT 0    | —        |
| GPIO_SD_B2_04 | usdhc2.CLK     | ALT 0    | —        |
| GPIO_SD_B2_05 | usdhc2.CMD     | ALT 0    | —        |
| GPIO_SD_B2_06 | usdhc2.RESET_B | ALT 0    | —        |
| GPIO_SD_B2_08 | usdhc2.DATA4   | ALT 0    | —        |
| GPIO_SD_B2_09 | usdhc2.DATA5   | ALT 0    | —        |
| GPIO_SD_B2_10 | usdhc2.DATA6   | ALT 0    | —        |
| GPIO_SD_B2_11 | usdhc2.DATA7   | ALT 0    | —        |

**Table 105. Boot through SPI1**

| PAD Name   | IO Function | Mux Mode | Comments |
|------------|-------------|----------|----------|
| GPIO_AD_28 | lpspi1.SCK  | ALT 0    | —        |
| GPIO_AD_29 | lpspi1.PCS0 | ALT 0    | —        |
| GPIO_AD_30 | lpspi1.SDO  | ALT 0    | —        |
| GPIO_AD_31 | lpspi1.SDI  | ALT 0    | —        |

**Table 106. Boot through SPI2**

| PAD Name      | IO Function | Mux Mode | Comments |
|---------------|-------------|----------|----------|
| GPIO_SD_B2_07 | lpspi2.SCK  | ALT 6    | —        |
| GPIO_SD_B2_08 | lpspi2.PCS0 | ALT 6    | —        |
| GPIO_SD_B2_09 | lpspi2.SDO  | ALT 6    | —        |
| GPIO_SD_B2_10 | lpspi2.SDI  | ALT 6    | —        |

**Table 107. Boot through SPI3**

| PAD Name        | IO Function | Mux Mode | Comments |
|-----------------|-------------|----------|----------|
| GPIO_DISP_B1_04 | lpspi3.SCK  | ALT 9    | —        |
| GPIO_DISP_B1_07 | lpspi3.PCS0 | ALT 9    | —        |
| GPIO_DISP_B1_06 | lpspi3.SDO  | ALT 9    | —        |
| GPIO_DISP_B1_05 | lpspi3.SDI  | ALT 9    | —        |

**Table 108. Boot through SPI4**

| PAD Name        | IO Function | Mux Mode | Comments |
|-----------------|-------------|----------|----------|
| GPIO_DISP_B2_12 | lpspi4.SCK  | ALT 9    | —        |
| GPIO_DISP_B2_15 | lpspi4.PCS0 | ALT 9    | —        |
| GPIO_DISP_B2_14 | lpspi4.SDO  | ALT 9    | —        |
| GPIO_DISP_B2_13 | lpspi4.SDI  | ALT 9    | —        |

**Table 109. Boot through UART1**

| PAD Name   | IO Function   | Mux Mode | Comments |
|------------|---------------|----------|----------|
| GPIO_AD_24 | lpuart1.TX    | ALT 0    | —        |
| GPIO_AD_25 | lpuart1.RX    | ALT 0    | —        |
| GPIO_AD_26 | lpuart1.CTS_B | ALT 0    | —        |
| GPIO_AD_27 | lpuart1.RTS_B | ALT 0    | —        |

**Table 110. Boot through UART12**

| PAD Name     | IO Function    | Mux Mode | Comments |
|--------------|----------------|----------|----------|
| GPIO_LPSR_04 | lpuart12.RTS_B | ALT 3    | —        |
| GPIO_LPSR_05 | lpuart12.CTS_B | ALT 3    | —        |
| GPIO_LPSR_06 | lpuart12.TX    | ALT 3    | —        |
| GPIO_LPSR_07 | lpuart12.RX    | ALT 3    | —        |

## 6.1 14 x 14 mm package information

### 6.1.1 14 x 14 mm, 0.8 mm pitch, ball matrix

SQT15.34-4



|                                                  |                        |                                |                   |                 |
|--------------------------------------------------|------------------------|--------------------------------|-------------------|-----------------|
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i.MX RT1160 Crossover Processors Data Sheet for Industrial Products, Rev. 0, 04/2021

## 6.1.2 14 x 14 mm supplies contact assignments and functional contact assignments

Table 111 shows the device connection list for ground, sense, and reference contact signals.

**Table 111. 14 x 14 mm supplies contact assignment**

| Supply Rail Name | Ball(s) Position(s) | Remark |
|------------------|---------------------|--------|
| ADC_VREFH        | G16                 | —      |
| DAC_OUT          | H16                 | —      |
| DCDC_ANA         | M7, M8              | —      |
| DCDC_ANA_SENSE   | M6                  | —      |
| DCDC_DIG         | K8, K9, L8          | —      |
| DCDC_DIG_SENSE   | L7                  | —      |
| DCDC_GND         | K6, K7, L6          | —      |
| DCDC_IN          | M5, N5              | —      |
| DCDC_IN_Q        | L5                  | —      |
| DCDC_LN          | T4, U4              | —      |
| DCDC_LP          | T3, U3              | —      |
| DCDC_MODE        | N4                  | —      |
| DCDC_PSWITCH     | P3                  | —      |
| NVCC_DISP1       | D12                 | —      |
| NVCC_DISP2       | E7                  | —      |
| NVCC_EMC1        | F6, F7, G6          | —      |
| NVCC_EMC2        | H6, J6              | —      |
| NVCC_GPIO        | M12                 | —      |
| NVCC_LPSR        | P7                  | —      |
| NVCC_SNVS        | U11                 | —      |
| NVCC_SD1         | D14                 | —      |
| NVCC_SD2         | G13                 | —      |
| VDD_LPSR_ANA     | P12                 | —      |
| VDD_LPSR_DIG     | P11                 | —      |
| VDD_LPSR_IN      | R12                 | —      |
| VDD_MIPI_1P0     | F10                 | —      |
| VDD_MIPI_1P8     | F9                  | —      |
| VDD_USB_1P8      | H12                 | —      |
| VDD_USB_3P3      | G12                 | —      |

**Table 111. 14 x 14 mm supplies contact assignment (continued)**

| Supply Rail Name | Ball(s) Position(s)                                                                                                                                       | Remark |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
| VDD_SOC_IN       | H8, H9, H10, J8, J9, J10, K10                                                                                                                             |        |
| VDD_SNVS_ANA     | U14                                                                                                                                                       | —      |
| VDD_SNVS_DIG     | T14                                                                                                                                                       | —      |
| VDD_SNVS_IN      | U12                                                                                                                                                       | —      |
| VDDA_1P0         | N11                                                                                                                                                       | —      |
| VDDA_1P8_IN      | M11                                                                                                                                                       | —      |
| VDDA_ADC_1P8     | K15                                                                                                                                                       |        |
| VDDA_ADC_3P3     | J13                                                                                                                                                       | —      |
| VSS              | A1, A17, B7, C8, C10, C12, C14, D4, F11, F12, F13, G3, G7, G8, G9, G10, G11, G15, H7, H11, J7, J11, K11, L3, L10, L11, L15, P4, P14, R4, R7, T12, U1, U17 | —      |

Table 112 shows an alpha-sorted list of functional contact assignments of the 14 x 14 mm package.

**Table 112. 14 x 14 mm functional contact assignment**

| Ball name  | 14 x 14 ball | Power group | Ball Types   | Default setting |                  |              |                     |
|------------|--------------|-------------|--------------|-----------------|------------------|--------------|---------------------|
|            |              |             |              | Default modes   | Default function | Input/output | Value               |
| CLK1_N     | T15          | —           | —            | —               |                  | —            | —                   |
| CLK1_P     | U15          | —           | —            | —               |                  | —            | —                   |
| GPIO_AD_00 | N12          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX2_IO31   | Input        | 35K PU <sup>1</sup> |
| GPIO_AD_01 | R14          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO0    | Input        | 35K PU              |
| GPIO_AD_02 | R13          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO1    | Input        | 35K PD <sup>2</sup> |
| GPIO_AD_03 | P15          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO2    | Input        | 35K PD              |
| GPIO_AD_04 | M13          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO3    | Input        | 35K PD              |
| GPIO_AD_05 | P13          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO4    | Input        | 35K PD              |
| GPIO_AD_06 | N13          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO5    | Input        | 35K PD              |
| GPIO_AD_07 | T17          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO6    | Input        | 35K PD              |
| GPIO_AD_08 | R15          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO7    | Input        | 35K PD              |

Table 112. 14 x 14 mm functional contact assignment (continued)

| Ball name  | 14 x 14 ball | Power group | Ball Types   | Default setting |                  |              |        |
|------------|--------------|-------------|--------------|-----------------|------------------|--------------|--------|
|            |              |             |              | Default modes   | Default function | Input/output | Value  |
| GPIO_AD_09 | R16          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO8    | Input        | 35K PD |
| GPIO_AD_10 | R17          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO9    | Input        | 35K PD |
| GPIO_AD_11 | P16          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO10   | Input        | 35K PD |
| GPIO_AD_12 | P17          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO11   | Input        | 35K PD |
| GPIO_AD_13 | L12          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO12   | Input        | 35K PD |
| GPIO_AD_14 | N14          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO13   | Input        | 35K PD |
| GPIO_AD_15 | M14          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO14   | Input        | 35K PD |
| GPIO_AD_16 | N17          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO15   | Input        | 35K PD |
| GPIO_AD_17 | N15          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO16   | Input        | 35K PD |
| GPIO_AD_18 | M16          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO17   | Input        | 35K PU |
| GPIO_AD_19 | L16          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO18   | Input        | 35K PD |
| GPIO_AD_20 | K13          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO19   | Input        | 35K PD |
| GPIO_AD_21 | K14          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO20   | Input        | 35K PD |
| GPIO_AD_22 | K12          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO21   | Input        | 35K PD |
| GPIO_AD_23 | J12          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO22   | Input        | 35K PD |
| GPIO_AD_24 | L13          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO23   | Input        | 35K PD |
| GPIO_AD_25 | M15          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO24   | Input        | 35K PD |
| GPIO_AD_26 | L14          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO25   | Input        | 35K PU |
| GPIO_AD_27 | N16          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO26   | Input        | 35K PU |

Table 112. 14 x 14 mm functional contact assignment (continued)

| Ball name       | 14 x 14 ball | Power group | Ball Types   | Default setting |                  |              |                        |
|-----------------|--------------|-------------|--------------|-----------------|------------------|--------------|------------------------|
|                 |              |             |              | Default modes   | Default function | Input/output | Value                  |
| GPIO_AD_28      | L17          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO27   | Input        | 35K PD                 |
| GPIO_AD_29      | M17          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO28   | Input        | 35K PD                 |
| GPIO_AD_30      | K17          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO29   | Input        | 35K PD                 |
| GPIO_AD_31      | J17          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO30   | Input        | 35K PD                 |
| GPIO_AD_32      | K16          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX3_IO31   | Input        | 35K PD                 |
| GPIO_AD_33      | H17          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX4_IO0    | Input        | 35K PD                 |
| GPIO_AD_34      | J16          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX4_IO1    | Input        | 35K PD                 |
| GPIO_AD_35      | G17          | NVCC_GPIO   | Digital GPIO | ALT 5           | GPIO_MUX4_IO2    | Input        | 35K PU                 |
| GPIO_DISP_B1_00 | E13          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO21   | Input        | 50/35K PD <sup>3</sup> |
| GPIO_DISP_B1_01 | D13          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO22   | Input        | 50/35K PD              |
| GPIO_DISP_B1_02 | D11          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO23   | Input        | 50/35K PD              |
| GPIO_DISP_B1_03 | E11          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO24   | Input        | 50/35K PD              |
| GPIO_DISP_B1_04 | E10          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO25   | Input        | 50/35K PD              |
| GPIO_DISP_B1_05 | C11          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO26   | Input        | 50/35K PD              |
| GPIO_DISP_B1_06 | D10          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO27   | Input        | Highz                  |
| GPIO_DISP_B1_07 | E12          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO28   | Input        | Highz                  |
| GPIO_DISP_B1_08 | A15          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO29   | Input        | Highz                  |
| GPIO_DISP_B1_09 | C13          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO30   | Input        | Highz                  |
| GPIO_DISP_B1_10 | B14          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX4_IO31   | Input        | Highz                  |

Table 112. 14 x 14 mm functional contact assignment (continued)

| Ball name       | 14 x 14 ball | Power group | Ball Types   | Default setting |                  |              |           |
|-----------------|--------------|-------------|--------------|-----------------|------------------|--------------|-----------|
|                 |              |             |              | Default modes   | Default function | Input/output | Value     |
| GPIO_DISP_B1_11 | A14          | NVCC_DISP1  | Digital GPIO | ALT 5           | GPIO_MUX5_IO0    | Input        | Highz     |
| GPIO_DISP_B2_00 | E8           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO1    | Input        | Highz     |
| GPIO_DISP_B2_01 | F8           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO2    | Input        | Highz     |
| GPIO_DISP_B2_02 | E9           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO3    | Input        | Highz     |
| GPIO_DISP_B2_03 | D7           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO4    | Input        | Highz     |
| GPIO_DISP_B2_04 | C7           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO5    | Input        | Highz     |
| GPIO_DISP_B2_05 | C9           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO6    | Input        | Highz     |
| GPIO_DISP_B2_06 | C6           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO7    | Input        | 35K PD    |
| GPIO_DISP_B2_07 | D6           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO8    | Input        | 35K PD    |
| GPIO_DISP_B2_08 | B5           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO9    | Input        | 35K PD    |
| GPIO_DISP_B2_09 | D8           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO10   | Input        | 35K PD    |
| GPIO_DISP_B2_10 | D9           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO11   | Input        | 35K PD    |
| GPIO_DISP_B2_11 | A6           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO12   | Input        | 35K PD    |
| GPIO_DISP_B2_12 | B6           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO13   | Input        | 35K PD    |
| GPIO_DISP_B2_13 | A5           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO14   | Input        | 35K PD    |
| GPIO_DISP_B2_14 | A7           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO15   | Input        | 35K PD    |
| GPIO_DISP_B2_15 | A4           | NVCC_DISP2  | Digital GPIO | ALT 5           | GPIO_MUX5_IO16   | Input        | 35K PU    |
| GPIO_EMCC_B1_00 | F3           | NVCC_EMCC1  | Digital GPIO | ALT 5           | GPIO_MUX1_IO0    | Input        | 50/35K PD |
| GPIO_EMCC_B1_01 | F2           | NVCC_EMCC1  | Digital GPIO | ALT 5           | GPIO_MUX1_IO1    | Input        | 50/35K PD |

Table 112. 14 x 14 mm functional contact assignment (continued)

| Ball name      | 14 x 14 ball | Power group | Ball Types   | Default setting |                  |              |           |
|----------------|--------------|-------------|--------------|-----------------|------------------|--------------|-----------|
|                |              |             |              | Default modes   | Default function | Input/output | Value     |
| GPIO_EMC_B1_02 | G4           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO2    | Input        | 50/35K PD |
| GPIO_EMC_B1_03 | E4           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO3    | Input        | 50/35K PD |
| GPIO_EMC_B1_04 | H5           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO4    | Input        | 50/35K PD |
| GPIO_EMC_B1_05 | F4           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO5    | Input        | 50/35K PD |
| GPIO_EMC_B1_06 | H4           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO6    | Input        | 50/35K PD |
| GPIO_EMC_B1_07 | H3           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO7    | Input        | 50/35K PD |
| GPIO_EMC_B1_08 | F5           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO8    | Input        | 50/35K PD |
| GPIO_EMC_B1_09 | A3           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO9    | Input        | 50/35K PD |
| GPIO_EMC_B1_10 | A2           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO10   | Input        | 50/35K PD |
| GPIO_EMC_B1_11 | C2           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO11   | Input        | 50/35K PD |
| GPIO_EMC_B1_12 | C5           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO12   | Input        | 50/35K PD |
| GPIO_EMC_B1_13 | D5           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO13   | Input        | 50/35K PD |
| GPIO_EMC_B1_14 | B1           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO14   | Input        | 50/35K PD |
| GPIO_EMC_B1_15 | C1           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO15   | Input        | 50/35K PD |
| GPIO_EMC_B1_16 | D3           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO16   | Input        | 50/35K PD |
| GPIO_EMC_B1_17 | B3           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO17   | Input        | 50/35K PD |
| GPIO_EMC_B1_18 | B4           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO18   | Input        | 50/35K PD |
| GPIO_EMC_B1_19 | C4           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO19   | Input        | 50/35K PD |
| GPIO_EMC_B1_20 | C3           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO20   | Input        | 50/35K PD |

Table 112. 14 x 14 mm functional contact assignment (continued)

| Ball name      | 14 x 14 ball | Power group | Ball Types   | Default setting |                  |              |           |
|----------------|--------------|-------------|--------------|-----------------|------------------|--------------|-----------|
|                |              |             |              | Default modes   | Default function | Input/output | Value     |
| GPIO_EMC_B1_21 | G2           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO21   | Input        | 50/35K PD |
| GPIO_EMC_B1_22 | H2           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO22   | Input        | 50/35K PD |
| GPIO_EMC_B1_23 | B2           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO23   | Input        | 50/35K PD |
| GPIO_EMC_B1_24 | J5           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO24   | Input        | 50/35K PD |
| GPIO_EMC_B1_25 | J4           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO25   | Input        | 50/35K PD |
| GPIO_EMC_B1_26 | J3           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO26   | Input        | 50/35K PD |
| GPIO_EMC_B1_27 | G5           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO27   | Input        | 50/35K PD |
| GPIO_EMC_B1_28 | E5           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO28   | Input        | 50/35K PD |
| GPIO_EMC_B1_29 | E6           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO29   | Input        | 50/35K PD |
| GPIO_EMC_B1_30 | E3           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO30   | Input        | 50/35K PD |
| GPIO_EMC_B1_31 | D2           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX1_IO31   | Input        | 50/35K PD |
| GPIO_EMC_B1_32 | D1           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX2_IO0    | Input        | 50/35K PD |
| GPIO_EMC_B1_33 | E2           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX2_IO1    | Input        | 50/35K PD |
| GPIO_EMC_B1_34 | E1           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX2_IO2    | Input        | 50/35K PD |
| GPIO_EMC_B1_35 | F1           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX2_IO3    | Input        | 50/35K PD |
| GPIO_EMC_B1_36 | G1           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX2_IO4    | Input        | 50/35K PD |
| GPIO_EMC_B1_37 | H1           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX2_IO5    | Input        | 50/35K PD |
| GPIO_EMC_B1_38 | J1           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX2_IO6    | Input        | 50/35K PD |
| GPIO_EMC_B1_39 | J2           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX2_IO7    | Input        | 50/35K PD |

Table 112. 14 x 14 mm functional contact assignment (continued)

| Ball name      | 14 x 14 ball | Power group | Ball Types   | Default setting |                  |              |           |
|----------------|--------------|-------------|--------------|-----------------|------------------|--------------|-----------|
|                |              |             |              | Default modes   | Default function | Input/output | Value     |
| GPIO_EMC_B1_40 | K1           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX2_IO8    | Input        | 50/35K PD |
| GPIO_EMC_B1_41 | L1           | NVCC_EMC1   | Digital GPIO | ALT 5           | GPIO_MUX2_IO9    | Input        | 50/35K PD |
| GPIO_EMC_B2_00 | K2           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO10   | Input        | 50/35K PD |
| GPIO_EMC_B2_01 | K4           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO11   | Input        | 50/35K PD |
| GPIO_EMC_B2_02 | K3           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO12   | Input        | 50/35K PD |
| GPIO_EMC_B2_03 | R1           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO13   | Input        | 50/35K PD |
| GPIO_EMC_B2_04 | M1           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO14   | Input        | 50/35K PD |
| GPIO_EMC_B2_05 | N1           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO15   | Input        | 50/35K PD |
| GPIO_EMC_B2_06 | T1           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO16   | Input        | 50/35K PD |
| GPIO_EMC_B2_07 | M3           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO17   | Input        | 50/35K PD |
| GPIO_EMC_B2_08 | P1           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO18   | Input        | 50/35K PU |
| GPIO_EMC_B2_09 | N2           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO19   | Input        | 50/35K PD |
| GPIO_EMC_B2_10 | R2           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO20   | Input        | 50/35K PD |
| GPIO_EMC_B2_11 | L4           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO21   | Input        | 50/35K PU |
| GPIO_EMC_B2_12 | M2           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO22   | Input        | 50/35K PD |
| GPIO_EMC_B2_13 | K5           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO23   | Input        | 50/35K PD |
| GPIO_EMC_B2_14 | M4           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO24   | Input        | 50/35K PD |
| GPIO_EMC_B2_15 | L2           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO25   | Input        | 50/35K PD |
| GPIO_EMC_B2_16 | P2           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO26   | Input        | 50/35K PD |

Table 112. 14 x 14 mm functional contact assignment (continued)

| Ball name      | 14 x 14 ball | Power group | Ball Types   | Default setting |                  |              |           |
|----------------|--------------|-------------|--------------|-----------------|------------------|--------------|-----------|
|                |              |             |              | Default modes   | Default function | Input/output | Value     |
| GPIO_EMC_B2_17 | T2           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO27   | Input        | 50/35K PD |
| GPIO_EMC_B2_18 | N3           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO28   | Input        | 50/35K PD |
| GPIO_EMC_B2_19 | U2           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO29   | Input        | 50/35K PD |
| GPIO_EMC_B2_20 | R3           | NVCC_EMC2   | Digital GPIO | ALT 5           | GPIO_MUX2_IO30   | Input        | 50/35K PD |
| GPIO_LPSR_00   | N6           | NVCC_LPSR   | Digital GPIO | ALT 10          | GPIO12_IO0       | Input        | 35K PD    |
| GPIO_LPSR_01   | R6           | NVCC_LPSR   | Digital GPIO | ALT 10          | GPIO12_IO1       | Input        | 35K PD    |
| GPIO_LPSR_02   | P6           | NVCC_LPSR   | Digital GPIO | ALT 0           | BOOT_MODE0       | Input        | 35K PD    |
| GPIO_LPSR_03   | T7           | NVCC_LPSR   | Digital GPIO | ALT 0           | BOOT_MODE1       | Input        | 35K PD    |
| GPIO_LPSR_04   | N7           | NVCC_LPSR   | Digital GPIO | ALT 10          | GPIO12_IO4       | Input        | 35K PD    |
| GPIO_LPSR_05   | N8           | NVCC_LPSR   | Digital GPIO | ALT 10          | GPIO12_IO5       | Input        | 35K PD    |
| GPIO_LPSR_06   | P8           | NVCC_LPSR   | Digital GPIO | ALT 10          | GPIO12_IO6       | Input        | 35K PD    |
| GPIO_LPSR_07   | R8           | NVCC_LPSR   | Digital GPIO | ALT 10          | GPIO12_IO7       | Input        | 35K PD    |
| GPIO_LPSR_08   | U8           | NVCC_LPSR   | Digital GPIO | ALT 10          | GPIO12_IO8       | Input        | 35K PD    |
| GPIO_LPSR_09   | P5           | NVCC_LPSR   | Digital GPIO | ALT 10          | GPIO12_IO9       | Input        | 35K PD    |
| GPIO_LPSR_10   | R5           | NVCC_LPSR   | Digital GPIO | ALT 0           | JTAG_MUX_TRSTB   | Input        | 35K PU    |
| GPIO_LPSR_11   | T5           | NVCC_LPSR   | Digital GPIO | ALT 0           | JTAG_MUX_TDO     | Input        | Highz     |
| GPIO_LPSR_12   | U5           | NVCC_LPSR   | Digital GPIO | ALT 0           | JTAG_MUX_TDI     | Input        | 35K PU    |
| GPIO_LPSR_13   | U6           | NVCC_LPSR   | Digital GPIO | ALT 0           | JTAG_MUX_MOD     | Input        | 35K PD    |
| GPIO_LPSR_14   | T6           | NVCC_LPSR   | Digital GPIO | ALT 0           | JTAG_MUX_TCK     | Input        | 35K PD    |

Table 112. 14 x 14 mm functional contact assignment (continued)

| Ball name     | 14 x 14 ball | Power group | Ball Types   | Default setting |                  |              |           |
|---------------|--------------|-------------|--------------|-----------------|------------------|--------------|-----------|
|               |              |             |              | Default modes   | Default function | Input/output | Value     |
| GPIO_LPSR_15  | U7           | NVCC_LPSR   | Digital GPIO | ALT 0           | JTAG_MUX_TMS     | Input        | 35K PU    |
| GPIO_SD_B1_00 | B16          | NVCC_SD1    | Digital GPIO | ALT 5           | GPIO_MUX4_IO3    | Input        | 50/35K PU |
| GPIO_SD_B1_01 | D15          | NVCC_SD1    | Digital GPIO | ALT 5           | GPIO_MUX4_IO4    | Input        | 50/35K PD |
| GPIO_SD_B1_02 | C15          | NVCC_SD1    | Digital GPIO | ALT 5           | GPIO_MUX4_IO5    | Input        | 50/35K PU |
| GPIO_SD_B1_03 | B17          | NVCC_SD1    | Digital GPIO | ALT 5           | GPIO_MUX4_IO6    | Input        | 50/35K PU |
| GPIO_SD_B1_04 | B15          | NVCC_SD1    | Digital GPIO | ALT 5           | GPIO_MUX4_IO7    | Input        | 50/35K PU |
| GPIO_SD_B1_05 | A16          | NVCC_SD1    | Digital GPIO | ALT 5           | GPIO_MUX4_IO8    | Input        | 50/35K PD |
| GPIO_SD_B2_00 | J15          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO9    | Input        | 50/35K PD |
| GPIO_SD_B2_01 | J14          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO10   | Input        | 50/35K PD |
| GPIO_SD_B2_02 | H13          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO11   | Input        | 50/35K PD |
| GPIO_SD_B2_03 | E15          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO12   | Input        | 50/35K PD |
| GPIO_SD_B2_04 | F14          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO13   | Input        | 50/35K PU |
| GPIO_SD_B2_05 | E14          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO14   | Input        | 50/35K PU |
| GPIO_SD_B2_06 | F17          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO15   | Input        | 50/35K PU |
| GPIO_SD_B2_07 | G14          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO16   | Input        | 50/35K PD |
| GPIO_SD_B2_08 | F15          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO17   | Input        | 50/35K PD |
| GPIO_SD_B2_09 | H15          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO18   | Input        | 50/35K PD |
| GPIO_SD_B2_10 | H14          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO19   | Input        | 50/35K PD |
| GPIO_SD_B2_11 | F16          | NVCC_SD2    | Digital GPIO | ALT 5           | GPIO_MUX4_IO20   | Input        | 50/35K PD |

Table 112. 14 x 14 mm functional contact assignment (continued)

| Ball name    | 14 x 14 ball | Power group  | Ball Types  | Default setting |                     |              |             |
|--------------|--------------|--------------|-------------|-----------------|---------------------|--------------|-------------|
|              |              |              |             | Default modes   | Default function    | Input/output | Value       |
| GPIO_SNVS_00 | R10          | NVCC_SNVS    | ANALOG GPIO | ALT 5           | GPIO13_IO3          | Input        | PD          |
| GPIO_SNVS_01 | P10          | NVCC_SNVS    | ANALOG GPIO | ALT 5           | GPIO13_IO4          | Input        | PD          |
| GPIO_SNVS_02 | L9           | NVCC_SNVS    | ANALOG GPIO | ALT 5           | GPIO13_IO5          | Input        | PD          |
| GPIO_SNVS_03 | M10          | NVCC_SNVS    | ANALOG GPIO | ALT 5           | GPIO13_IO6          | Input        | PD          |
| GPIO_SNVS_04 | N10          | NVCC_SNVS    | ANALOG GPIO | ALT 5           | GPIO13_IO7          | Input        | PD          |
| GPIO_SNVS_05 | P9           | NVCC_SNVS    | ANALOG GPIO | ALT 5           | GPIO13_IO8          | Input        | PD          |
| GPIO_SNVS_06 | M9           | NVCC_SNVS    | ANALOG GPIO | ALT 5           | GPIO13_IO9          | Input        | PD          |
| GPIO_SNVS_07 | R9           | NVCC_SNVS    | ANALOG GPIO | ALT 5           | GPIO13_IO10         | Input        | PD          |
| GPIO_SNVS_08 | N9           | NVCC_SNVS    | ANALOG GPIO | ALT 5           | GPIO13_IO11         | Input        | PD          |
| GPIO_SNVS_09 | R11          | NVCC_SNVS    | ANALOG GPIO | ALT 5           | GPIO13_IO12         | Input        | PD          |
| MIPI_CSI_CKP | B12          | VDD_MIPI_1P8 | CSI         | —               | —                   | —            | —           |
| MIPI_CSI_CKN | A12          | VDD_MIPI_1P8 | CSI         | —               | —                   | —            | —           |
| MIPI_CSI_DN0 | A11          | VDD_MIPI_1P8 | CSI         | —               | —                   | —            | —           |
| MIPI_CSI_DN1 | A13          | VDD_MIPI_1P8 | CSI         | —               | —                   | —            | —           |
| MIPI_CSI_DP0 | B11          | VDD_MIPI_1P8 | CSI         | —               | —                   | —            | —           |
| MIPI_CSI_DP1 | B13          | VDD_MIPI_1P8 | CSI         | —               | —                   | —            | —           |
| MIPI_DSI_CKP | B9           | VDD_MIPI_1P8 | DSI         | —               | —                   | —            | —           |
| MIPI_DSI_CKN | A9           | VDD_MIPI_1P8 | DSI         | —               | —                   | —            | —           |
| MIPI_DSI_DN0 | A8           | VDD_MIPI_1P8 | DSI         | —               | —                   | —            | —           |
| MIPI_DSI_DN1 | A10          | VDD_MIPI_1P8 | DSI         | —               | —                   | —            | —           |
| MIPI_DSI_DP0 | B8           | VDD_MIPI_1P8 | DSI         | —               | —                   | —            | —           |
| MIPI_DSI_DP1 | B10          | VDD_MIPI_1P8 | DSI         | —               | —                   | —            | —           |
| ONOFF        | U10          | NVCC_SNVS    | ANALOG GPIO | ALT 0           | RESET_B             | Input        | PU          |
| PMIC_ON_REQ  | U9           | NVCC_SNVS    | ANALOG GPIO | ALT 0           | SNVS_LP_PMIC_ON_REQ | Output       | Output high |

Table 112. 14 x 14 mm functional contact assignment (continued)

| Ball name     | 14 x 14 ball | Power group | Ball Types  | Default setting |                    |              |            |
|---------------|--------------|-------------|-------------|-----------------|--------------------|--------------|------------|
|               |              |             |             | Default modes   | Default function   | Input/output | Value      |
| PMIC_STBY_REQ | T9           | NVCC_SNVs   | ANALOG GPIO | ALT 0           | CCM_PMIC_VSTBY_REQ | Output       | Output low |
| POR_B         | T10          | NVCC_SNVs   | ANALOG GPIO | ALT 0           | POR_B              | —            | PU         |
| RTC_XTALI     | T13          | —           | —           | —               | —                  | —            | —          |
| RTC_XTALO     | U13          | —           | —           | —               | —                  | —            | —          |
| TEST_MODE     | T11          | NVCC_SNVs   | ANALOG GPIO | ALT 0           | TEST_MODE          | Input        | PD         |
| USB1_DN       | E16          | —           | —           | —               | —                  | —            | —          |
| USB1_DP       | E17          | —           | —           | —               | —                  | —            | —          |
| USB2_DN       | C16          | —           | —           | —               | —                  | —            | —          |
| USB2_DP       | C17          | —           | —           | —               | —                  | —            | —          |
| USB1_VBUS     | D17          | —           | —           | —               | —                  | —            | —          |
| USB2_VBUS     | D16          | —           | —           | —               | —                  | —            | —          |
| XTALI         | U16          | —           | —           | —               | —                  | —            | —          |
| XTALO         | T16          | —           | —           | —               | —                  | —            | —          |
| WAKEUP        | T8           | NVCC_SNVs   | ANALOG GPIO | ALT 5           | GPIO13_IO0         | Input        | PU         |

<sup>1</sup> Pull-up<sup>2</sup> Pull-down<sup>3</sup> Typical resistance value is 50 k $\Omega$  for 3.3 V and 35 k $\Omega$  for 1.8 V. The range is from 10 k $\Omega$  to 100 k $\Omega$  (3.3 V) and 20 k $\Omega$  to 50 k $\Omega$  (1.8 V).

### 6.1.3 14 x 14 mm, 0.8 mm pitch, ball map

Table 113 shows the 14 x 14 mm, 0.8 mm pitch ball map for the i.MX RT1160.

**Table 113. 14 x 14 mm, 0.8 mm pitch, ball map**

|          | 1                      | 2                      | 3                      | 4                       | 5                       | 6                       | 7                       | 8                       | 9                       | 10                      | 11                      | 12                      | 13                      | 14                      | 15                      | 16                    | 17                    |
|----------|------------------------|------------------------|------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-----------------------|-----------------------|
| <b>A</b> | VSS                    | GPIO_<br>EMC_<br>B1_10 | GPIO_<br>EMC_<br>B1_09 | GPIO_<br>DISP_<br>B2_15 | GPIO_<br>DISP_<br>B2_13 | GPIO_<br>DISP_<br>B2_11 | GPIO_<br>DISP_<br>B2_14 | MIPI_<br>DSI_<br>DN0    | MIPI_<br>DSI_<br>CKN    | MIPI_<br>DSI_<br>DN1    | MIPI_<br>CSI_<br>DN0    | MIPI_<br>CSI_<br>CKN    | MIPI_<br>CSI_<br>DN1    | GPIO_<br>DISP_<br>B1_11 | GPIO_<br>DISP_<br>B1_08 | GPIO_<br>SD_<br>B1_05 | VSS                   |
| <b>B</b> | GPIO_<br>EMC_<br>B1_14 | GPIO_<br>EMC_<br>B1_23 | GPIO_<br>EMC_<br>B1_17 | GPIO_<br>EMC_<br>B1_18  | GPIO_<br>DISP_<br>B2_08 | GPIO_<br>DISP_<br>B2_12 | VSS                     | MIPI_<br>DSI_<br>DP0    | MIPI_<br>DSI_<br>CKP    | MIPI_<br>DSI_<br>DP1    | MIPI_<br>CSI_<br>DP0    | MIPI_<br>CSI_<br>CKP    | MIPI_<br>CSI_<br>DP1    | GPIO_<br>DISP_<br>B1_10 | GPIO_<br>SD_<br>B1_04   | GPIO_<br>SD_<br>B1_00 | GPIO_<br>SD_<br>B1_03 |
| <b>C</b> | GPIO_<br>EMC_<br>B1_15 | GPIO_<br>EMC_<br>B1_11 | GPIO_<br>EMC_<br>B1_20 | GPIO_<br>EMC_<br>B1_19  | GPIO_<br>EMC_<br>B1_12  | GPIO_<br>DISP_<br>B2_06 | GPIO_<br>DISP_<br>B2_04 | VSS                     | GPIO_<br>DISP_<br>B2_05 | VSS                     | GPIO_<br>DISP_<br>B1_05 | VSS                     | GPIO_<br>DISP_<br>B1_09 | VSS                     | GPIO_<br>SD_<br>B1_02   | USB2_<br>DN           | USB2_<br>DP           |
| <b>D</b> | GPIO_<br>EMC_<br>B1_32 | GPIO_<br>EMC_<br>B1_31 | GPIO_<br>EMC_<br>B1_16 | VSS                     | GPIO_<br>EMC_<br>B1_13  | GPIO_<br>DISP_<br>B2_07 | GPIO_<br>DISP_<br>B2_03 | GPIO_<br>DISP_<br>B2_09 | GPIO_<br>DISP_<br>B2_10 | GPIO_<br>DISP_<br>B1_06 | GPIO_<br>DISP_<br>B1_02 | NVCC_<br>DISP1          | GPIO_<br>DISP_<br>B1_01 | NVCC_<br>SD1            | GPIO_<br>SD_<br>B1_01   | USB2_<br>VBUS         | USB1_<br>VBUS         |
| <b>E</b> | GPIO_<br>EMC_<br>B1_34 | GPIO_<br>EMC_<br>B1_33 | GPIO_<br>EMC_<br>B1_30 | GPIO_<br>EMC_<br>B1_03  | GPIO_<br>EMC_<br>B1_28  | GPIO_<br>EMC_<br>B1_29  | NVCC_<br>DISP2          | GPIO_<br>DISP_<br>B2_00 | GPIO_<br>DISP_<br>B2_02 | GPIO_<br>DISP_<br>B1_04 | GPIO_<br>DISP_<br>B1_03 | GPIO_<br>DISP_<br>B1_07 | GPIO_<br>DISP_<br>B1_00 | GPIO_<br>SD_<br>B2_05   | GPIO_<br>SD_<br>B2_03   | USB1_<br>DN           | USB1_<br>DP           |
| <b>F</b> | GPIO_<br>EMC_<br>B1_35 | GPIO_<br>EMC_<br>B1_01 | GPIO_<br>EMC_<br>B1_00 | GPIO_<br>EMC_<br>B1_05  | GPIO_<br>EMC_<br>B1_08  | NVCC_<br>EMC1           | NVCC_<br>EMC1           | GPIO_<br>DISP_<br>B2_01 | VDD_<br>MIPI_<br>1P8    | VDD_M<br>IPI_<br>1P0    | VSS                     | VSS                     | VSS                     | GPIO_<br>SD_<br>B2_04   | GPIO_<br>SD_<br>B2_08   | GPIO_<br>SD_<br>B2_11 | GPIO_<br>SD_<br>B2_06 |
| <b>G</b> | GPIO_<br>EMC_<br>B1_36 | GPIO_<br>EMC_<br>B1_21 | VSS                    | GPIO_<br>EMC_<br>B1_02  | GPIO_<br>EMC_<br>B1_27  | NVCC_<br>EMC1           | VSS                     | VSS                     | VSS                     | VSS                     | VSS                     | VDD_<br>USB_<br>3P3     | NVCC_<br>SD2            | GPIO_<br>SD_<br>B2_07   | VSS                     | ADC_<br>VREFH         | GPIO_<br>AD_35        |
| <b>H</b> | GPIO_<br>EMC_<br>B1_37 | GPIO_<br>EMC_<br>B1_22 | GPIO_<br>EMC_<br>B1_07 | GPIO_<br>EMC_<br>B1_06  | GPIO_<br>EMC_<br>B1_04  | NVCC_<br>EMC2           | VSS                     | VDD_<br>SOC_<br>IN      | VDD_<br>SOC_<br>IN      | VDD_<br>SOC_<br>IN      | VSS                     | VDD_<br>USB_<br>1P8     | GPIO_<br>SD_<br>B2_02   | GPIO_<br>SD_<br>B2_10   | GPIO_<br>SD_<br>B2_09   | DAC_<br>OUT           | GPIO_<br>AD_33        |
| <b>J</b> | GPIO_<br>EMC_<br>B1_38 | GPIO_<br>EMC_<br>B1_39 | GPIO_<br>EMC_<br>B1_26 | GPIO_<br>EMC_<br>B1_25  | GPIO_<br>EMC_<br>B1_24  | NVCC_<br>EMC2           | VSS                     | VDD_<br>SOC_<br>IN      | VDD_<br>SOC_<br>IN      | VDD_<br>SOC_<br>IN      | VSS                     | GPIO_<br>AD_23          | VDDA_<br>ADC_<br>3P3    | GPIO_<br>SD_<br>B2_01   | GPIO_<br>SD_<br>B2_00   | GPIO_<br>AD_34        | GPIO_<br>AD_31        |

Table 113. 14 x 14 mm, 0.8 mm pitch, ball map (continued)

|          |                        |                        |                        |                        |                        |                        |                        |                      |                       |                      |                      |                      |                |                      |                      |                |                |
|----------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|----------------------|-----------------------|----------------------|----------------------|----------------------|----------------|----------------------|----------------------|----------------|----------------|
| <b>K</b> | GPIO_<br>EMC_<br>B1_40 | GPIO_<br>EMC_<br>B2_00 | GPIO_<br>EMC_<br>B2_02 | GPIO_<br>EMC_<br>B2_01 | GPIO_<br>EMC_<br>B2_13 | DCDC_<br>_GND          | DCDC_<br>_GND          | DCDC_<br>_DIG        | DCDC_<br>_DIG         | VDD_<br>SOC_<br>IN   | VSS                  | GPIO_<br>AD_22       | GPIO_<br>AD_20 | GPIO_<br>AD_21       | VDDA_<br>ADC_<br>1P8 | GPIO_<br>AD_32 | GPIO_<br>AD_30 |
| <b>L</b> | GPIO_<br>EMC_<br>B1_41 | GPIO_<br>EMC_<br>B2_15 | VSS                    | GPIO_<br>EMC_<br>B2_11 | DCDC_<br>_IN_Q         | DCDC_<br>_GND          | DCDC_<br>_DIG<br>SENSE | DCDC_<br>_DIG        | GPIO_<br>SNVS_<br>02  | VSS                  | VSS                  | GPIO_<br>AD_13       | GPIO_<br>AD_24 | GPIO_<br>AD_26       | VSS                  | GPIO_<br>AD_19 | GPIO_<br>AD_28 |
| <b>M</b> | GPIO_<br>EMC_<br>B2_04 | GPIO_<br>EMC_<br>B2_12 | GPIO_<br>EMC_<br>B2_07 | GPIO_<br>EMC_<br>B2_14 | DCDC_<br>_IN           | DCDC_<br>_ANA<br>SENSE | DCDC_<br>_ANA          | DCDC_<br>_ANA        | GPIO_<br>SNVS_<br>06  | GPIO_<br>SNVS_<br>03 | VDDA_<br>1P8_IN      | NVCC_<br>GPIO        | GPIO_<br>AD_04 | GPIO_<br>AD_15       | GPIO_<br>AD_25       | GPIO_<br>AD_18 | GPIO_<br>AD_29 |
| <b>N</b> | GPIO_<br>EMC_<br>B2_05 | GPIO_<br>EMC_<br>B2_09 | GPIO_<br>EMC_<br>B2_18 | DCDC_<br>MODE          | DCDC_<br>_IN           | GPIO_<br>LPSR_<br>00   | GPIO_<br>LPSR_<br>04   | GPIO_<br>LPSR_<br>05 | GPIO_<br>SNVS_<br>08  | GPIO_<br>SNVS_<br>04 | VDDA_<br>1P0         | GPIO_<br>AD_00       | GPIO_<br>AD_06 | GPIO_<br>AD_14       | GPIO_<br>AD_17       | GPIO_<br>AD_27 | GPIO_<br>AD_16 |
| <b>P</b> | GPIO_<br>EMC_<br>B2_08 | GPIO_<br>EMC_<br>B2_16 | DCDC_<br>_PSWI<br>TCH  | VSS                    | GPIO_<br>LPSR_<br>09   | GPIO_<br>LPSR_<br>02   | NVCC_<br>LPSR          | GPIO_<br>LPSR_<br>06 | GPIO_<br>SNVS_<br>05  | GPIO_<br>SNVS_<br>01 | VDD_<br>LPSR_<br>DIG | VDD_<br>LPSR_<br>ANA | GPIO_<br>AD_05 | VSS                  | GPIO_<br>AD_03       | GPIO_<br>AD_11 | GPIO_<br>AD_12 |
| <b>R</b> | GPIO_<br>EMC_<br>B2_03 | GPIO_<br>EMC_<br>B2_10 | GPIO_<br>EMC_<br>B2_20 | VSS                    | GPIO_<br>LPSR_<br>10   | GPIO_<br>LPSR_<br>01   | VSS                    | GPIO_<br>LPSR_<br>07 | GPIO_<br>SNVS_<br>07  | GPIO_<br>SNVS_<br>00 | GPIO_<br>SNVS_<br>09 | VDD_<br>LPSR_<br>IN  | GPIO_<br>AD_02 | GPIO_<br>AD_01       | GPIO_<br>AD_08       | GPIO_<br>AD_09 | GPIO_<br>AD_10 |
| <b>T</b> | GPIO_<br>EMC_<br>B2_06 | GPIO_<br>EMC_<br>B2_17 | DCDC_<br>_LP           | DCDC_<br>_LN           | GPIO_<br>LPSR_<br>11   | GPIO_<br>LPSR_<br>14   | GPIO_<br>LPSR_<br>03   | WAKE<br>UP           | PMIC_<br>STBY_<br>REQ | POR_B                | TEST_<br>MODE        | VSS                  | RTC_<br>XTALI  | VDD_<br>SNVS_<br>DIG | CLK1_<br>N           | XTALO          | GPIO_<br>AD_07 |
| <b>U</b> | VSS                    | GPIO_<br>EMC_<br>B2_19 | DCDC_<br>_LP           | DCDC_<br>_LN           | GPIO_<br>LPSR_<br>12   | GPIO_<br>LPSR_<br>13   | GPIO_<br>LPSR_<br>15   | GPIO_<br>LPSR_<br>08 | PMIC_<br>ON_<br>REQ   | ONOFF                | NVCC_<br>SNVS        | VDD_<br>SNVS_<br>IN  | RTC_<br>XTALO  | VDD_<br>SNVS_<br>ANA | CLK1_<br>P           | XTALI          | VSS            |
|          | <b>1</b>               | <b>2</b>               | <b>3</b>               | <b>4</b>               | <b>5</b>               | <b>6</b>               | <b>7</b>               | <b>8</b>             | <b>9</b>              | <b>10</b>            | <b>11</b>            | <b>12</b>            | <b>13</b>      | <b>14</b>            | <b>15</b>            | <b>16</b>      | <b>17</b>      |

## 7 Revision history

Table 114 provides a revision history for this data sheet.

**Table 114. i.MX RT1160 Data Sheet document revision history (continued)**

| Rev.<br>Number | Date    | Substantive Change(s) |
|----------------|---------|-----------------------|
| Rev. 0         | 04/2021 | • Initial version     |

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