MIC58P42

8-Bit Serial-Input Protected Latched Driver

General Description

The MIC58P42 serial-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common STROBE, CLOCK, SERIAL DATA INPUT, and OUTPUT ENABLE functions. Similar to the MIC5842, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and over-current shutdown.

The bipolar/CMOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC58P42 has open-collector outputs capable of sinking 500 mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V (50V sustaining). The drivers can be operated with a split supply, where the negative supply is down to –20V and may be paralleled for higher load current capability.

With a 5V logic supply, the MIC58P42 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors. By using the serial data output, drivers may be cascaded for interface applications requiring additional drive lines.

Each of these eight outputs has an independent over current shutdown of 500 mA. Upon over-current detection, the affected channel will turn OFF until V_{DD} is cycled or the ENABLE/RESET pin is pulsed high. Current pulses less than 2µs will not activate current shutdown. Temperatures above 165°C will shut down the device. The UVLO circuit prevents operation at low V_{DD}; hysteresis of 0.5V is provided. See the MIC59P60 for a similar device that additionally provides an error flag output.

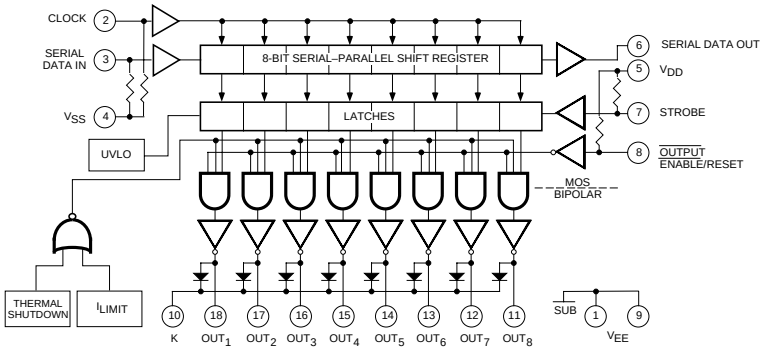
Features

- 3.3 MHz Minimum Data-Input Rate
- CMOS, PMOS, NMOS, and TTL Compatible
- Internal Pull-Up/Pull-Down Resistors
- Low Power CMOS Logic and Latches
- High Voltage (80V) Current-Sink Outputs
- Output Transient-Protection Diodes
- Single or Split Supply Operation
- Thermal Shutdown
- Under-Voltage Lockout
- Per-Output Over-Current Shutdown (500mA typical)

Ordering Information

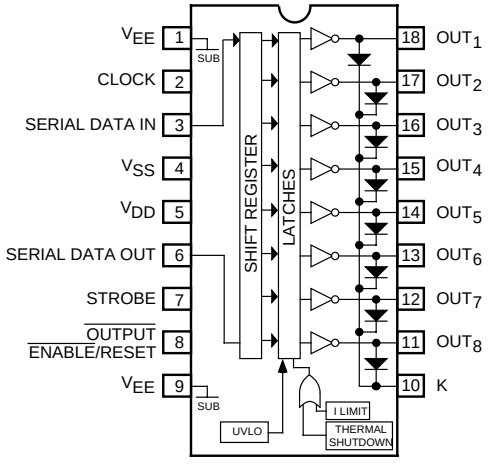
Part Number	Temperature Range	Package
MIC58P42BN	–40°C to +85°C	18-Pin Plastic DIP
MIC58P42BV	–40°C to +85°C	20-Pin PLCC
MIC58P42BWM	–40°C to +85°C	18-Pin Wide SOIC

Functional Diagram

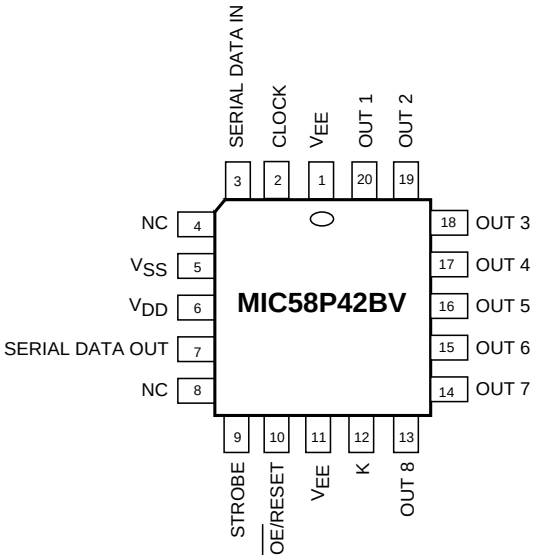


Pin Configuration

(DIP and SOIC)



PLCC Pin Configuration



Absolute Maximum Ratings (Note 1, 2)

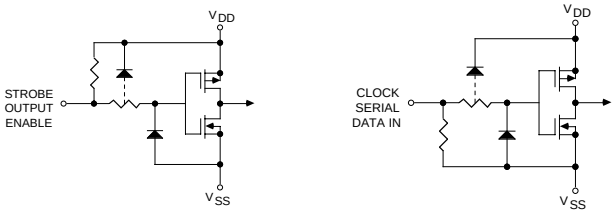
at 25°C Free-Air Temperature and V_{SS} = 0V

Output Voltage	80V
Output Voltage, $V_{CE(SUS)}$ (Note 1)	50V
Logic Supply Voltage Range, V_{DD}	4.5V to 15V
V_{DD} with Reference to V_{EE}	25V
Emitter Supply Voltage (Substrate), V_{EE}	–20V
Input Voltage Range, V_{IN}	–0.3V to V_{DD} + 0.3V
Package Power Dissipation, P_D	
MIC58P42BN	1.82W
Derate above T_A = +25°C	18mW/°C
MIC58P42BV	1.4W
Derate above T_A = +25°C	14mW/°C
MIC58P42BWM	1.2W
Derate above T_A = +25°C	12mW/°C
Operating Temperature Range, T_A	–55°C to +125°C
Storage Temperature Range, T_S	–65°C to +150°C

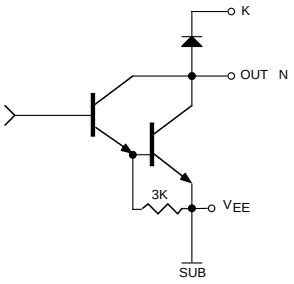
Note 1: For Inductive load applications.

Note 2: CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

Typical Input Circuits



Typical Output Driver



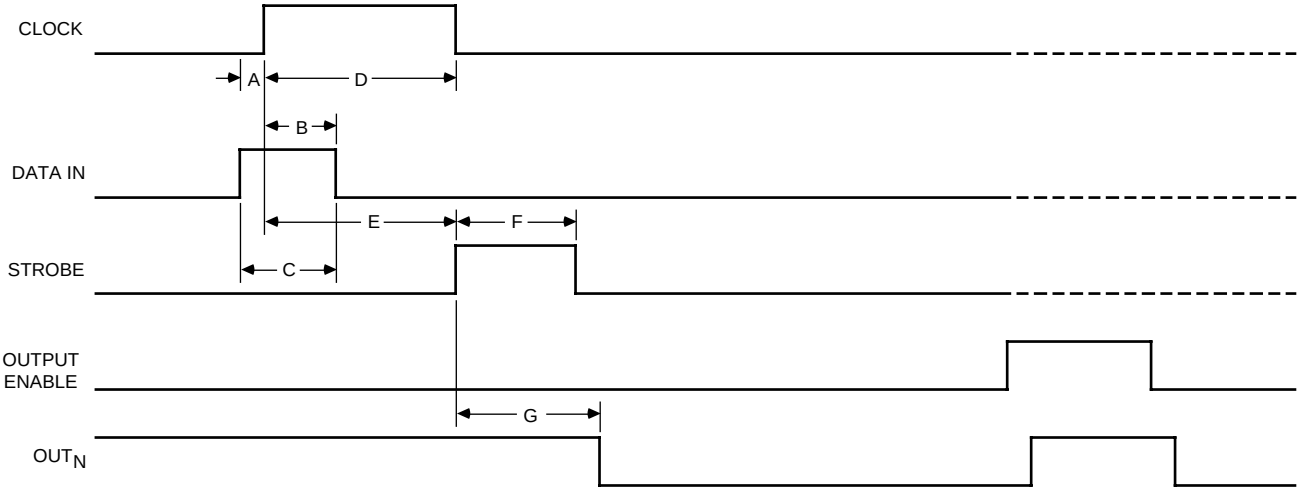
Pin Description

Pin (DIP & S.O.)	Name	Description
1,9	V_{EE}	Substrate. Most Negative voltage in the system connects here.
2	CLOCK	Serial Data Clock. A CLEAR input must also be clocked into the latches.
3	SERIAL DATA IN	Serial Data Input pin.
4	V_{SS}	Logic reference (Ground) pin.
5	V_{DD}	Logic Positive Supply voltage.
6	SERIAL DATA OUT	Serial Data Output pin. (Flow–through).
7	STROBE	Output Strobe pin. Loads output latches when high. Strobe is needed to clear latch.
8	$\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE/RESET}}$	When Low, Outputs are active. When High, device is reset from a fault condition.
10	K	Transient suppression diode's cathode common pin.
11—18	OUTPUT N	Open Collector outputs 8 through 1.

Electrical Characteristics at T_A = +25°C, V_{DD} = 5V, V_{SS} = V_{EE} = 0V (unless otherwise noted)

			Limits			
Characteristic	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Output Leakage Current	I_{CEX}	V_{OUT} = 80V			50	µA
		V_{OUT} = 80V, T_A = +70°C			100	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 100mA I_{OUT} = 200mA I_{OUT} = 350mA		0.9 1.1 1.3	1.1 1.3 1.6	V
Collector-Emitter Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 350mA, L = 2mH	50			V
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	V_{DD} = 12V V_{DD} = 10V V_{DD} = 5.0V, **Note 1**		10.5 8.5 3.5		
Input Resistance	R_{IN}	V_{DD} = 12V V_{DD} = 10V V_{DD} = 5.0V	50 50 50	200 300 600		kΩ
Supply Current	$I_{DD(ON)}$	All Drivers ON, V_{DD} = 12V All Drivers ON, V_{DD} = 10V All Drivers ON, V_{DD} = 5.0V		6.4 6.0 4.6	10.0 9.0 7.5	mA
	$I_{DD\ (1\ ON)}$	One Driver ON, All others OFF, V_{DD} = 12V One Driver ON, All others OFF, V_{DD} = 10V One Driver ON, All others OFF, V_{DD} = 5V		3.1 2.9 2.3	4.5 4.5 3.6	
	$I_{DD(OFF)}$	All Drivers OFF, V_{DD} = 12V All Drivers OFF, V_{DD} = 10V All Drivers OFF, V_{DD} = 5.0V		2.6 2.4 1.9	4.2 3.6 3.0	
Clamp Diode Leakage Current	I_R	V_R = 80V			50	µA
Clamp Diode Forward Voltage	V_F	I_F = 350mA		1.7	2.0	V
Output Current Shutdown Threshold	I_{LIM}			500		mA
Start Up Voltage	V_{SU}	**Note 2**	3.5	4.0	4.5	V
Minimum Supply (V_{DD})	$V_{DD\ MIN}$		3.0	3.5	4.0	V
Thermal Shutdown				165		°C
Thermal Shutdown Hysteresis				10		°C

Note 1: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".
Note 2: Undervoltage Lockout is guaranteed to release device at no more than 4.5V, and disable the device at no less than 3.0V.



Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS}), V_{DD} = 5V

A. Typical Data Active Time Before Clock Pulse (Data Set-Up Time) ..... 75 ns
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... 75 ns
C. Minimum Data Pulse Width ..... 150 ns
D. Minimum Clock Pulse Width ..... 150 ns
E. Minimum Time Between Clock Activation and Strobe ..... 300 ns
F. Minimum Strobe Pulse Width ..... 100 ns
G. Typical Time Between Strobe Activation and Output Transition ..... 500 ns

SERIAL DATA present at the input is transferred to the shift register on the logic “0” to logic “1” transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the ENABLE input be high to prevent invalid output states.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches. A positive OUTPUT ENABLE/ RESET pulse resets the output after a current shutdown fault. Thermal limit faults are not latched and require no reset pulse.

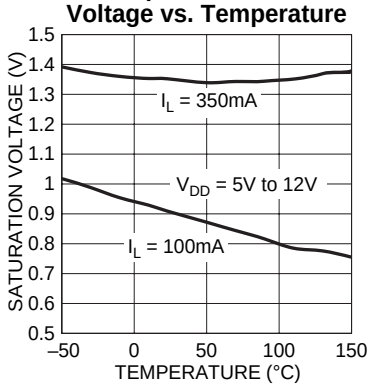
MIC58P42 Truth Table

Serial Data Input	Clock Input	Shift Register Contents I_1	I_2	I_3	I_8	Serial Data Output	Strobe Input	Latch Contents I_1	I_2	I_3	I_8	Output Enable	Output Contents I_1	I_2	I_3	I_8
H	⌐¬	H	R_1	R_2	R_7	R_7										
L	⌐¬	L	R_1	R_2	R_7	R_7										
X	¬⌐	R1	R2	R_3	R_8	R_8										
	⌐¬	O	O	O	O	L										
		X	X	X	X	X	L	R_1	R_2	R_3	R_8					
		P_1	P_2	P_3	P_8	P_8	H	P_1	P_2	P_3	P_8	L	P_1	P_2	P_3	P_8
								X	X	X	X	H	H	H	H	H

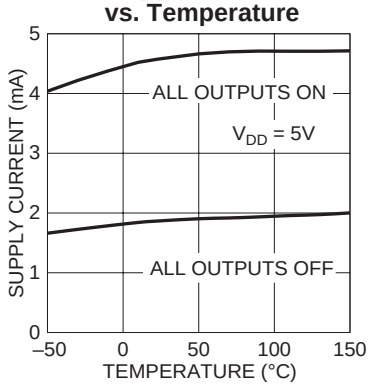
L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State
O = Output OFF

Typical Characteristic Curves

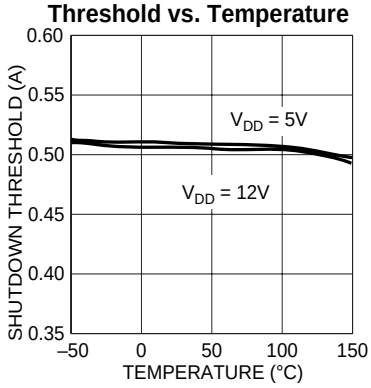
Output Saturation Voltage vs. Temperature



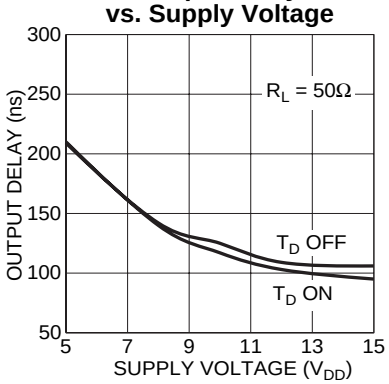
Supply Current vs. Temperature



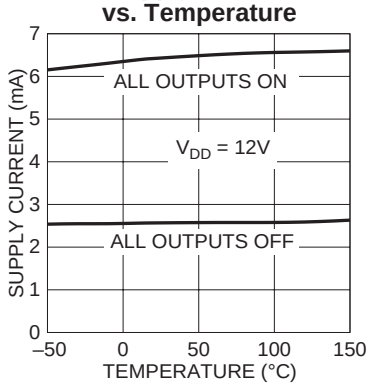
Current Shutdown Threshold vs. Temperature



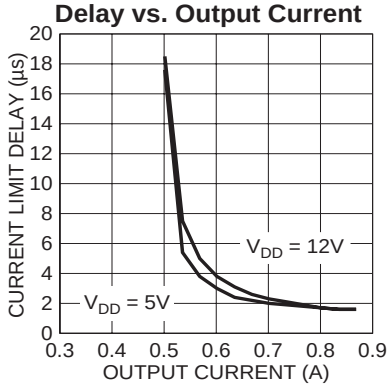
Output Delay vs. Supply Voltage



Supply Current vs. Temperature



Current Shutdown Delay vs. Output Current



Maximum Allowable Duty Cycle, Plastic DIP

V_{DD} = 5.0V

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 5.0V)	Max. Allowable Duty Cycle at Ambient Temperature of:				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

V_{DD} = 12V

Number of Outputs ON (I_{OUT} = 200mA V_{DD} = 12V)	Max. Allowable Duty Cycle at Ambient Temperature of:				
	25°C	40°C	50°C	60°C	70°C
8	80%	68%	60%	52%	44%
7	91%	77%	68%	59%	50%
6	100%	90%	79%	69%	58%
5	100%	100%	95%	82%	69%
4	100%	100%	100%	100%	86%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%