Features

- PWM and Direction-controlled Driving of Four Externally-powered NMOS Transistors
- A Programmable Dead Time Is Included to Avoid Peak Currents Within the H-bridge
- Integrated Charge Pump to Provide Gate Voltages for High-side Drivers and to Supply the Gate of the External Battery Reverse Protection NMOS
- 5V/3.3V Regulator and Current Limitation Function
- Reset Derived From 5V/3.3V Regulator Output Voltage
- Sleep Mode With Supply Current of Typically < 45 µA, Wake-up by Signal on Pins EN2 or on LIN Interface
- A Programmable Window Watchdog
- Battery Overvoltage Protection and Battery Undervoltage Management
- Overtemperature Warning and Protection (Shutdown)
- LIN 2.1 Compliant
- 3.3V/5V Regulator with Trimmed Band Gap
- QFN32 Package

H-bridge Motor Driver

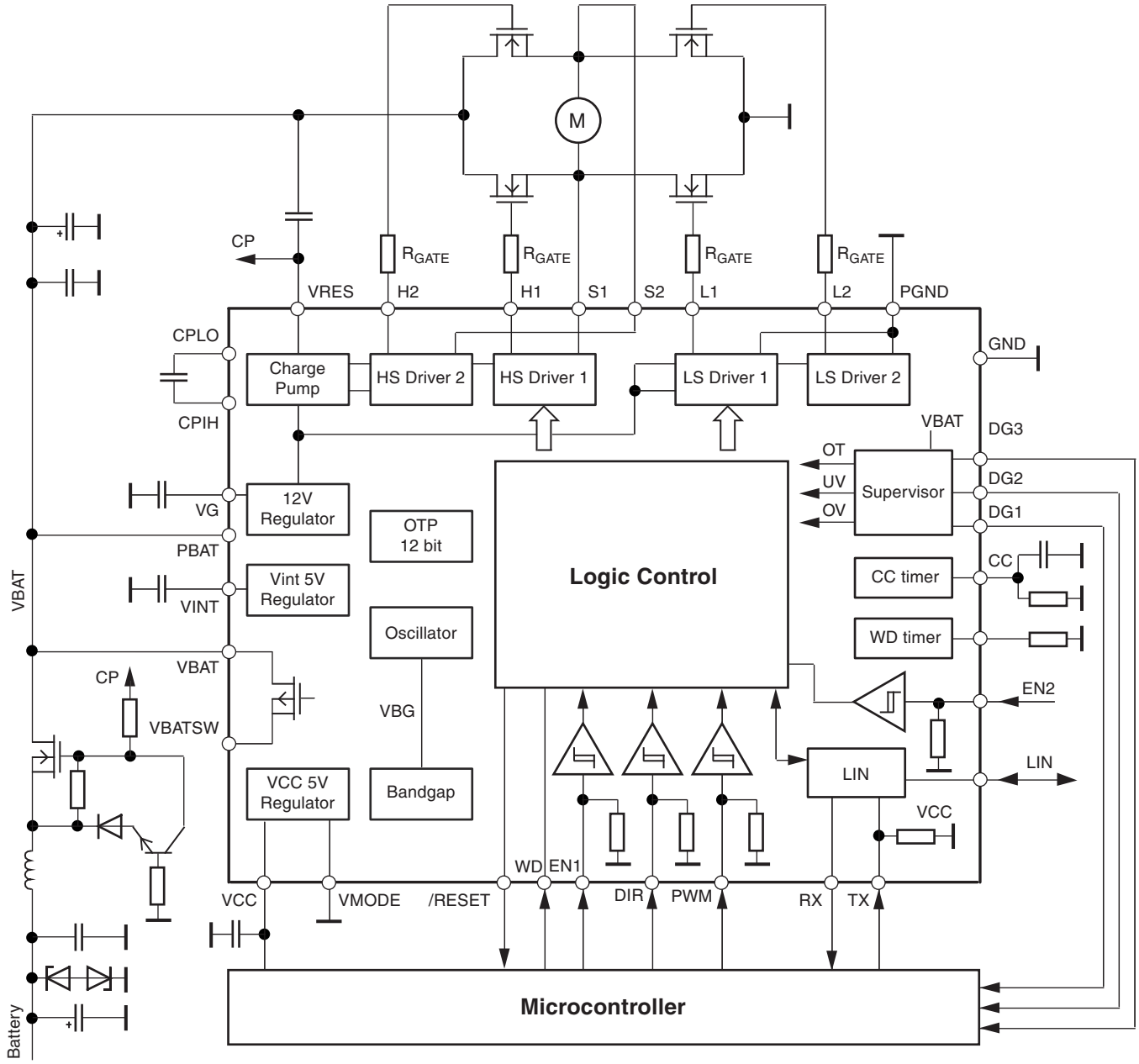
ATA6823

1. Description

The ATA6823 is designed for several body and powertrain applications. The IC is used to drive a continuous current motor in a full H-bridge configuration. An external microcontroller controls the driving function of the IC by providing a PWM signal and a direction signal and allows the use of the IC in a motor-control application. The PWM control is performed by the low-side switch; the high-side switch is permanently on in the driving phase. The VMODE configuration pin can be set to 5V or 3.3V mode (for regulator and interface high level). The window watchdog has a programmable time, programmable by choosing a certain value of the external watchdog resistor RWD, internally trimmed to an accuracy of 10%. For communication a LIN transceiver 2.1 is integrated.

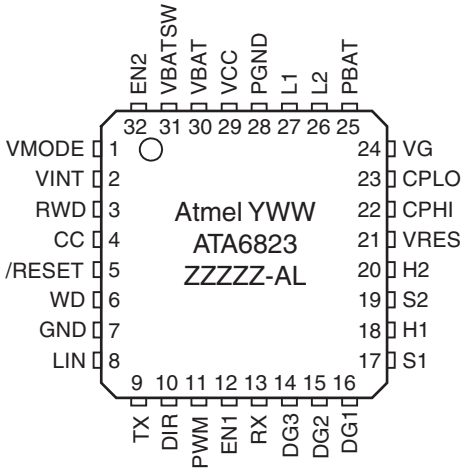
4856H–AUTO–07/09

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN32



Note:

YWW	Date code (Y = Year - above 2000, WW = week number)
ATA6823	Product name
ZZZZZ	Wafer lot number
AL	Assembly sub-lot number

Table 2-1. Pin Description

Pin	Symbol	I/O	Function
1	VMODE	I	Selector for V_{CC} and interface logic voltage level
2	VINT	I/O	Blocking capacitor 220 nF/10V/X7R
3	RWD	I	Resistor defining the watchdog interval
4	CC	I/O	RC combination to adjust cross conduction time
5	/RESET	O	Reset signal for microcontroller
6	WD	I	Watchdog trigger signal
7	GND	I	Ground for chip core
8	LIN	I/O	LIN-bus terminal
9	TX	I	Transmit signal to LIN bus from microcontroller
10	DIR	I	Defines the rotation direction for the motor
11	PWM	I	PWM input controls motor speed
12	EN1	I	Microcontroller output to keep the chip in Active mode
13	RX	O	Receive signal from LIN bus for microcontroller
14	DG3	O	Diagnostic output 3
15	DG2	O	Diagnostic output 2
16	DG1	O	Diagnostic output 1
17	S1	I/O	Source voltage H-bridge, high-side 1
18	H1	O	Gate voltage H-bridge, high-side 1
19	S2	I/O	Source voltage H-bridge, high-side 2
20	H2	O	Gate voltage H-bridge, high-side 2
21	VRES	I/O	Gate voltage for reverse protection NMOS, blocking capacitor 470 nF/25V/X7R

Table 2-1. Pin Description (Continued)

Pin	Symbol	I/O	Function
22	CPHI	I	Charge pump capacitor 220 nF/25V/X7R
23	CPLO	O	
24	VG	I/O	Blocking capacitor 470 nF/25V/X7R
25	PBAT	I	Power supply (after reverse protection) for charge pump and H-bridge
26	L2	O	Gate voltage H-bridge, low-side 2
27	L1	O	Gate voltage H-bridge, low-side 1
28	PGND	I	Power ground for H-bridge and charge pump
29	VCC	O	5V/100 mA supply for microcontroller, blocking capacitor 2.2 µF/10V/X7R
30	VBAT	I	Supply voltage for IC core (after reverse protection)
31	VBATSW	O	100Ω PMOS switch from V_{VBAT}
32	EN2	I	Enable input

3. Functional Description

3.1 Power Supply Unit with Supervisor Functions

3.1.1 Power Supply

The IC is supplied by a reverse-protected battery voltage. To prevent it from destruction, proper external protection circuitry has to be added. It is recommended to use at least a capacitor combination of storage and HF caps behind the reverse protection circuitry and closed to the VBAT pin of the IC (see Figure 1-1 on page 2).

A fully-internal low-power and low-drop regulator, stabilized by an external blocking capacitor provides the necessary low-voltage supply needed for the wake-up process. The low-power band gap reference is trimmed and is used for the bigger VCC regulator, too. All internal blocks are supplied by the internal regulator.

Note: The internal supply voltage V_{INT} must not be used for any other supply purpose!

Nothing inside the IC except the logic interface to the microcontroller is supplied by the 5V/3.3V VCC regulator.

A power-good comparator checks the output voltage of the V_{INT} regulator and keeps the whole chip in reset as long as the voltage is too low.

There is a high-voltage switch which brings out the battery voltage to the pin VBATSW for measurement purposes. This switch is switched ON for VCC = HIGH and stays ON in case of a watchdog reset going to sleep mode, VBATSW turns OFF. The signal can be used to switch on external voltage regulators, etc.

3.1.2 Voltage Supervisor

This block is intended to protect the IC and the external power MOS transistors against overvoltage on battery level and to manage undervoltage on it.

Function: in case of both overvoltage alarm (V_{THOV}) and of undervoltage alarm (V_{THUV}) the external NMOS motor bridge transistors will be switched off. The failure state will be flagged via DG2. No other actions will be carried out. The voltage supervision block is connected to VBAT and filtered by a first-order low pass with a corner frequency of typical 15 kHz.

3.1.3 Temperature Supervisor

There is a temperature sensor integrated on-chip to prevent the IC from overheating due to a failure in the external circuitry and to protect the external NMOSFET transistors.

In case of detected overtemperature (150°C), the diagnostic pin DG3 will be switched to "H" to signalize this event to the microcontroller. It should undertake actions to reduce the power dissipation in the IC. In case of detected overtemperature (165°C), the V_{CC} regulator and all drivers including the LIN transceiver will be switched OFF immediately and /RESET will go LOW.

Both temperature thresholds are correlated. The absolute tolerance is ±10°C and there is a built-in hysteresis of about 10°C to avoid fast oscillations. After cooling down below the 155°C threshold; the IC will go into Active mode.

The LIN interface has a separate thermal shutdown with disabled the low-side driver at typically 165°C.

3.2 Sleep Mode

To be able to guarantee the low quiescent current of the inactive IC, a Sleep mode is established. In Sleep mode it is possible to wake-up the IC by using the pins EN2 or LIN. In Sleep mode, the following blocks are active:

- Band gap
- Internal 5V regulator (VINT) with external blocking capacitor of 220 nF
- Input structure for detecting the EN2 pins threshold
- Wake-up block of the LIN receive part

3.3 Wake-up and Sleep Mode Strategy

The IC has two modes: Sleep and Active. The change between the modes is described below.

The default state after power-on is Active mode.

The wake-up procedure brings the IC from a standby mode (Sleep) to an active mode (Active). The internal 5V supply VINT, the EN2 pin input structure and a certain part of the LIN receiver are permanently active to ensure a proper startup of the system.

The *Go to Active* and *Go to Sleep* procedures are implemented as follows:

- Go to Active by activating pin EN2

The input EN2 is intended as a switch-on pin from an external signal. Its input structure consists of a comparator with built-in hysteresis. It is ESD-protected by diodes against GND and V_{VBAT}; for this reason the input voltage level must be positive and not higher than V_{VBAT}.

Pulling the EN2 pin up to the V_{VBAT} level will drive the IC into Active mode. EN2 is debounced with a time constant of 20 µs, based on a 100 kHz clock.

- Go to Active using the LIN interface

The second possibility for wake-up can be performed using the LIN transceiver. In Sleep mode, the LIN receiver is partially active.

The wake-up by LIN requires 2 steps:

1. If the voltage on pin LIN is below a value of $V_{/DATwake}$ (about V_{VBAT} – 2V) the receive part of the LIN interface is active (not to be confused with Active mode of the whole IC). The active receive part is able to detect a valid LOW on the LIN pin.
2. If LIN = LOW during a filter time $t_{wakeLIN}$ (typically 70 µs) the IC will change to Active mode. A short change back to HIGH during the filter time will reset the filter. This information is stored in a latch after entering Active mode

If the change to Active mode was caused by LIN, the EN1 or EN2 pins may remain LOW without disturbing the Active mode.

- Stay in Active via EN1

The input EN1 is intended to keep the IC in Active Mode via a signal from the microcontroller. The input is ESD-protected by diodes against GND and VCC. Therefore, the input voltage must be positive and not higher than V_{CC}. EN1 cannot be used to switch from Sleep to Active because the VCC regulator is off in the Sleep mode and V_{CC} will be zero.

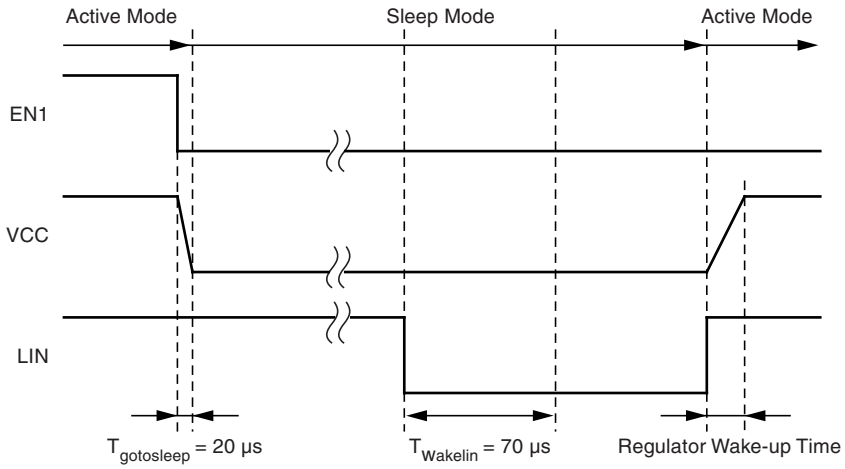
- Go to Sleep

A HIGH to LOW transition at pin EN1 and a following permanent LOW for the time $t_{gotosleep}$ (typically 20 µs) switches the IC to Sleep mode.

Figure 3-1 illustrates the wake-up by LIN. The status PREWAKE is characterized by the activated receive block of the LIN interface. After going to Active mode, the V_{CC} regulator starts working.

Go to Sleep is possible with a valid HIGH to LOW transition at pin EN1 (permanent LOW for longer than t_{db}) if EN1 was in a valid HIGH state (HIGH for longer than t_{db}) before.

Figure 3-1. Wake-up by pin LIN



3.4 5V/3.3V VCC Regulator

The 5V/3.3V regulator is fully integrated on-chip. It requires only a 2.2 µF ceramic capacitor for stability and has 100 mA current capability. Using the VMODE pin, the output voltage can be selected to either 5V or 3.3V. Switching of the output voltage during operation is not intended to be supported. The VMODE pin must be hard-wired to either VINT for 5V or to GND for 3.3V. The logic HIGH level of the microcontroller interface will be adapted to the VCC regulator voltage.

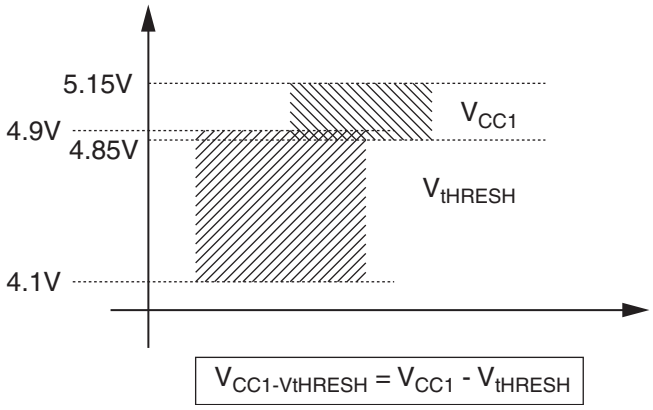
The output voltage accuracy is in general < ±3%; in the 5V mode with V_{VBAT} < 9V it is limited to < 5%.

To prevent destruction of the IC, the current delivered by the regulator is limited to maximum 100 mA to 350 mA. The delivered voltage will break down and a reset may occur.

Please note that this regulator is the main heat source on the chip. The maximum output current at maximum battery voltage and high ambient temperature can only guaranteed if the IC is mounted on an efficient heat sink.

A power-good comparator checks the output voltage of the VCC regulator and keeps the external microcontroller in reset as long as the voltage is too low.

Figure 3-2. Correlation between VCC Output Voltage and Reset Threshold



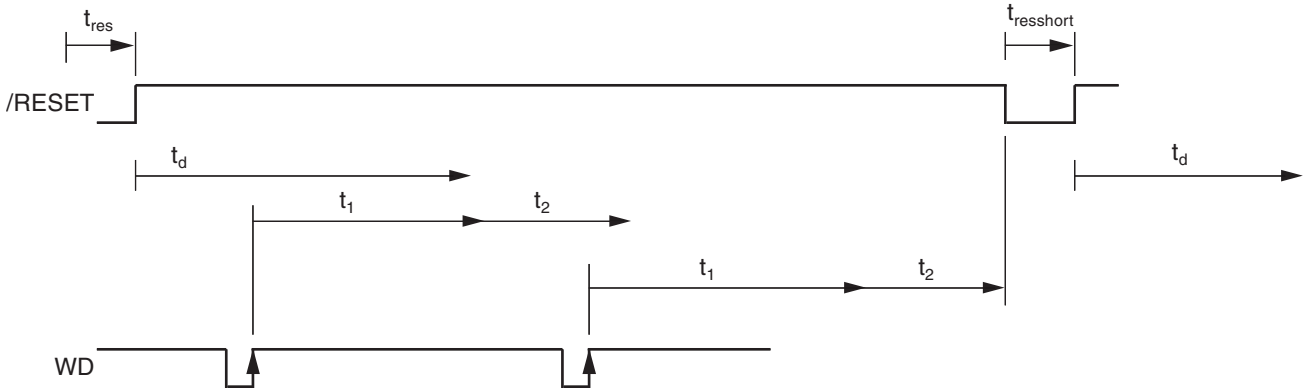
The voltage difference between the regulated output voltage and the upper reset threshold voltage is higher than 75 mV (VMODE = HIGH) and higher than 50 mV (VMODE = LOW).

3.5 Reset and Watchdog Management

The timing basis of the watchdog is provided by the trimmed internal oscillator. Its period T_{OSC} is adjustable via the external resistor R_{WD}.

The watchdog expects a triggering signal (a rising edge) from the microcontroller at the WD input within a period time window of T_{WD}. In order to save current consumption, the watchdog is switched off during Sleep mode.

Figure 3-3. Timing Diagram of the Watchdog Function



3.5.1 Timing Sequence

For example, with an external resistor R_{WD} = 33 kΩ ±1% we get the following typical parameters of the watchdog.

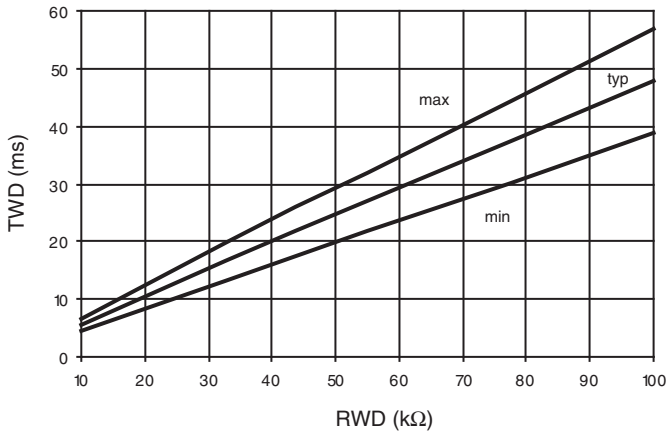
T_{OSC} = 12.32 µs, t_1 = 12.1 ms, t_2 = 9.61 ms, T_{WD} = 16.88 ms ±10%

The times t_{res} = 68 ms and t_d = 68 ms are fixed values with a tolerance of 10%.

After ramp-up of the battery voltage (power-on reset), the V_{CC} regulator is switched on. The reset output, /RESET, stays low for the time t_{res} (typically 68 ms), then switches to high. For an initial lead time t_d (typically 68 ms for setups in the controller) the watchdog waits for a rising edge on WD to start its normal window watchdog sequence. If no rising edge is detected, the watchdog will reset the microcontroller for t_{res} and wait t_d for the rising edge on WD.

Times t_1 (close window) and t_2 (open window) form the window watchdog sequence. To avoid receiving a reset from the watchdog, the triggering signal from the microcontroller must hit the time frame of t_2 = 9.61 ms. The trigger event will restart the watchdog sequence.

Figure 3-4. T_{WD} versus R_{WD}



If triggering fails, /RESET will be pulled to ground for a shortened reset time of typically 2 ms. The watchdog start sequence is similar to the power-on reset.

The internal oscillator is trimmed to a tolerance of < ±10%. This means that t_1 and t_2 can also vary by ±10%. The following calculation shows the worst case calculation of the watchdog period T_{wd} which the microcontroller has to provide.

$t_{1min} = 0.90 \times t_1 = 10.87$ ms, $t_{1max} = 1.10 \times t_1 = 13.28$ ms

$t_{2min} = 0.90 \times t_2 = 8.65$ms, $t_{2max} = 1.10 \times t_2 = 10.57$ ms

$T_{wdmax} = t_{1min} + t_{2min} = 10.87$ ms + 8.65 ms = 19.52 ms

$T_{wdmin} = t_{1max} = 13.28$ ms

$T_{wd} = 16.42$ ms ±3.15 ms (±19.1%)

Figure 3-4 above shows the typical watchdog period T_{WD} depending on the value of the external resistor R_{OSC}.

A reset will be active for $V_{CC} < V_{tHRESx}$; the level V_{tHRESx} is realized with a hysteresis (HYS_{RESth}).

3.6 LIN Transceiver

A bi-directional bus interface is implemented for data transfer between the LIN bus and the local LIN protocol controller.

The transceiver consists of a low side driver (1.2V at 40 mA) with slew rate control, wave shaping, current limitation, and a high-voltage comparator followed by a debouncing unit in the receiver.

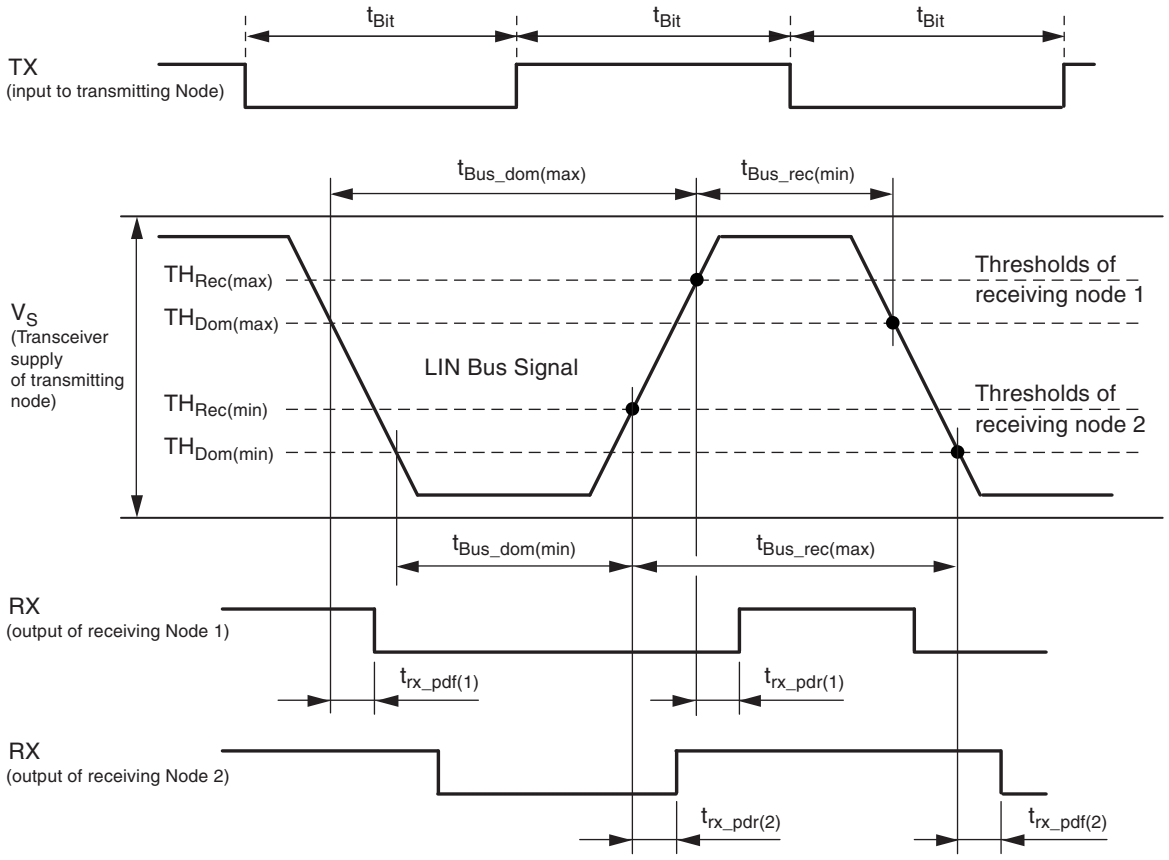
3.6.1 Transmit Mode

During transmission, the data at the pin TX will be transferred to the bus driver to generate a bus signal on pin LIN.

To minimize the electromagnetic emission of the bus line, the bus driver has an integrated slew rate control and wave-shaping unit. Transmission will be interrupted in the following cases:

- Thermal shutdown active or overtemperature LIN active
- Sleep mode

Figure 3-5. Definition of Bus Timing Parameters



The recessive BUS level is generated from the integrated 30 kΩ pull-up resistor in series with an active diode. This diode prevents the reverse current of VBUS during differential voltage between VSUP and BUS ($V_{BUS} > V_{SUP}$).

No additional termination resistor is necessary to use the ATA6823 in LIN slave nodes. If this IC is used for LIN master nodes, it is necessary that the BUS pin be terminated via an external 1 kΩ resistor in series with a diode to VBAT.

3.6.2 TXD Dominant Time-out Function

The TXD input has an internal pull-down resistor. An internal timer prevents the bus line from being driven permanently in dominant state. If TXD is forced low longer than $t_{dom} > 18.4$ ms, the pin LIN will be switched off to recessive mode. To reset this mode switch TXD to high (> 10 µs) before switching LIN to dominant again.

3.7 Control Inputs EN1, EN2, DIR, PWM

3.7.1 Pins EN1, EN2

Any of the enable pins may be used to activate the IC with a HIGH. EN1 is a low level input, EN2 can withstand a voltage up to 40V. Internal pull-down resistors are included.

3.7.2 Pin DIR

Logical input to control the direction of the external motor to be controlled by the IC. An internal pull-down resistor is included.

3.7.3 Pin PWM

Logical input for PWM information delivered by external microcontroller. Duty cycle and frequency at this pin are passed through to the H-bridge. An internal pull-down resistor is included.

Table 3-1. Status of the IC Depending on Control Inputs and Detected Failures

Control Inputs			Driver Stage for External Power MOS				Comments
ON	DIR	PWM	H1	L1	H2	L2	
0	X	X	OFF	OFF	OFF	OFF	Standby mode
1	0	PWM	ON	OFF	/PWM	PWM	Motor PWM forward
1	1	PWM	/PWM	PWM	ON	OFF	Motor PWM reverse

The internal signal ON is high when

- At least one valid trigger has been accepted (SYNC = 1)
- V_{VBAT} is inside the specified range (UV = 0 and nOV = 1)
- The charge pump has reached its minimum voltage (CPOK = 1) and
- The device is not overheated (OT2 = 0)

In case of a short circuit, the appropriate transistor is switched off after a debounce time of about 10 µs. In order to avoid cross current through the bridge, a cross conduction timer is implemented. Its time constant is programmable by means of an RC combination.

Table 3-2. Status of the Diagnostic Outputs

Device Status					Diagnostic Outputs			Comments
CPOK	OT1	OV	UV	SC	DG1	DG2	DG3	
0	X	X	X	X	–	1	–	Charge pump failure
X	1	X	X	X	–	–	1	Overtemperature warning
X	X	1	X	X	–	1	–	Overvoltage
X	X	X	1	X	–	1	–	Undervoltage
X	X	X	X	1	1	–	–	Short circuit

Note: X represents: don't care – no effect)
OT1: Overtemperature warning
OV: Overvoltage of VBAT
UV: Undervoltage of VBAT
SC: Short circuit
CPOK: Charge pump OK

In order to be able to distinguish between a wake-up from LIN or from EN2, the source of wake-up is flagged in DG1 until the first valid trigger (LIN = 0, EN2 = 1).

3.8 VG Regulator

The VG regulator is used to generate the gate voltage for the low-side driver. Its output voltage will be used as one input for the charge pump, which generates the gate voltage for the high-side driver. The purpose of the regulator is to limit the gate voltage for the external power MOS transistors to 12V. It needs a ceramic capacitor of 470 nF for stability. The output voltage is reduced if the supply voltage at VBAT falls below 12V.

3.9 Charge Pump

The integrated charge pump is needed to supply the gates of the external power MOS transistors. It needs a shuffle capacitor of 220 nF and a reservoir capacitor of 470 nF. Without load, the output voltage on the reservoir capacitor is V_{VBAT} plus VG. The charge pump is clocked with a dedicated internal oscillator of 100 KHz. The charge pump is designed to reach a good EMC level.

3.10 Thermal Shutdown

There is a thermal shutdown block implemented. With rising junction temperature, a first warning level will be reached at 150°C. At this point the IC stays fully functional and a warning will be sent to the microcontroller. At junction temperature 165°C the VCC regulator will be switched off and a reset occurs.

3.11 H-bridge Driver

The IC includes two push-pull drivers for control of two external power NMOS used as high-side drivers and two push-pull drivers for control of two external power NMOS used as low-side drivers. The drivers are able to be used with standard and logic-level power NMOS.

The drivers for the high-side control use the charge pump voltage to supply the gates with a voltage of VG above the battery voltage level. The low-side drivers are supplied by VG directly. It is possible to control the external load (motor) in the forward and reverse direction (see Table 3-1 on page 11). The duty cycle of the PMW controls the speed. A duty cycle of 100% is possible in both directions.

3.11.1 Cross Conduction Time

To prevent high peak currents in the H-bridge, a non-overlapping phase for switching the external power NMOS is realized. An external RC combination defines the cross conduction time in the following way:

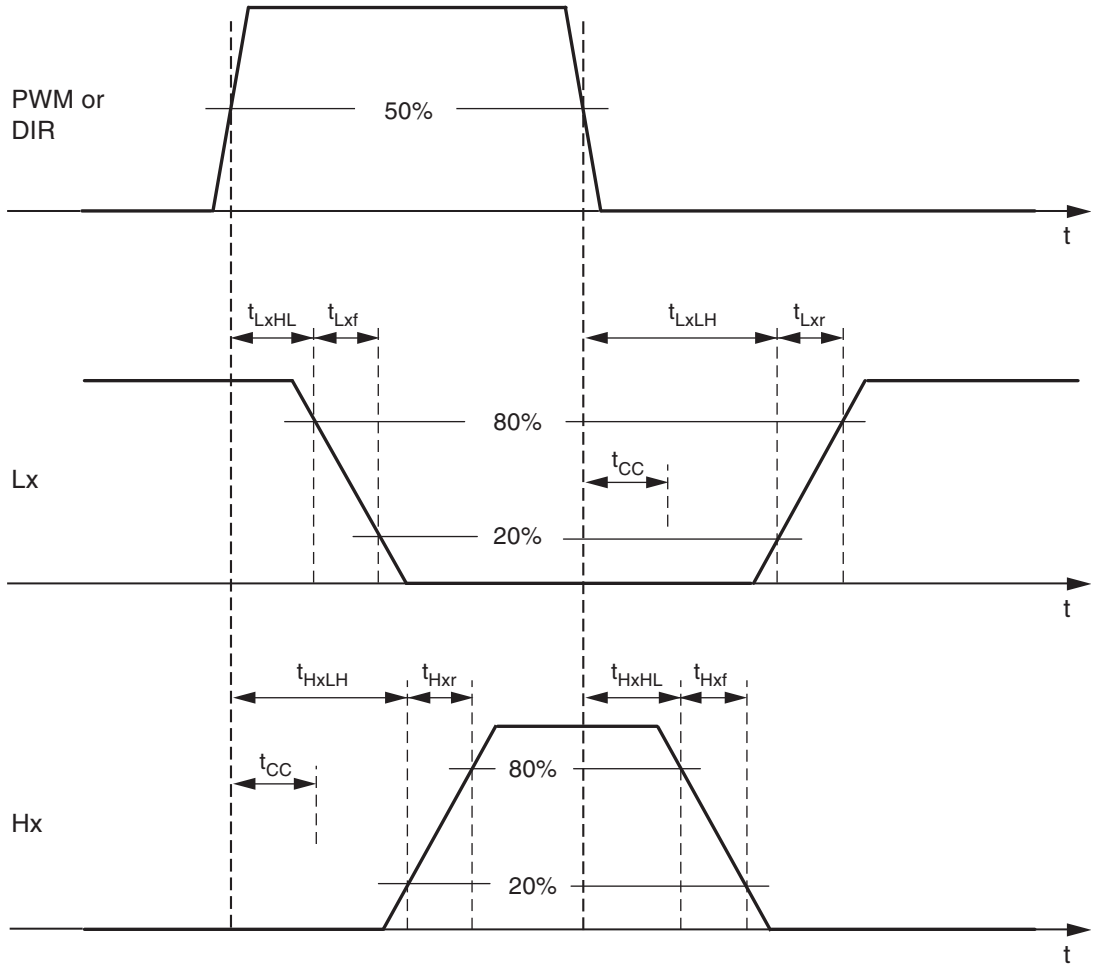
t_{CC} (µs) = 0.41 × R_{CC} (kΩ) × C_{CC} (nF) (tolerance: ±5% ±0.15 µs)

The RC combination is charged to 5V and the switching level of the internal comparator is 67% of the start level.

The resistor R_{CC} must be greater than 5 kΩ and should be as close as possible to 10 kΩ, the C_{CC} value has to be ≤ 5 nF. Use of COG capacitor material is recommended.

The time measurement is triggered by the PWM or DIR signal crossing the 50% level.

Figure 3-6. Timing of the Drivers



The delays t_{HxLH} and t_{LxLH} include the cross conduction time t_{CC}.

3.12 Short Circuit Detection

To detect a short in H-bridge circuitry, internal comparators detect the voltage difference between source and drain of the external power NMOS. If the transistors are switched ON and the source-drain voltage difference is higher than the value V_{SC} (4V with tolerances) for a time > t_{SC} (typically 10 µs) the signal SC (short circuit) will be set and the drivers will be switched off immediately. The diagnostic pin DG1 will be set to “H”. With the next transition on pin PWM, the bit will be cleared and the corresponding drivers, depending on the DIR pin, will be switched on again.

There is a PBAT supervision block implemented to detect the possible voltage drop on PBAT during a short circuit. If the voltage at PBAT falls under V_{SCPB} (5.6V with tolerances) for a time > t_{SC} the drivers will be switched off immediately and DG1 will be set to “H”. It will be cleared as above.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Description	Pin Name	Min.	Max.	Unit
Ground	GND	0	0	V
Power ground	PGND	–0.3	+0.3	V
Reverse protected battery voltage	VBAT	–0.3	+40	V
Reverse protected battery voltage	PBAT	–0.3	+40	V
Digital output	/RESET	–0.3	V_{VCC} + 0.3	V
Digital output	DG1, DG2, DG3	–0.3	V_{VCC} + 0.3	V
4.9V output, external blocking capacitor	VINT	–0.3	+5.5	V
Cross conduction time capacitor/resistor combination	CC	–0.3	V_{VINT} + 0.3	V
Digital input coming from microcontroller	WD	–0.3	V_{VINT} + 0.3	V
Watchdog timing resistor	RWD	–0.3	V_{VCC} + 0.3	V
Digital input direction control	DIR	–0.3	V_{VCC} + 0.3	V
Digital input PWM control + Test mode	PWM	–0.3	V_{VCC} + 0.3	V
Digital input for enable control	EN1	–0.3	V_{VCC} + 0.3	V
Digital input for enable control	EN2	–0.3	V_{VBAT} + 0.3	V
5V regulator output	VCC	–0.3	+5.5	V
Digital input	VMODE	–0.3	V_{VINT} + 0.3	V
12V output, external blocking capacitor	VG	–0.3	+16	V
Digital output	RX	–0.3	V_{VCC} + 0.3	V
Digital input	TX	–0.3	V_{VCC} + 0.3	V
LIN data pin	LIN	–27[1]	V_{VBAT} + 2	V
Source external high-side NMOS	S1, S2	–2	+40[3]	V
Gates external low-side NMOS	L1, L2	V_{PGND} – 0.3	V_{VG} + 0.3	V
Gates of external high-side NMOS	H1, H2	V_{Sx} – 1[2]	V_{Sx} + 16[2]	V
Charge pump	CPLO	–0.3	V_{PBAT} + 0.3	V
Charge pump	CPHI	–0.3	V_{VRES} + 0.3	V
Charge pump output	VRES	–0.3	+40[4]	V
Switched VBAT	VBATSW	–0.3	V_{VBAT} + 0.3	V
Storage temperature	ϑ_{STORE}	–40	+150	°C

Notes:
1. For $V_{VBAT} \leq 13.5V$
2. x = 1.2
3. t < 0.5s
4. Load dump of t < 0.5s tolerated

5. Thermal Resistance

Parameters	Symbol	Value	Unit
Thermal resistance junction to heat slug	R_{thjc}	< 5	K/W
Thermal resistance junction to ambient when heat slug is soldered to PCB[1]	R_{thja}	29	K/W

Note: 1. Thermal resistance junction ambient: 29 K/W (at airflow of 0 LFPM), valid for JEDEC Standard 4-layer Thermal test board with 5 x 5 thermal via matrix (100 µm drill hole, filled vias).

6. Operating Range

The operating conditions define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not implied unless otherwise stated explicitly.

Parameters	Symbol	Min.	Max.	Unit
Operating supply voltage(1)	V_{VBAT1}	V_{THUV}	V_{THOV}	V
Operating supply voltage(2)	V_{VBAT2}	6	V_{THUV}	V
Operating supply voltage(3)	V_{VBAT3}	3	< 6	V
Operating supply voltage(4)	V_{VBAT4}	0	< 3	V
Operating supply voltage(5)	V_{VBAT5}	> V_{THOV}	40	V
Operating supply voltage(6)	V_{VBAT6}	7	18	V
Normal functionality	T_j	–40	+150	°C
Normal functionality, overtemperature warning	T_j	150	165	°C
Drivers for H1, H2, L1, L2, and LIN are switched OFF, VCC regulator is OFF	T_j	165	180	°C

Note: 1. Full functionality
2. H-bridge drivers are switched off (undervoltage detection)
3. H-bridge drivers are switched off, 5V/3.3V regulator with reduced parameters, RESET works correctly
4. H-bridge drivers are switched off, 5V regulator not working, RESET not correct
5. H-bridge drivers are switched off
6. Full LIN functionality in conformance with LIN specification 2.1

7. Noise and Surge Immunity, ESD and Latch-up

Parameters	Standard and Test Conditions	Value
Conducted interferences	ISO 7637-1	Level 4(1)
Conducted disturbances	CISP25	Level 5
ESD according to IBEE LIN EMC - Pins LIN, PBAT, VBAT - Pin EN2 (33 kΩ serial resistor)	Test specification 1.0 following IEC 61000-4-2	 ±6 kV ±5 kV
ESD HBM with 1.5 kΩ/100 pF	ESD- STM5.1-2001 JESD22-A114E 2007 CEI/IEC 60749-26: 2006 AEC-Q100-002-Ref_D	±4 kV
ESD HBM with 1.5 kΩ/100 pF Pins EN2, LIN, PBAT, VBAT against GND	ESD- STM5.1-2001 JESD22-A114E 2007 CEI/IEC 60749-26: 2006 AEC-Q100-002-Ref_D	±8 kV
ESD CDM (field induced method)	ESD STM5.3.1 - 1999	±1 kV

Note: 1. Test pulse 5: $V_{bat\ max}$ = 40V

Static latch-up tested according to AEC-Q100-004 and JESD78.

- 3 to 6 samples, 0 failures
- Electrical post stress testing at room temperature

In test, the voltage at the pins VBAT, LIN, CP, VBATSW, Hx, and Sx must not exceed 45V when not able to drive the specified current.

8. Electrical Characteristics

All parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 125°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Power Supply and Supervisor Functions**								
1.1	Current consumption V_{VBAT}	V_{VBAT} = 13.5V(1)	25, 30	I_{VBAT1}			7	mA	A
1.2	Current consumption V_{VBAT} in Standby mode	V_{VBAT} =13.5V	25, 30	I_{VBAT2}			50	µA	A
1.3	Internal power supply		2	V_{INT}	4.8	4.94	5.1	V	A
1.4	Band gap voltage		3	V_{BG}	1.225	1.235	1.245	V	A
1.5	Overvoltage threshold Up V_{VBAT}		30	V_{THOV_UP}	21.2		22.7	V	A
1.5.1	Overvoltage threshold Down V_{VBAT}		30	V_{THOV_DOWN}	19.8		21.3	V	A
1.6	Overvoltage threshold hysteresis V_{VBAT}		30	V_{TOVhys}	1		2.4	V	A
1.7	Undervoltage threshold Up V_{VBAT}		30	V_{THUV_UP}	6.8		7.4	V	A
1.7.1	Undervoltage threshold Down V_{VBAT}		30	V_{THUV_DOWN}	6.5		7.0	V	A
1.8	Undervoltage threshold hysteresis V_{VBAT}	Measured during qualification only	30	V_{TUVhys}	0.2		0.6	V	A
1.9	On resistance of V_{VBAT} switch	V_{VBAT} = 13.5V	31	R_{ON_VBATSW}			100	Ω	A
2	**5V/3.3V Regulator**								
2.1	Regulated output voltage	9V < V_{VBAT} < 40V I_{load} = 0 mA to 100 mA	29	V_{CC1}	4.85 (3.2)		5.15 (3.4)	V	A
2.2	Regulated output voltage	6V < $V_{VBAT} \le$ 9V I_{load} = 0 mA to 100 mA	29	V_{CC2}	4.75 (3.2)		5.25 (3.4)	V	A
2.3	Line regulation	I_{load} = 0 mA to 100 mA	29	DC line regulation		<1	50	mV	A
2.4	Load regulation	I_{load} = 0 mA to 100 mA	29	DC load regulation		<10	50	mV	A
2.5	Output current limitation	V_{VBAT} > 6V	29	I_{OS1}	100		350	mA	A
2.6	Serial inductance to C_{VCC} including PCB		29	ESL	1		20	nH	D

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6. Tested during characterization only
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8. See section "Cross Conduction Time"
9. Voltage between source-drain of external switching transistors in active case
10. The short-circuit message will never be generated for switch-on time < t_{sc}

8. Electrical Characteristics (Continued)

All parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta$ambient $\le 125°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.7	Serial resistance to C_{VCC} including PCB		29	ESR	0		0.5	Ω	D
2.8	Blocking cap at VCC	(2), (3)	29	C_{VCC}	1.1		3.3	µF	D
2.9	HIGH threshold VMODE		1	VMODE H			4.0	V	A
2.10	LOW threshold VMODE		1	VMODE L	0.7			V	A
3	**Reset and Watchdog**								
3.1	V_{CC} threshold voltage level for /RESET	VMODE = “H” (VMODE = “L”)	29	V_{tHRESH}			4.9 (3.25)	V	A
3.1a	Tracking of reset threshold with regulated output voltage	VMODE = “H” (VMODE = “L”)	29	$V_{VCC1-VtHRESH}$	75 (50)			mV	A
3.2	V_{CC} threshold voltage level for /RESET	VMODE = “H” (VMODE = “L”)	29	V_{tHRESL}	4.3 (2.86)			V	A
3.3	Hysteresis of /RESET level	VMODE = “H” (VMODE = “L”)(4)	29	HYS_{RESth}	70	200	350 (220)	mV	A
3.4	Length of pulse at /RESET pin	(5)	5	t_{res}		6800		T_{100}	A
3.5	Length of short pulse at /RESET pin	(5)	5	$t_{resshort}$		200		T_{100}	A
3.6	Wait for the first WD trigger	(5)	5	t_d		6800		T_{100}	A
3.7	Time for VCC < V_{tHRESL} before activating /RESET	(4)	29	$t_{delayRESL}$	0.5		2	µs	C
3.8	Resistor defining internal bias currents for watchdog oscillator		3	R_{RWD}	10		91	kΩ	D
3.9	Watchdog oscillator period	R_{RWD} = 33 kΩ	3	T_{OSC}	11.09		13.55	µs	A
3.11	Watchdog input low-voltage threshold		6	V_{ILWD}			$0.3 \times V_{VCC}$	V	A
3.12	Watchdog input high-voltage threshold		6	V_{IHWD}	$0.7 \times V_{VCC}$			V	A
3.13	Hysteresis of watchdog input voltage threshold		6	V_{hysWD}	0.3		0.7	V	A
3.14	Close window	(5)	6	t1		$980 \times T_{OSC}$			A

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8. Electrical Characteristics (Continued)

All parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 125°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
3.15	Open window	(5)	6	t2		$780 \times T_{OSC}$			A
3.16	Output low-voltage of /RESET	At I_{OLRES} = 1 mA	5	V_{OLRES}			0.4	V	A
3.17	Internal pull-up resistor at pin /RESET		5	R_{PURES}	5	10	15	kΩ	A
4	**LIN Transceiver, 7V ≤ V_{VBAT} ≤ 18V**								
4.1	Low-level output current	Normal mode; V_{LIN} = 0V, V_{RX} = 0.4V	13	IL_{RXD}	2			mA	A
4.2	High-level output current	Normal mode; $V_{LIN} = V_{VBAT}$ $V_{RX} = V_{CC} - 0.4V$	13	IH_{RXD}	1			mA	A
4.3	Driver recessive output voltage	R_{LOAD} = 1000Ω to VBAT	8	$V_{BUSrecdrv}$	$0.9 \times V_{VBAT}$			V	A
4.4	Driver dominant voltage $V_{BUSdom_DRV_LoSUP}$	V_{VBAT} = 7.0V R_{load} = 500Ω	8	$V_{_LoSUP}$			1.2	V	A
4.5	Driver dominant voltage $V_{BUSdom_DRV_HiSUP}$	V_{VBAT} = 18V R_{load} = 500Ω	8	$V_{_HiSUP}$			2	V	A
4.6	Driver dominant voltage $V_{BUSdom_DRV_LoSUP}$	V_{VBAT} = 7.0V R_{load} = 1000Ω	8	$V_{_LoSUP_1k}$	0.6			V	A
4.7	Driver dominant voltage $V_{BUSdom_DRV_HiSUP}$	V_{VBAT} = 18V R_{load} = 1000Ω	8	$V_{_HiSUP_1k_}$	0.8			V	A
4.8	Pull up resistor to VS	serial diode required	8	R_{LIN}	20		47	kΩ	A
4.9	Current limitation	$V_{BUS} = V_{VBAT_max}$	8	I_{BUS_LIM}	50		200	mA	A
4.10	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current driver off V_{BUS} = 0V V_{VBAT} = 12V	8	$I_{BUS_PAS_dom}$	–1			mA	A
4.11	Leakage current LIN recessive	Driver off 7V < V_{VBAT} < 18V 7V < V_{BUS} < 18V $V_{BUS} = V_{VBAT}$	8	$I_{BUS_PAS_rec}$			20	µA	A

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6. Tested during characterization only
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8. See section "Cross Conduction Time"
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8. Electrical Characteristics (Continued)

All parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 125°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.12	Leakage current at ground loss Control unit disconnected from ground Loss of local ground must not affect communication in the residual network	$7V < V_{VBAT} < 18V$ $GND_{Device} = VS$ $V_{VBAT} = 12V$ $0V < V_{BUS} < 18V$	8	$I_{BUS_NO_gnd}$	–1		+1	mA	A
4.13	Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition	$7V < V_{VBAT} < 18V$ V_{VBAT} disconnected $V_{SUP_Device} = GND$ $0V < V_{BUS} < 18V$	8	I_{BUS}			100	µA	A
4.14	Center of receiver threshold	$7V < V_{VBAT} < 18V$ $V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2$	8	V_{BUS_CNT}	$0.475 \times V_{VBAT}$	$0.5 \times V_{VBAT}$	$0.525 \times V_{VBAT}$	V	A
4.15	Receiver dominant state	$7V < V_{VBAT} < 18V$ $V_{EN} = 5V$	8	V_{BUSdom}			$0.4 \times V_{VBAT}$	V	A
4.16	Receiver recessive state	$7V < V_{VBAT} < 18V$ $V_{EN} = 5V$	8	V_{BUSrec}	$0.6 \times V_{VBAT}$			V	A
4.17	Receiver input hysteresis	$7V < V_{VBAT} < 18V$ $V_{HYS} = V_{th_rec} - V_{th_dom}$	8	V_{BUShys}			$0.175 \times V_{VBAT}$	V	A
4.18	Duty cycle 1	$7V < V_{VBAT} < 18V$ $TH_{rec(max)} = 0.744 \times V_{VBAT}$ $TH_{Dom(max)} = 0.581 \times V_{VBAT}$ $t_{Bit} = 50$ µs $D1 = t_{Bus_rec(min)}/(2 \times t_{Bit})$ Load1: 1 nF + 1 kΩ Load2: 10 nF + 500Ω	8	D1	0.396				A
4.19	Duty cycle 2	$7V < V_{VBAT} < 18V$ $TH_{rec(min)} = 0.422 \times V_{VBAT}$ $TH_{Dom(min)} = 0.284 \times V_{VBAT}$ $t_{Bit} = 50$ µs $D2 = t_{Bus_rec(max)}/(2 \times t_{Bit})$ Load1: 1 nF + 1 kΩ Load2: 10 nF + 500Ω	8	D2			0.581		A

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6. Tested during characterization only
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8. See section "Cross Conduction Time"
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8. Electrical Characteristics (Continued)

All parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 125°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.20	Duty cycle 3	$7V < V_{VBAT} < 18V$ $TH_{rec(max)} = 0.778 \times V_{VBAT}$ $TH_{Dom(max)} = 0.616 \times V_{VBAT}$ $t_{Bit} = 96\ \mu s$ $D3 = t_{Bus_rec(min)}/(2 \times t_{Bit})$ Load1: 1 nF + 1 kΩ Load2: 10 nF + 500Ω	8	D3	0.417				A
4.21	Duty cycle 4	$7V < V_{VBAT} < 18V$ $TH_{rec(min)} = 0.389 \times V_{VBAT}$ $TH_{Dom(min)} = 0.251 \times V_{VBAT}$ $t_{Bit} = 96\ \mu s$ $D4 = t_{Bus_rec(max)}/(2 \times t_{Bit})$ Load1: 1 nF + 1 kΩ Load2: 10 nF + 500Ω	8	D4			0.590		A
4.22	Receiver propagation delay	$7V < V_{VBAT} < 18V$ $t_{rec_pd} = \max(t_{rx_pdr}, t_{rx_pdf})$	13	t_{rx_pd}			6	µs	A
4.23	Symmetry of receiver propagation delay rising edge minus falling edge	$7V < V_{VBAT} < 18V$ $t_{rx_sym} = t_{rx_pdr} - t_{rx_pdf}$	13	t_{rx_sym}	–2		+2	µs	
4.24	Dominant time for wake-up via LIN-bus	$7V < V_{VBAT} < 18V$ $V_{LIN} = 0V$	8	T_{BUS}	30	90	150	µs	A
5	**Control Inputs EN1, DIR, PWM, WD, TX**								
5.1	Input low-voltage threshold		12, 10, 11, 6, 9	V_{IL}			$0.3 \times V_{VCC}$	V	A
5.2	Input high-voltage threshold		12, 10, 11, 6, 9	V_{IH}	$0.7 \times V_{VCC}$			V	A
5.3	Hysteresis		12, 10, 11, 6, 9	HYS	0.3	0.5	0.7	V	A
5.4	Pull-down resistor	EN1, DIR, PWM, WD	12, 10, 11, 6,	R_{PD}	25	50	100	kΩ	A
5.5	Pull-up resistor	TX	9	R_{PU}	25	50	100	kΩ	A
5.6	Rise/fall time		12, 10, 11, 6, 9	t_{rf}			100	ns	D
5.7	Debounce time EN1	(6)	12	t_{db}	$2 \times T_{100}$		$3 \times T_{100}$	µs	B

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6. Tested during characterization only
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8. See section "Cross Conduction Time"
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8. Electrical Characteristics (Continued)

All parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 125°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6	**Charge Pump**								
6.1	Charge pump voltage	Load = 0A	21	VCP			V_{VBAT} + V_{VG}	V	A
6.2	Charge pump voltage	Load = 3 mA, C_{CP} = 100 nF	21	VCP	V_{VBAT} + V_{VG} – 1			V	A
6.3	Period charge pump oscillator		21	T_{100}	9		11	µs	A
6.4	CP load current in VG without CP load	Load = 0A	24	I_{VGCPz}			0.6	mA	A
6.5	CP load current in VG with CP load	Load = 3 mA, C_{CP} = 100 nF	24	I_{VGCP}			4	mA	A
6.6	Charge pump OK threshold UP		21	V_{CPOK_UP}	TBD	5.6	TBD	V	A
6.7	Charge pump OK threshold DOWN		21	V_{CPOK_DOWN}	TBD	4.8	TBD	V	A
7	**H-bridge Driver**								
7.1	Low-side driver HIGH output voltage		26, 27	V_{LxH}	V_{VG} – 0.5V		V_{VG}	V	A
7.2	ON-resistance of sink stage of pins L1, L2		26, 27	R_{DSON_LxL}, x = 1, 2			20	Ω	A
7.3	ON-resistance of source stage of pins L1, L2		26, 27	R_{DSON_LxH}, x = 1, 2			20	Ω	A
7.4	Output peak current at pins L1, L2, switched to LOW	V_{Lx} = 3V	26, 27	I_{LxL}, x = 1, 2	100			mA	A
7.5	Output peak current at pins L1, L2, switched to HIGH	V_{Lx} = 3V	26, 27	I_{LxH}, x = 1, 2			–100	mA	A
7.6	Pull-down resistance at pins L1, L2		26, 27	R_{PDLx} x = 1, 2	30		140	kΩ	A
7.7	ON-resistance of sink stage of pins H1, H2	V_{Sx} = 0	18, 20	R_{DSON_HxL}, x = 1, 2			20	Ω	A
7.8	ON-resistance of source stage of pins H1, H2	$V_{Sx} = V_{VBAT}$	18, 20	R_{DSON_HxH}, x = 1, 2			20	Ω	A

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8. Electrical Characteristics (Continued)

All parameters given are valid for $V_{THUV} \le V_{VBAT} \le V_{THOV}$ and for $-40°C \le \vartheta_{ambient} \le 125°C$ unless stated otherwise.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.9	Output peak current at pins Hx, switched to LOW	V_{VBAT} = 13.5V $V_{Sx} = V_{VBAT}$ $V_{Hx} = V_{VBAT}$ + 3V	18, 20	I_{HxL}, x = 1, 2	100			mA	A
7.10	Output peak current at pins Hx, switched to HIGH	V_{VBAT} = 13.5V $V_{Sx} = V_{VBAT}$ $V_{Hx} = V_{VBAT}$ + 3V	18, 20	I_{HxH}, x = 1, 2			–100	mA	A
7.11	Static switch output low voltage at pins Hx and Lx	V_{Sx} = 0V I_{Hx} = 1 mA I_{Lx} = 1 mA	18, 20, 26, 27	V_{HxL}, V_{LxL} x = 1, 2			0.3	V	A
7.12	Static high-side switch output high-voltage pins H1, H2	I_{Lx} = –10 µA (PWM = static)	18, 20	$V_{HxHstat1}$ (7)	V_{VBAT} + V_{VG} – 1		V_{VBAT} + V_{VG}	V	A
7.13	Sink resistance between Hx and Sx	$V_{VBAT} = V_{PBAT}$ = 9V, I_VG = –20 mA	17, 18, 19, 20	R_{PDHx}	30		150	kΩ	A
	Dynamic Parameters								
7.15	Propagation delay time, low-side driver from high to low	Figure 3-6 on page 13 V_{VBAT} = 13.5V	26, 27	t_{LxHL}			0.5	µs	A
7.16	Propagation delay time, low-side driver from low to high	V_{VBAT} = 13.5V	26, 27	t_{LxLH}			0.5 + t_{CC}	µs	A
7.17	Fall time low-side driver	V_{VBAT} = 13.5V C_{Gx}=5 nF	26, 27	t_{Lxf}			0.5	µs	A
7.18	Rise time low-side driver	V_{VBAT} = 13.5V	26, 27	t_{Lxr}			0.5	µs	A
7.19	Propagation delay time, high-side driver from high to low	Figure 3-6 on page 13 V_{VBAT} = 13.5V	18, 20	t_{HxHL}			0.5	µs	A
7.20	Propagation delay time, high-side driver from low to high	V_{VBAT} = 13.5V	18, 20	t_{HxLH}			0.5 + t_{CC}	µs	A
7.21	Fall time high-side driver	V_{VBAT} = 13.5V, C_{Gx} = 5 nF	18, 20	t_{Hxf}			0.5	µs	A
7.22	Rise time high-side driver	V_{VBAT} = 13.5V	18, 20	t_{Hxr}			0.5	µs	A
7.23	Cross conduction time	R_{CC} = 10 kΩ, C_{CC} = 1 nF(8)	4	t_{CC}	3.75		4.45	µs	A
7.24	External resistor		4	R_{CC}	5			kΩ	D

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.25	External capacitor		4	C_{CC}			5	nF	D
7.26	R_{ON} of t_{CC} switching transistor		4	R_{ONCC}			200	Ω	A
7.28	Short circuit detection voltage	(9)	17, 19	V_{SC}	3.5	4	4.7	V	A
7.29	Short circuit detection time	(10)	17, 19	t_{SC}	5	10	15	µs	A
7.30	VG regulator output voltage	$V_{VBAT} = V_{PBAT} = 18V$, I_VG = –20 mA	24	V_{VG}	11		14	V	A
7.31	VG regulator output voltage switch mode	$V_{VBAT} = V_{PBAT} = 9V$, I_VG = –20 mA	24	$V_{VGswitch}$	11		14	V	A
8	**Input EN2**								
8.1	Input low-voltage threshold		32	V_{IL}	2.3		3.6	V	A
8.2	Input high-voltage threshold		32	V_{IH}	2.8		4.0	V	A
8.3	Hysteresis	(6)	32	HYS		0.47		V	A
8.4	Pull-down resistor		32	R_{PD}	50	100	200	kΩ	A
8.5	Rise/fall time		32	t_{rf}			100	ns	D
8.6	Debounce time	(6)	32	t_{db}	$2 \times T_{100}$		$3 \times T_{100}$	µs	B
9	**Diagnostic Outputs DG1, DG2, DG3**								
9.1	Low level output current	$V_{DG} = 0.4V$(6)	15, 16	IL	2			mA	A
9.2	High level output current	$V_{DG} = VCC - 0.4V$(6)	15, 16	IH	1			mA	A

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1. EN, DIR, PWM = high
2. The use of X7R material is recommended
3. For higher values, stability at zero load is not guaranteed
4. Tested during qualification only
5. Value depends on T_{OSC}; function tested with digital test pattern
6. Tested during characterization only
7. Supplied by charge pump
8. See section "Cross Conduction Time"
9. Voltage between source-drain of external switching transistors in active case
10. The short-circuit message will never be generated for switch-on time < t_{sc}

9. Application

9.1 General Remark

This chapter describes the principal application for which the ATA6823 was designed. Because Atmel® cannot be considered to understand fully all aspects of the system, application, and environment, no warranties of fitness for a particular purpose are given.

Table 9-1. Typical External Components

Component	Function	Value	Tolerance
C_{VINT}	Blocking capacitor at VINT	220 nF, 10V, X7R	50%
C_{VCC}	Blocking capacitor at VCC	2.2 µF, 10V, X7R	50%
C_{CC}	Cross conduction time definition capacitor	Typical 330 pF, 100V, COG	
R_{CC}	Cross conduction time definition resistor	Typical 10 kΩ	
C_{VG}	Blocking capacitor at VG	Typical 470 nF, 25V, X7R	50%
C_{CP}	Charge pump capacitor	Typical 220 nF, 25V, X7R	
C_{VRES}	Reservoir capacitor	Typical 470 nF, 25V, X7R	
R_{RWD}	Watchdog time definition resistor	Typical 51 kΩ	
R_{LIN}	Pull-up resistor for LIN bus (master only)	Typical 1 kΩ	
C_{LIN}	Filter capacitor for LIN bus	Typical 220 pF, 100V	

10. Errata

10.1 Faulty Pulse at DG1

A faulty pulse of approximately 100 ns appears at pin 16 (DG1), signalizing short circuit condition, under following circumstances:

General condition: PWM = HIGH

and

detected undervoltage of VBAT (signalized at pin 15 = DG2)

or

detected overvoltage of VBAT (signalized at pin 15 = DG2)

or

detected undervoltage of the charge pump (signalized at pin 15 = DG2)

or

overtemperature shutdown.

10.2 Problem Fix/Workaround

Set the software to ignore the faulty pulse.

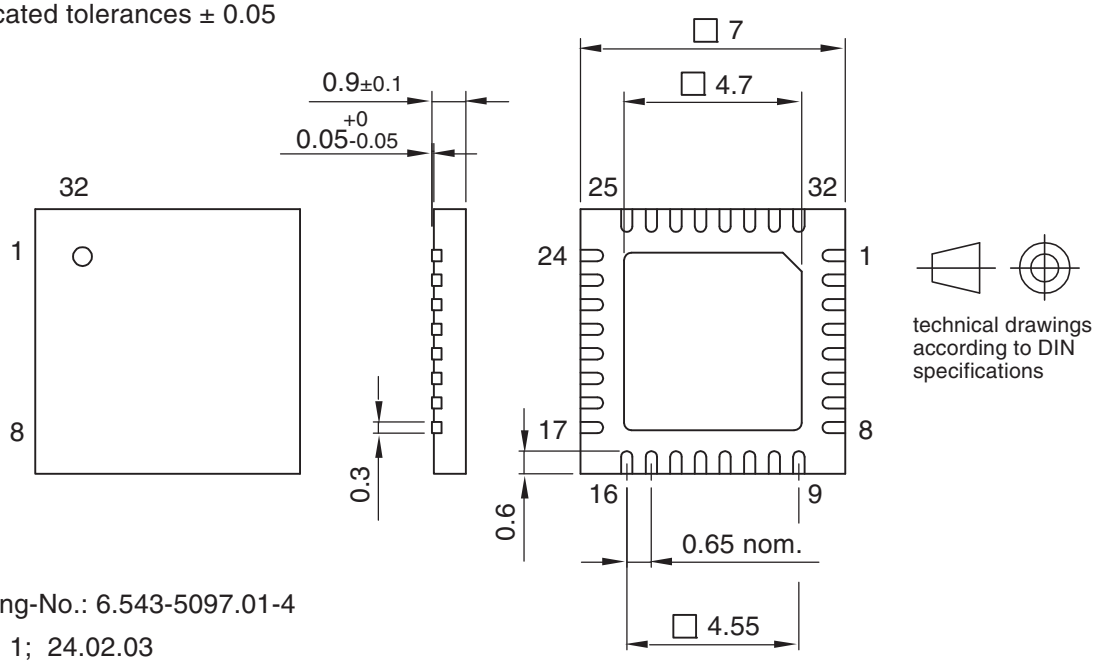
11. Ordering Information

Extended Type Number	Package	Remarks
ATA6823-PHQW	QFN32	Pb-free

12. Package Information

Package: QFN 32 - 7 x 7
Exposed pad 4.7 x 4.7
Dimensions in mm

Not indicated tolerances ± 0.05



Drawing-No.: 6.543-5097.01-4
Issue: 1; 24.02.03

13. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4856H-AUTO-07/09	• LIN 2.0 to LIN 2.1 in whole document changed • Section 6 “Operating Range” on page 16 changed • LIN Transceiver part in Section 8 “Electrical Characteristics” on pages 19 to 21 changed
4856G-AUTO-01/09	• Section 3 “General Statement and Conventions” on page 4 deleted • Section 4 “Application” from page 5 to page 24 removed • Figure 3-1 “Wake-up by pin LIN” on page 7 changed • Section 4 “Absolute Maximum Ratings” on page 15 changed • Section 5 “Thermal Resistance” on page 15 changed • Section 6 “Operating Range” on page 16 changed • Section 7 “Noise and Surge Immunity, ESD and Latch-up” on page 16 added • Section 8 “Electrical Characteristics” on pages 17 to 23 changed • Section 10 “Schaffner and Electromagentic Compatibility” on pages 24 to 26 deleted • Table 9-1 “Typical External Components” on page 24 changed • Section 10 “Errata” on page 24 added • Section 11 “ESD and Latch-up Requirements” on page 26 deleted
4856F-AUTO-01/08	• Section 5.4 “5V/3.3V VCC Regulator” on pages 8 to 9 changed • Section 10 “Electrical Characteristics” number 3.3 on page 18 changed • Section 12 “Ordering Information” on page 27 changed
4856E-AUTO-07/07	• Put datasheet in a new template

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
auto_control@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

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