SC2602L
Synchronous Voltage Mode Controller for Distributed Power Supply

Description

The SC2602L is low-cost, full featured, synchronous voltage-mode controller designed for use in single ended power supply applications where efficiency is of primary concern. Synchronous operation allows for the elimination of heat sinks in many applications. The SC2602L is ideal for implementing DC/DC converters needed to power advanced microprocessors in low cost systems, or in distributed power applications where efficiency is important. Internal level-shift, high-side drive circuitry, and preset shoot-through control, allows the use of inexpensive N-channel power MOSFETs.

SC2602L features include temperature compensated voltage reference, triangle wave oscillator and current sense comparator circuitry. Power good signaling, shutdown, and over voltage protection are also provided.

The SC2602L operates at a fixed 200kHz which is for optimum compromise between efficiency, external component size, and cost.

Two SC2602L can be used together to sequence two voltage regulators for power up in telecom systems. The power good of the first SC2602L connected to the enable of the second SC2602L makes this possible.

Features

- Synchronous operation for high efficiency (95%)
- $R_{DS(ON)}$ current sensing
- Output voltage can be programmed as low as 0.8V
- On-chip power good and OVP functions
- Small size with minimum external components
- Soft Start
- Enable function
- SO-14 package is fully WEEE and RoHS compliant

Applications

- Microprocessor core supply
- Low cost synchronous applications
- Voltage Regulator Modules (VRM)
- DDR termination supplies
- Networking power supplies
- Sequenced power supplies

Typical Application Circuit

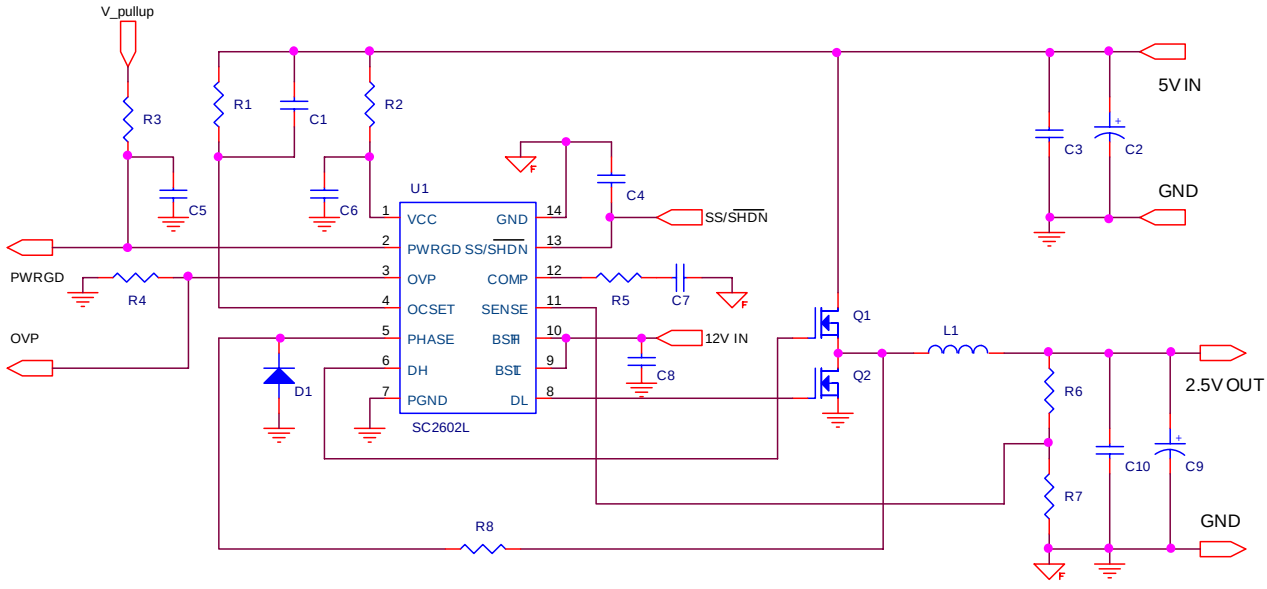


Figure 1. Typical distributed power supply

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
VCC, BSTL to GND	V_{IN}	-1.0 to 16 (20V Surge)	V
PGND to GND		± 0.5	V
PHASE to GND(1)		-0.5 to 18 (20V Surge)	V
BSTH to PHASE		16 (20V Surge)	V
Thermal Resistance Junction to Case	θ_{JC}	45	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	115	°C/W
Operating Temperature Range	T_A	-40 to +85	°C
Maximum Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	ESD	2	kV

Note: (1) -1.5V to 20V for 25ns repetitive every cycle.

Electrical Characteristics

Unless specified: V_{CC} = 4.75V to 12.6V; GND = PGND = 0V; V_{BSTL} = 12V; $V_{BSTH-PHASE}$ = 12V; T_J = 25°C

Parameter	Conditions	Min	Typ	Max	Units
Power Supply					
Supply Voltage	V_{CC}	4.2		12.6	V
Supply Current	EN = V_{CC}		6	10	mA
Line Regulation	V_O = 2.5V		0.5		%
Error Amplifier					
Transconductance	G_m		1.8		mS
Gain (AOL)			50		dB
Input Bias			5	8	µA
Oscillator					
Oscillator Frequency			200		kHz
Oscillator Max Duty Cycle		90	95		%
Internal Ramp Peak to Peak			1		V
MOSFET Drivers					
DH Source/Sink	BSTH - DH = 4.5V, DH - PHASE = 2V	1			A
DL Source/Sink	BSTL - DL = 4.5V. DL - PGND. = 2V	1			A

Electrical Characteristics (Cont.)

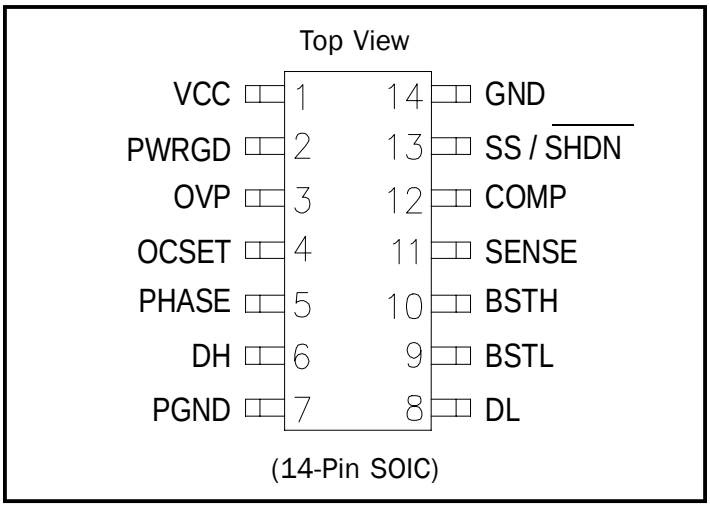
Unless specified: V_{CC} = 4.75V to 12.6V; GND = PGND = 0V; V_{BSTL} = 12V; $V_{BSTH-PHASE}$ = 12V; T_J = 25°C

Parameter	Conditions	Min	Typ	Max	Units
PROTECTION					
OVP Threshold Voltage			20		%
OVP Source Current	V_{OVP} = 3V	10			mA
Power Good Threshold		88		112	%
Dead Time		45		100	nS
Over Current Set (Isink)	2.0V < V_{OCSET} < 12V	180	200	220	µA
Reference					
Reference Voltage	0°C to 70°C	0.792	0.8	0.808	V
Soft Start					
Charge Current	V_{SS} = 1.5V	8.0	10	12	µA
Discharge Current	V_{SS} = 1.5V		1.5		µA
Power Good					
Sink Current Capability	Sink 1mA			0.4	V
Shut Down					
Shut Down Threshold			0.6		V

Note:

(1) Specification refers to application circuit (Figure 1).

Pin Configuration



Ordering Information

Device[2]	Frequency	Package[1]
SC2602LSTRT	200kHz	SO-14
SC2602LEVB	Evaluation Board	

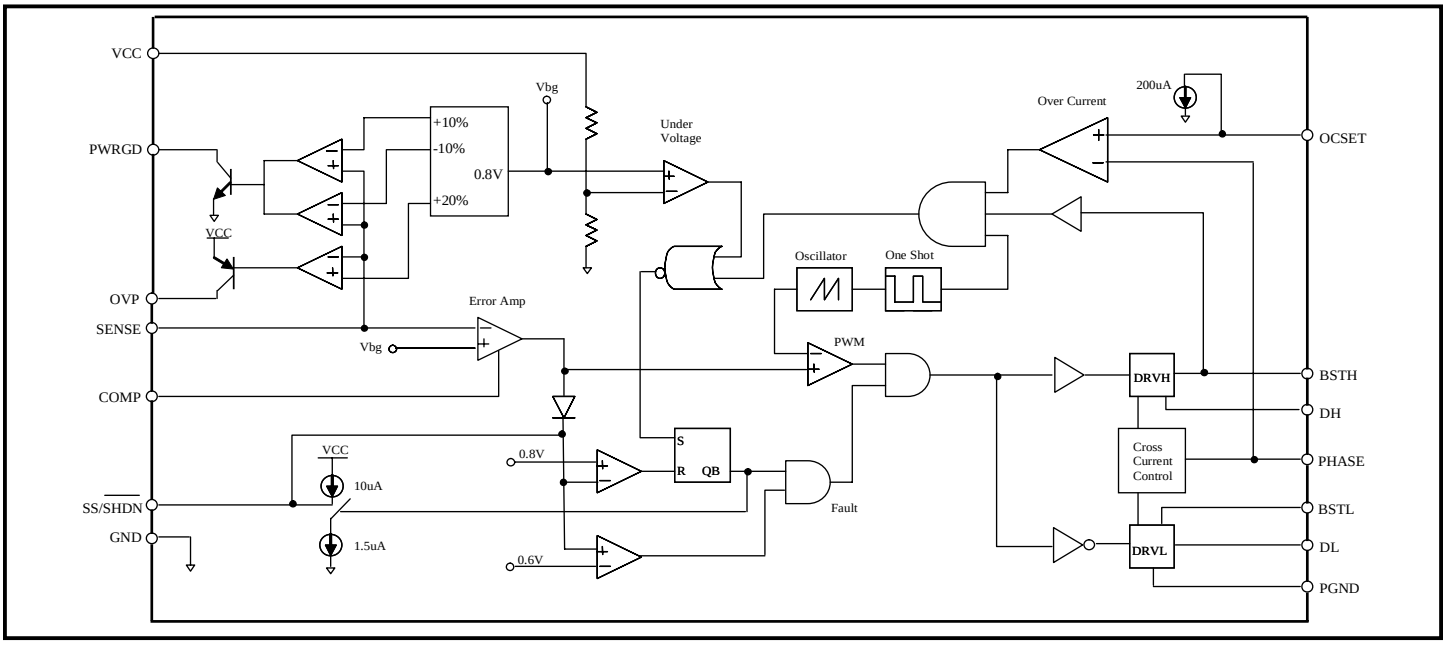
Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	VCC	Chip supply voltage.
2	PWRGD	Open collector output. Logic high indicates correct ouput voltage.
3	OVP	Over voltage protection output. Source at least 10mA when Vsense > 1.2 * $V_{BG.}$
4	OCSET	Set the converter over current trip point.
5	PHASE	Input from the phase node between the MOSFETs.
6	DH	High side driver output.
7	PGND	Power ground.
8	DL	Low side driver output.
9	BSTL	Bootstrap, low side driver.
10	BSTH	Bootstrap, high side driver.
11	SENSE	Voltage sense input.
12	COMP	Compensation pin.
13	$\overline{\text{SS/SHDN}}$	Gate Drive return Ground for the 1.5V GMCH regulator. Connect to Source of bottom FET.
14	GND	Signal ground.

Note:
(1) All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Theory of Operation

Synchronous Buck Converter

The output rail is regulated by a synchronous, voltage-mode pulse width modulated (PWM) controller. This section has all the features required to build a high efficiency synchronous buck converter, including "Power Good" flag, shut-down, and cycle-by-cycle current limit.

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The external resistive divider reference voltage is derived from an internal trimmed-bandgap voltage reference (See Fig. 1). The inverting input of the error amplifier receives its voltage from the SENSE pin.

The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 200kHz. The triangular output of the oscillator sets the reference voltage at the inverting input of the comparator. The non-inverting input of the comparator receives it's input voltage from the error amplifier. When the oscillator output voltage drops below the error amplifier output voltage, the comparator output goes high. This pulls DL low, turning off the low-side FET, and DH is pulled high, turning on the high-side FET (once the cross-current control allows it). When the oscillator voltage rises back above the error amplifier output voltage, the comparator output goes low. This pulls DH low, turning off the high-side FET, and DL is pulled high, turning on the low-side FET (once the cross-current control allows it).

As SENSE increases, the output voltage of the error amplifier decreases. This causes a reduction in the on-time of the high-side MOSFET connected to DH, hence lowering the output voltage.

Under Voltage Lockout

The under voltage lockout circuit of the SC2602L assures that the high-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 4.1V. Normal operation resumes once V_{CC} rises above 4.2V.

Over-Voltage Protection

The over-voltage protection pin (OVP) is high only when the voltage at SENSE is 20% higher than the target value programmed by the external resistor divider. The OVP pin is internally connected to a PNP's collector.

Power Good

The power good function is to confirm that the regulator outputs are within +/-10% of the programmed level. PWRGD remains high as long as this condition is met. PWRGD is connected to an internal open collector NPN transistor.

Applications Information (Cont.)

Soft Start

Initially, SS/$\overline{SHDN}$ sources 10µA of current to charge an external capacitor. The outputs of the error amplifiers are clamped to a voltage proportional to the voltage on SS/$\overline{SHDN}$. This limits the on-time of the high-side MOSFETs, thus leading to a controlled ramp-up of the output voltages.

$R_{DS(ON)}$ Current Limiting

The current limit threshold is set by connecting an external resistor from the V_{CC} supply to OCSET. The voltage drop across this resistor is due to the 200µA internal sink sets the voltage at the pin. This voltage is compared to the voltage at the PHASE node. This comparison is made only when the high-side drive is high to avoid false current limit triggering due to uncontributing measurements from the MOSFETs off-voltage. When the voltage at PHASE is less than the voltage at OCSET, an overcurrent condition occurs and the soft start cycle is initiated. The synchronous switch turns off and SS/$\overline{SHDN}$ starts to sink 1.5µA. When SS/$\overline{SHDN}$ reaches 0.8V, it then starts to source 10µA and a new cycle begins.

Hiccup Mode

During power up, the SS/$\overline{SHDN}$ pin is internally pulled low until VCC reaches the undervoltage lockout level of 4.2V. Once V_{CC} has reached 4.2V, the SS/$\overline{SHDN}$ pin is released and begins to source 10µA of current to the external soft-start capacitor. As the soft-start voltage rises, the output of the internal error amplifier is clamped to this voltage. When the error signal reaches the level of the internal triangular oscillator, which swings from 1V to 2V at a fixed frequency of 200kHz, switching occurs. As the error signal crosses over the oscillator signal, the duty cycle of the PWM signal continues to increase until the output comes into regulation. If an overcurrent condition has not occurred the soft-start voltage will continue to rise and level off at about 2.2V.

An over-current condition occurs when the high-side drive is turned on, but the PHASE node does not reach the voltage level set at the OCSET pin. The PHASE node is sampled only once per cycle during the valley of the triangular oscillator. Once an over-current occurs, the high-side drive is turned off and the low-side drive turns on and the SS/$\overline{SHDN}$ pin begins to sink 1.5µA. The soft-start voltage will begin to decrease as the 1.5µA of current discharges the external capacitor. When the soft-start voltage reaches 0.8V, the SS/$\overline{SHDN}$ pin will begin to source 10µA and begin to charge the external capacitor causing the soft-start voltage to rise again. Again, when the soft-start voltage reaches the level of the internal oscillator, switching will occur.

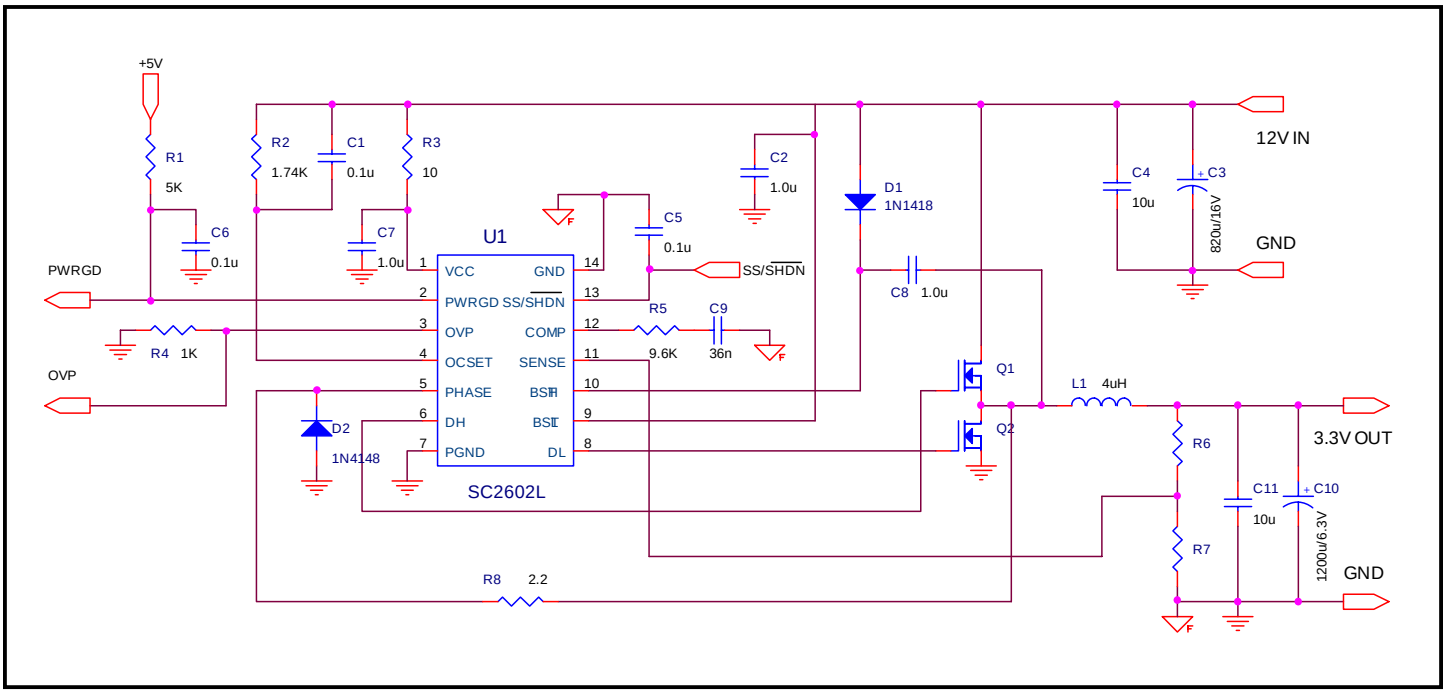
If the over-current condition is no longer present, normal operation will continue. If the over-current condition is still present, the SS/$\overline{SHDN}$ pin will again begin to sink 1.5µA. This cycle will continue indefinitely until the over-current condition is removed.

In conclusion, below is shown a typical “12V Application Circuit” which has a BSTH voltage derived by bootstrapping input voltage to the PHASE node through diode D1. This circuit is very useful in cases where only input power of 12V is available.

In order to prevent substrate glitching, a small-signal diode should be placed in close proximity to the chip with cathode connected to PHASE and anode connected to PGND.

Application Circuit

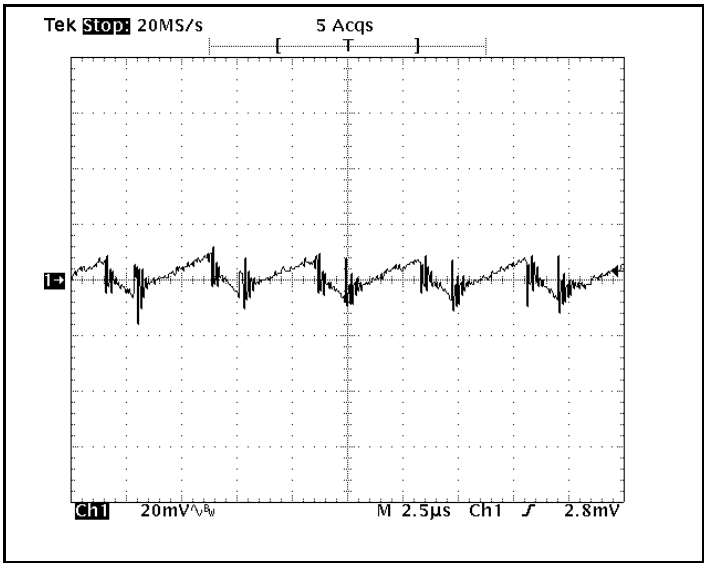
Typical 12V Application Circuit with Bootstrapped BSTH



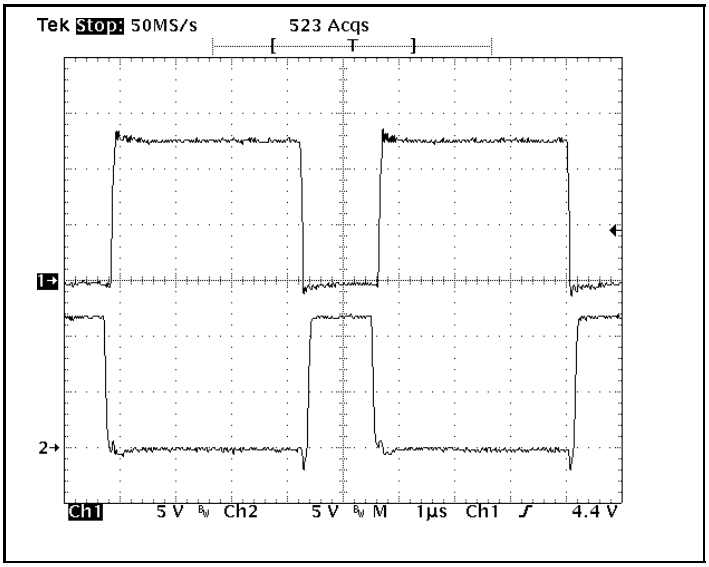
Typical Characteristics

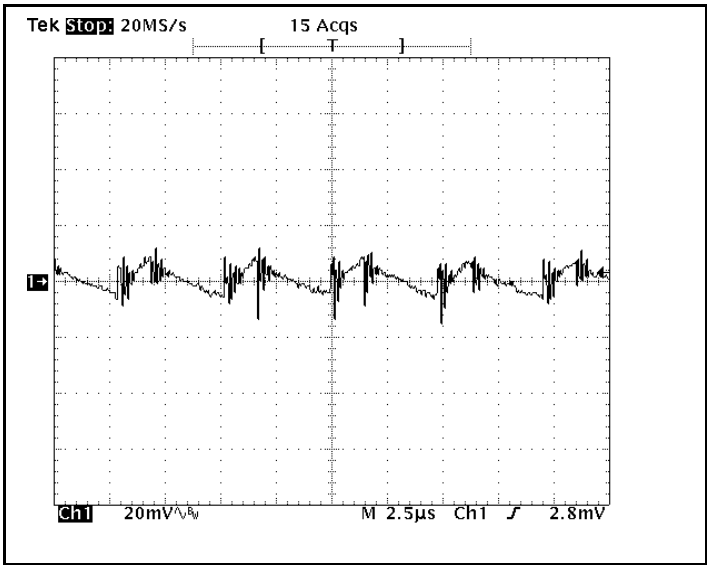
Output Ripple Voltage
Ch1: Vo_rpl

1. V_{IN} = 5V; V_O = 3.3V; I_{OUT} = 12A

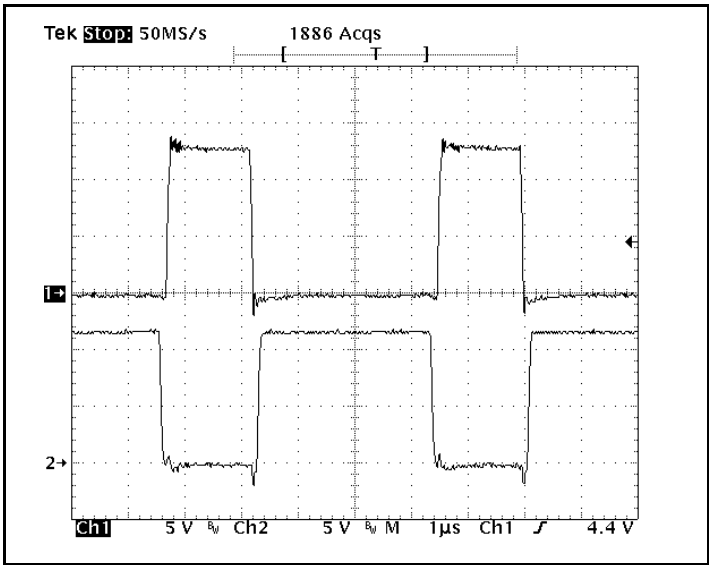


Gate Drive Waveforms
Ch1: Top FET
Ch2: Bottom FET





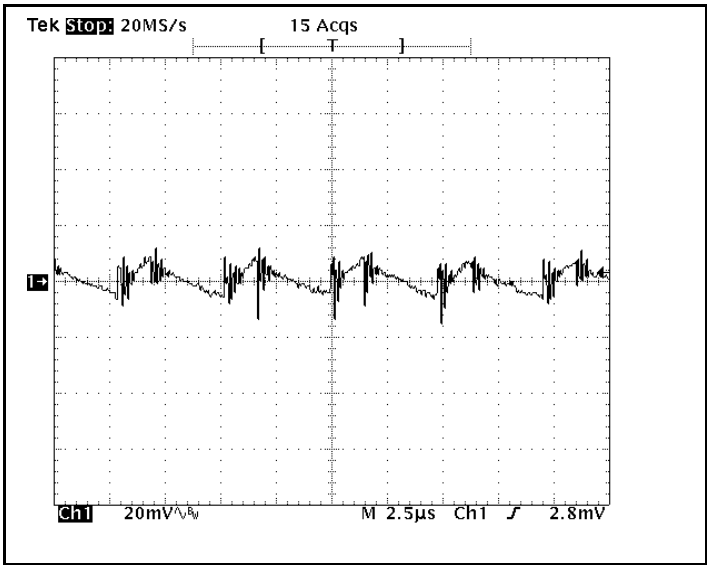
Ch1: Vo_rpl
2. V_{IN} = 5V; V_{OUT} = 1.3V; I_{OUT} = 12A



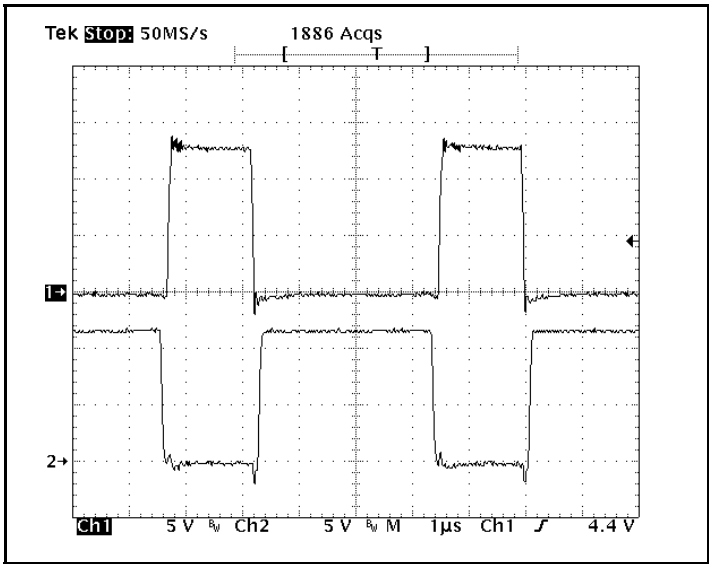
Ch1: Top FET
Ch2: Bottom FET

Typical Characteristics (Cont.)

Ch1: Vo_rpl
2. V_{IN} = 5V; V_{OUT} = 1.3V; I_{OUT} = 12A

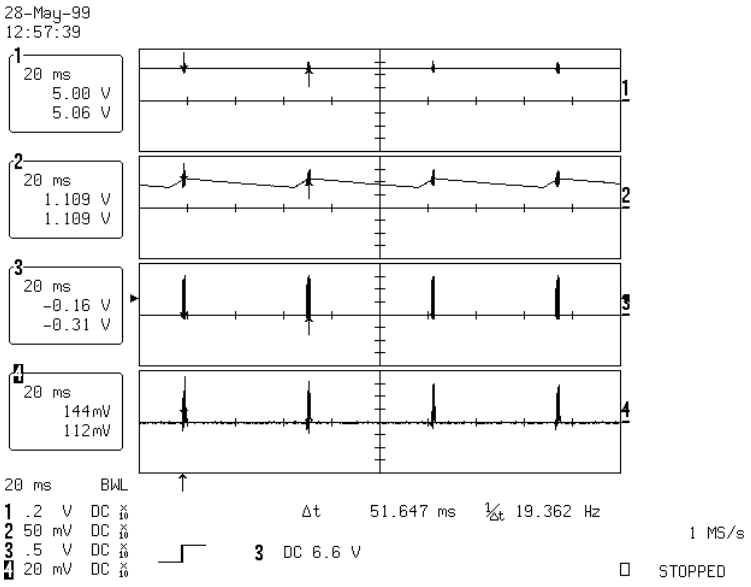


Ch1: Top FET
Ch2: Bottom FET



Typical Characteristics (Cont.)

Hiccup Mode

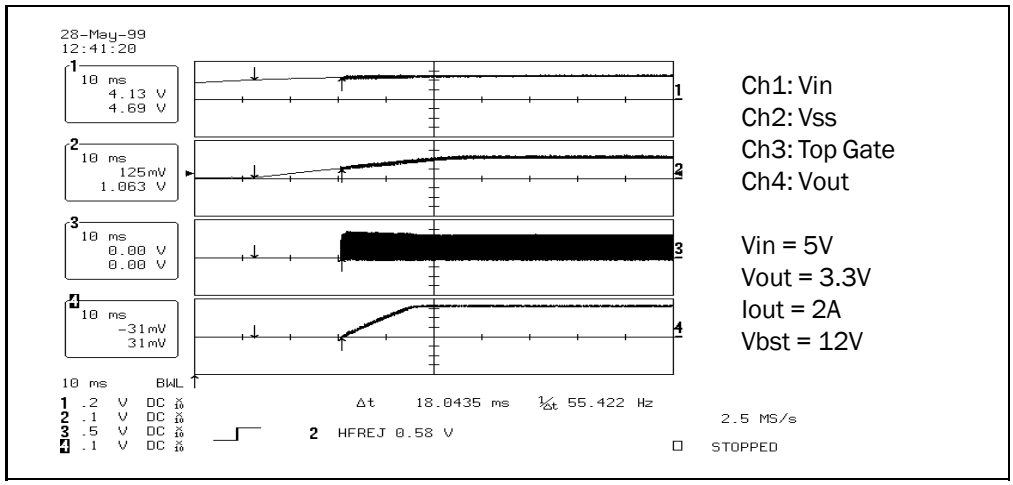


Ch1: Vin
Ch2: Vss
Ch3: Top Gate
Ch4: Vout

Vin = 5V
Vout = 3.3V
Vbst = 12V

Iout = S.C.

Start Up Mode



Ch1: Vin
Ch2: Vss
Ch3: Top Gate
Ch4: Vout

Vin = 5V
Vout = 3.3V
Iout = 2A
Vbst = 12V

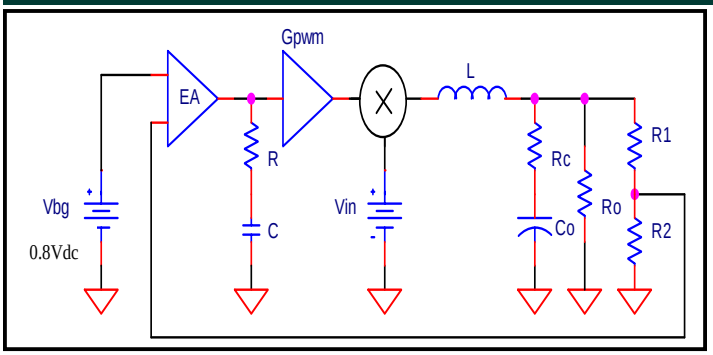


Fig. 2. SC2602L small signal model.

The control model of SC2602L control loop small signal can be depicted in Fig. 2. This model can also be used in SPICE kind of simulator to generate loop gain Bode plots. The bandgap reference is 0.8V and trimmed to +/-1% accuracy. The desired output voltage can be achieved by setting the resistive divider network, R1 and R2.

The error amplifier is transconductance type with fixed gain of:

$$G_m := \frac{1.8 \cdot mA}{V}$$

The compensation network includes a resistor and a capacitor in series, which terminates from the output of the error amplifier to the ground.

This device uses voltage mode control with input voltage feed forward. The peak-to-peak ramp voltage is proportional to the input voltage, which results in an excellent performance to reject input voltage variation. The PWM gain is inversion of the ramp amplitude, and this gain is given by:

$$G_{pwm} := \frac{1}{V_{ramp}}$$

where the ramp amplitude (peak-to-peak) is 1.0 volts when input voltage is 12 volts.
The total control loop-gain can then be derived as follows:

$$T(s) = T_o \cdot \left(\frac{1 + s \cdot R \cdot C}{s \cdot R \cdot C}\right) \cdot \frac{1 + s \cdot R_c \cdot C_o}{1 + s \cdot \left(R_c \cdot C_o + \frac{L}{R_o}\right) + s^2 \cdot L \cdot C_o \cdot \left(1 + \frac{R_c}{R_o}\right)}$$

$$T_o := G_m \cdot G_{pwm} \cdot V_{in} \cdot R \cdot \left(\frac{V_{bg}}{V_o}\right)$$

The task here is to properly choose the compensation network for a nicely shaped loop-gain Bode plot. The following design procedures are recommended to accomplish the goal:

(1) Calculate the corner frequency of the output filter:

$$F_o := \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_o}}$$

(2) Calculate the ESR zero frequency of the output filter capacitor:

$$F_{esr} := \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o}$$

(3) Check that the ESR zero frequency is not too high.

$$F_{esr} < \frac{F_{sw}}{5}$$

If this condition is not met, the compensation structure may not provide loop stability. The solution is to add some electrolytic capacitors to the output capacitor bank to correct the output filter corner frequency and the ESR zero frequency. In some cases, the filter inductance may also need to be adjusted to shift the filter corner frequency. It is not recommended to use only high frequency multi-layer ceramic capacitors for output filter.

(4) Choose the loop gain cross over frequency (0 dB frequency). It is recommended that the crossover frequency is always less than one fifth of the switching frequency :

$$F_{x_over} \le \frac{F_{sw}}{5}$$

If the transient specification is not stringent, it is better to choose a crossover frequency that is less than one tenth of the switching frequency for good noise immunity. The resistor in the compensation network can then be calculated as:

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_m} \cdot \left(\frac{F_{esr}}{F_o}\right)^2 \cdot \left(\frac{F_{x_over}}{F_{esr}}\right) \cdot \left(\frac{V_o}{V_{bg}}\right)$$

when

$$F_o < F_{esr} < F_{x_over}$$

Applications Information (Cont.)

or

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_m} \cdot \left(\frac{F_o}{F_{esr}} \right)^2 \cdot \left(\frac{F_{x_over}}{F_o} \right) \cdot \left(\frac{V_o}{V_{bg}} \right)$$

when

$$F_{esr} < F_o < F_{x_over}$$

(5) The compensation capacitor is determined by choosing the compensator zero to be about one fifth of the output filter corner frequency:

$$F_{zero} := \frac{F_o}{5}$$

$$C := \frac{1}{2 \cdot \pi \cdot R \cdot F_{zero}}$$

(6) The final step is to generate the Bode plot, either by using the simulation model in Fig. 2 or using the equations provided here with Mathcad. The phase margin can then be checked using the Bode plot. Usually, this design procedure ensures a healthy phase margin.
(7) An additional capacitor should be reserved at the compensation pin to ground to have another high frequency pole.
An example is given below to demonstrate the procedure introduced above. The parameters of the power supply are given as :

The parameters of the power supply are given as :

$$V_{in} := 12 \cdot V$$

$$V_o := 3.3 \cdot V$$

$$I_o := 12 \cdot A$$

$$F_{sw} := 200 \cdot KHz$$

$$L := 4 \cdot \mu H$$

$$C_o := 1200 \cdot \mu F$$

$$R_c := 0.02 \cdot \Omega$$

$$V_{bg} := 0.8 \cdot V$$

$$V_{ramp} := 1 \cdot V$$

$$G_m := \frac{1.8 \cdot mA}{V}$$

Step 1. Output filter corner frequency

$$F_o = 2.516 \cdot KHz$$

Step 2. ESR zero frequency:

$$F_{esr} = 7.958 \cdot KHz$$

Step 3. Check the following condition:

$$F_{esr} < \frac{F_{sw}}{5}$$

Which is satisfied in this case.

Step 4. Choose crossover frequency and calculate compensator R:

$$F_{x_over} = 20 \cdot KHz$$

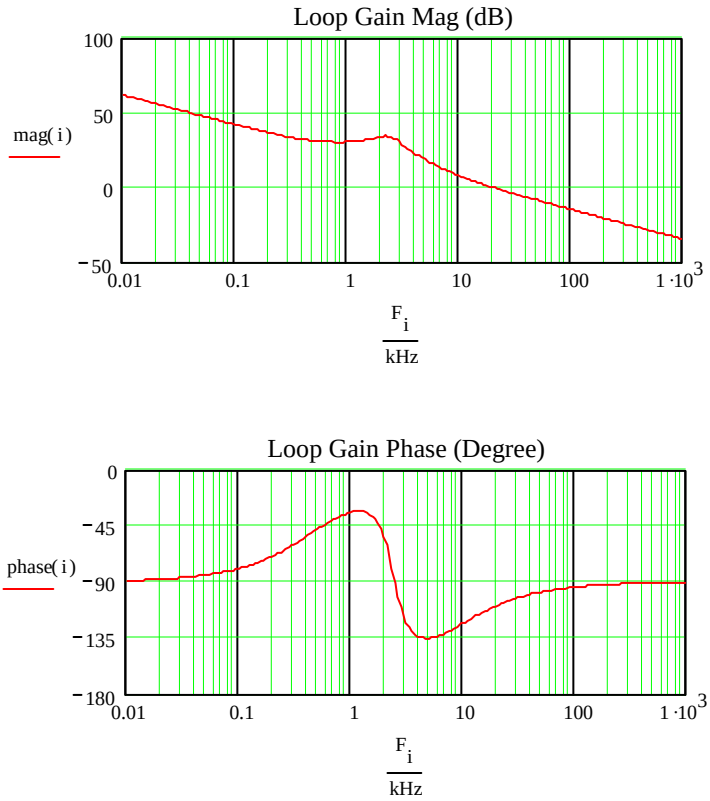
$$R = 4.8 \cdot K\Omega$$

Step 5. Calculate the compensator C:

$$C = 65.886 \cdot nF$$

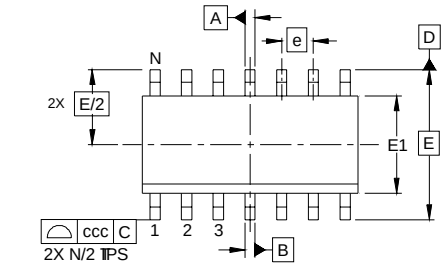
Step 6. Generate Bode plot and check the phase margin. In this case, the phase margin is about 85°C that ensures the loop stability.

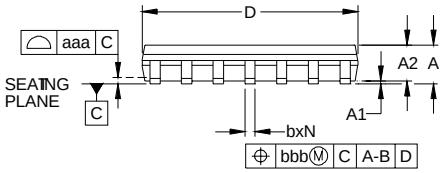
Applications Information (Cont.)

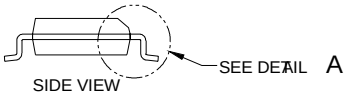


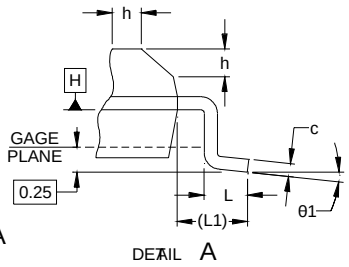
Bode plot of the control loop

Outline Drawing - S0-14







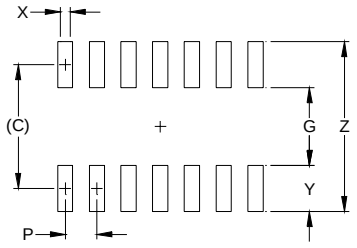


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.337	.341	.344	8.55	8.65	8.75
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	14			14		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AB.

Land Pattern - S0-14



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET
2. REFERENCE IPC-SM-782A, RLP NO. 302A.

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