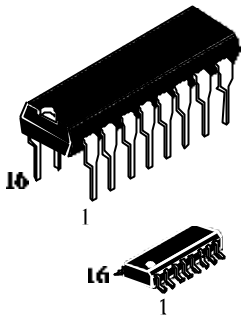
Presettable BCD/Decade UP/DOWN Counter

High-Performance Silicon-Gate CMOS



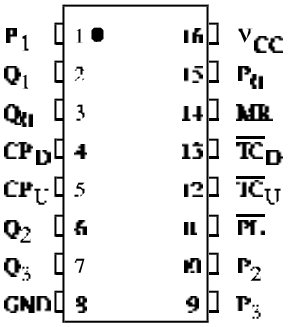
ORDERING INFORMATION
SL74HC192N Plastic
SL74HC192D SOIC
T_A = -55° to 125° C for all packages

The SL74HC192 is identical in pinout to the LS/ALS192. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

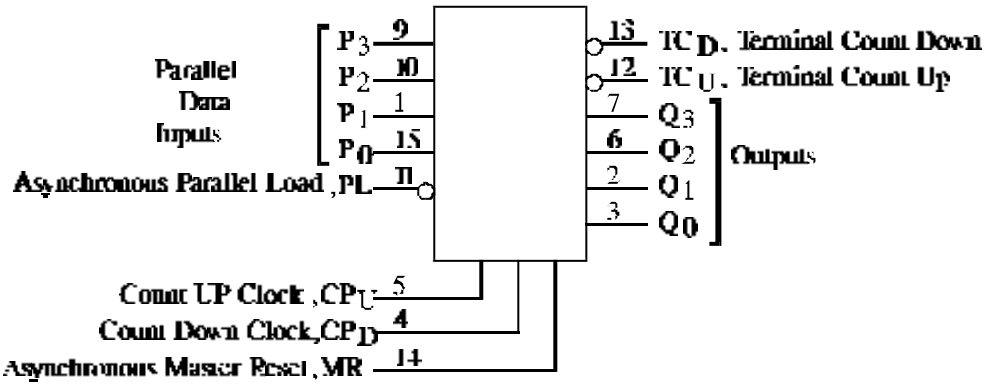
The counter has two separate clock inputs, a Count Up Clock and Count Down Clock inputs. The direction of counting is determined by which input is clocked. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs. This counter may be preset by entering the desired data on the P0, P1, P2, P3 input. When the Parallel Load input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as devide-by-n by modifying the count lenght with the preset inputs. In addition the counter can also be cleared. This is accomplished by inputting a high on the Master Reset input. All 4 internal stages are set to low independently of either clock input.Both a Terminal Count Down (TC_D) and Terminal Count Up (TC_U) Outputs are provided to enable cascading of both up and down counting functions. The TC_D output produces a negative going pulse when the counter underflows and TC_U outputs a pulse when the counter overflows. The counter can be cascaded by connecting the TC_U and TC_D outputs of one device to the Count Up Clock and Count Down Clock inputs, respectively, of the next device.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 µA
- High Noise Immunity Characteristic of CMOS Devices

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} =2.0 V V_{CC} =4.5 V V_{CC} =6.0 V	0 0 0	1000 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V_{IL}	Maximum Low -Level Input Voltage	V_{OUT}=0.1 V or V_{CC}-0.1 V $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	 4.5 6.0	 3.98 5.48	 3.84 5.34	 3.7 5.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA $\|I_{OUT}\| \le 5.2$ mA	 4.5 6.0	 0.26 0.26	 0.33 0.33	 0.4 0.4	
I_{IN}	Maximum Input Leakage Current	V_{IN}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}=V_{CC} or GND I_{OUT}=0μA	6.0	8.0	80	160	μA

FUNCTION TABLE

Inputs				Mode
MR	$\overline{PL}$	CP_U	CP_D	
H	X	X	X	Reset(Asyn.)
L	L	X	X	Preset(Asyn.)
L	H	↓	H	No Count
L	H	↑	H	Count Up
L	H	H	↑	Count Down
L	H	H	↓	No Count

X = don't care

The IN74HC192 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, it will follow the sequence 10, 11, 6: 12, 13, 4: 14, 15, 2 if counting Up, and follow the sequence 15, 14, 13, 12, 11, 10, 9 if counting Down.

Logic equations

For Terminal Count:

$\overline{TC_U} = Q_0 \bullet Q_3 \bullet \overline{CP_U}$

$\overline{TC_D} = \overline{Q_0} \bullet \overline{Q_1} \bullet \overline{Q_2} \bullet \overline{Q_3} \bullet \overline{CP_D}$

AC ELECTRICAL CHARACTERISTICS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25 °C to -55°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
f_{max}	Minimum Clock Frequency (50% Duty Cycle) (Figures 1 and 6)	2.0 4.5 6.0	12 36 43	3.2 16 19	2.6 13 15	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 6)	2.0 4.5 6.0	215 43 37	270 54 46	325 65 55	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{PL}$ to Q (Figures 3 and 6)	2.0 4.5 6.0	215 43 37	270 54 46	325 65 55	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Terminal Count (Figures 2 and 6)	2.0 4.5 6.0	125 25 21	155 31 26	190 38 32	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time,Any Output (Figures 1 and 6)	2.0 4.5 6.0	75 15 13	95 20 18	110 23 20	ns
C_{IN}	Maximum Input Capacitance	-	10	10	10	pF

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 60	pF

TIMING REQUIREMENTS (C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit 25 °C to -55°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
t_{su}	Minimum Setup Time, Pn to $\overline{PL}$ (Figure 4)	2.0 4.5 6.0	100 20 18	125 35 22	150 30 26	ns
t_h	Minimum Hold Time, Pn to $\overline{PL}$ (Figure 4)	2.0 4.5 6.0	0 0 0	0 0 0	0 0 0	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 4.5 6.0	150 30 26	190 38 33	225 45 38	ns
t_w	Minimum Pulse Width, $\overline{PL}$ (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 26	150 30 26	ns
t_w	Minimum Pulse Width, MR (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 26	150 30 26	ns
t_r, t_f	Minimum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	100 500 400	100 500 400	100 500 400	ns

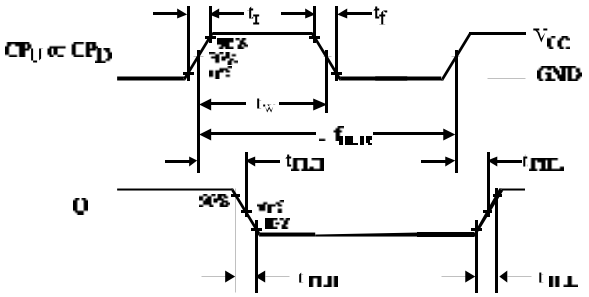


Figure 1. Switching Waveforms

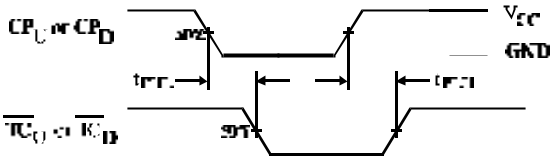


Figure 2. Switching Waveforms

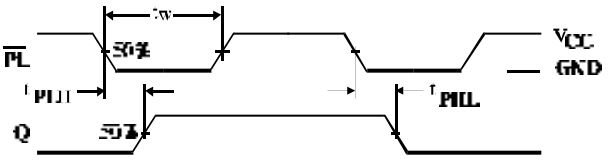


Figure 3. Switching Waveforms

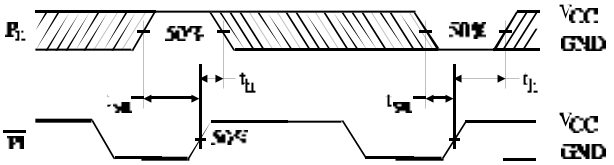


Figure 4. Switching Waveforms

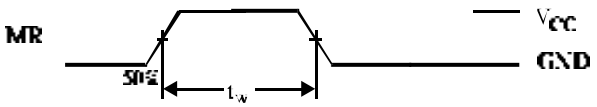


Figure 5. Switching Waveforms

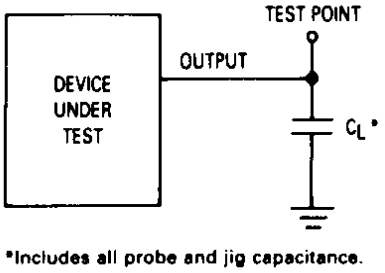
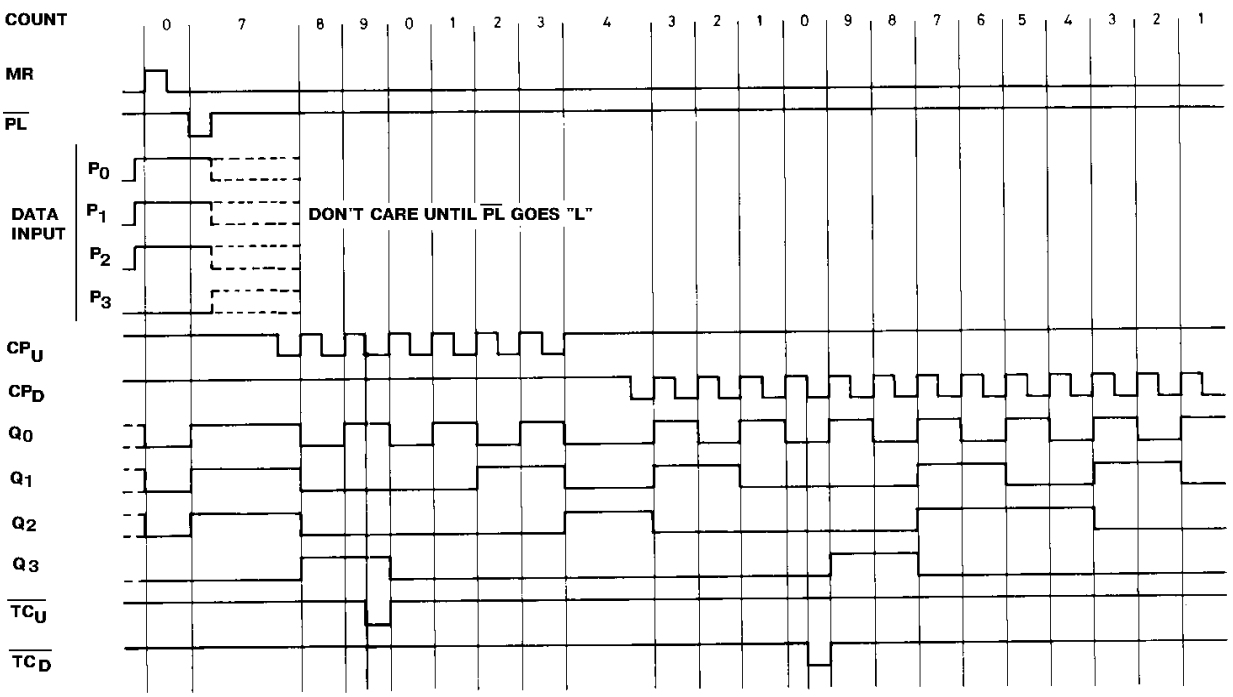


Figure 6. Test Circuit

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM

