HMC627LP5 / 627LP5E

0.5 dB LSB GaAs MMIC 6-BIT DIGITAL VARIABLE GAIN AMPLIFIER, DC - 1 GHz

Typical Applications

The HMC627LP5(E) is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

-11.5 to 20 dB Gain Control in 0.5 dB Steps

High Output IP3: +36 dBm

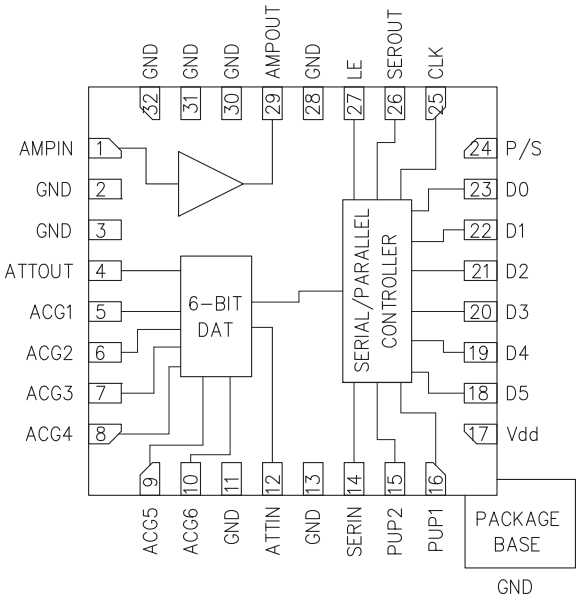
TTL/CMOS Compatible Serial or Parallel Control

±0.25 dB Typical Gain Step Error

Single +5V Supply

32 Lead 5x5mm SMT Package: 25mm²

Functional Diagram



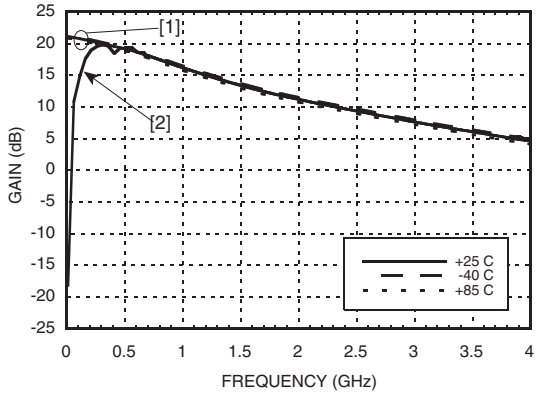
General Description

The HMC627LP5(E) is a digitally controlled variable gain amplifier which operates from DC to 1 GHz, and can be programmed to provide anywhere from 11.5 dB attenuation, to 20 dB of gain, in 0.5 dB steps. The HMC627LP5(E) delivers noise figure of 4.3 dB in its maximum gain state, with output IP3 of up to +36 dBm in any state. The dual mode gain control interface accepts either three wire serial input or 6 bit parallel word. The HMC627LP5(E) also features a user selectable power up state and a serial output for cascading other Hittite serially controlled components. The HMC627LP5(E) is housed in a RoHS compliant 5x5 mm QFN leadless package, and requires no external matching components.

Electrical Specifications, T_A = +25° C, Vdd = +5V, Vs= +5V

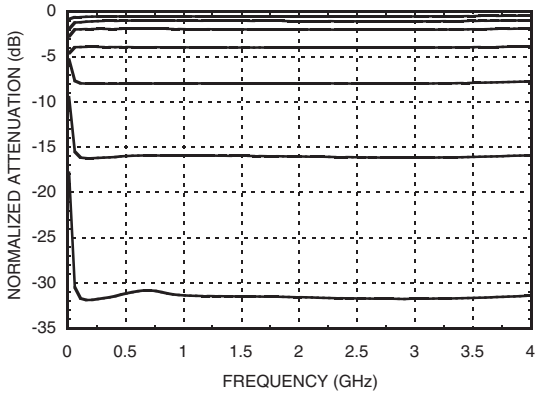
Parameter	Frequency	Min.	Typ.	Max.	Units
Gain (Maximum Gain State)	DC - 0.5 GHz 0.5 - 1.0 GHZ	18 15	20 17.5		dB dB
Gain Control Range			31.5		dB
Input Return Loss	DC - 1.0 GHz		17		
Output Return Loss	DC - 1.0 GHz		12		dB
Gain Accuracy: (Referenced to Maximum Gain State) All Gain States	DC - 0.8 GHz 0.8 - 1.0 GHZ	± (0.10 + 5% of Gain Setting) Max. ± (0.30 + 3% of Gain Setting) Max.			dB
Output Power for 1 dB Compression	DC - 1.0 GHz	16	20		dBm
Output Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone)	DC - 1.0 GHz		36		dBm
Noise Figure	DC - 1.0 GHz		4.3		dB
Supply Current (Idd)	DC - 1.0 GHz		90		mA

Maximum Gain vs. Frequency [1]



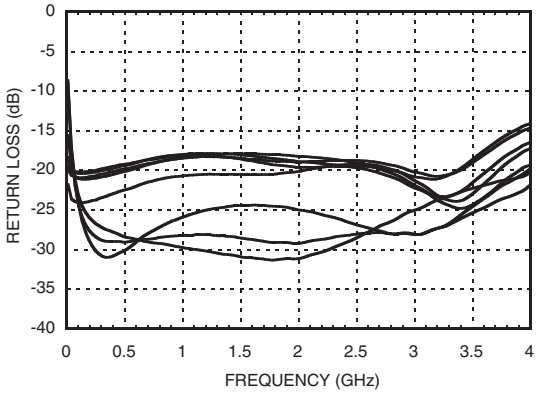
Normalized Attenuation

(Only Major States are Shown)



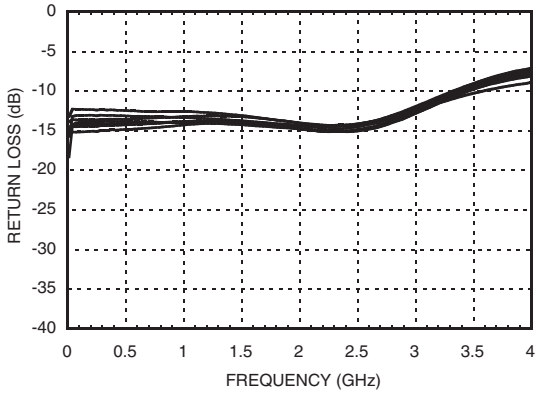
Input Return Loss [1]

(Only Major States are Shown)



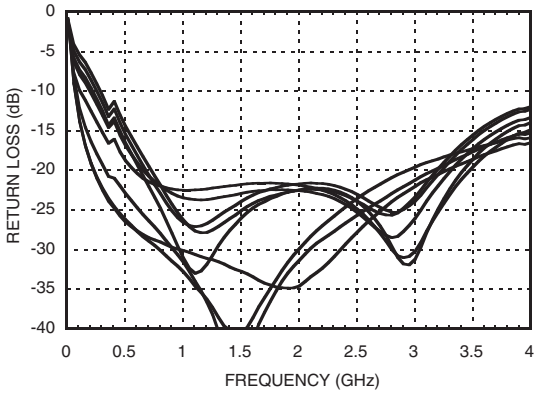
Output Return Loss [1]

(Only Major States are Shown)



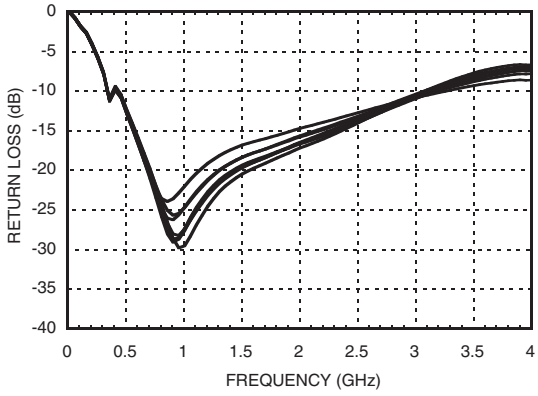
Input Return Loss [2]

(Only Major States are Shown)



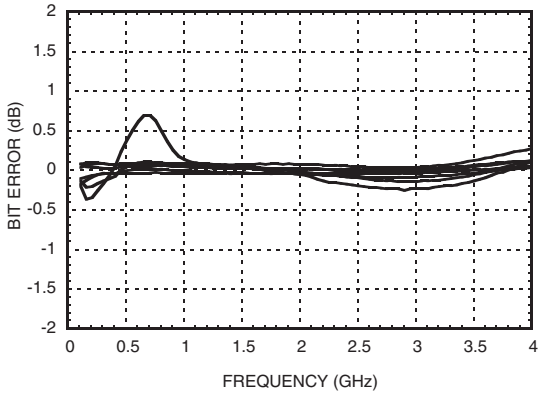
Output Return Loss [2]

(Only Major States are Shown)

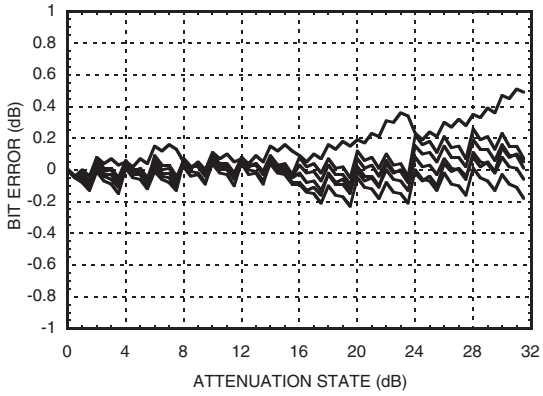


[1] Tested with broadband bias tee on RF ports and C1 = 10,000pF
[2] C1, C6 and C8 = 100pF, L1 = 270nF

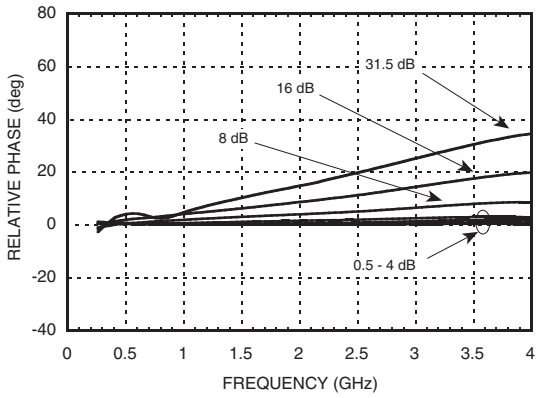
Bit Error vs. Frequency [2]
(Only Major States are Shown)



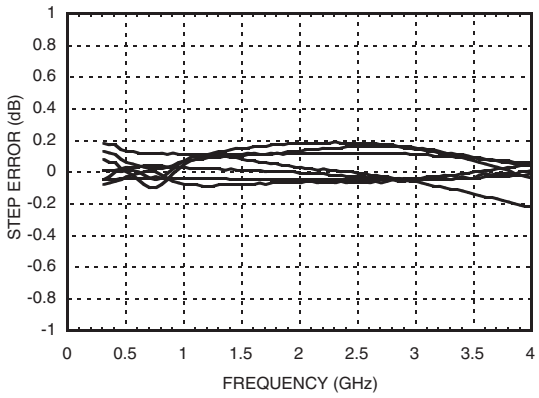
Bit Error vs. Attenuation State [2]



Normal Relative Phase vs. Frequency [2]
(Only Major States are Shown)



Step Error vs. Frequency [2]
(Only Major States are Shown)



[1] Tested with broadband bias tee on RF ports and C1 = 10,000pF
[2] C1, C6 and C8 = 100pF, L1 = 270nF

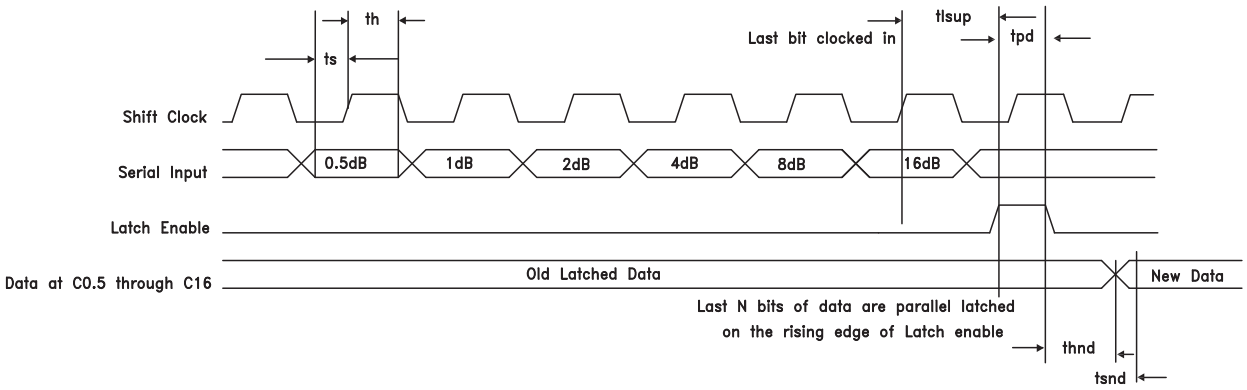
For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

Serial Mode

The serial mode is enabled then P/S is set to high. Data is entered LSB first and after the 6th shift clock cycle the LE (Latch Enable) is pulsed High and then Low. See timing diagram below for reference.

Timing Diagram

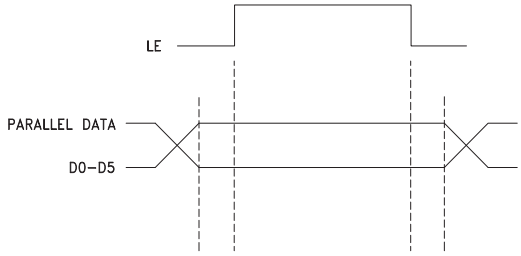
Serial data is shifted in on the rising edge of the Shift Clock, LSB first, and is latched on the rising edge of Latch Enable.



Timing

Parameter	Symbol	Vdd = +5V (Typ.)	Units
Serial Input Setup Time	ts	20	ns
Hold Time from Serial Input to Shift Clock	th	20	ns
Setup Time from Shift Clock to Latch Enable	tlsup	40	ns
Propagation Delay	tpd	10	ns
Setup Time for New Data	tsnd	10	ns

Timing Diagram *(Latched Parallel Mode)*



Parallel Mode *(Direct Parallel Mode & Latched Parallel Mode)*

Direct Parallel Mode - The attenuation state is changed by the Control Voltage Inputs directly. The LE (Latch Enable) must be at a logic high to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the Control Voltage Inputs and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram below for reference.

Power-Up States

Using the Parallel PUP truth table the attenuator can be turned on at a specific attenuation state. By using the PUP1 and PUP2 line four different attenuation states can be selected. It can also be used in the Direct Parallel Mode using the Control Voltage Inputs to select attenuation values.

Parallel PUP Truth Table

P/S	LE	PUP2	PUP1	Gain Relative to Maximum Gain
0	0	0	0	-31.5
0	0	1	0	-24
0	0	0	1	-16
0	0	1	1	-8
0	1	X	X	-0.5 to -31.5 dB

Note: Power-Up with LE= 1 provides normal parallel operation with D0 - D5, and PUP1 and PUP2 are not active.

Absolute Maximum Ratings

RF Input Power [1]	11.5 dBm (T = +85 °C)
Digital Inputs ($\overline{\text{Reset}}$, Shift Clock, Latch Enable & Serial Input)	-1.5V to (Vdd +1.5V) Vdc
Bias Voltage (Vdd)	5.6 Vdc
Collector Bias Voltage (Vcc)	5.5 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 9 mW/°C above 85 °C) [1]	0.593 W
Thermal Resistance	110 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

[1] At max gain settling

Truth Table

Control Voltage Input						Gain Relative to Maximum Gain
D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	0 dB
High	High	High	High	High	Low	-0.5 dB
High	High	High	High	Low	High	-1 dB
High	High	High	Low	High	High	-2 dB
High	High	Low	High	High	High	-4 dB
High	Low	High	High	High	High	-8 dB
Low	High	High	High	High	High	-16 dB
Low	Low	Low	Low	Low	Low	-31.5 dB

Any combination of the above states will provide a reduction in gain approximately equal to the sum of the bits selected.

Bias Voltage

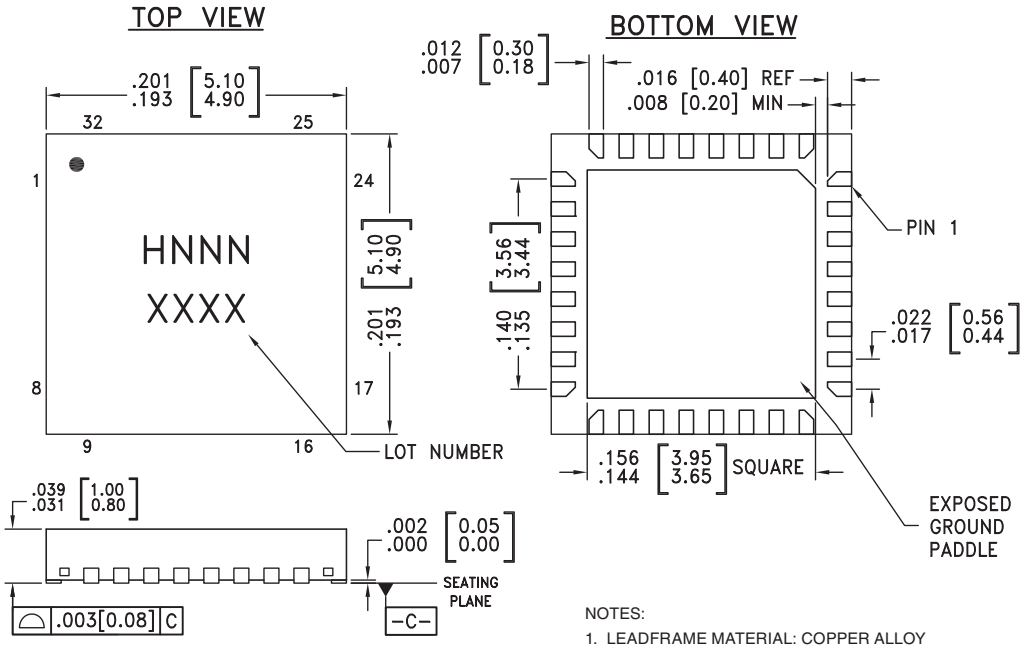
Vdd (V)	Idd (Typ.) (mA)
+5.0	2
Vs (V)	Is (mA)
+5.0	88

TTL/CMOS Control Voltage

State	Vdd= +3V or +5V
Low	0 to 0.8V
High	2.0V to Vdd

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

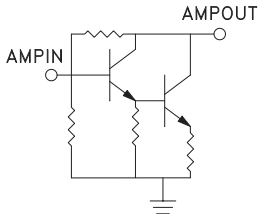
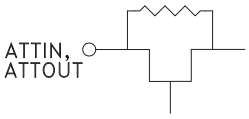
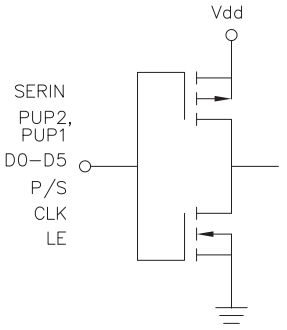
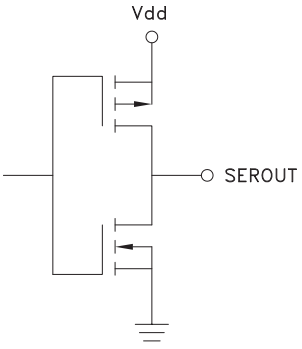
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

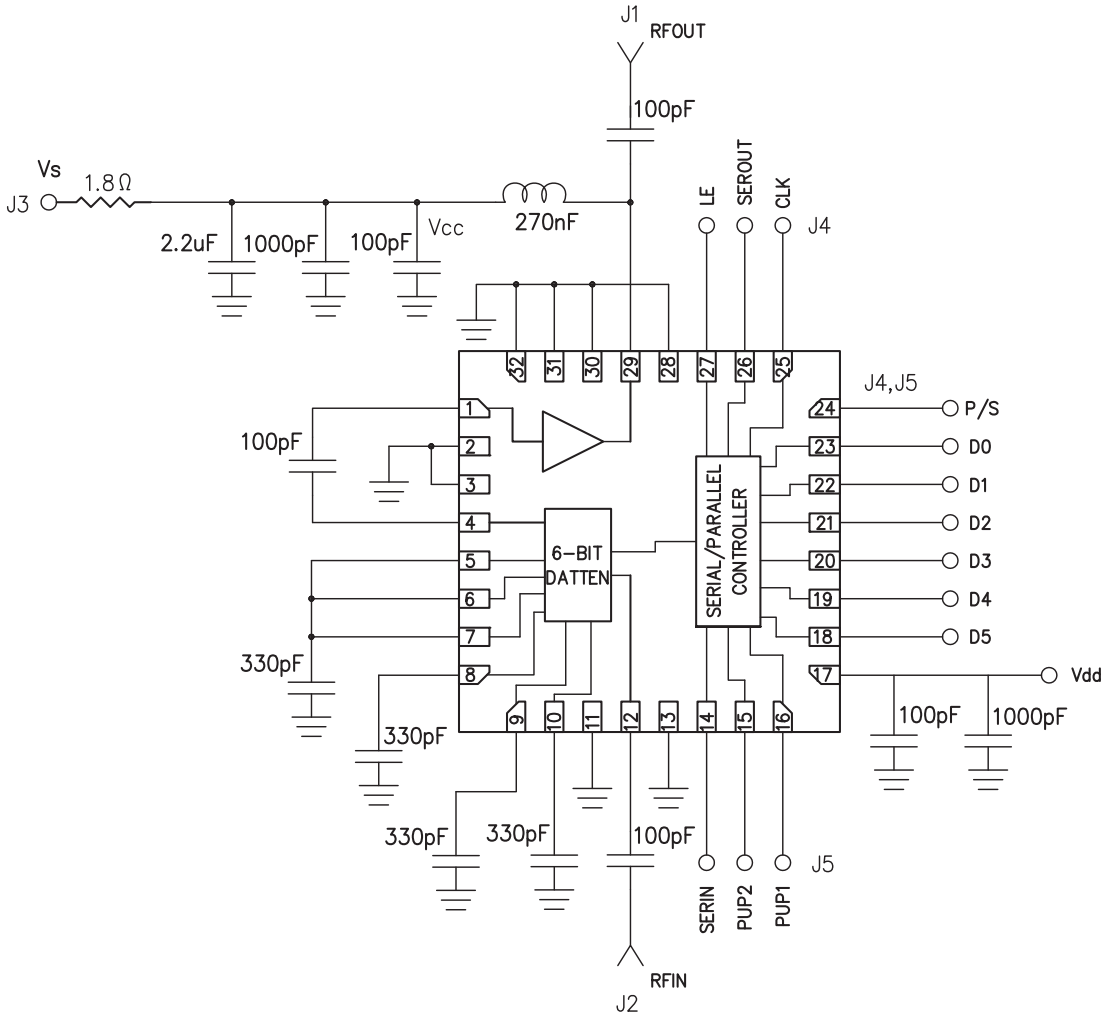
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC627LP5	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H627 XXXX
HMC627LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H627 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

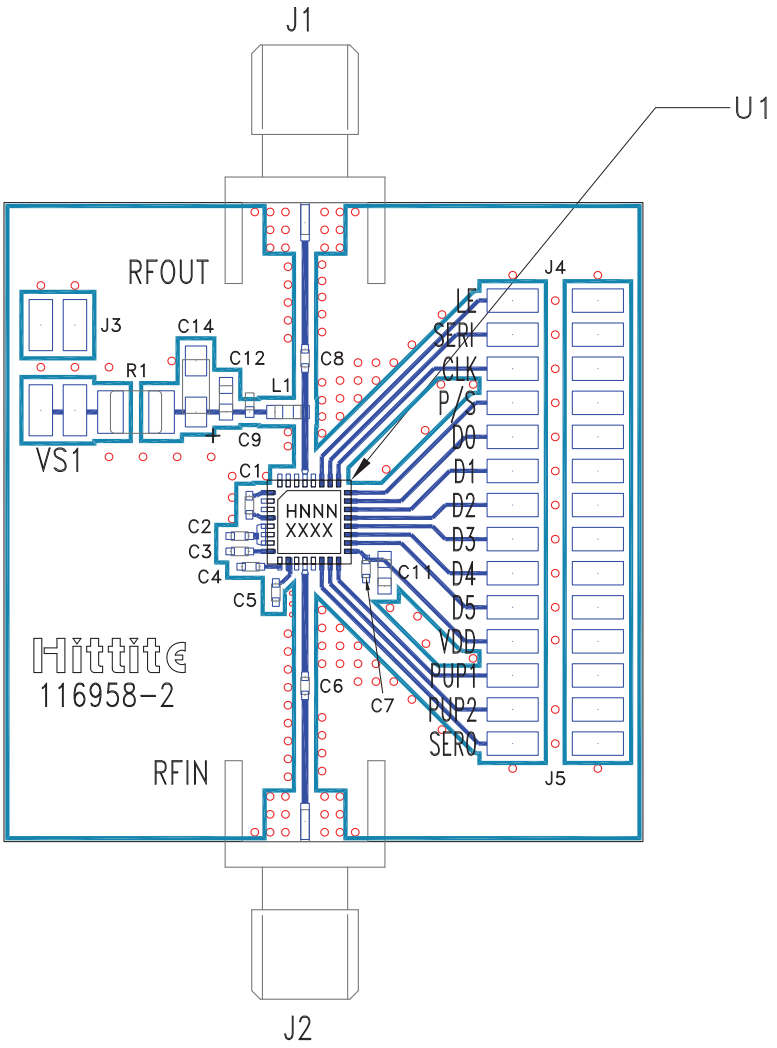
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	AMPIN	This pin is DC coupled. An off chip DC blocking capacitor is required.	
29	AMPOUT	RF output and DC bias (Vcc) for the output stage of the amplifier.	
2, 3, 11, 13, 28, 30 - 32	GND	These pins and package bottom must be connected to RF/DC ground.	
4, 12	ATTIN, ATTOUT	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
5 - 10	ACG1 - ACG6	External capacitors to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
14	SERIN	See truth table, control voltage table and timing diagram.	
15, 16	PUP2, PUP1		
18 - 23	D5, D4, D3, D2, D1, D0		
24	P/S		
25	CLK		
27	LE		
17	Vdd	Supply Voltage	
26	SEROUT	Serial input data delayed by 6 clock cycles.	

Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB 118329 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3	4 Pin DC Connector
J4, J5	14 Pin DC Connector
C1 - C9	100 pF Capacitor, 0402 Pkg.
C11 - C12	1000 pF Capacitor, 0402 Pkg.
C14	2.2 µF Capacitor, CASEA Pkg.
R1	1.8 Ohm Resistor, 1206 Pkg.
L1	270 nH Inductor, 0603 Pkg.
U1	HMC627LP5(E) Variable Gain Amplifier
PCB [2]	116958 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Notes: