Data Sheet | December 1992 | File Number 3338

CMOS Presettable Up/Down Counters

CD4510BMS Presettable BCD Up/Down Counter and the CD4516BMS Presettable Binary Up/Down counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The CD4510BMS will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode.

If the CARRY IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY OUT of a less significant stage to the CARRY IN of a more significant stage.

The CD4510BMS and CD4516BMS can be cascaded in the ripple mode by connecting the CARRY OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage. (See Figures 13, 14.)

These devices are similar to types MC14510 and MC14516.

The CD4510BMS and CD4516BMS are supplied in these 16-lead outline packages:

Braze Seal DIP	*H4W	†H45
Frit Seal DIP	*FBF	†H1F
Ceramic Flatpack	H6W	

*CD4510B Only †CD4516B Only

Features

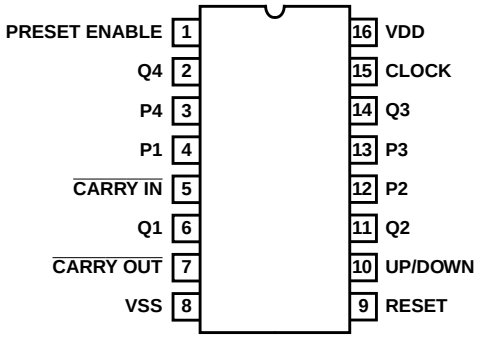
- **High Voltage Types (20V Rating)**
- **CD4510BMS - BCD Type**
- **CD4516BMS - Binary Type**
- **Medium Speed Operation**
  - **fCL = 8MHz Typ. at 10V**
- **Synchronous Internal Carry Propagation**
- **Reset and Preset Capability**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Standardized Symmetrical Output Characteristics**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Noise Margin (Over Full Package/Temperature Range)**
  - **1V at VDD = 5V**
  - **2V at VDD = 10V**
  - **2.5V at VDD = 15V**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Applications

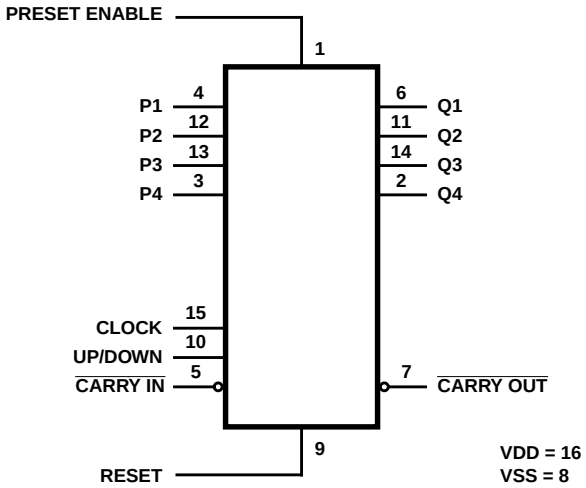
- **Up/Down Difference Counting**
- **Multistage Synchronous Counting**
- **Multistage Ripple Counting**
- **Synchronous Frequency Dividers**

Pinout

CD4510BMS, CD4516BMS
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input. . . . . ±10mA
Operating Temperature Range . . . . . -55^{o}C to +125^{o}C
Package Types D, F, K, H
Storage Temperature Range (TSTG). . . . . -65^{o}C to +150^{o}C
Lead Temperature (During Soldering) . . . . . +265^{o}C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80^{o}C/W	20^{o}C/W
Flatpack Package	70^{o}C/W	20^{o}C/W

Maximum Package Power Dissipation (PD) at +125^{o}C
For TA = -55^{o}C to +100^{o}C (Package Type D, F, K) 500mW
For TA = +100^{o}C to +125^{o}C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/^{o}C to 200mW
Device Dissipation per Output Transistor. 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175^{o}C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25^{o}C	-	10	µA
				2	+125^{o}C	-	1000	µA
		VDD = 18V, VIN = VDD or GND		3	-55^{o}C	-	10	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25^{o}C	-100	-	nA
				2	+125^{o}C	-1000	-	nA
			VDD = 18V	3	-55^{o}C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25^{o}C	-	100	nA
				2	+125^{o}C	-	1000	nA
			VDD = 18V	3	-55^{o}C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25^{o}C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25^{o}C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25^{o}C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25^{o}C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25^{o}C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25^{o}C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25^{o}C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25^{o}C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25^{o}C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25^{o}C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25^{o}C			
		VDD = 18V, VIN = VDD or GND		8A	+125^{o}C			
		VDD = 3V, VIN = VDD or GND		8B	-55^{o}C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25^{o}C, +125^{o}C, -55^{o}C	11	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Clock to Q Output	TPHL1 TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Preset or Reset to Q	TPHL2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	420	ns
			10, 11	+125°C, -55°C	-	567	ns
Propagation Delay Clock to Carry Out	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	480	ns
			10, 11	+125°C, -55°C	-	648	ns
Propagation Delay Carry In to Carry Out	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	250	ns
			10, 11	+125°C, -55°C	-	338	ns
Propagation Delay Preset or Reset to Carry Out	TPHL5 TPLH5	VDD = 5V, VIN = VDD or GND (Note 3)	9	+25°C	-	640	ns
			10, 11	+125°C, -55°C	-	864	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns
Maximum Clock Input Frequency	FCL	VDD = 5V, VIN = VDD or GND	9	+25°C	2	-	MHz
			10, 11	+125°C, -55°C	1.48	-	MHz

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.
3. Reset to Carry Out (TPLH) only.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	5	µA
				+125°C	-	150	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	300	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	10	µA
				+125°C	-	600	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125^{O}C	-	-1.15	mA
				-55^{O}C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125^{O}C	-	-0.9	mA
				-55^{O}C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125^{O}C	-	-2.4	mA
				-55^{O}C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25^{O}C, +125^{O}C, -55^{O}C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25^{O}C, +125^{O}C, -55^{O}C	+7	-	V
Propagation Delay Clock to Q Output	TPHL1 TPLH1	VDD = 10V	1, 2, 3	+25^{O}C	-	200	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	150	ns
Propagation Delay Preset or Reset to Q	TPHL2 TPLH2	VDD = 10V	1, 2, 3	+25^{O}C	-	210	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	160	ns
Propagation Delay Clock to Carry Out	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25^{O}C	-	240	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	180	ns
Propagation Delay Carry In to Carry Out	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25^{O}C	-	120	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	100	ns
Propagation Delay Preset or Reset to Carry Out	TPHL5 TPLH5	VDD = 10V	1, 2, 3, 4	+25^{O}C	-	320	ns
		VDD = 15V	1, 2, 3, 4	+25^{O}C	-	250	ns
Transition Time	TTLH TTHL	VDD = 10V	1, 2, 3	+25^{O}C	-	100	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	80	ns
Maximum Clock Input Frequency	FCL	VDD = 10V	1, 2	+25^{O}C	4	-	MHz
		VDD = 15V	1, 2	+25^{O}C	5.5	-	MHz
Minimum Hold Time Preset Enable to JN	TH	VDD = 5V	1, 2, 3	+25^{O}C	-	70	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	40	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	40	ns
Minimum Data Setup Time Preset Enable to JN	TS	VDD = 5V	1, 2, 3	+25^{O}C	-	25	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	10	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	10	ns
Minimum Data Hold Time Clock to Carry In	TH	VDD = 5V	1, 2, 3	+25^{O}C	-	60	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	30	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	30	ns
Minimum Clock Hold Time Clock to Up/Down	TH	VDD = 5V	1, 2, 3	+25^{O}C	-	30	ns
		VDD = 10V	1, 2, 3	+25^{O}C	-	30	ns
		VDD = 15V	1, 2, 3	+25^{O}C	-	30	ns
Input Capacitance	CIN	Any Input	1, 2	+25^{O}C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
4. Reset to Carry Out (TPLH) only.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25^{o}C	-	25	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25^{o}C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25^{o}C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25^{o}C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25^{o}C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25^{o}C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25^{o}C	-	1.35 x +25^{o}C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25^{o}C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25^{o}C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-2	IDD	± 1.0µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
CD4510BMS						
Static Burn-In 1 (Note 1)	2, 6, 7, 11, 14	1, 3-5, 8-10, 12, 13, 15	16			
Static Burn-In 2 (Note 1)	2, 6, 7, 11, 14	8	1, 3-5, 9, 10, 12, 13, 15, 16			
Dynamic Burn-In (Note 1)	-	1, 3, 4, 8, 9, 12, 13	10, 16	2, 6, 7, 11, 14	15	5
Irradiation (Note 2)	2, 6, 7, 11, 14	8	1, 3-5, 9, 10, 12, 13, 15, 16			

NOTES:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

Logic Diagrams

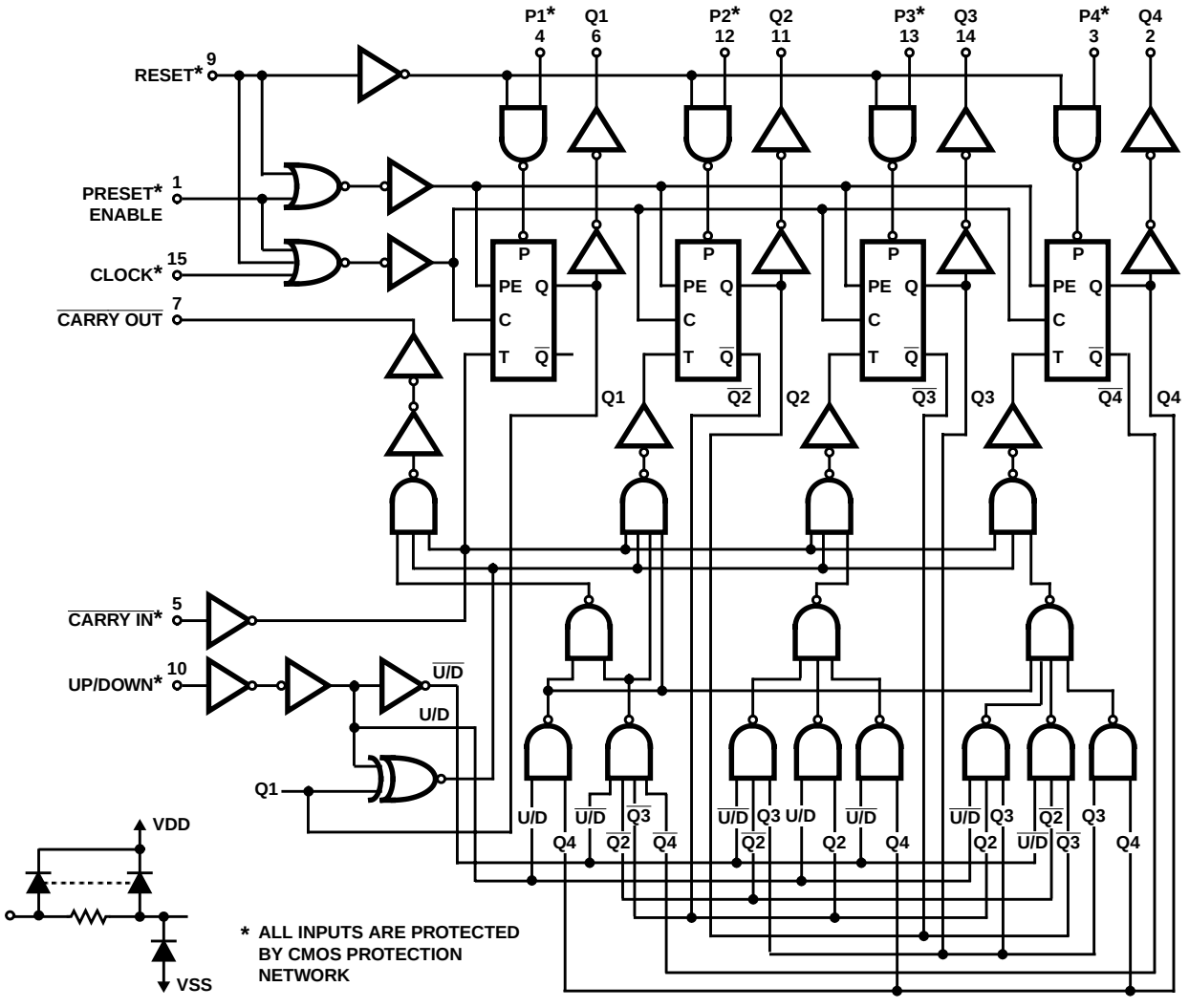


FIGURE 1. CD4510BMS

Logic Diagrams (Continued)

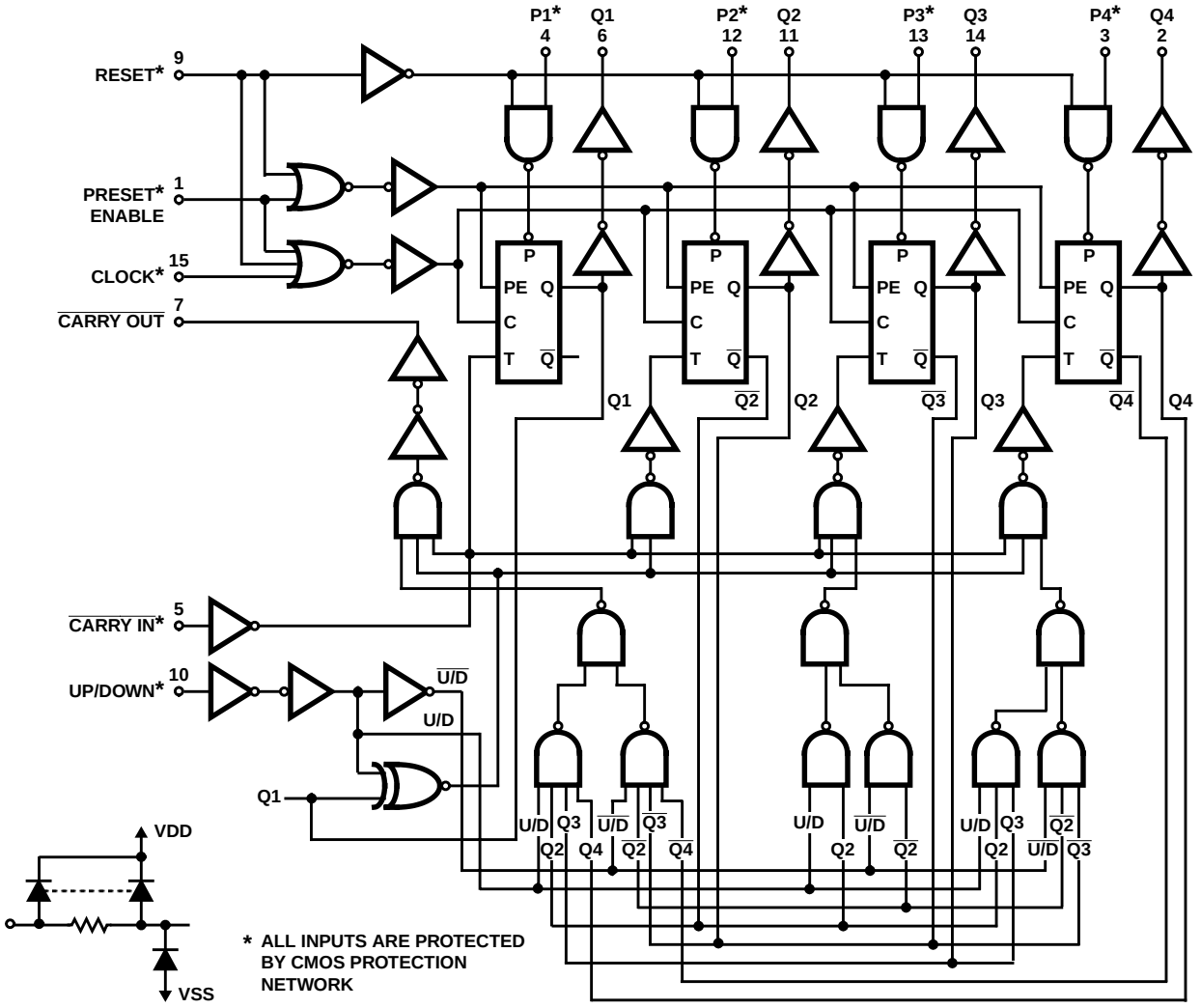


FIGURE 2. CD4516BMS

TRUTH TABLE

CL	CI	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
⎍	0	1	0	0	COUNT UP
⎍	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

X = DON'T CARE

Typical Performance Characteristics

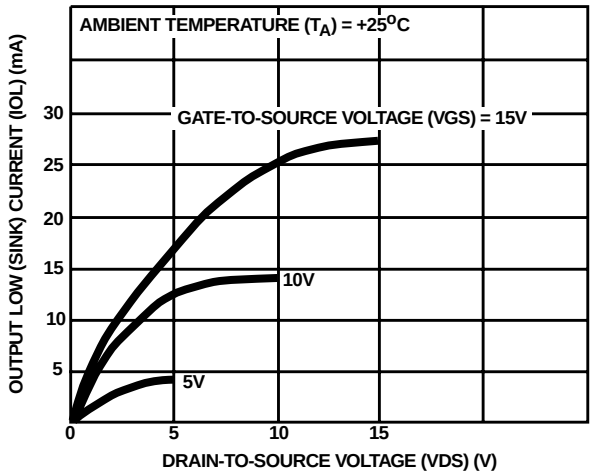


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

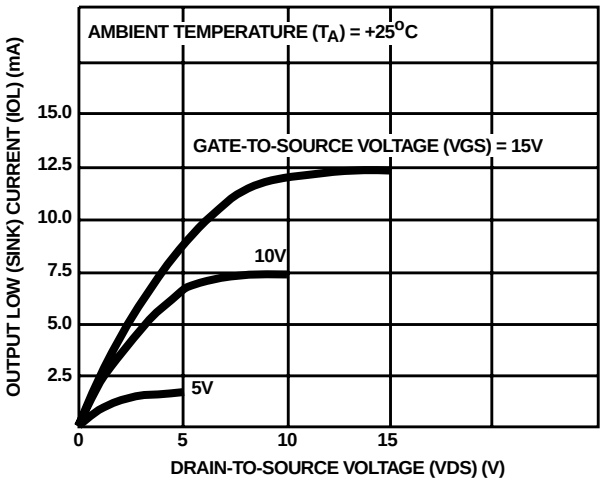


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

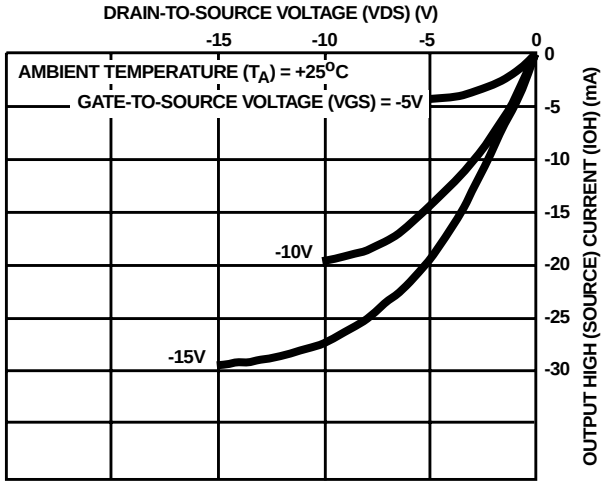


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

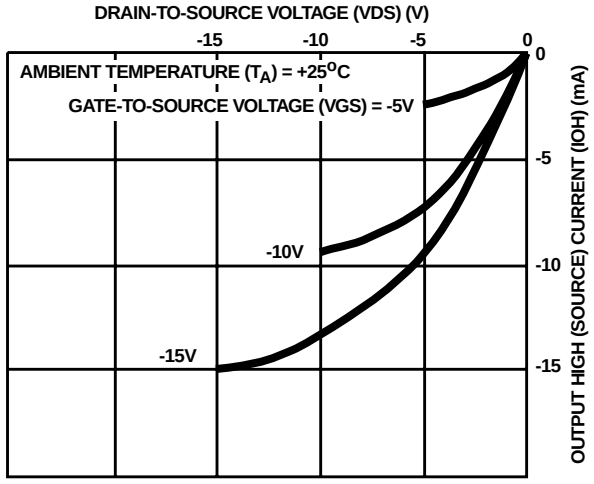


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

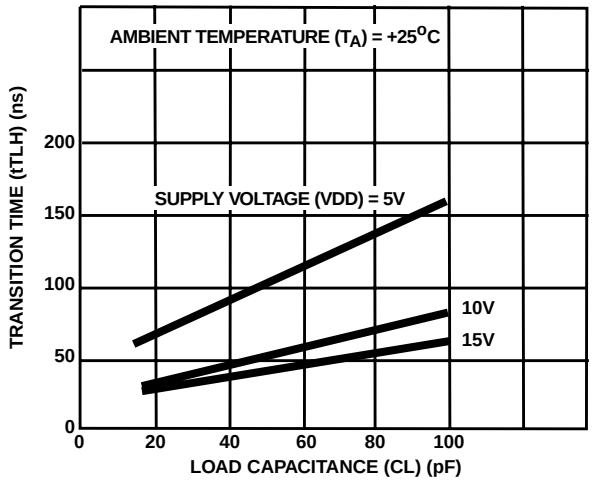


FIGURE 7. TYPICAL TRANSITION TIME vs LOAD CAPACITANCE

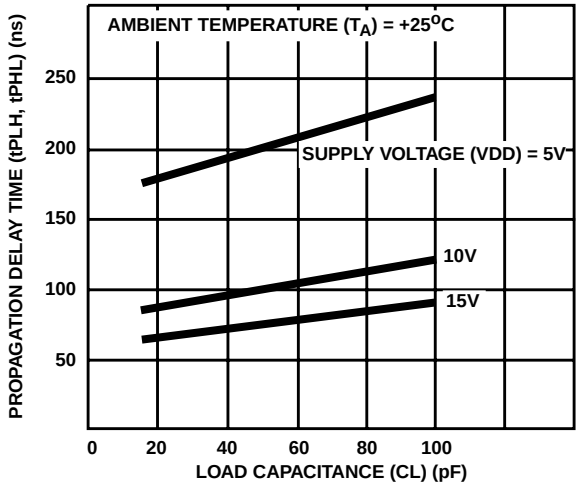


FIGURE 8. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE FOR CLOCK-TO-Q OUTPUTS

Typical Performance Characteristics (Continued)

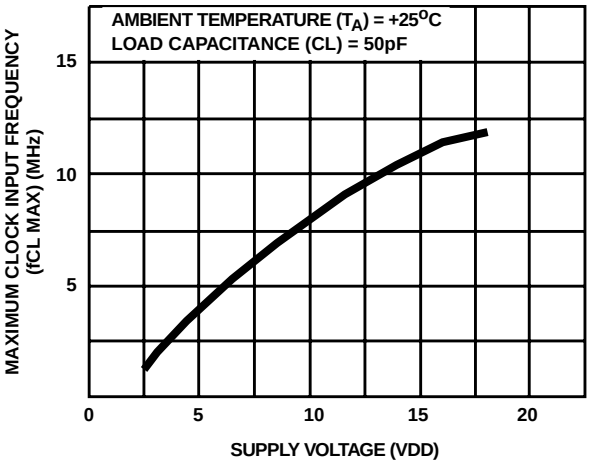


FIGURE 9. TYPICAL MAXIMUM CLOCK INPUT FREQUENCY vs SUPPLY VOLTAGE

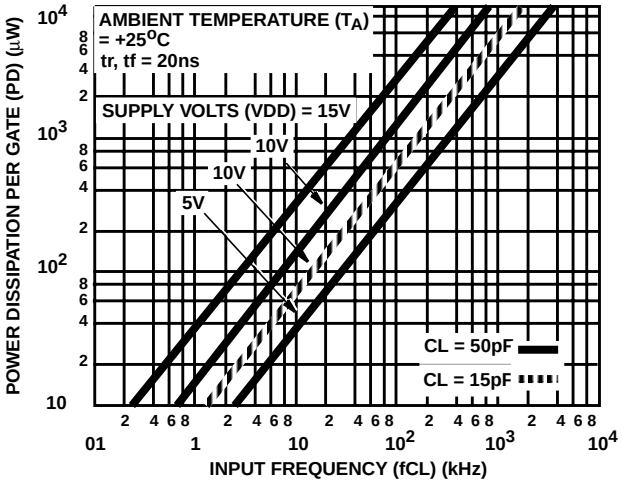
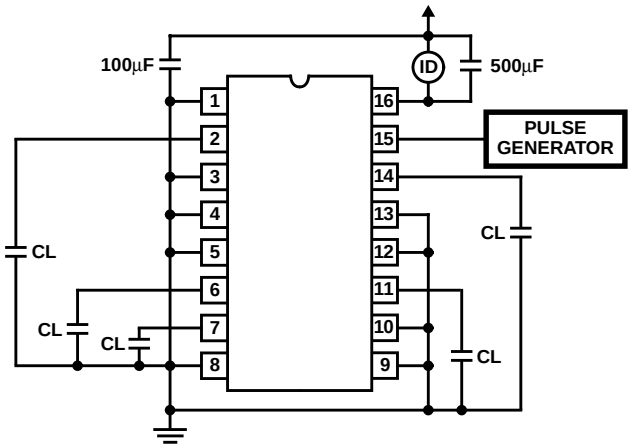


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION vs FREQUENCY

Test Circuit and Waveform



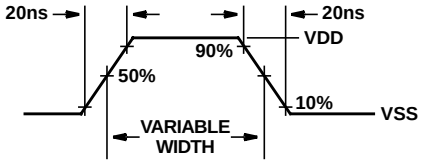
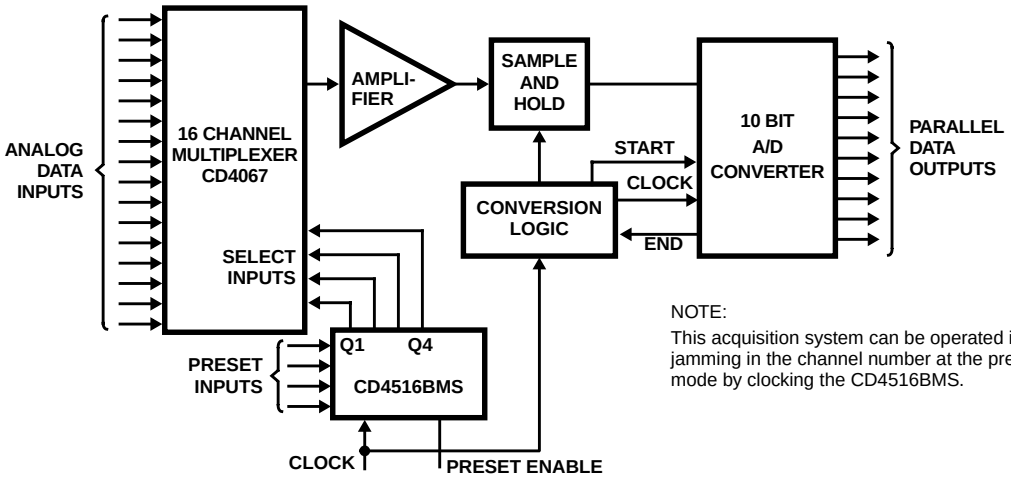


FIGURE 11. POWER DISSIPATION TEST CIRCUIT AND INPUT WAVEFORM

Acquisition System



NOTE:
This acquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the CD4516BMS.

FIGURE 12. TYPICAL 16 CHANNEL, 10 BIT DATA ACQUISITION SYSTEM

Timing Diagrams

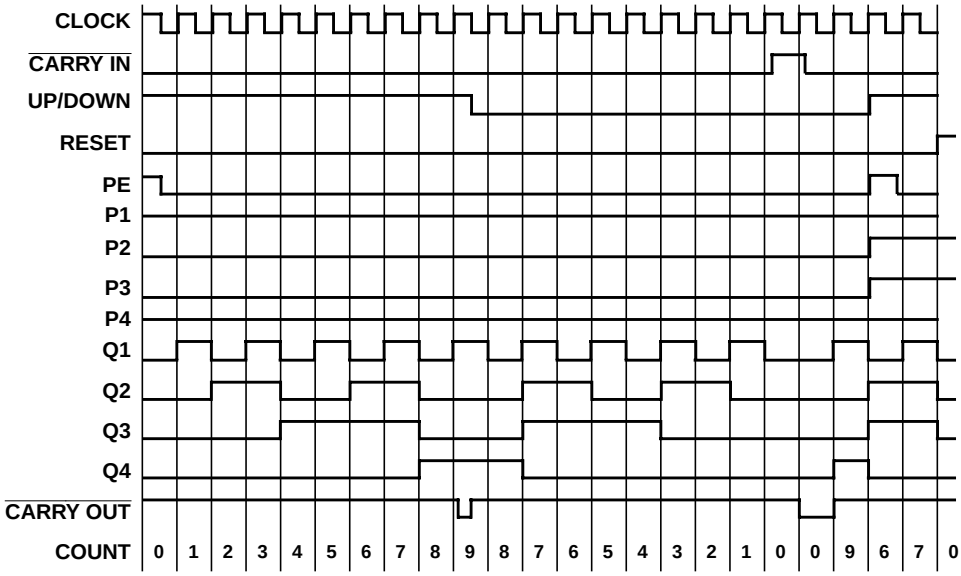


FIGURE 13. CD4510BMS

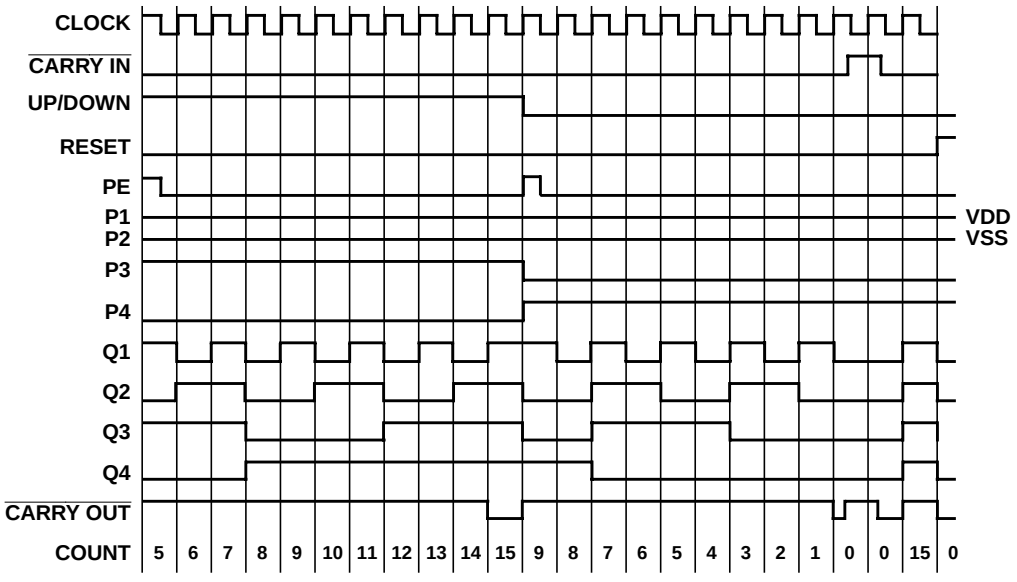
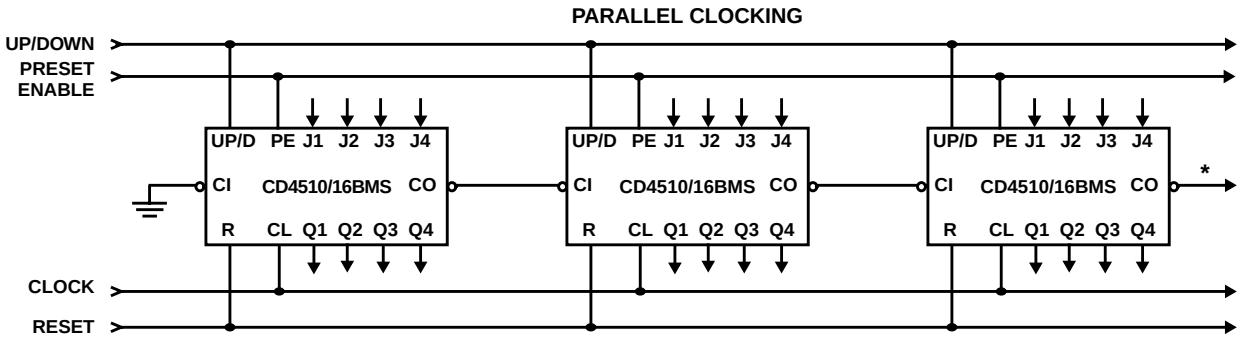
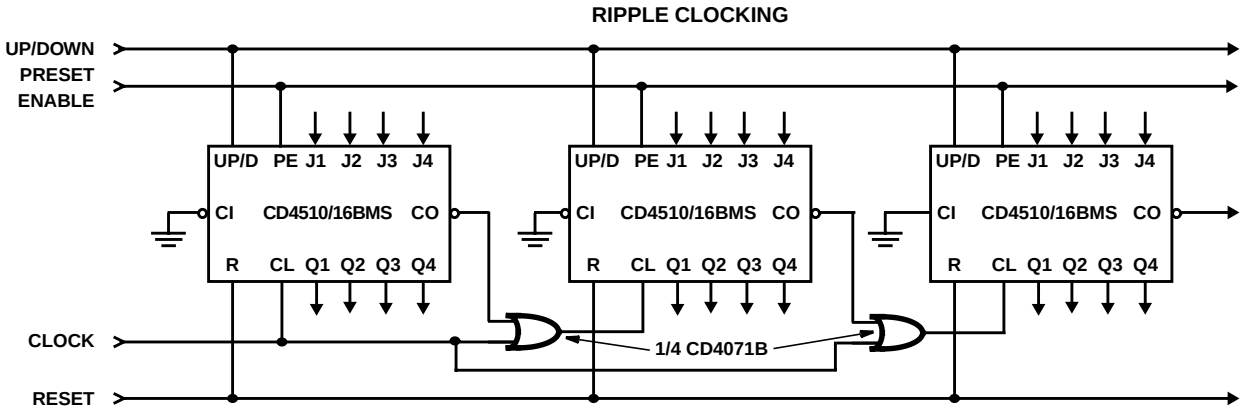


FIGURE 14. CD4516BMS



* CARRY OUT lines at the 2nd, 3rd, etc., stages may have a negative-going glitch pulse resulting from differential delays of different CD4010/16BMS IC'S. These negative going glitches do not affect proper CD4029BMS operation. However, if the CARRY OUT signals are used to trigger other edge-sensitive logic devices, such as FF'S or counters, the CARRY OUT signals should be gated with the clock signal using a 2-input OR gate such as CD4071BMS.



Ripple Clocking Mode: The up/down control can be changed at any count. The only restriction on changing the up/down control is that the clock input to the first counting stage must be high. For cascading counters operating in a fixed up-count or down-count mode, the OR gates are not required between stages, and CO is connected directly to the CL input of the next stage with CI grounded.

FIGURE 15. CASCADING COUNTER PACKAGES

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