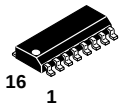
MC145076

Product Preview

MC145076 Stereo Audio FIR Smoothing Filter

CMOS



D SUFFIX
16–PIN SOG
CASE 751B–05

ORDERING INFORMATION

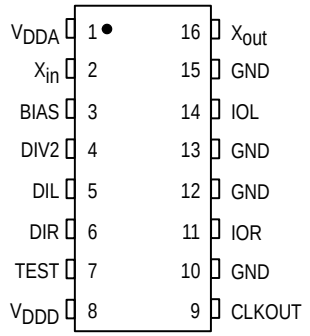
MC145076D SOG Package

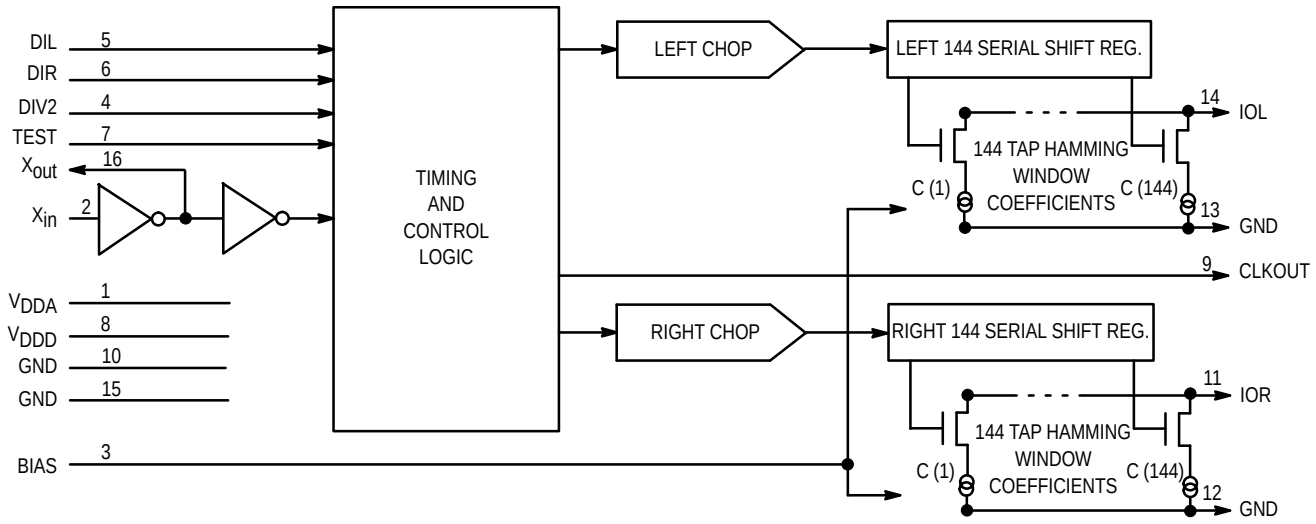
The MC145076 is a combination re–clocking and smoothing filter designed especially for the MC145074 Stereo Audio DAC. Its versatility however, allows it to be used with any single bit–stream data converter to provide output reconstruction filtering, and to improve performance by restoring pulse shape integrity. The MC145076 provides a well controlled, filtered output that can be used directly, or with a current summing operational amplifier.

The MC145076 is intended to be one half of a two–chip solution for serial bit steam DACs. The analog filtering function of the MC145076 eases the digital filtering requirements at the input to the digital noise shaping modulator, and eliminates the need for precision analog output filtering capacitors, resulting in lower overall system cost. The MC145076 pulse shape restoration frees the designer from analog pitfalls that can impact performance, thereby lowering the risk of new product development with a sigma–delta DAC.

- Single–Ended Stereo Outputs Require no Additional Smoothing Filters
- 86 dB S/D, 96 dB S/N with MC145074 @ 192 x OSR Single Ended
- > 100 dB S/(N+D) @ 256 OSR, Differential Mode
- 18.5 MHz Maximum Serial Data Input Rate
- – 80 dB Cross Channel Interference
- 72–Tap FIR with > 40 dB Alias Filtering
- Operating Temperature Range: – 40 to + 85°C
- Buffered Data Clock Output for Ease of Data Generation
- 16–Pin Narrow Body SOIC Package
- Single Supply Operation: + 5 V

PIN ASSIGNMENT





This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 1
9/96

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to GND)	6.0	V
V_{in}	DC Input Voltage	GND – 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	GND – 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 20	mA
I_{DD}, I_{GND}	DC Supply Current, V_{DD} and GND Pins	± 60	mA
T_{stg}	Storage Temperature	– 55 to 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{DD}). Unused outputs must be left open.

OPERATION RANGES (Applicable to Guaranteed Limits)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	4.5 to 5.5	V
V_{IOL}, V_{IOR}	IOL, IOR Virtual Ground	V_{DD} – 2.0 to V_{DD}	V
T_A	Ambient Operating Temperature	– 40 to + 85	°C

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to GND, Full Temperature and Voltage Ranges per Operation Ranges Table, unless otherwise indicated)

Symbol	Parameter		Guaranteed Limit	Unit
V_{IH}	Minimum High–Level Input Voltage		0.7 x V_{DD}	V
V_{IL}	Maximum Low–Level Input Voltage		0.3 x V_{DD}	V
V_{OH}	Minimum High–Level Output Voltage	I_{OH} = 0.4 mA	V_{DD} – 0.3	V
V_{OL}	Maximum Low–Level Output Voltage	I_{OL} = 0.4 mA	GND + 0.3	V
I_{DD}	Maximum Power Supply Current	R_{bias} = 4640 Ω	40	mA
I_{OL}, I_{OR}	Left/Right Channel Output Current*		2 ± 20%	mA
I_{lkg}	Input Leakage Current		± 10	μA

* 50% Duty Cycle, V_{DDA} = 5 V, R_{bias} = 4640 Ω

SINGLE ENDED ANALOG CHARACTERISTICS

(X_{in} = 16.9344 MHz, DIV2 = 0, f_{in} = 990.527 Hz, 20 Bit 2nd Order Modulator Input Data)

Parameter	Test Conditions	Min	Typ	Max	Unit
Dynamic Range	S/(N+D) @ – 60 dB input, + 60 dB	—	96	—	dB
S/(N+D) Flat	(– 6 dB) 25 to 75% peak to peak input duty cycle	86	90	—	dB
A–weighted	(– 20 dB)	—	80*		
Idle Channel Noise	CLKOUT/4 digital input data pattern	—	105	—	dB
60 Hz Power Supply Rejection	With 47 μF and 4640 Ω on Bias Pin	—	40	—	dB

* Noise performance limited by second order digital modulator.

AC ELECTRICAL CHARACTERISTICS (Full Temperature and Voltage Ranges per Operation Ranges Table)

Symbol	Parameter	Guaranteed Limit	Unit
f	Clock Frequency, X_{in}	37	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, X_{in} to X_{out}	5	ns
t_{TLH}, t_{THL}	Maximum Rise/Fall Time, X_{out}	10	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, X_{in} to CLKOUT	30	ns
t_{TLH}, t_{THL}	Maximum Rise/Fall Time, CLKOUT	10	ns
t_{su}	Minimum DIR, DIL Setup Time From X_{in}	5	ns
t_h	Maximum DIR, DIL Hold Time From X_{in}	20	ns

NOTE: 10 pF load capacitance, X_{in} rise and fall times set at 2 ns.

TIMING WAVEFORMS

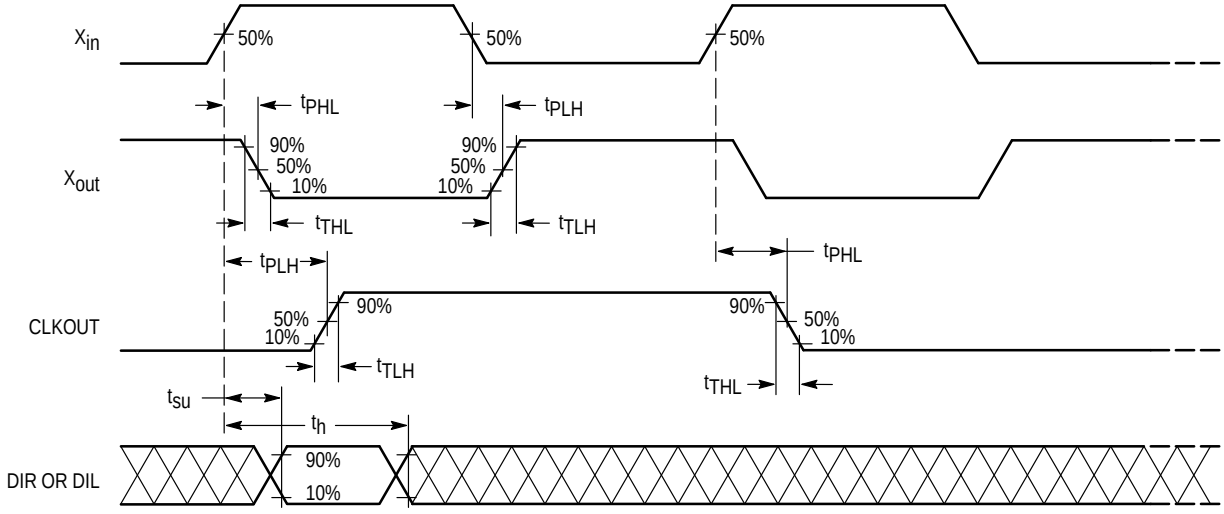


Figure 1.

PIN DESCRIPTIONS

X_{in}, X_{out}
Oscillator Inverter Input and Output (Pins 2, 16)

If an external clock is used to drive the MC145076, the clock should be connected to X_{in} pin. For maximum performance however, it is recommended that these pins be used in conjunction as a crystal oscillator.

BIAS
Bias Adjust (Pin 3)

For normal device operation, this pin should be connected to ground through a 4.7 kΩ resistor, which provides nominal quiescent output current of 2 mA each channel. In addition to the 4.7 kΩ resistor, a 47 μF capacitor may be connected from this pin to the V_{DD} supply.

DIV2
Active–High Clock Divider Control Input (Pin 4)

When this pin is at a logic low level, the internal clock will be equal to the oscillator, (X_{in}) frequency, and data can be clocked into the device at an $fX_{in}/2$ rate. When this pin is at a logic high level, the internal clock is one–half the X_{in} oscillator frequency, and data can be clocked into the device at an $fX_{in}/4$ rate.

DIL, DIR
Left/Right Channel Data Inputs (Pins 5,6)

These pins are the left and right digital input data pins from the single bit–stream sigma–delta DAC. Serial input data to the MC145076 is clocked in near the rising edge of CLKOUT.

TEST
Active–High Factory Test Mode Input (Pin 7)

This pin is reserved for factory testing, and should be connected to device ground for normal device operation.

CLKOUT
Buffered Divided Clock Output (Pin 9)

This pin provides a buffered clock output to be used as the clock source for a sigma–delta bit stream generator. The CLKOUT frequency is one–half the X_{in} frequency if DIV2 = 0, and one–fourth the X_{in} frequency if DIV2 = 1. The serial input data is clocked in near the rising edge of CLKOUT.

IOR, IOL
Left/Right Channel Current Outputs (Pins 11,14)

These pins are the current sink outputs of the smoothed single–bit input data.

V_{DDD}, V_{DDA}
Device Supply Pins (Pins 1,8)

These two pins are the positive power supply pins for the MC145076, nominally 5 V. For proper device operation, it is recommended that 0.1 μF and 10 μF capacitors be connected from these pins to ground via the shortest possible path.

GND
Device Ground Pins (Pins 10,12,13,15)

These pins are the ground pins for the device.

FUNCTIONAL DESCRIPTION

Serial bitstream Digital–to–Analog Converters (DACs) have become commonplace due to their ability to use over–sampling techniques to shape quantization noise. This noise shaping ability enables devices to be built that do not require the component matching of conventional architectures.

The MC145076 bitstream FIR smoothing filter consists of two shift registers, two sets of Hamming Window weighted current source summing networks, and a crystal oscillator inverting buffer.

The current source summing networks are used to implement a Hamming Window function within the MC145076. Each current source tap sinks a constant current that does not change with the number of bits that are set in the shift register. Therefore, each tap acts as a separate single–bit converter with excellent linearity characteristics. The Hamming window was chosen for the FIR filter coefficients because this allows a slightly better second lobe attenuation close to the band where the sampling images are the most troublesome. For a 256 OSR, the MC145076 FIR filter provides greater than 40 dB of stop band attenuation, with approximately 50 dB of attenuation at the 8x image frequencies. This results in an output with full scale images of less than – 70 dB and out–of–band noise better than – 60 dB. For other OSR rates, the filter response scales linearly.

CRYSTAL OSCILLATOR

Provisions for an on–chip crystal oscillator are provided to insure that the clock will be as clean as possible internal to the MC145076 where the digital–to–analog conversion occurs, thus assuring maximum performance. An output clock buffer is provided for driving additional off–chip digital circuitry such as a digital noise shaper, over–sampling FIR filter, or DSP. The off–chip digital processing ensures that the digital switching noise on chip is kept to a minimum.

APPLICATIONS

A smoothing filter is required when using a sigma–delta DAC to reduce the out–of–band noise, and to prevent the high frequencies from intermodulating to lower frequencies. Using the MC145076 with its current sink output is easier than a voltage output filter because it gives a degree of immunity to mutual ground paths between it and the next amplifier.

The circuit shown in Figure 2 is excellent for most applications. However, differential operation does reduce low level switching noise that appears as second harmonic distortion and weak background noise. Although a simple resistor on each current source output to V_{DDA} may be adequate for some applications, the OpAmps provide power supply noise rejection, and, in Figures 2 and 4, also reduce the signal swing on the current output pin of the part to further improve distortion.

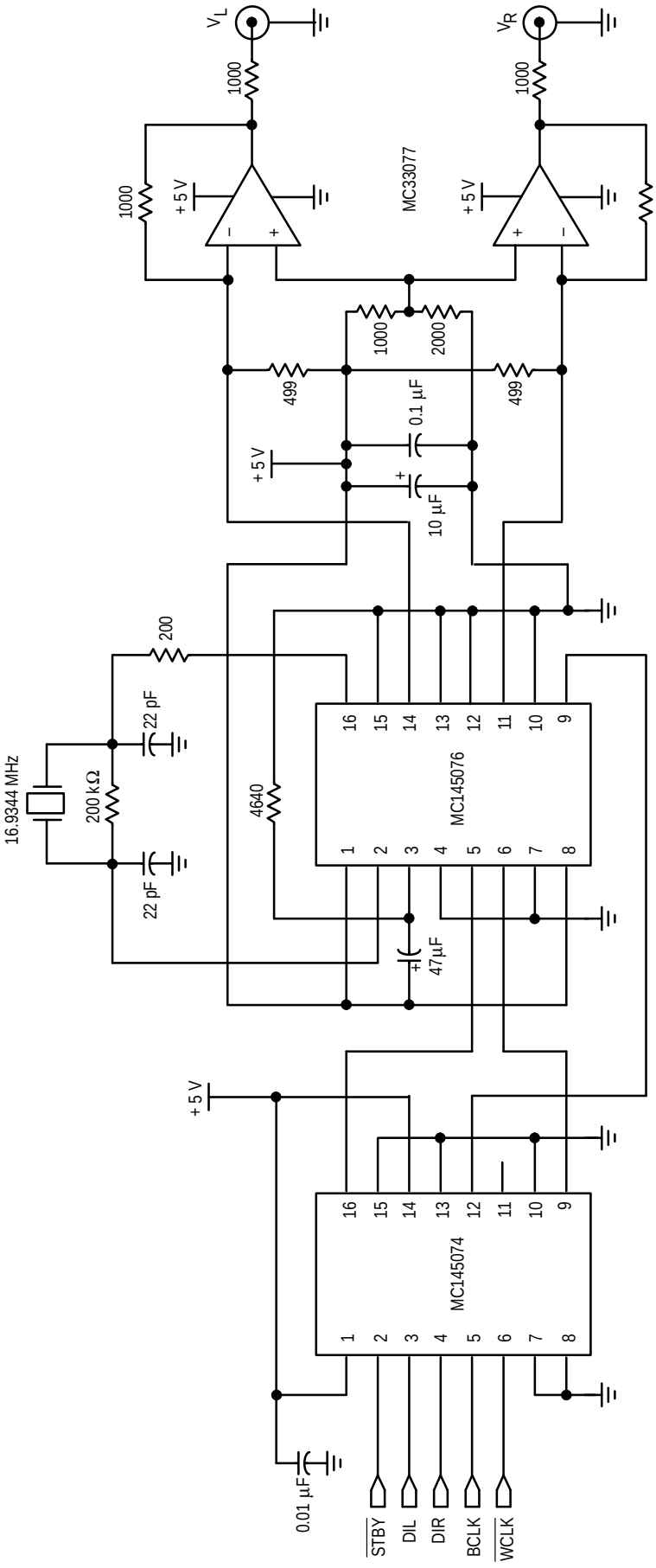


Figure 2. Low Cost +5 V Stereo Audio System, Typically 88 dB S/(N+D)

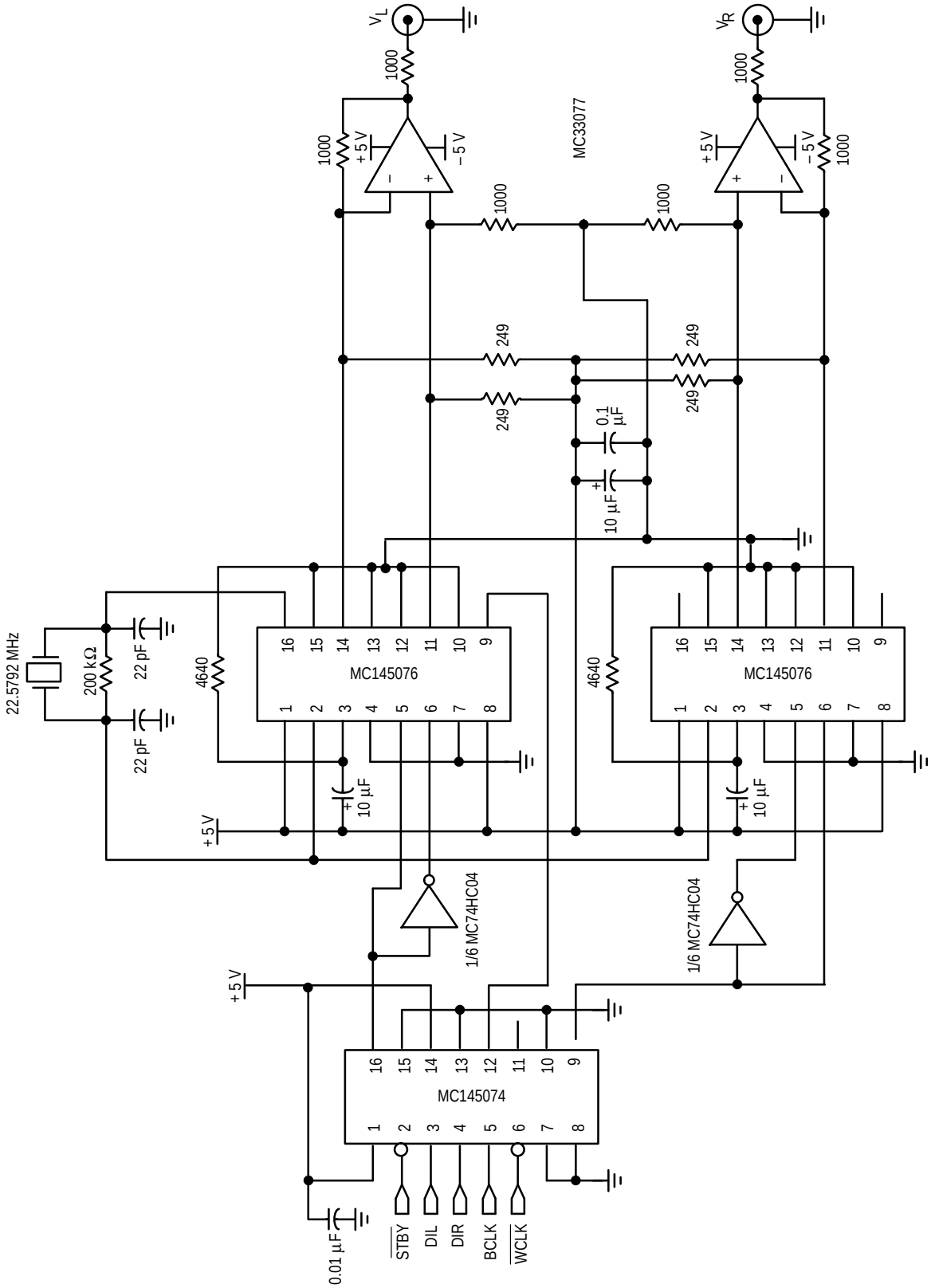


Figure 3. Mid Performance Stereo Audio System, Typically 98 dB S/(N+D)

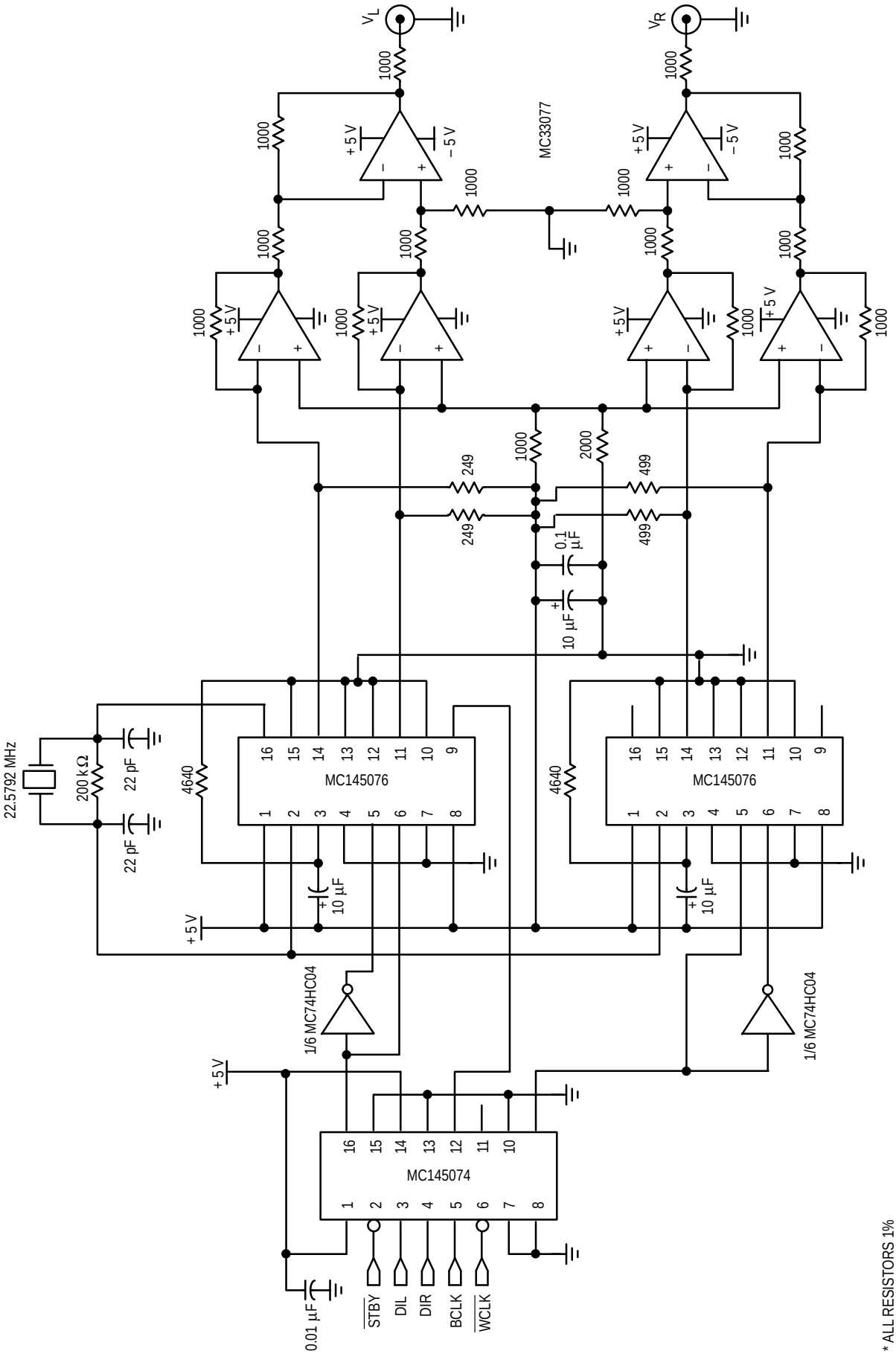
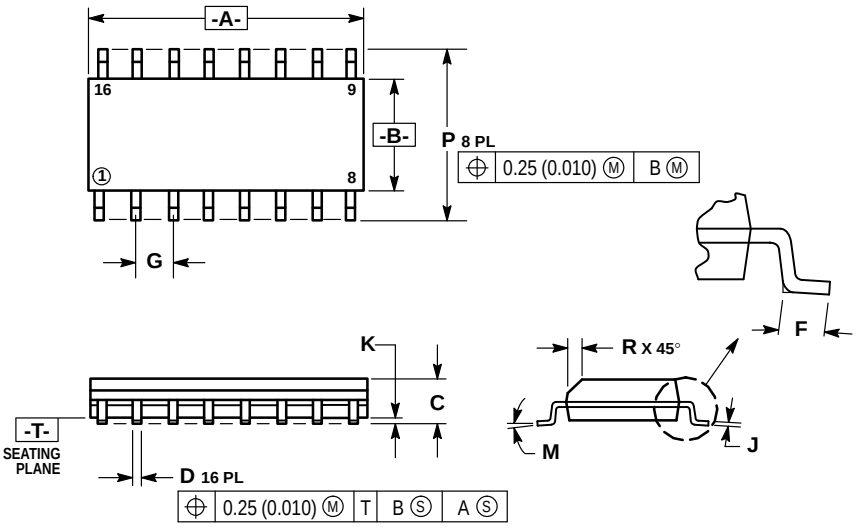


Figure 4. High Performance Stereo Audio System, Typically 105 dB S/(N+D)

PACKAGE DIMENSIONS

SOIC PACKAGE
CASE 751B–05



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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