2.5V or 3.3V 200-MHz 1:15 Clock Distribution Buffer

Features

- **2.5V or 3.3V operation**
- **200-MHz clock support**
- **LVPECL or LVCMOS/LVTTL clock input**
- **LVCMOS-/LVTTL-compatible outputs**
- **15 clock outputs: drive up to 30 clock lines**
- **1X and 1/2X configurable outputs**
- **Output three-state control**
- **350 ps max. output-to-output skew**
- **Pin compatible with MPC949, MPC9449**
- **Available in Commercial and Industrial temp. range**
- **52-pin TQFP package**

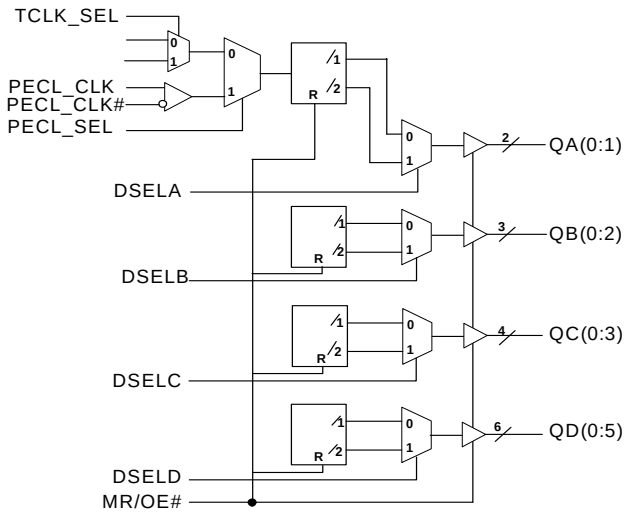
Description

The CY29949 is a low-voltage 200-MHz clock distribution buffer with the capability to select either a differential LVPECL or LVCMOS/LVTTL compatible input clocks. These clock sources can be used to provide for test clocks as well as the primary system clocks. All other control inputs are LVCMOS/LVTTL compatible. The 15 outputs are LVCMOS or LVTTL compatible and can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:30.

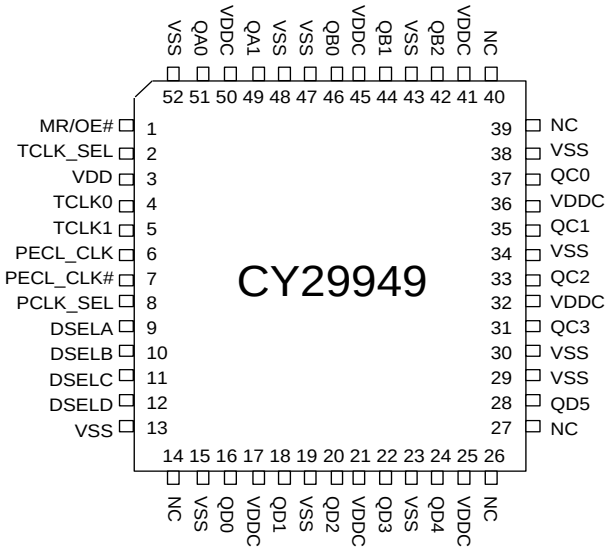
The CY29949 is capable of generating 1X and 1/2X signals from a 1X source. These signals are generated and retimed internally to ensure minimal skew between the 1X and 1/2X signals. SEL(A:D) inputs allow flexibility in selecting the ratio of 1X to1/2X outputs.

The CY29949 outputs can also be three-stated via the MR/OE# input. When MR/OE# is set HIGH, it resets the internal flip-flops and three-states the outputs.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	PWR	I/O	Description
6	PECL_CLK		I, PD	**PECL Input Clock**
7	PECL_CLK#		I, PU	**PECL Input Clock**
4, 5	TCLK(0,1)		I, PU	**External Reference/Test Clock Input**
49, 51	QA(1,0)	VDDC	O	**Clock Outputs**
42, 44, 46	QB(2:0)	VDDC	O	**Clock Outputs**
31, 33, 35, 37	QC(3:0)	VDDC	O	**Clock Outputs**
16, 18, 20, 22, 24, 28	QD(5:0)	VDDC	O	**Clock Outputs**
9, 10, 11, 12	DSEL(A:D)		I, PD	**Divider Select Inputs**. When HIGH, selects ÷2 input divider. When LOW, selects ÷1 input divider.
2	TCLK_SEL		I, PD	**TCLK Select Input**. When LOW, TCLK0 clock is selected and when HIGH TCLK1 is selected.
8	PCLK_SEL		I, PD	**PECL Select Input**. When HIGH, PECL clock is selected and when LOW TCLK(0,1) is selected
1	MR/OE#		I, PD	**Output Enable Input**. When asserted LOW, the outputs are enabled and when asserted HIGH, internal flip-flops are reset and the outputs are three-stated. If more than 1 bank is being used in /2 mode, a reset must be performed (MR/OE# asserted high) after power-up to ensure that all internal flip flops are set to the same state.
17, 21, 25, 32, 36, 41, 45, 50	VDDC			**2.5V or 3.3V Power Supply for Output Clock Buffers**
3	VDD			**2.5V or 3.3V Power Supply**
13, 15, 19, 23, 29, 30, 34, 38, 43, 47, 48, 52	VSS			**Common Ground**
14, 26, 27, 39, 40,	NC			**Not Connected**

Note:
1. PD = internal pull-down, PU = internal pull-up.

Maximum Ratings[2]

Maximum Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V

Maximum Input Voltage Relative to V_{DD}: ..... V_{DD} + 0.3V

Storage Temperature: .....–65°C to + 150°C

Operating Temperature: .....–40°C to +85°C

Maximum ESD Protection.....2 kV

Maximum Power Supply: 5.5V

Maximum Input Current: .....±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters ($V_{DD} = V_{DDC}$ = 3.3V ±10% or 2.5V ±5%, over the specified temperature range)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	V_{DD} = 3.3V, PECL_CLK single ended	1.49	–	1.825	V
		V_{DD} = 2.5V, PECL_CLK single ended	1.10	–	1.45	
		All other inputs	V_{SS}	–	0.8	
V_{IH}	Input High Voltage	V_{DD} = 3.3V, PECL_CLK single ended	2.135	–	2.42	V
		V_{DD} = 2.5V, PECL_CLK single ended	1.75	–	2.0	
		All other inputs	2.0	–	V_{DD}	
I_{IL}	Input Low Current[3]		–	–	–100	µA
I_{IH}	Input High Current[3]		–	–	100	
V_{PP}	Peak-to-Peak Input Voltage PECL_CLK		300	–	1000	mV
V_{CMR}	Common Mode Range[4] PECL_CLK	V_{DD} = 3.3V	V_{DD} – 2.0	–	V_{DD} – 0.6	V
		V_{DD} = 2.5V	V_{DD} – 1.2	–	V_{DD} – 0.6	
V_{OL}	Output Low Voltage[5]	I_{OL} = 20 mA	–	–	0.4	V
V_{OH}	Output High Voltage[5]	I_{OH} = –20 mA, V_{DD} = 3.3V	2.5	–	–	V
		I_{OH} = –20 mA, V_{DD} = 2.5V	1.8		–	
I_{DDQ}	Quiescent Supply Current		–	5	7	mA
I_{DD}	Dynamic Supply Current	V_{DD} = 3.3V, Outputs @ 100 MHz, CL = 30 pF	–	200	–	mA
		V_{DD} = 3.3V, Outputs @ 160 MHz, CL = 30 pF	–	330	–	
		V_{DD} = 2.5V, Outputs @ 100 MHz, CL = 30 pF	–	140	–	
		V_{DD} = 2.5V, Outputs @ 160 MHz, CL = 30 pF	–	235	–	
Zout	Output Impedance	V_{DD} = 3.3V	12	15	18	Ω
		V_{DD} = 2.5V	14	18	22	
C_{in}	Input Capacitance		–	4	–	pF

Notes:

2. **Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. The V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the V_{CMR} range and the input lies within the V_{PP} specification.
5. Driving series or parallel terminated 50Ω (or 50Ω to $V_{DD}/2$) transmission lines.

AC Parameters (V_{DD} = V_{DDC} = 3.3V ±10% or 2.5V ±5%, over the specified temperature range)[6]

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency[7]	V_{DD} = 3.3V	–	–	200	MHz
		V_{DD} = 2.5V	–	–	170	
Tpd	PECL_CLK to Q Delay[7]	V_{DD} = 3.3V	4.0	–	8.6	ns
	TCLK to Q Delay[7]		4.2	–	10.5	
	PECL_CLK to Q Delay[7]	V_{DD} = 2.5V	6.0	–	10.6	
	TCLK to Q Delay[7]		6.2	–	10.5	
FoutDC	Output Duty Cycle[7, 8]	Measured at VDD/2	45	–	55	%
tpZL, tpZH	Output Enable Time (all outputs)		2	–	10	ns
tpLZ, tpHZ	Output Disable Time (all outputs)		2	–	10	ns
Tskew	Output-to-Output Skew[7, 9]		–	250	350	ps
Tskew(pp)	Part-to-Part Skew[10]	PECL_CLK to Q	–	1.5	2.75	ns
		TCLK to Q	–	2.0	4.0	
Tr/Tf	Output Clocks Rise/Fall Time[9]	0.8V to 2.0V, V_{DD} = 3.3V	0.10	–	1.0	ns
		0.6V to 1.8V, V_{DD} = 2.5V	0.10	–	1.3	

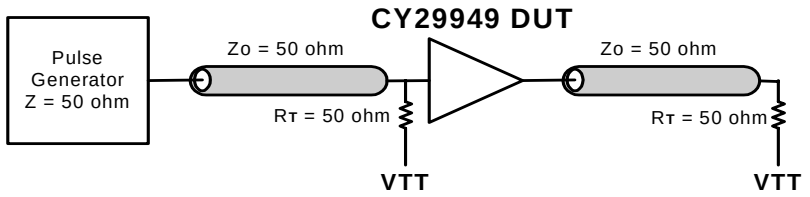


Figure 1. LVCMOS_CLK CY29949 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

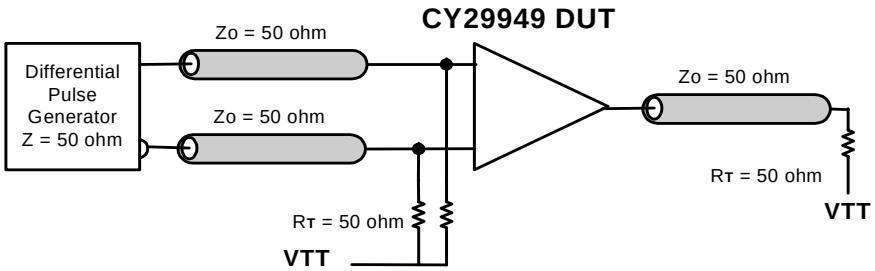


Figure 2. PECL_CLK CY29949 Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

Notes:

6. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
7. Outputs driving 50Ω transmission lines.
8. 50% input duty cycle.
9. See *Figures 1 and 2.*
10. Part-to-Part skew at a given temperature and voltage.

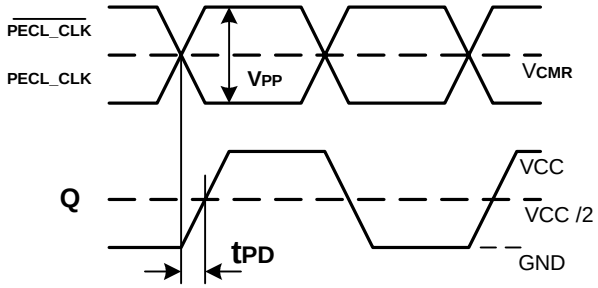


Figure 3. Propagation Delay (TPD) Test Reference

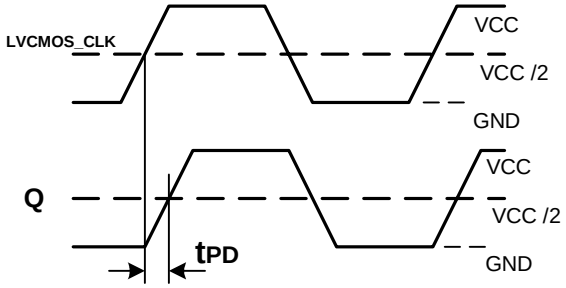
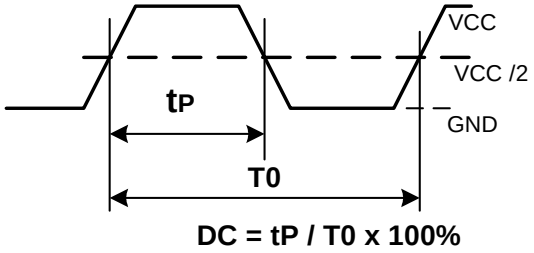


Figure 4. LVCMOS Propagation Delay (TPD) Test Reference



DC = tP / T0 x 100%

Figure 5. Output Duty Cycle (FoutDC)

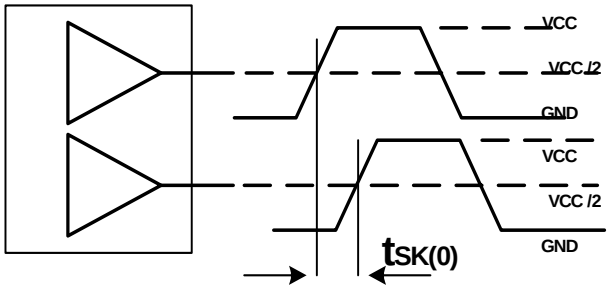


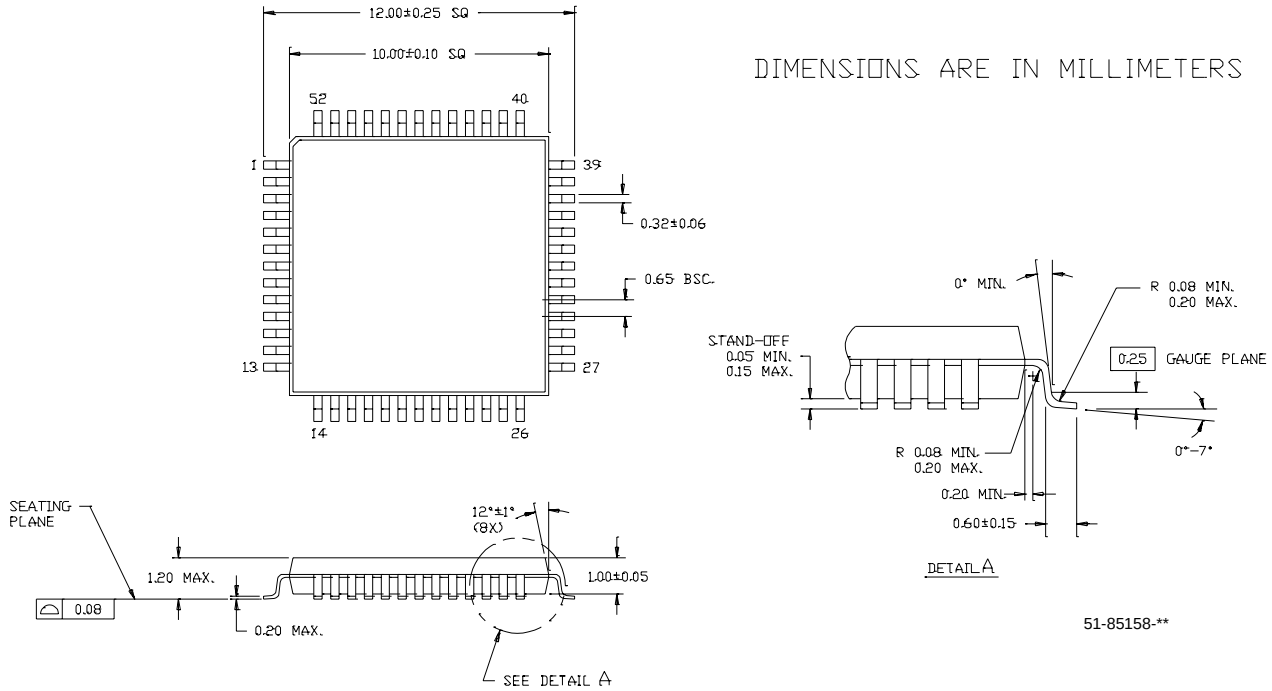
Figure 6. Output-to-Output Skew tsk(0)

Ordering Information

Part Number	Package Type	Production Flow
CY29949AI	52 Pin TQFP	Industrial, –40°C to +85°C
CY29949AIT	52 Pin TQFP - Tape and Reel	Industrial, –40°C to +85°C
CY29949AC	52 Pin TQFP	Commercial, 0°C to +70°C
CY29949ACT	52 Pin TQFP - Tape and Reel	Commercial, 0°C to +70°C

Package Drawing and Dimensions

52-Lead Thin Plastic Quad Flat Pack (10 x 10 x 1.0 mm) A52B



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Document History Page

Document Title: CY29949 2.5V or 3.3V 200-MHz 1:15 Clock Distribution Buffer Document Number: 38-07289				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111100	02/01/02	BRK	New data sheet
*A	116783	08/14/02	HWT	Added commercial temperature range to the Ordering Information table
*B	118463	09/09/02	HWT	Corrected the package diagram from 52 LQFP to 52 TQFP
*C	122881	12/22/02	RBI	Added power-up requirements to Maximum Ratings
*D	130132	11/07/03	RGL	Fixed block diagram and MR/OE# description in the Pin Description table