TPS650842 PMIC for Intel Braswell Platform

1 Device Overview

1.1 Features

- Three Variable-Output Voltage Step-Down Controllers
  - Wide V_{IN} Range From 5.4 V to 21 V
  - Up to 7-A Output Current for BUCK1 (VCC) and BUCK6 (VDDQ), and 11-A for BUCK2 (VGG) Using External FETs
  - I^2C DVS Control (0.5 V to 1.45 V in 10-mV Steps) for BUCK1 and BUCK2
  - Pin-Selectable Dual Output Voltages (1.2 V or 1.35 V) for BUCK6 (VDDQ)
- Three Variable-Output Voltage Synchronous Step-Down Converters
  - V_{IN} Range From 4.5 V to 5.5 V
  - Up to 3.5 A of Output Current for BUCK3 (VNN) With I^2C DVS Control (0.65 V to 1.45 V in 25-mV Steps)
  - Up to 3 A of Output Current for BUCK4 (V1P05A) and up to 1.5 A of Output Current for BUCK5 (V1P8A)
- Three LDO Regulators With Adjustable Output Voltage
  - LDOA1: I^2C-Selectable Output Voltage From 1.35 V to 3.3 V for up to 200 mA of Output Current
  - LDOA2: I^2C-Selectable Output Voltage From 1.05 V, 1.1 V, 1.15 V, and 1.2 V
  - LDOA3: I^2C-Selectable Output Voltage From 1.1 V, 1.15 V, 1.2 V, and 1.24 V
- VTT LDO for DDR3 and DDR4 Memory Termination
- Three Load Switches With Slew Rate Control
  - Up to 300 mA of Output Current With Voltage Drop Less Than 1.5% of Nominal Input Voltage
  - R_{DSON} < 96 mΩ at Input Voltage of 1.8 V
- I^2C Interface (Device Address 0x5E) Supports Standard Mode (100 kHz), Fast Mode (400 kHz), and Fast Mode Plus (1 MHz)
- 64-Pin, Single-Row, 0.4-mm Pitch QFN Package

1.2 Applications

- 2-, 3-, or 4-Series Cell Li-Ion Battery Powered Products (NVDC or Non-NVDC)
- Tablet, Ultrabook, and Notebook Computers
- Mobile PCs and Mobile Internet Devices

1.3 Description

The TPS650842 device is a single-chip solution, power-management IC designed specifically for the latest Intel™ processors targeted for tablets, ultrabooks, and notebooks with NVDC or non-NVDC power architectures, using 2S, 3S, or 4S Li-Ion battery packs. The TPS650842 device is used for essential systems with low-voltage rails merged for the smallest footprint and lowest-cost system-power solution. The TPS650842 device provides the complete power solution based on the Intel Reference Designs. Six highly efficient step-down voltage regulators (VRs), a sink or source LDO (VTT), two LDOs, and three load switches are controlled by power-up sequence logic to provide the proper power rails, sequencing, and protection—including DDR3 and DDR4 memory power. The three regulators (BUCK1–BUCK3) support dynamic voltage scaling (DVS) for maximum efficiency—including support for Connected Standby. The high-frequency VRs use small inductors and capacitors to achieve a small solution size. An I^2C interface allows simple control by an embedded controller (EC) or by a system on chip (SoC). The PMIC comes in an 8-mm × 8-mm single-row QFN package with a thermal pad for good thermal dissipation and ease of board routing.

Use the following email address to request the full version of this data sheet: ipgmkt@list.ti.com.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS650842	RSK (64)	8.00 mm × 8.00 mm

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

1.4 Functional Block Diagram

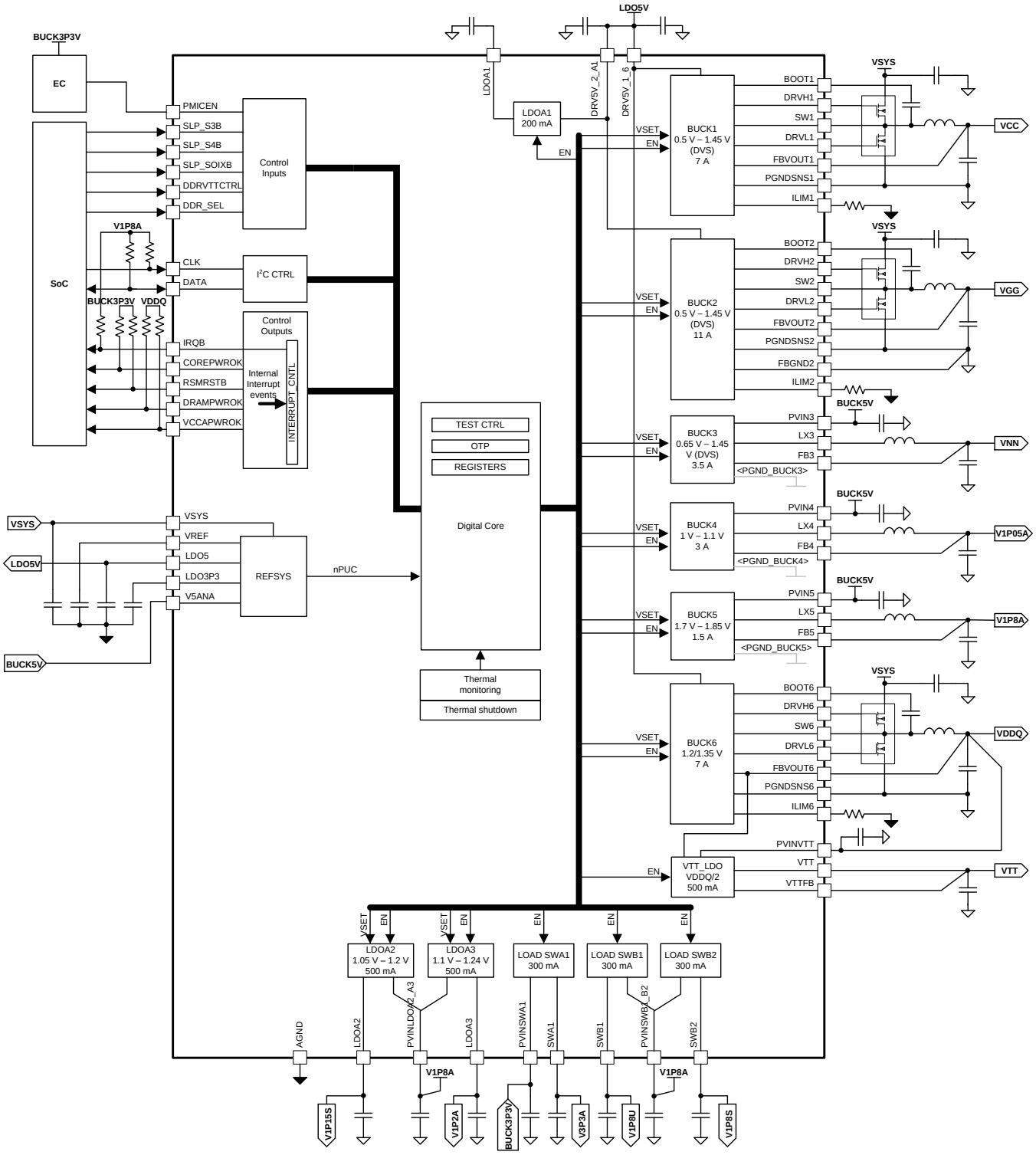


Figure 1-1. PMIC Functional Block Diagram

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2 Device and Documentation Support

2.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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2.2 Trademarks

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2.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

2.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS650842A0RSKT	PREVIEW	QFN	RSK	64		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650842A0 PG1.0	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

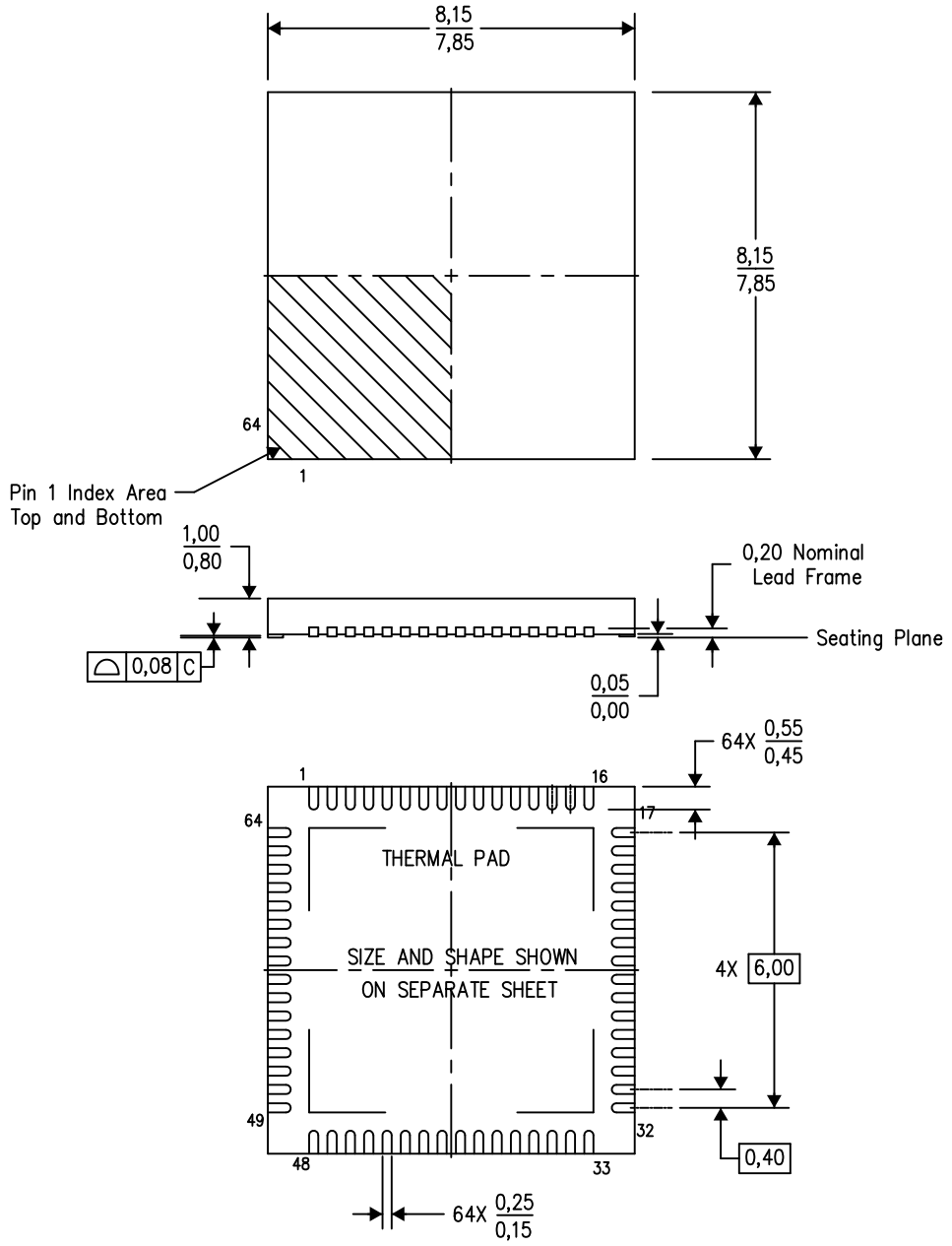
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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