

LMK05028 Low-Jitter Dual Channel Clock Synchronizer With Eight Outputs and Integrated EEPROM

1 Features

- Two Independent PLL Cores, Each Featuring:
 - Jitter: 150-fs RMS for Outputs $\geq$ 100 MHz
 - Phase Noise: -102 dBc/Hz at 100-Hz Offset for 122.88 MHz
 - Hitless Switching: 50-ps Phase Transient With Phase Cancellation
 - Programmable Loop Bandwidth With Fastlock
 - Standards-Compliant Synchronization and Holdover Using a Low-Cost TCXO/OCXO
 - Any Input to Any Output Frequency Translation
- Four Reference Clock Inputs
 - Priority-Based Input Selection (Auto or Manual)
 - Digital Holdover on Loss of Reference
- Eight Clock Outputs With Programmable Drivers
 - Up to Six Different Output Frequencies
 - AC-LVDS, AC-CML, AC-LVPECL, HCSL, and 1.8-V or 2.5-V LVCMOS Output Formats
- EEPROM/ROM for Custom Startup Clock Profiles⁽²⁾
- Flexible Configuration Options
 - 1 Hz (1 PPS) to 750 MHz on Input and Output
 - XO: 10 to 100 MHz, TCXO: 10 to 54 MHz
 - DCO Mode: < 1 ppt/Step for Fine Frequency and Phase Steering (IEEE 1588 Slave Operation)
 - Zero Delay for Deterministic Phase Offset
 - Robust Clock Monitoring and Status
 - I2C or SPI Interface
- Excellent Power Supply Noise Rejection
- Supply: 3.3-V Core With 1.8-V, 2.5-V, or 3.3-V Output
- Industrial Temperature Range: -40°C to $+85^{\circ}\text{C}$

2 Applications

- SyncE (G.8262), SONET/SDH (Stratum 3/3E, G.813, GR-1244, GR-253), IEEE 1588 (PTP) Slave Clock, or Optical Transport Network (G.709) Synchronization
- Telecom and Enterprise Line Cards
- Wireless Base Station (BTS)
- Test and Measurement, Broadcast Video, and Medical Ultrasound
- Jitter and Wander Attenuation, Precise Frequency Translation, and Low-Jitter Clock Generation for FPGA, DSP, ASIC, and CPU Devices.

3 Description

The LMK05028 device is a high-performance clock generator, jitter cleaner, and clock synchronizer with advanced reference clock selection and hitless switching to meet the stringent requirements of communications infrastructure applications. The ultra-low jitter reduces bit error rates (BER) in high-speed serial links.

The device has two independent PLL cores that can each synchronize or lock to one of four reference clock inputs, and the LMK05028 can generate up to eight output clocks with up to six different frequencies.

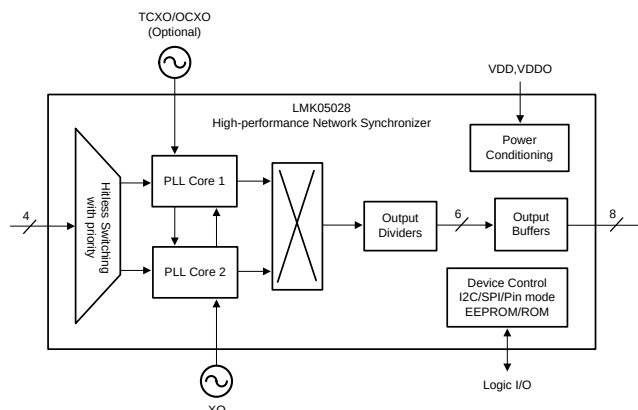
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMK05028	VQFN (64)	9.00 mm $\times$ 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Contact TI Field Sales to inquire about custom factory pre-programmed devices.

LMK05028 Simplified Block Diagram



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4 Revision History

DATE	REVISION	NOTES
February 2018	*	Initial release.

5 Description (continued)

The flexible PLL cores provide programmable loop bandwidth for input jitter and wander attenuation and fractional frequency translation to generate any output frequency from any input frequency. Each PLL core has up to 3 feedback loops with two digital PLLs (DPLLs) and one analog PLL (APLL) with integrated VCO. Each core supports 3 loop or 2 loop mode configurations to optimize clock performance and solution cost for different use cases.

In three-loop mode, the TCXO/OCXO source determines the free-run and holdover frequency stability and accuracy, and the XO source determines the output phase noise and jitter performance over the 12-kHz to 20-MHz band. Three-loop mode allows the use of a cost-effective, low-frequency TCXO/OCXO (10 or 12.8 MHz) to support standards-compliant frequency stability and low loop bandwidth (≤ 10 Hz) required in synchronization applications like SyncE and SONET/SDH. Two-loop mode allows for either higher loop bandwidth, relaxed holdover operation where the XO determines the free-run and holdover frequency stability and accuracy, or both.

The reference input muxes supports automatic input selection or manual input selection through software or pin control. The reference switchover event will be hitless with superior phase transient performance (50 ps typical). The reference clock input monitoring block monitors the clock inputs and will perform a switchover or holdover when a loss of reference (LOR) is detected. A LOR can be detected upon any violation of the threshold limits set for the input clock amplitude, frequency, missing pulse, and runt pulse monitors. The threshold limits for each input monitor can be set and enabled independently per clock input. The holdover output frequency accuracy can be determined by the historical average frequency to minimize frequency and phase disturbance during LOR.

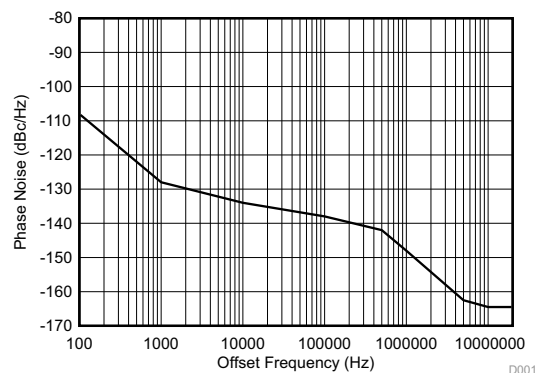
The device has eight outputs with programmable drivers, allowing up to eight differential clocks, eight LVCMOS pairs (two per pair), or a combination of both. The output clocks can be derived from either PLL/VCO domain through the output channel muxes. A 1-PPS output can be supported on outputs 0 and 7. The output dividers have a SYNC feature to allow multiple outputs to be phase-aligned. If needed, zero delay can be enabled to achieve a deterministic phase offset between any specified PLL output clock and its selected input clock.

To support IEEE 1588 PTP slave clock or other clock steering applications, each PLL core also supports DCO mode with <1 -ppt (part per trillion) frequency resolution for precise frequency and phase adjustment through external software or pin control.

The device is fully programmable through I2C or SPI interface and features custom start-up clock configuration with the internal EEPROM, which is factory-set and in-system programmable. Internal LDO regulators provide excellent power supply noise rejection (PSNR) to reduce the cost and complexity of the power delivery network. The clock input and PLL monitors can be observed through the interrupt registers and status pins for full diagnostic capability.

Table 1. Clock Output Phase Jitter for 156.25 MHz

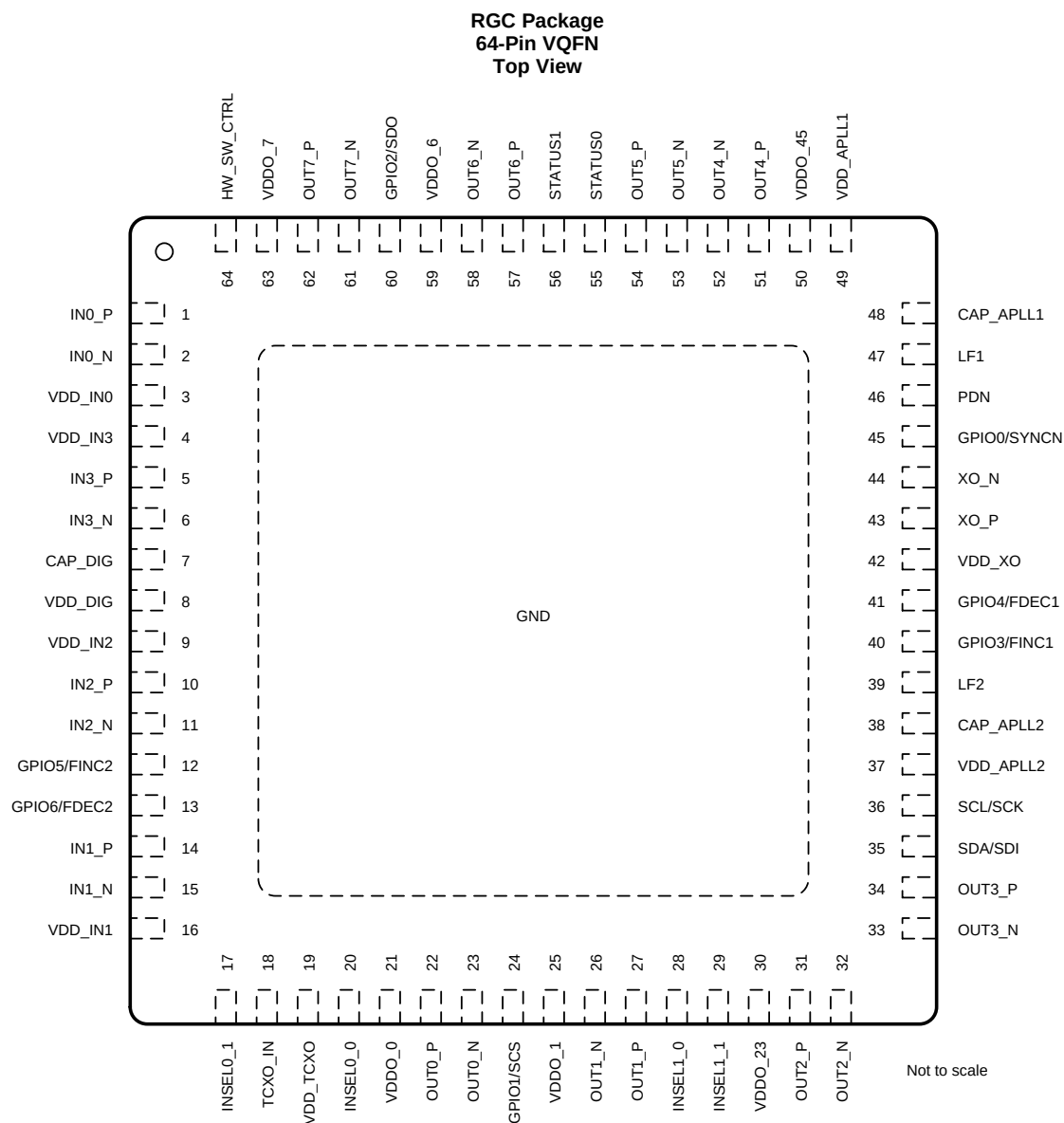
INTEGRATION BANDWIDTH	TYPICAL JITTER	MAXIMUM JITTER
12 kHz – 20 MHz	150-fs RMS	225-fs RMS



AC-LVPECL output, IN = 19.44 MHz, XO = 48 MHz, TCXO = 10 MHz

Figure 1. Clock Output Phase Noise for 156.25 MHz

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
POWER			
GND	PAD	G	Ground / Thermal Pad. The exposed pad must be connected to PCB ground for proper electrical and thermal performance. A 7x7 via pattern is recommended to connect the IC ground pad to the PCB ground layers.
VDD_IN0	3	P	
VDD_IN1	16	P	
VDD_IN2	9	P	
VDD_IN3	4	P	
			Core Supply (3.3 V) for Reference Inputs 0 to 3. Place a nearby 0.1-μF bypass capacitor on each pin.

(1) G = Ground, P = Power, I = Input, O = Output, I/O = Input or Output, A = Analog.

Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
VDD_XO	42	P	Core Supply (3.3 V) for XO and TCXO Inputs. Place a nearby 0.1-μF bypass capacitor on each pin.
VDD_TCXO	19	P	
VDD_APLL1	49	P	Core Supply (3.3 V) for PLL1, PLL2, and Digital Blocks. Place a nearby 0.1-μF bypass capacitor on each pin.
VDD_APLL2	37	P	
VDD_DIG	8	P	
VDDO_0	21	P	Output Supply (1.8, 2.5, or 3.3 V) for Clock Outputs 0 to 7. Place a nearby 0.1-μF bypass capacitor on each pin.
VDDO_1	25	P	
VDDO_23	30	P	
VDDO_45	50	P	
VDDO_6	59	P	
VDDO_7	63	P	
CORE BLOCKS			
LF1	47	A	External Loop Filter Capacitor for APLL1 and APLL2. Place a nearby 0.1-μF capacitor on each pin.
LF2	39	A	
CAP_APLL1	48	A	External Bypass Capacitors for APLL1, APLL2, and Digital Blocks. Place a nearby 10-μF bypass capacitor on each pin.
CAP_APLL2	38	A	
CAP_DIG	7	A	
INPUT BLOCKS			
IN0_P	1	I	DPLL Reference Clock Inputs 0 to 3. Each input pair can accept a differential or single-ended clock signal for synchronizing the DPLLs. Each pair has programmable input type with internal termination to support AC- or DC-coupled clocks. A single-ended LVCMOS clock can applied to the P input with the N input pulled down to ground. An unused input pair can be left floating. LVCMOS input mode is recommended for input frequencies below 1 MHz.
IN0_N	2	I	
IN1_P	14	I	
IN1_N	15	I	
IN2_P	10	I	
IN2_N	11	I	
IN3_P	5	I	
IN3_N	6	I	
XO_P	43	I	XO Input. This input pair can accept a differential or single-ended clock signal from a low-jitter local oscillator to lock the APLLs. This input has programmable input type with internal termination to support AC- or DC-coupled clocks. A single-ended LVCMOS clock can applied to the P input with the N input pulled down to ground.
XO_N	44	I	
TCXO_IN	18	I	TCXO Input. This input can accept an AC-coupled sinewave, clipped-sinewave, or single-ended clock signal from a stable oscillator (TCXO/OCXO) to lock the TCXO-DPLL if used by a DPLL configuration. The input swing must be less than 1.2 Vpp before AC-coupling to the input pin, which a weak internal biasing to about 0.6 V and no internal termination. Leave pin floating if unused.
OUTPUT BLOCKS			
OUT0_P	22	O	Clock Outputs 0 to 3 Bank. Each programmable output driver pair can support AC-LVDS, AC-CML, AC-LVPECL, HCSL, or 1.8/2.5-V LVCMOS clocks (one or two per pair). Unused differential outputs should be terminated if active or left floating if disabled through registers. The OUT[0:3] bank requires at least one clock from PLL2 domain if enabled. This bank is preferred for PLL2 clocks to minimize output crosstalk.
OUT0_N	23	O	
OUT1_P	27	O	
OUT1_N	26	O	
OUT2_P	31	O	
OUT2_N	32	O	
OUT3_P	34	O	
OUT3_N	33	O	

Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
OUT4_P	51	O	Clock Outputs 4 to 7 Bank. Each programmable output driver pair can support AC-LVDS, AC-CML, AC-LVPECL, HCSL, or 1.8/2.5-V LVCMOS clocks (one or two per pair). Unused differential outputs should be terminated if active or left floating if disabled through registers. The OUT[4:7] bank requires at least one clock from PLL1 domain. This bank is preferred for PLL1 clocks to minimize output crosstalk.
OUT4_N	52	O	
OUT5_P	54	O	
OUT5_N	53	O	
OUT6_P	57	O	
OUT6_N	58	O	
OUT7_P	62	O	
OUT7_N	61	O	
LOGIC CONTROL / STATUS ⁽²⁾⁽³⁾			
HW_SW_CTRL	64	I	Device Start-Up Mode Select (3-level, 1.8-V compatible). This input selects the device start-up mode that determines the memory page used to initialize the registers, serial interface, and logic pin functions. The input level is sampled only at device power-on reset (POR). See Table 2 for start-up mode descriptions and logic pin functions.
PDN	46	I	Device Power-Down (active low). When PDN is pulled low, the device is in hard reset and all blocks including the serial interface are powered-down. When PDN is pulled high, the device is started according to device mode selected by HW_SW_CTRL and begins normal operation with all internal circuits reset to their initial state.
SDA/SDI	35	I/O	I2C Serial Data I/O (SDA) or SPI Serial Data Input (SDI). See Table 2 . The default 7-bit I2C address is 11000xxb, where the MSB bits (11000b) are initialized from on-chip EEPROM and the LSB bits (xxb) are determined by the logic input pins. When HW_SW_CTRL is 0, the LSBs are determined by the GPIO[2:1] input levels during POR. When HW_SW_CTRL is 1, the LSBs are fixed to 00b.
SCL/SCK	36	I	I2C Serial Clock Input (SCL) or SPI Serial Clock Input (SCK). See Table 2 .
GPIO0/SYNCN	45	I	
GPIO1/SCS	24	I	Multifunction Inputs or Outputs. See Table 2 .
GPIO2/SDO	60	I/O	
GPIO3/FINC1	40	I	
GPIO4/FDEC1	41	I	
GPIO5/FINC2	12	I/O	
GPIO6/FDEC2	13	I/O	
STATUS1	56	I/O	Status Outputs [1:0]. Each output has programmable status signal selection, driver type (3.3-V LVCMOS or open-drain), and status polarity. Open-drain requires an external pullup resistor. Leave pin floating if unused.
STATUS0	55	I/O	
INSEL0_1	17	I	Manual Reference Input Selection for DPLL1. INSEL0_[1:0] = 00b (IN0), 01b (IN1), 10b (IN2), or 11b (IN3). Leave pin floating if unused.
INSEL0_0	20	I	
INSEL1_1	29	I	Manual Reference Input Selection for DPLL2. INSEL1_[1:0] = 00b (IN0), 01b (IN1), 10b (IN2), or 11b (IN3). Leave pin floating if unused.
INSEL1_0	28	I	

- (2) Internal resistors: PDN pin has 200-k Ω pullup to VDD. Each HW_SW_CTRL, GPIO, and STATUS pin has a 150-k Ω bias to V_{IM} (~0.9 V) when PDN = 0 or 400-k Ω pulldown when PDN = 1. Each INSEL pin has a 85-k Ω pullup to 1.8 V when PDN = 0 or 400-k Ω pulldown when PDN = 1.

- (3) Unless otherwise noted: Logic inputs are 2-level, 1.8-V compatible inputs. Logic outputs are 3.3-V LVCMOS levels.

Table 2. Device Start-Up Modes With Logic Pin Functions

HW_SW_CTRL INPUT LEVEL ⁽¹⁾	START-UP MODE	MODE DESCRIPTION
0	EEPROM + I2C (Soft pin mode)	Registers are initialized from EEPROM, and I2C interface is enabled. Logic pins: <ul style="list-style-type: none"> • SDA, SCL: I2C Data, I2C Clock (open-drain). Pins require external pullups > 1 kΩ. • GPIO0: Output SYNC Input (active low). Tie pin high externally if not used. • GPIO[2:1] ⁽¹⁾: I2C Address LSB Select Input (00, 01, 10, 11b) • GPIO[4:3] ⁽²⁾: DPLL1 DCO Frequency Decrement and Increment Inputs (active high) • GPIO[6:5] ⁽²⁾⁽³⁾: DPLL2 DCO Frequency Decrement and Increment Inputs (active high), or Status Outputs
Float (V _{IM})	EEPROM + SPI ⁽⁴⁾ (Soft pin mode)	Registers are initialized from EEPROM, and SPI interface is enabled. Logic pins: <ul style="list-style-type: none"> • SDA, SCL: SPI Data Input (SDI), SPI Clock (SCK) • GPIO1: SPI Chip Select (SCS) • GPIO2: SPI Data Output (SDO) • GPIO[6:3, 0]: Same as for HW_SW_CTRL = 0
1	ROM + I2C (Hard pin mode)	Registers are initialized from the ROM page selected by GPIO pins, and I2C interface is enabled. Logic pins: <ul style="list-style-type: none"> • SDA, SCL: I2C Data, I2C Clock (open-drain). Pins require external pullups > 1 kΩ. • GPIO[3:0] ⁽¹⁾: ROM Page Select Input (0000 to 1111b) • GPIO[6:5] ⁽³⁾: Status Outputs • GPIO4: Not used during POR After POR, GPIO[6:3] can function the same as for HW_SW_CTRL = 0 if enabled by registers.

(1) The input levels on these pins are sampled only during POR.

(2) These GPIO pins are only functional when the DCO feature and FINC/FDEC pin controls are enabled by registers.

(3) As status outputs, the GPIO[6:5] pins have the same capabilities as the STATUS[1:0] pins described in .

(4) When HW_SW_CTRL = Float (V_{IM}), the STATUS[1:0] pins momentarily function as 3-level inputs and both pins must be biased to V_{IM} (internally or externally) during device POR to ensure proper start-up. If either STATUS pin is connected to an external host device (MCU, FPGA), the external device must be configured with high-impedance inputs (no pullup or pulldown) to avoid conflict with the internal bias to V_{IM}. If needed, external biasing resistors (10-kΩ pullup to 3.3 V and 3.75-kΩ pulldown) can be connected on each STATUS pin to bias the inputs to V_{IM} during POR.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
VDD ⁽²⁾	Core Supply Voltages	−0.3	3.6	V
VDDO ⁽³⁾	Output Supply Voltages	−0.3	3.6	V
Vin	Input Voltage for Clock and Logic Inputs	−0.3	VDD + 0.3	V
Vout	Output Voltage for Clock and Logic Outputs	−0.3	VDD + 0.3	V
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) VDD refers to all core supply pins or voltages. All VDD core supplies should be powered-on before internal power-on reset (POR).

(3) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD ⁽¹⁾	Core Supply Voltages	3.135	3.3	3.465	V
VDDO ⁽¹⁾	Output Supply Voltages	AC-LVDS/CML/LVPECL, HCSL		3.465	V
		1.8-V or 2.5-V LVCMOS ⁽²⁾		2.625	V
T _A	Ambient Temperature	–40	25	85	°C
T _J	Junction Temperature			135	°C
t _{VDD}	Power Supply Ramp Time ⁽³⁾	0.01		100	ms
n _{EEcyc}	EEPROM Programming Cycles			100	cycles

- (1) VDD refers to all core supply pins or voltages. All VDD core supplies should be powered-on before internal power-on reset (POR).
- (2) The LVCMOS driver supports full rail-to-rail swing when VDDO_x is 1.8 V or 2.5 V ± 5%. When VDDO_x is 3.3 V, the LVCMOS driver cannot swing fully to the positive rail due to the dropout voltage of the output channel's internal LDO regulator.
- (3) Time for VDD to ramp monotonically above 2.7 V for proper internal POR. For slower or non-monotonic VDD ramp, hold PDN low until after VDD voltages are valid.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾ (2) (3)		LMK05028	UNIT
		RGC (VQFN)	
		64 PINS	
		0-LFM AIRFLOW	
R _{θJA}	Junction-to-ambient thermal resistance	20.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	6.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	4.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	0.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	4.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The thermal information is based on a 10-layer 200 mm x 250 mm board with 49 thermal vias (7 x 7 pattern, 0.3 mm holes)
- (3) ψ_{JB} can allow the system designer to measure the board temperature (T_{PCB}) with a fine-gauge thermocouple and back-calculate the device junction temperature, T_J = T_{PCB} + (ψ_{JB} × Power). Measurement of ψ_{JB} is defined by JESD51-6.

7.5 Power Supply Characteristics⁽¹⁾

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C. Specification applies to both Configuration A ⁽²⁾ and Configuration B ⁽³⁾ unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD_IN[0,1,3]	Core Supply Current (VDD_INx)		3.5		mA
IDD_IN2	Core Supply Current (VDD_INx)		6		mA
IDD_PLL1	Core Supply Current (VDD_PLL1)	Configuration A ⁽²⁾	160		mA
		Configuration B ⁽³⁾	185		mA
IDD_PLL2	Core Supply Current (VDD_PLL2)	Configuration A	138		mA
		Configuration B	160		mA
IDD_DIG	Core Supply Current (VDD_DIG)	Configuration A	34		mA
		Configuration B	42		mA
IDD_XO	Core Supply Current (VDD_XO)		25		mA

- (1) Total device current can be estimated by summing the individual IDD_x and IDDO_x per pin for all blocks enabled in a given configuration.
- (2) Configuration A (All blocks on except TCXO_IN and both TCXO-DPLLs): IN[0:3] = 25 MHz, XO = 48.0048 MHz, TCXO_IN disabled. Both DPLLs in 2 loop mode, DPLL[1:2] REF-TDC ~ 0.4 MHz, VCO1 = 5 GHz, PLL1_P1 = 8, VCO2 = 5.5296 GHz, PLL2_P1 = 9.
- (3) Configuration B (All blocks on): IN[0:3] = 25 MHz, XO = 48.0048 MHz, TCXO_IN = 10 MHz. Both DPLLs in 3 loop mode, DPLL[1:2] REF-TDC ~ 0.4 MHz, TCXO-TDC = 10 MHz, VCO1 = 5 GHz, PLL1_P1 = 8, VCO2 = 5.5296 GHz, PLL2_P1 = 9.

Power Supply Characteristics⁽¹⁾ (continued)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C. Specification applies to both Configuration A ⁽²⁾ and Configuration B ⁽³⁾ unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD_TCXO Core Supply Current (VDD_TCXO)	Configuration A		1		mA
	Configuration B		6		mA
IDDO_X Output Supply Current (VDDO_x = 3.3 V ± 5%)	AC-LVDS (one pair), 156.25 MHz		22		mA
	AC-CML (one pair), 156.25 MHz		24		mA
	AC-LVPECL (one pair), 156.25 MHz		27		mA
	HCSL (one pair), 156.25 MHz		33		mA
	2.5-V LVCMOS (two outputs), 156.25 MHz, 5-pF load		40		mA
	1.8-V LVCMOS (two outputs), 156.25 MHz, 5-pF load		33		mA
IDD_PD Total Supply Current in Power-down (all VDD and VDDO pins)	Device powered-down (PDN pin = 0)		40		mA

7.6 Clock Input Characteristics (INx_P/N)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{CLK} Input frequency ⁽¹⁾	LVCMOS input	1E-6		250	MHz
	Differential input ⁽²⁾	1		750	
V _{IH} Input high voltage	LVCMOS input	1.4			V
V _{IL} Input low voltage		0		0.8	V
V _{IN_DIFF} Differential input voltage swing, peak-peak (V _P – V _N)	Differential input	0.2		2	V
dV/dt Input slew rate ⁽¹⁾		0.2			V/ns
I _{IN} Input leakage current		–100		100	μA
C _{IN} Input capacitance	Single-ended, each pin		2		pF

(1) Parameter is specified by characterization and is not tested in production.

(2) For inputs less than 1 MHz, use LVCMOS input or else disable the amplitude monitor.

7.7 XO Input Characteristics (XO_P/N)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{CLK} Input frequency ⁽¹⁾		10		100	MHz
V _{IH} Input high voltage	LVCMOS input	1.4		2.6	V
V _{IL} Input low voltage		0		0.8	V
V _{IN_DIFF} Differential input voltage swing, peak-peak (V _P – V _N)	Differential input	0.2		2	V
dV/dt Input slew rate ⁽¹⁾		0.2			V/ns
IDC Input duty cycle		40		60	%
I _{IN} Input leakage current		–100		100	uA
C _{IN} Input capacitance	Single-ended, each pin		1		pF

(1) Parameter is specified by characterization and is not tested in production.

7.8 TCXO/OCXO Input Characteristics (TCXO_IN)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{CLK} Input frequency ⁽¹⁾		10		54	MHz
V _{IN} Input voltage swing		0.8		1.3	V
V _{BIAS} Input bias voltage	Biased internally	TBD	0.6	TBD	V
dV/dt Input slew rate ⁽¹⁾		0.2			V/ns
IDC Input duty cycle		40		60	%
C _{IN} Input capacitance			10		pF

(1) Parameter is specified by characterization and is not tested in production.

7.9 APLL/VCO Characteristics

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{VCO1} VCO1 Frequency range ⁽¹⁾		4.8		5.4	GHz
f _{VCO2} VCO2 Frequency range ⁽¹⁾		5.5		6.2	GHz

(1) Parameter is specified by characterization and is not tested in production.

7.10 2.5-V LVCMOS Output Characteristics (OUTx_P/N)

VDD = 3.3 V ± 5%, VDDO = 2.5 V ± 5%, T_A = –40°C to 85°C, Fast slew rate

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OUT} Output frequency ⁽¹⁾		1E-6		200	MHz
V _{OH} Output high voltage	I _{OH} = 1 mA	1.9			V
V _{OL} Output low voltage	I _{OL} = 1 mA			0.525	V
I _{OH} Output high current			-48		mA
I _{OL} Output low current			55		mA
t _R /t _F Output rise/fall time ⁽¹⁾	20% to 80%		250	TBD	ps
t _{SKEW} Output-to-output skew ⁽¹⁾	Same post divider, output divide values, and output type			100	ps
t _{SKEW} Output-to-output skew ⁽¹⁾	Same post divider and output divide values, LVCMOS-to-DIFF			1.5	ns
PN-Floor Output phase noise floor (f _{OFFSET} = 10 MHz) ⁽¹⁾	66.66 MHz		-155		dBc/Hz
ODC Output duty cycle ⁽¹⁾	Not PLL bypass output	45		55	%
R _{OUT} Output impedance			50		Ω

(1) Parameter is specified by characterization and is not tested in production.

7.11 1.8-V LVCMOS Output Characteristics (OUTx_P/N)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, T_A = –40°C to 85°C, Fast slew rate

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OUT} Output frequency ⁽¹⁾		1E-6		200	MHz
V _{OH} Output high voltage	I _{OH} = 1 mA	1.2			V
V _{OL} Output low voltage	I _{OL} = 1 mA			0.4	V
I _{OH} Output high current			-23		mA
I _{OL} Output low current			24		mA
t _R /t _F Output rise/fall time ⁽¹⁾	20% to 80%		250	TBD	ps
t _{SKEW} Output-to-output skew ⁽¹⁾	Same post divider, output divide values, and output type			100	ps
t _{SKEW} Output-to-output skew ⁽¹⁾	Same post divider and output divide values, LVCMOS-to-DIFF			1.5	ns

(1) Parameter is specified by characterization and is not tested in production.

1.8-V LVCMOS Output Characteristics (OUTx_P/N) (continued)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, T_A = –40°C to 85°C, Fast slew rate

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN-Floor Output phase noise floor (f _{OFFSET} = 10 MHz) ⁽¹⁾	66.66 MHz		–155		dBc/Hz
ODC Output duty cycle ⁽¹⁾	Not PLL bypass output	45		55	%
R _{OUT} Output impedance			50		Ω

7.12 AC-LVDS Output Characteristics (OUTx_P/N)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C, Output pair AC-coupled to 100-Ω differential load, Fast slew rate

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OUT} Output frequency ^{(1) (2)}				750	MHz
V _{OD} Output voltage swing (V _{OH} –V _{OL})	f _{OUT} ≥ 25 MHz	250	400	450	mV
V _{ODpp} Differential output voltage swing, peak-to-peak		2 × V _{OD}			V
V _{OS} Output common mode		100		430	mV
t _{SKW} Output-to-output skew ⁽¹⁾	Same post divider, output divide values, and output type			100	ps
t _R /t _F Output rise/fall time ⁽¹⁾	20% to 80%, < 300 MHz		150	300	ps
	±100 mV around center point, > 300 MHz			200	
PN-Floor Output phase noise floor (f _{OFFSET} = 10 MHz)	156.25 MHz		–160		dBc/Hz
ODC Output duty cycle ⁽¹⁾	Not PLL bypass output	45		55	%

(1) Parameter is specified by characterization and is not tested in production.

(2) An output frequency over the f_{OUT} max spec is possible, but the output swing may be less than the V_{OD} min spec.

7.13 AC-CML Output Characteristics (OUTx_P/N)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C, Output pair AC-coupled to 100-Ω differential load, Fast slew rate

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OUT} Output frequency ^{(1) (2)}				750	MHz
V _{OD} Output voltage swing (V _{OH} –V _{OL})	f _{OUT} ≥ 25 MHz	400	600	800	mV
V _{ODpp} Differential output voltage swing, peak-to-peak		2 × V _{OD}			V
V _{OS} Output common mode		150		550	mV
t _{SKW} Output-to-output skew ⁽¹⁾	Same post divider, output divide values, and output type			100	ps
t _R /t _F Output rise/fall time ⁽¹⁾	20% to 80%, < 300 MHz		150	300	ps
	±100 mV around center point, > 300 MHz			200	
PN-Floor Output phase noise floor (f _{OFFSET} = 10 MHz)	156.25 MHz		–160		dBc/Hz
ODC Output duty cycle ⁽¹⁾	Not PLL bypass output	45		55	%

(1) Parameter is specified by characterization and is not tested in production.

(2) An output frequency over the f_{OUT} max spec is possible, but the output swing may be less than the V_{OD} min spec.

7.14 AC-LVPECL Output Characteristics (OUTx_P/N)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C, Output pair AC-coupled to 100-Ω differential load, Fast slew rate

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OUT}	Output frequency ^{(1) (2)}				750	MHz
V _{OD}	Output voltage swing (V _{OH} -V _{OL})	f _{OUT} ≥ 25 MHz	500	800	1000	mV
V _{ODpp}	Differential output voltage swing, peak-to-peak		2 × V _{OD}			V
V _{OS}	Output common mode		300		700	mV
t _{SKEW}	Output-to-output skew ⁽¹⁾	Same post divider, output divide values, and output type			100	ps
t _R /t _F	Output rise/fall time ⁽¹⁾	20% to 80%, < 300 MHz		150	300	ps
		±100 mV around center point, > 300 MHz			200	
PN-Floor	Output phase noise floor (f _{OFFSET} = 10 MHz)	156.25 MHz		−162		dBc/Hz
ODC	Output duty cycle ⁽¹⁾	Not PLL bypass output	45		55	%

(1) Parameter is specified by characterization and is not tested in production.

(2) An output frequency over the f_{OUT} max spec is possible, but the output swing may be less than the V_{OD} min spec.

7.15 HCSL Output Characteristics (OUTx_P/N)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C, Output pair terminated with 50 Ω to GND, Fast slew rate

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{OUT}	Output frequency			400	MHz
V _{OH}	Output high voltage	600		880	mV
V _{OL}	Output low voltage	–150		150	mV
t _{SKEW}	Output-to-output skew ⁽¹⁾	Same post divider, output divide values, and output type		100	ps
dV/dt	Output slew rate ⁽¹⁾	Measured from –150 mV to +150 mV on the differential waveform	2.5	8	V/ns
PN-Floor	Output phase noise floor (f _{OFFSET} = 10 MHz)	100 MHz	–158		dBc/Hz
ODC	Output duty cycle ⁽¹⁾	Not PLL bypass output	45	55	%

(1) Parameter is specified by characterization and is not tested in production.

7.16 2-Level Logic Input Characteristics (PDN, GPIO[6:0], INSELx_[1:0])

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	Input high voltage	1.2			V
V _{IL}	Input low voltage			0.6	V
I _{IH}	Input high current	V _{IH} = VDD	–40	40	uA
I _{IL}	Input low current	V _{IL} = GND	–40	40	uA
t _{WIDTH}	Input pulse width	Monotonic edges	10		ns
C _{IN}	Input capacitance		2		pF

7.17 3-Level Logic Input Characteristics (HW_SW_CTRL, STATUS[1:0])

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IH}	Input high voltage	1.4			V
V _{IM}	Input mid voltage	Input floating with internal bias	0.9		V
V _{IL}	Input low voltage			0.4	V

3-Level Logic Input Characteristics (HW_SW_CTRL, STATUS[1:0]) (continued)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{IH}	Input high current V _{IH} = VDD	–40		40	uA
I _{IL}	Input low current V _{IL} = GND	–40		40	uA
C _{IN}	Input capacitance		2		pF

7.18 Logic Output Characteristics (STATUS[1:0], GPIO[6:5], GPIO2/SDO)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	Output high voltage I _{OH} = 3 mA, LVCMOS mode	TBD			V
V _{OL}	Output low voltage I _{OL} = 3 mA			0.6	V
t _R /t _F	Output rise/fall time 20% to 80%, LVCMOS mode, 1 kΩ to GND		500		ps

7.19 I²C Interface Characteristics (SDA, SCL)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
V _{IH}	Input high voltage	1.2			V
V _{IL}	Input low voltage			0.5	V
I _{IH}	Input leakage	–15		15	uA
C _{IN}	Input capacitance		1		pF
V _{OL}	Output low voltage I _{OL} = 3 mA			0.3	V
f _{SCL}	SCL clock rate Standard			100	kHz
f _{SCL}	SCL clock rate Fast mode			400	kHz
t _{SU_STA}	START condition setup time SCL high before SDA low	0.6			us
t _{H_STA}	START condition hold time SCL low after SDA low	0.6			us
t _{PH_STA}	SCL pulse width high	0.6			us
t _{PL_STA}	SCL pulse width low	1.3			us
t _{SU_SDA}	SDA hold time SDA valid after SCL low	0		0.9	us
t _{H_SDA}	SDA setup time	100			ns
t _{R_IN}	SCL/SDA input rise time			300	ns
t _{F_IN}	SCL/SDA input fall time			300	ns
t _{F_OUT}	SDA output fall time C _{BUS} ≤ 400 pF			300	ns
t _{SU_STOP}	STOP condition setup time	0.6			us
t _{BUS}	Bus free time between STOP and START	1.3			us
t _{VD-DAT}	Data valid time			0.9	us
t _{VD-ACK}	Data valid acknowledge time			0.9	us

7.20 SPI Timing Requirements (SDA, SCL, GPIO1/SCS, GPIO2/SDO)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	MIN	NOM	MAX	UNIT
f _{Clock}			20	MHz
t ₁	10			ns
t ₂	10			ns
t ₃	10			ns
t ₄	25			ns
t ₅	25			ns

SPI Timing Requirements (SDA, SCL, GPIO1/SCS, GPIO2/SDO) (continued)

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C

PARAMETER	MIN	NOM	MAX	UNIT
t ₆ SCL to SDO valid read-back data	10		TBD	ns
t ₇ SCS pulse width	20			ns
t ₈ SCS to CLK hold time	10			ns

7.21 Other Characteristics

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C, OUTx = 156.25 MHz, Differential output pair AC-coupled to 100-Ω differential load, HCSL output pair terminated with 50 Ω to GND, LVCMOS output terminated with 50 Ω to VDDO / 2.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t _{PHO,CMO} _S IN-to-OUT Phase Offset, LVCMOS outputs ⁽¹⁾	Zero delay enabled		TBD		ns
t _{PHO,DIFF} IN-to-OUT Phase Offset, DIFF outputs ⁽¹⁾	Zero delay enabled		TBD		ns
PSNR Spur level induced by power supply noise (V _N = 50 mVpp)	VDDO _x = 2.5 V or 3.3 V, AC-Diff or HCSL output		–70		dBc
	VDDO _x = 2.5 V, LVCMOS output		–55		dBc
PSNR Spur level induced by power supply noise (V _N = 25 mVpp)	VDDO _x = 1.8 V, AC-Diff or HCSL output		–70		dBc
	VDDO _x = 1.8 V, LVCMOS output		–45		dBc
SPUR Spur level due to isolation/cross coupling (adjacent outputs)	OUTx = 156.25 MHz, OUTy = 155.52 MHz, AC-Diff or HCSL (same output type for both channels)		–75		dBc

(1) Parameter is specified by characterization and is not tested in production.

7.22 PLL Clock Output Performance Characteristics

VDD = 3.3 V ± 5%, VDDO = 1.8 V ± 5%, 2.5 V ± 5%, 3.3 V ± 5%, T_A = –40°C to 85°C, OUTx = 156.25 MHz, Differential output pair AC-coupled to 100-Ω differential load, HCSL output pair terminated with 50 Ω to GND, LVCMOS output terminated with 50 Ω to VDDO / 2.

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
RJ RMS Phase Jitter ⁽¹⁾ (12 kHz – 20 MHz)	OUT = 156.25 MHz AC-Diff or HCSL, XO = 48.0048 MHz		150	225	fs RMS
PN-TDC Output Close-in Phase Noise (f _{OFFSET} = 100 Hz)	OUT = 122.88 MHz AC-Diff or HCSL, IN = 10 MHz, XO = 48.0048 MHz, LBW = 100 Hz		–102		dBc/Hz
LBW DPLL Loop Bandwidth Range ⁽¹⁾⁽²⁾	Programmed bandwidth setting		0.01 to 4000		Hz
JPK Jitter Peaking ⁽¹⁾	IN = 25 MHz, OUT = 25 MHz, DPLL BW = TBD Hz			0.1	dB
JTOL Jitter tolerance ⁽¹⁾	Jitter Modulation = 10 Hz, 10.3125 Gbps		2488		UI p-p
PHTR Maximum phase transient during Hitless Switch ⁽¹⁾	Valid for a single switchover event between two clock inputs at the same frequency		±100		ps
f _{ERROR} Maximum additive frequency error ⁽¹⁾	Valid for a single switchover event between two clock inputs at the same frequency		100		ppb
t _{START-XO} ⁽³⁾ Initial Clock Start-up Time	From rising edge of PDN to free-running output clocks from first PLL domain		20		ms
STD Standards Compliance			G.813 Opt. 1 G.8262 Opt. 1 and 2 G.709 GR-253-CORE GR-1244 CORE		

(1) Parameter is specified by characterization and is not tested in production.

(2) Actual loop bandwidth may be lower. Applies to REF-DPLL and TCXO-DPLL. The valid loop bandwidth range may be constrained by the DPLL loop mode and REF and/or TCXO input frequencies used in a given configuration.

(3) First PLL domain to start-up is selected by PLLSTRMODE bit. Assumes XO input clock is stable before rising edge of PDN, PLL/VCO wait timers set to 3 ms/0.4 ms, and output channels auto-muted during APLL lock only.

7.23 Timing Diagrams

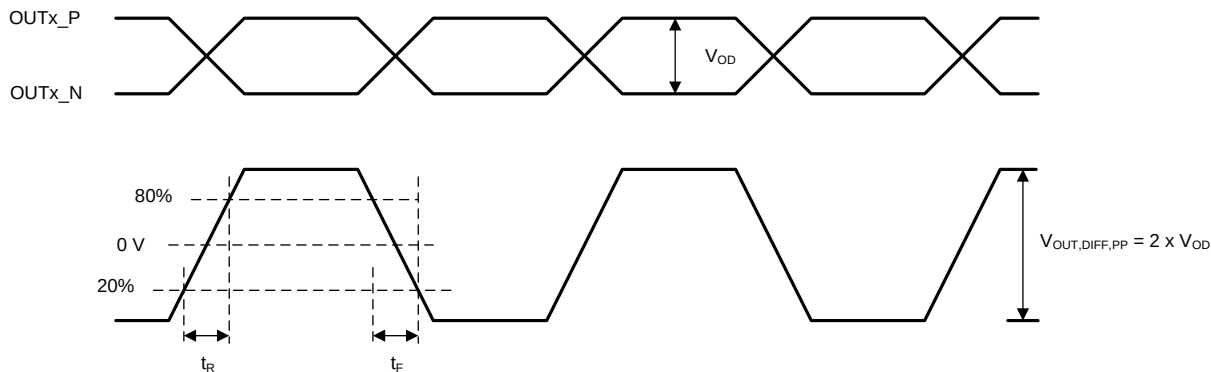


Figure 2. Differential Output Voltage and Rise/Fall Time

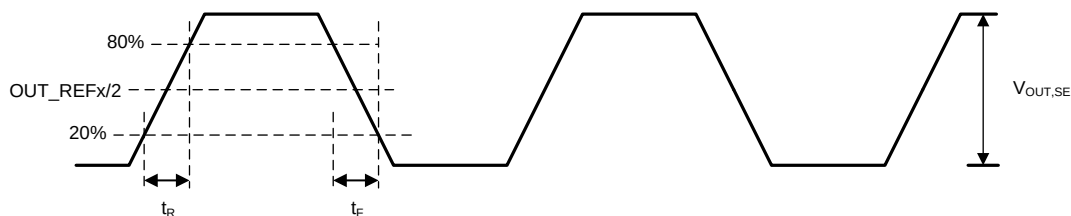
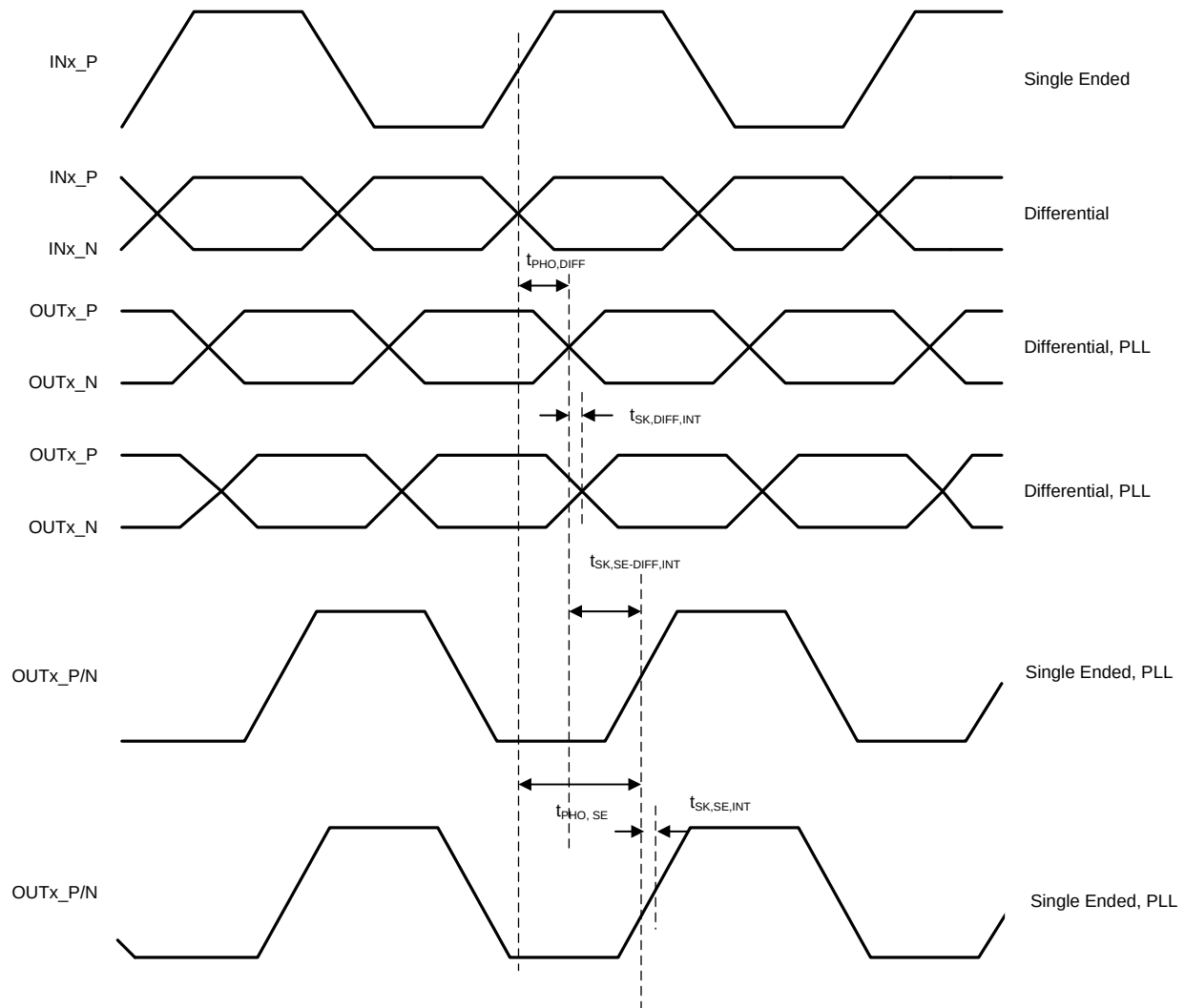


Figure 3. Single-Ended Output Voltage and Rise/Fall Time

Timing Diagrams (continued)

Figure 4. Differential and Single-Ended Output Skew and Phase Offset

8 Parameter Measurement Information

8.1 Test Configuration

This section describes the test configuration for several electrical characteristics.

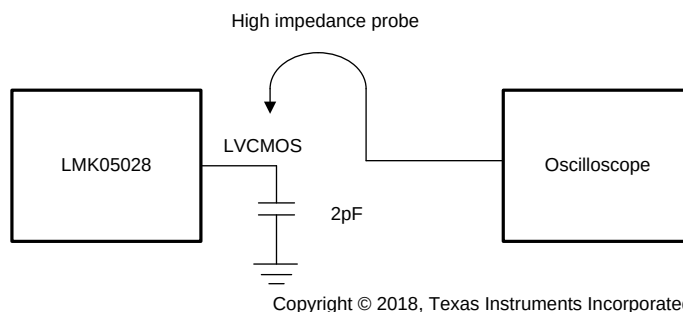


Figure 5. LVCMOS Output DC Configuration During Device Test

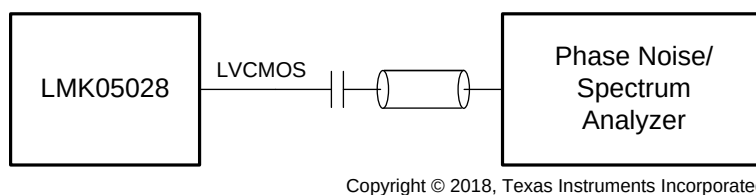


Figure 6. LVCMOS Output AC Configuration During Device Test

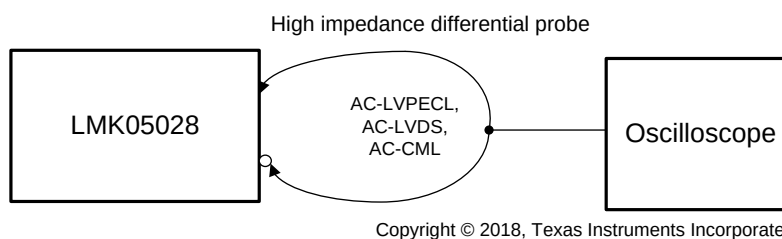


Figure 7. AC-LVPECL, AC-LVDS, AC-CML Output DC Configuration During Device Test

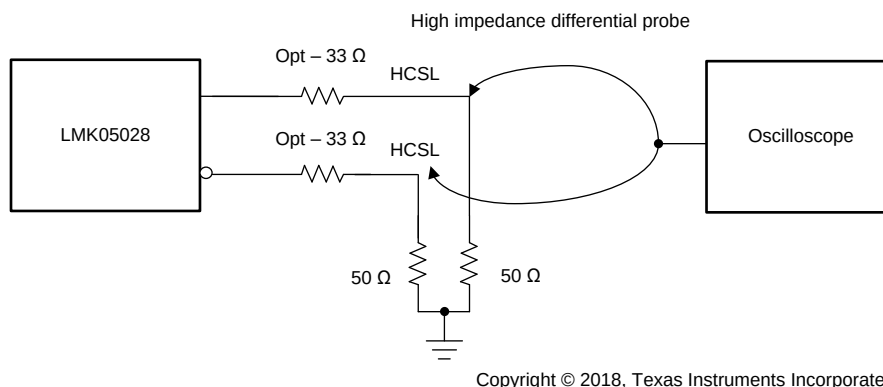
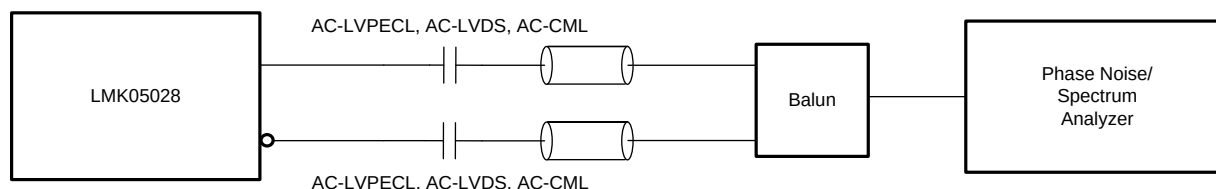


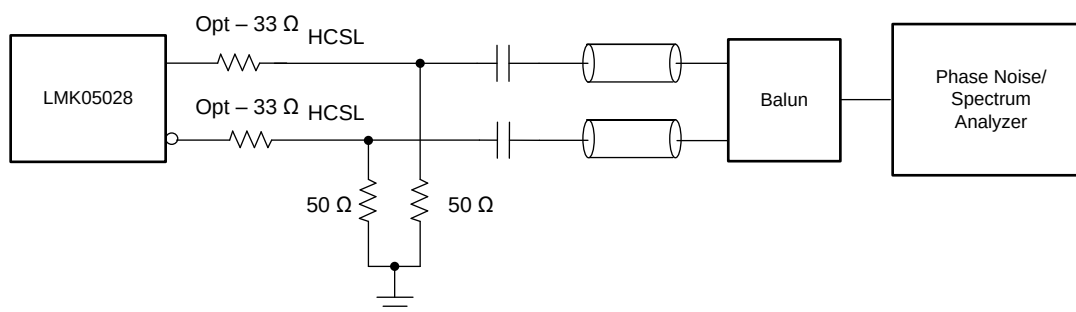
Figure 8. HCSL Output Driving 100- Ω Differential Trace Impedance DC Configuration During Device Test

Test Configuration (continued)



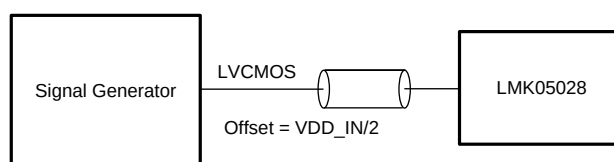
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Figure 9. AC-LVPECL, AC-LVDS, AC-CML Output AC Configuration During Device Test



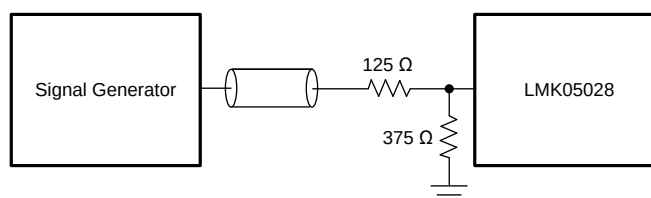
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Figure 10. HCSL Output Driving 100-Ω Differential Trance Impedance AC Configuration During Device Test



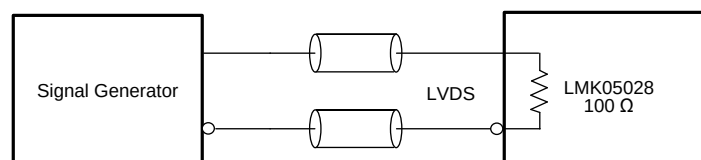
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Figure 11. LVCMOS Reference Input DC Configuration During Device Test



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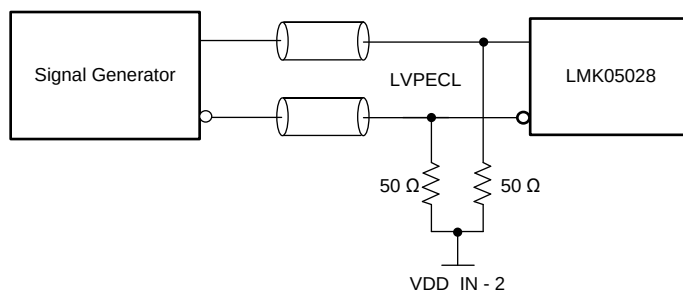
Figure 12. LVCMOS XO Input DC Configuration During Device Test



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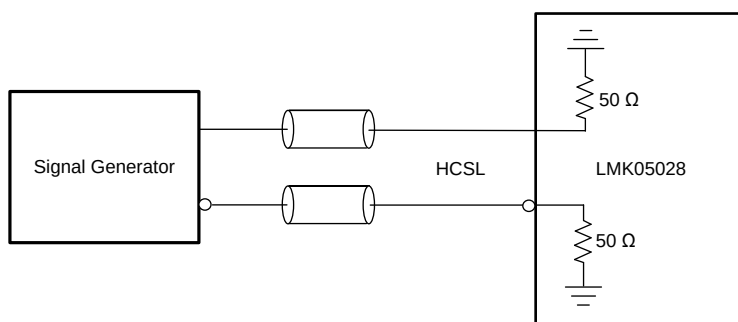
Figure 13. LVDS Input DC Configuration During Device Test

Test Configuration (continued)



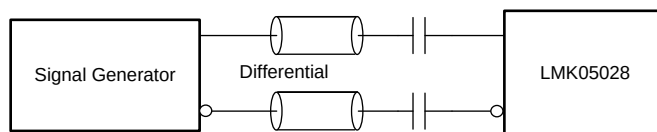
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Figure 14. LVPECL Input DC Configuration During Device Test



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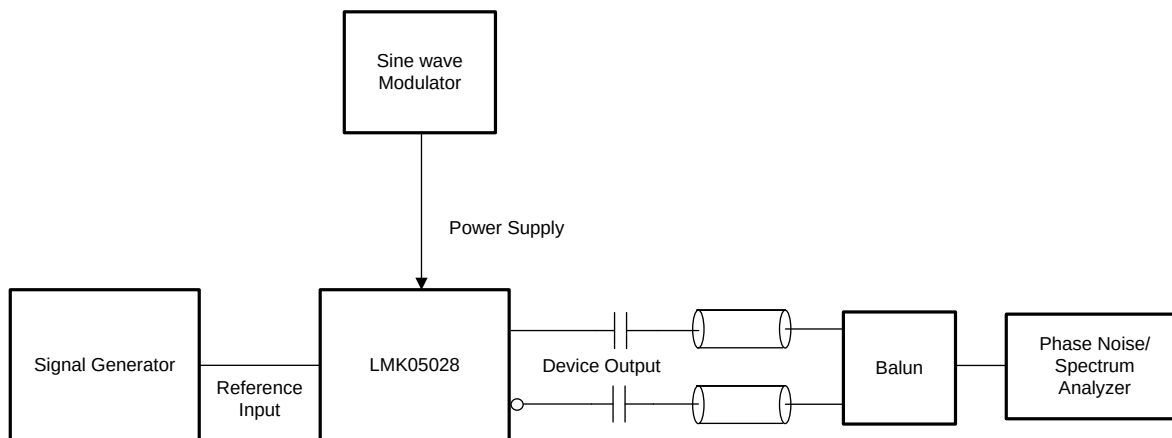
Figure 15. HCSL Input DC Configuration During Device Test



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100-Ω differential input termination with AC biasing enabled internally (not shown)

Figure 16. Differential Input AC Configuration During Device Test



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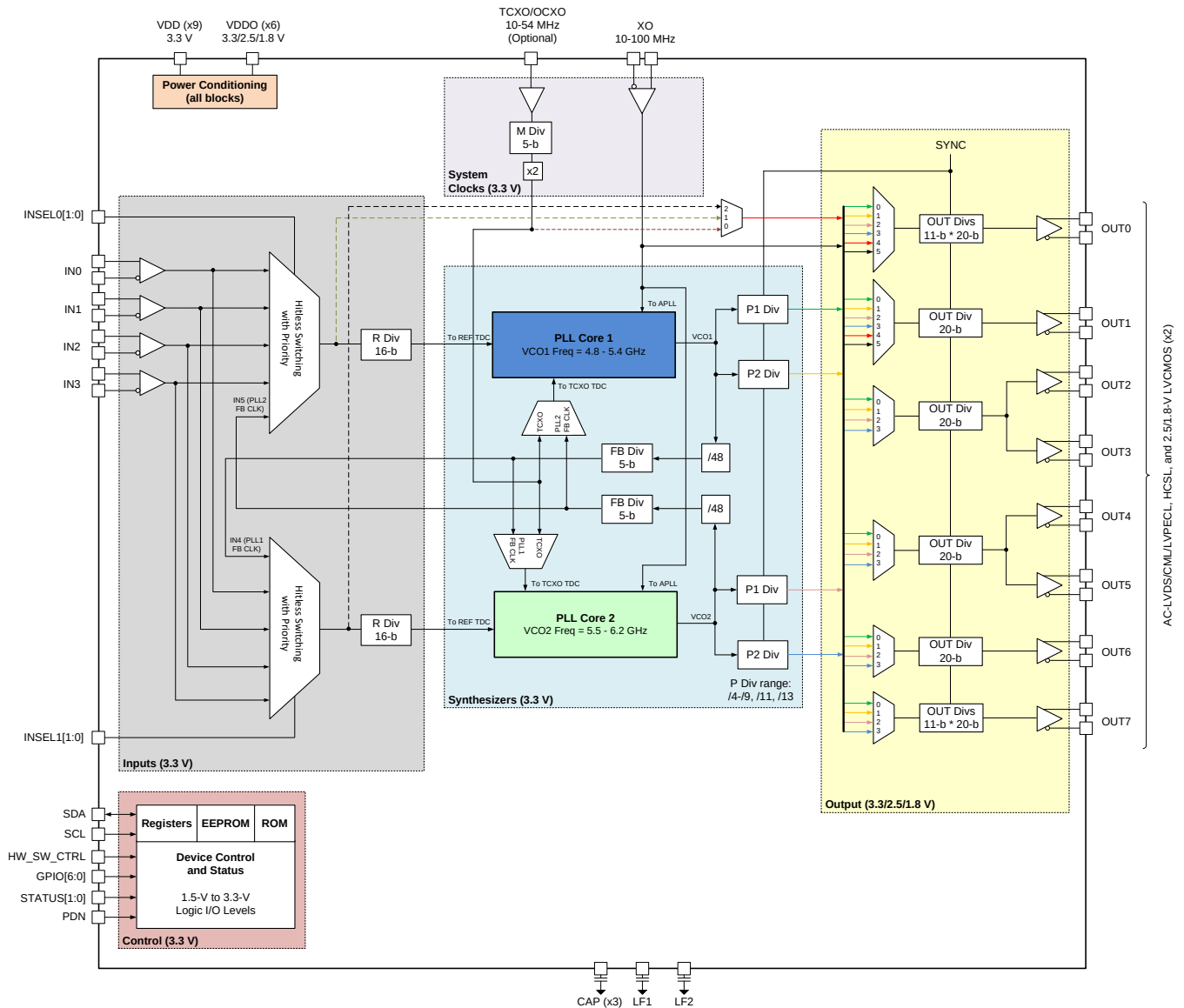
Figure 17. PSNR Test Setup

9 Detailed Description

9.1 Overview

The LMK05028 is a high-performance clock generator and jitter cleaner with advanced clock synchronization capabilities to meet the stringent timing requirements of communications infrastructure and other industrial applications. The device features four reference inputs, two independent PLL domains, and eight output clocks with RMS phase jitter of 150 fs typical. Each PLL core supports programmable loop bandwidth for jitter or wander attenuation, and fractional frequency translation for flexible frequency planning. The advanced synchronization options in each PLL core include superior hitless switching, digital holdover, DCO mode with <1 ppt/step for precise clock steering (IEEE 1588 PTP slave operation), and zero delay for deterministic input-to-output phase offset. The device can use a low-frequency TCXO/OCXO to determine the free-run or holdover frequency stability for standards-compliant operation, or a standard XO when long-term stability and wander are non-critical. The device is programmable through I2C or SPI registers and supports custom start-up clock configuration with internal EEPROM, which can be programmed in-system or factory pre-programmed.

9.2 Functional Block Diagrams



ADVANCE INFORMATION

Figure 18. LMK05028 Block Diagram

9.3 Feature Description

The following section describes the features of the device functional blocks.

9.3.1 Oscillator Input (XO_P/N)

The XO input is the reference clock for the Fractional-N APLLs. The combination of XO and APLL determine the jitter and phase noise performance of the output clocks. For optimal performance, the XO frequency should be between 48 to 54 MHz and have a non-integer frequency relationship with the VCO frequencies so the APLLs operate in Fractional mode.

The XO input buffer has programmable input on-chip termination and biasing controls to support any oscillator interface type.

Feature Description (continued)

9.3.2 TCXO Input (TCXO_IN)

The TCXO input is the reference clock to the TCXO-DPLL loop in each PLL core. When the PLL core uses the TCXO-DPLL in 3-loop mode (typically), the TCXO input determines the wander and close-in phase noise performance when the DPLL is locked, and the frequency accuracy and stability during holdover mode. A TCXO input with high phase noise floor should have minimal or no impact on the output jitter performance, provided the TCXO loop bandwidth is designed low enough to attenuate its noise contribution. When the TCXO input is not used, the XO determines the frequency accuracy and stability during free-run or holdover modes.

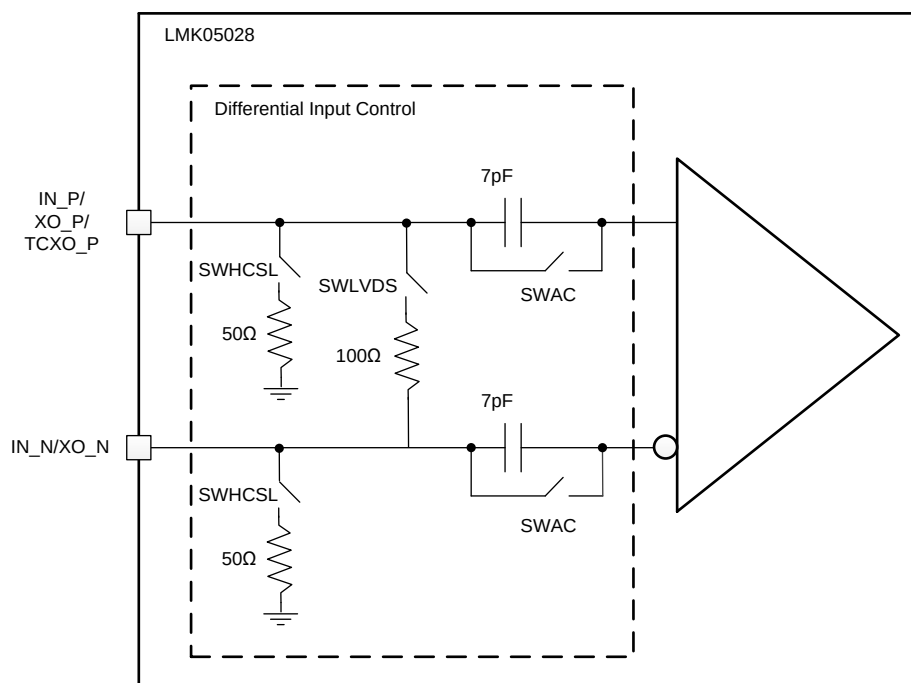
The TCXO input accepts an AC-coupled single-ended clock (sine, clipped-sine, or square wave) and has a internal weak bias of about 0.6 V. The input voltage swing should be less than 1.2 V_{pp} and attenuated or terminated before AC-coupling to the pin. This input can be driven from a low-frequency TCXO, OCXO, or external timing reference that conforms to the frequency accuracy and holdover stability requirements required by the application. TCXO and OCXO frequencies of 10 to 12.8 MHz are widely available and cost-effective options.

9.3.3 Reference Inputs (INx_P/N)

The reference inputs (IN0 to IN3) can accept differential or LVCMOS clocks to lock either or both DPLLs. Each DPLL has an input mux to select one of the four inputs. Each DPLL can support switching between two or more inputs with different frequencies provided each input can be divided down by DPLL reference dividers (DPLL_y_REF_x_RDIV) to a single common frequency.

Each input has programmable input type, on-chip termination, and biasing controls to support any clock interface type.

Figure 19 shows the input termination and biasing options implemented on the reference and XO inputs. The internal switch options are register configurable. Table 3 shows the typical input buffer configurations to interface with LVDS, CML, LVPECL HCSL, and LVCMOS drivers.



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Figure 19. Input Buffer Termination Options for Reference, XO, and TCXO Inputs

Feature Description (continued)

Table 3. Input Buffer Configurations for Reference and XO Inputs

MODE	INTERNAL COUPLING	TERMINATION
HCSL	AC	Internal (50 Ω)
LVDS (DC-coupled)	AC	Internal (100 Ω)
LVDS, CML, LVPECL (AC-coupled)	AC	Internal (100 Ω)
CML or LVPECL (DC-coupled)	AC	External
LVC MOS	DC	External

Figure 20 through Figure 24 show recommendations for interfacing LMK05028's clock inputs with LVC MOS, LVPECL, LVDS, CML, and HCSL drivers, respectively.

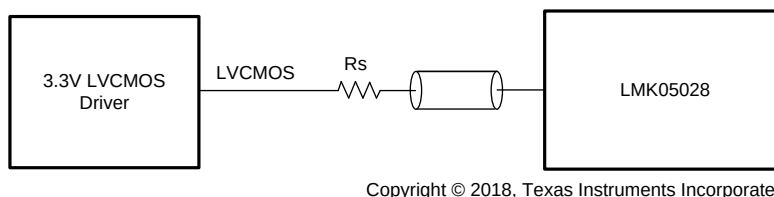


Figure 20. Interfacing LMK05028 Input With LVC MOS Driver (3.3 V, 2.5 V, 1.8 V)

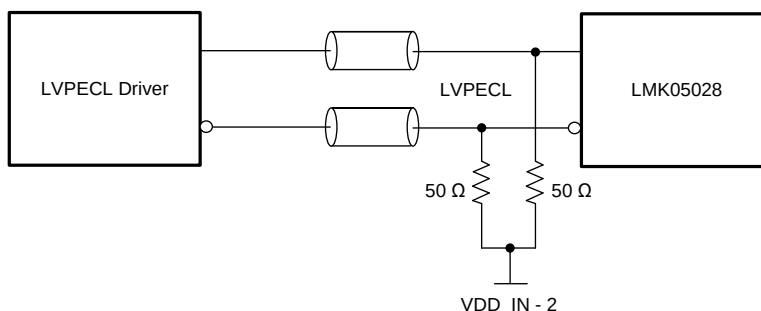


Figure 21. Interfacing LMK05028 Inputs With DC-Coupled LVPECL Driver

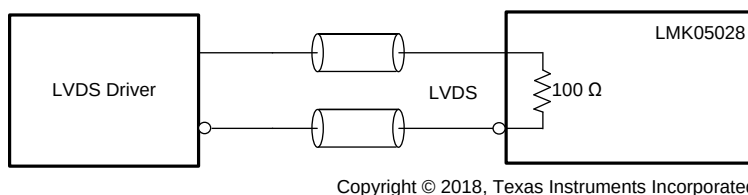


Figure 22. Interfacing LMK05028 Inputs With DC-Coupled LVDS Driver

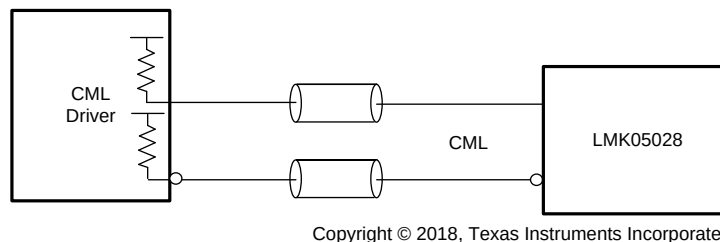
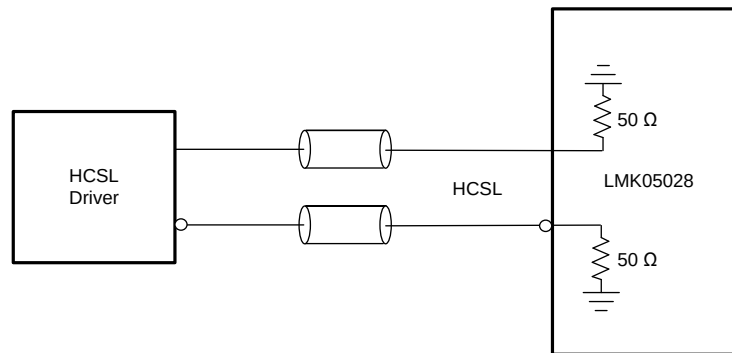


Figure 23. Interfacing LMK05028 Inputs With DC-Coupled CML Driver (Source Terminated)



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Figure 24. Interfacing LMK05028 Inputs With HCSL Driver (Load Terminated)

9.3.4 Reference Input Mux Selection

For each DPLL, the reference input mux selection can be done automatically using an internal state machine with a configurable input priority scheme manually through register control or hardware pin controls. The input mux can select from IN0 to IN3. Additionally, DPLL1 can select IN5 as an internal loopback clock divided from PLL2 VCO (VCO2), and DPLL2 can select IN4 as an internal loopback clock from PLL1 VCO (VCO2).

The priority for all inputs can be assigned for each DPLL through registers. The priority ranges from 0 to 6, where 0 means Ignored (never select) and 1 to 6 are highest (1st) to lowest (6th) priority. When two or more inputs are configured with the same priority setting, the reference input with lower index (INx) will be given higher priority.

The currently selected reference input for each DPLL can be read through a status pin or register.

9.3.4.1 Automatic Input Selection

There are two automatic input selection modes that can be set by a register: Auto Revertive and Auto Non-Revertive.

- *Auto Revertive:* In this mode, the DPLL automatically selects the valid input with the highest configured priority. If a clock with higher priority becomes valid, the DPLL will automatically switch over to that clock immediately.
- *Auto Non-Revertive:* In this mode, the DPLL automatically selects the highest priority input that is valid. If a higher priority input becomes valid, the DPLL will not switch-over until the currently selected input becomes invalid.

9.3.4.2 Manual Input Selection

There are two manual input selection modes that can be set by a register: Manual with Auto-Fallback and Manual with Auto-Holdover. In either manual mode, the input selection can be done through register control (Table 4) or hardware pin control (Table 5).

- *Manual with Auto-Fallback:* In this mode, the manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically fallback to the highest priority input that is valid or qualified. If no prioritized inputs are valid, the DPLL will enter holdover mode (if tuning word history is valid) or free-run mode. The DPLL will exit holdover mode when the selected input becomes valid.
- *Manual with Auto-Holdover:* In this mode, the manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically enter holdover mode (if tuning word history is valid) or free-run mode. The DPLL will exit holdover mode when the selected input becomes valid.

Table 4. Manual Input Selection by Register Bits

DPLLx_REF_MAN_REG_SEL[2:0] BITS	DPLLx_REF_MAN_SEL BIT	SELECTED INPUT
00b	0	IN0

Table 4. Manual Input Selection by Register Bits (continued)

DPLLx_REF_MAN_REG_SEL[2:0] BITS	DPLLx_REF_MAN_SEL BIT	SELECTED INPUT
01b	0	IN1
10b	0	IN2
11b	0	IN3

Table 5. Manual Input Selection by Hardware Pins

INSELx [1:0] PINS	DPLLx_REF_MAN_SEL BIT	SELECTED INPUT
00b	1	IN0
01b	1	IN1
10b	1	IN2
11b	1	IN3

9.3.5 Hitless Switching

Each DPLL supports hitless switching through phase cancellation which restricts the rate of change of output phase during a reference switchover event in accordance with Stratum 3/4E, Stratum 2/3E, and Synchronous Ethernet EEC Option 1.

During hitless switching, the phase cancellation filter averages the input to find a common position and is necessary to reduce the noise of input to obtain the true center. The switching scheme involves an inbuilt interpolation algorithm that allows interpolation below 1-ps step size on the output phase perturbation. This implementation allows minimal phase hit on the outputs when all inputs are synchronous to the same source. In the case of the inputs derived in an asynchronous manner, the output phase smoothly tracks the new frequency and phase with reduced transient. The hitless switching specification is valid for reference inputs that are wander-free.

The hitless switching flowchart is shown in [Figure 25](#).

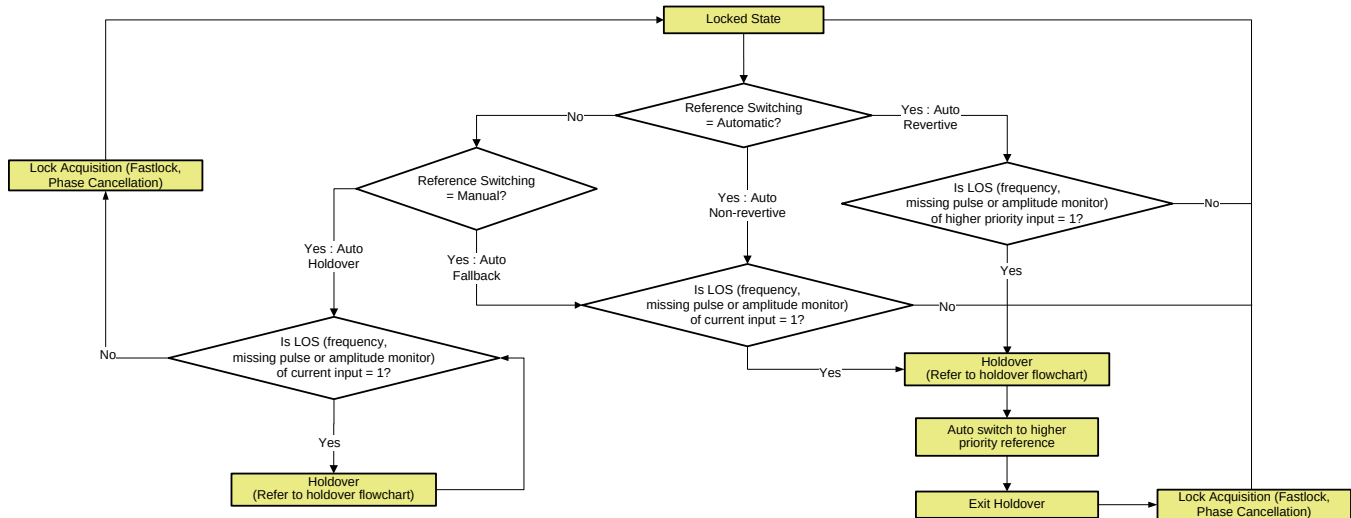


Figure 25. Hitless Switching Flowchart

9.3.6 Gapped Clock Support on Reference Inputs (INx_P/N)

Each DPLL supports locking to an input clock that has missing periods and is referred to as a gapped clock. Gapping a clock severely increases its jitter, so the device provides the high input jitter tolerance and low loop bandwidth necessary to generate a low-jitter periodic output clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every 8. The fault monitors can be configured to avoid triggering on any flags and achieve phase lock. Reference switchover between gapped clocks may violate the hitless switching specification if the switch occurs during a gap in either input clock.

9.3.7 Clock Monitoring, Status, and Interrupts

The following section describes the clock monitoring, status, and interrupt features.

9.3.7.1 Reference Monitoring

All reference clock inputs are monitored for input qualification or validation for DPLL input selection. An input can be selected if it is qualified or if it falls within the valid threshold for all enabled input monitoring blocks. The input monitoring blocks include amplitude, a missing pulse, a runt pulse, or both, and frequency monitors. Additionally, a validation timer sets the minimum time for all enabled input monitors to be clear of flags before an input is qualified.

The enablement and valid threshold for all input monitors and validation timers are configurable per input through the registers. The monitors and validation timers are optional to enable, but can be very useful to avoid selection of an unreliable clock input. If a given monitor is not enabled, it will not trigger a flag and will be ignored. The status flag of an enabled input monitor can be observed through status pin for any input (selected or non-selected), or through the corresponding interrupt register bit for the selected input of each DPLL. The valid status of all inputs can also be read through a status register.

9.3.7.1.1 Amplitude Monitor

The amplitude monitor detects if the input meets or violates the amplitude-related thresholds for differential or LVCMOS input modes. The differential input detector clears its flag when the input voltage swing is above the minimum setting selected by the registers (200, 300, or 400 mVpp nominal). The LVCMOS input slew rate detector clears its flag when its slew rate is faster than the fixed threshold on the clock edge selected by the registers (rising edge only, falling edge only, or both edges). If either the differential or LVCMOS clock does not meet the specified thresholds, the detector will set its flag to disqualify the input.

Below about 1 MHz, the differential input detector may signal a false flag; in that case, the input detector should be disabled or bypassed. The LVCMOS input detector can be used for low-frequency clocks down to 1 Hz or 1 PPS.

9.3.7.1.2 Missing Pulse Monitor

The missing pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period plus a programmable late window threshold (T_{LATE}). When an input pulse arrives before T_{LATE} , the pulse is considered valid and the missing pulse flag will be cleared. When an input pulse does not arrive before T_{LATE} (due to missing or late pulse), the flag will be set immediately to disqualify the input.

T_{LATE} should be typically set higher than the input's longest clock period (including periodic jitter), or higher than the gap width for a gapped clock. The missing pulse monitor can act as a coarse frequency detector with faster fault detection than the precision frequency monitor. The missing pulse monitor is supported for input frequencies between 2 kHz and TBD MHz and should be disabled for any input outside this range.

9.3.7.1.3 Runt Pulse Monitor

The runt pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period minus a programmable early window threshold (T_{EARLY}). When an input pulse arrives after T_{EARLY} , the pulse is considered valid and the runt pulse flag will be cleared. When an early or runt input pulse arrives before T_{EARLY} , the monitor will set the flag immediately to disqualify the input.

T_{EARLY} should be typically set higher than the input's shortest clock period (including periodic jitter). The early pulse monitor can act as a coarse frequency detector with faster fault detection than the precision frequency monitor. The early pulse monitor is supported for input frequencies between 2 kHz and TBD MHz and should be disabled for any input outside this range.

The missing pulse and runt pulse monitors operate from the same window detector block, and the status flags for both monitors are logically OR-ed together. The OR-ed output flag can be observed through status pin for any input, or through the MISSCLK interrupt register bit for the selected input of each DPLL.

9.3.7.1.4 Frequency Monitoring

The frequency monitor measures the frequency ppm offset for all input clocks relative to a "0-ppm" reference clock, which can be selected from either the XO or TCXO input. The valid and invalid ppm frequency thresholds are configurable through the registers. The monitor will clear the LOR_FREQ flag when the relative input frequency error is less than the valid ppm threshold. Otherwise, it will set its flag when the relative input frequency error is greater than the invalid ppm threshold. The ppm delta between the valid and invalid thresholds provides hysteresis to prevent the LOR_FREQ flag from toggling when the input frequency offset is crossing these thresholds or has high wander. A measurement averaging factor is also used in computing the frequency threshold register settings. A higher averaging factor increases the delay to set or clear the LOR_FREQ flag to allow more time for the input frequency to settle and can provide better frequency measurement resolution for an input with high wander. Higher averaging also reduces the maximum frequency detector thresholds that can be configured.

9.3.7.1.5 Reference Validation Timer

Each reference input has a dedicated validation timer. The validation timer sets the amount of time that a reference must be clear of flags from all enabled input monitors before it is qualified and valid for selection. The validation timer count and enable settings are register-configurable.

9.3.7.2 XO Input Monitoring

The XO input has an amplitude and frequency monitor for input qualification before it can be used to lock the APLLs. The XO input amplitude monitor can be configured and operates the same as the reference input amplitude detector. The XO loss-of-signal (LOS) status flags can be observed through status pin or interrupt register bits. The XO detectors can be bypassed or ignored through register bits, so the input is always considered to be valid by the PLL control state machines.

9.3.7.3 TCXO Input Monitoring

The TCXO input has an amplitude and frequency monitor for input qualification before it can be used to lock the TCXO-DPLLs. The TCXO input amplitude monitor can be configured and operates the same as the reference input's LVCMOS input slew rate detector. The TCXO loss-of-signal (LOS) status flags can be observed through status pin or interrupt register bits. The TCXO detectors can be bypassed or ignored through register bits, so the input is always considered to be valid by the PLL control state machines.

9.3.7.4 Loss of Lock (LOL)

The loss-of-lock (LOL) status is available for each APLL and DPLL. The APLLs are monitored for loss-of-frequency lock only, and the REF-DPLLs are monitored for both loss-of-phase lock (LOPL) and loss-of-frequency lock (LOFL). The DPLL lock and loss-of-lock thresholds for both LOPF and LOFL detectors are configurable through the registers.

Each DPLL LOFL monitor will clear its flag when the DPLL frequency error relative the selected reference input is less than the lock ppm threshold. Otherwise, it will set its flag when the DPLL frequency error is greater than the unlock ppm threshold. The ppm delta between the lock and unlock thresholds provides hysteresis to prevent the LOFL flag from toggling when the DPLL frequency error is crossing these thresholds. A measurement averaging factor is also used in computing the lock and unlock threshold register settings. A higher averaging factor increases the delay to set or clear the LOFL flag to allow more time for the DPLL frequency to acquire lock. Higher averaging may be useful when locking to an input with high wander or when the DPLL is configured with a narrow loop bandwidth. Note that higher averaging reduces the maximum frequency thresholds that can be measured.

The LOL flags can be observed through status pins for all APLLs and DPLLs, as well as through the corresponding interrupt register bits.

9.3.7.5 Tuning Word History

Each REF-DPLL domain has a tuning word history monitor block that determines the initial output frequency accuracy upon entry into holdover. The tuning word can be updated from one of three sources depending on the DPLL operating mode:

- a. Locked Mode: From the output of the digital loop filter when locked
- b. Holdover Mode: From the final output of the history monitor
- c. Free Run Mode: From the free-run tuning word register (user defined)

When the history monitor is enabled and the DPLL is locked, it effectively averages the reference input frequency by accumulating history from the digital loop filter output during a programmable averaging time (Tavg). Once the input becomes invalid, the final tuning word value is stored to determine the initial holdover frequency accuracy. Generally, a longer the Tavg time will produce a more accurate initial holdover frequency. The stability of 0-ppm reference clock (XO or TCXO input) determines the long-term stability and accuracy of the holdover output frequency.

There is also a separate programmable delay timer (Tign) that can be set to ignore the history data that is corrupted just prior to entry into holdover. The history data could be corrupted if a tuning word update occurs while the input clock is failing and before it is detected by the input monitors. Both Tavg and Tign times are programmable through HISTCNT and HISTDLY bits, respectively, and are related to the REF-TDC rate.

The tuning word history is initial cleared after a device hard reset or soft reset. The history monitor begins to accumulate history once the DPLL locks to a new reference. The previous history will be cleared when a switchover to a new reference occurs assuming the history persistence bit (HIST_HOLD) is not set. The history can be manually cleared by asserting the history soft reset bit (HIST_SW_RST). If the history persistence bit is set, the history monitor will not clear the previous history value during reference switchover, holdover exit, or history soft reset. Whenever the tuning word is cleared, the history monitor waits for the first Tavg timer to expire before storing the first tuning word value.

If the Tavg period is set very long (minutes or hours) to a more precise historical average frequency, it is possible for a switchover or holdover event to occur before the first tuning word is stored and available for use. To overcome this, there is an intermediate history update option (HIST_INTMD). If the history is reset, then the intermediate average can be updated at intervals of $Tavg/2^K$, where $K = HIST_INTMD$ to 0, *during the first Tavg period only*. If $HIST_INTMD = 0$, there is no intermediate updates and the first average is stored after the first Tavg period. However, if $HIST_INTMD = 4$, then four intermediate averages are taken at $Tavg/16$, $Tavg/8$, $Tavg/4$, and $Tavg/2$, as well as at Tavg. After the first Tavg period, all subsequent history updates occur at the Tavg period.

When the history monitor is disabled, the user-programmable, free-run tuning word value (TUNING_FREE_RUN) determines the initial holdover output frequency accuracy.

9.3.7.6 Status Outputs

STATUS[1:0] and GPIO[6:5] pins can be used to output various internal status signals or interrupt flag for device diagnostic or debug purposes. The status signal, output driver type, and output polarity settings are configurable by registers.

The following lists the available status outputs (active high):

- XO Input Loss of Signal (LOS)
- TCXO Input Loss of Signal (LOS)
- PLLy Lock Detected (LOLb)
- PLLy VCO Calibration Active
- PLLy N Divider, div-by-2
- EEPROM Active
- Interrupt (INTR)
- PLLy VCO div-by-96
- REFx monitor divider output, div-by-2

- REFx amplitude monitor fault
- REFx frequency monitor fault
- REFx missing clock monitor fault
- REFx ppm timer active
- REFx validation timer active
- REFx phase validation monitor fault
- DPLL R Divider, div-by-2
- DPLL REF N Divider, div-by-2
- DPLL TCXO M Divider, div-by-2
- DPLL TCXO N Divider, div-by-2
- DPLL REF HS Clock, div-by-2
- DPLL TCXO HS Clock, div-by-2
- DPLL REFx selected
- DPLL Holdover active
- DPLL Reference switchover event
- DPLL R Divider Reset
- DPLL Tuning history update
- DPLL Fast lock active
- DPLL Fast lock done
- DPLL Loss of Lock
- DPLL Phase Cancellation done
- DPLL Loop filter saturation
- DPLL lock ppm timer active
- DPLL REF N Divider Reset

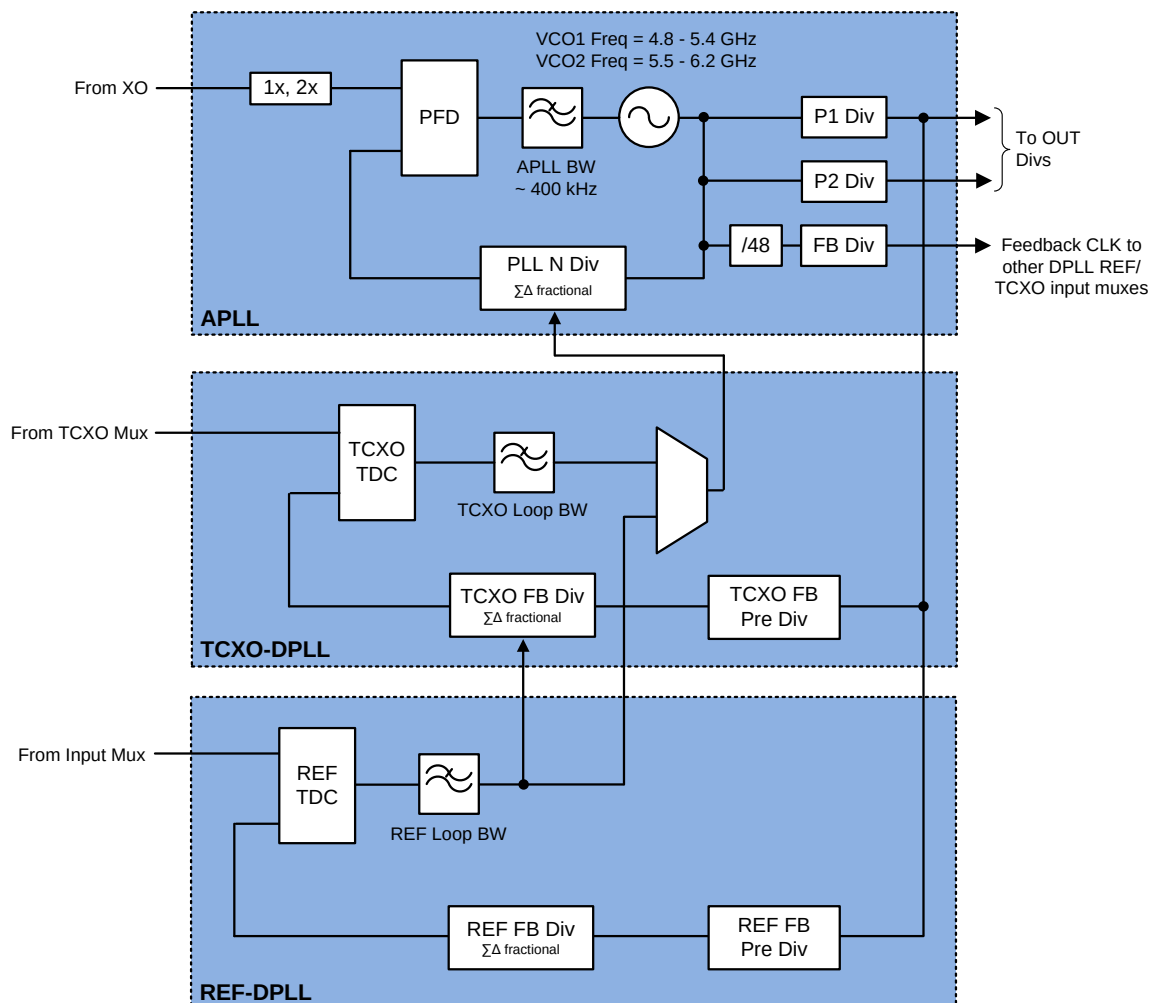
9.3.7.7 Interrupt

Any of the 4 status pins can be configured as a device interrupt output pin. The interrupt configuration is set through registers. When the interrupt is enabled, the interrupt flag can be triggered from any combination of interrupt status indicators, including LOS for the XO, TCXO, and DPLL-selected inputs, LOL for each DPLL and APLL, and holdover and switchover events for each DPLL. Any status indicator can be masked so it will not trigger the interrupt pin. Any unmasked status indicator can have its polarity inverted before it is combined at the interrupt OR/AND gate and output to the status pin.

9.3.8 PLL Core

9.3.8.1 PLL Core Block Diagram

Figure 26 shows a functional block diagram of a single PLL core. The LMK05028 has two independent PLL cores implemented identically, except for the VCO frequency ranges (shown below). The VCO frequency ranges do not overlap to help minimize cross-coupling between the two PLL domains.


Figure 26. PLL Core Block Diagram

9.3.8.2 PLL Frequency Relationships

The following equations provide the frequency relationships for closed-loop operation according to the loop mode configured on each PLL core.

- To operate in free-run mode (APLL only), the condition in [Equation 1](#) must be met.
- To operate in 3-loop mode (REF-DPLL, TCXO-DPLL, and APLL), the conditions in [Equation 1](#), [Equation 2](#), [Equation 3](#), and [Equation 4](#) must be met.
- To operate in 2-loop mode (REF-DPLL and APLL), the conditions in [Equation 1](#), [Equation 3](#), and [Equation 4](#) must be met.
- To operate in 2-loop mode (TCXO-DPLL and APLL), the conditions in [Equation 1](#) and [Equation 2](#) must be met.

[Equation 1](#) relates to the APLL.

$$F_{VCO} = F_{XO} \times D_{XO} \times (INT_{APLL} + NUM_{APLL} / DEN_{APLL})$$

where

- F_{VCO} : APLL/VCO frequency
- F_{XO} : Crystal Oscillator (XO) input frequency
- D_{XO} : APLL input doubler, 1 = disabled and 2 = enabled
- INT_{APLL} : APLL feedback N divider integer value (9 bits, 1 to 2^9-1)
- NUM_{APLL} : APLL feedback N divider numerator value (40 bits, 0 to $2^{40}-1$)

- DEN_{APLL} : APLL feedback N divider denominator value (40 bits, 1 to 2^{40}) (1)

Equation 2 relates to the TCXO-DPLL.

$$F_{VCO} = (F_{TCXO} \times D_{TCXO} / MDIV) \times P1 \times PR_{TCXO-DPLL} \times (INT_{TCXO-DPLL} + NUM_{TCXO-DPLL} / DEN_{TCXO-DPLL})$$

where

- F_{VCO} : APLL/VCO frequency
- F_{TCXO} : TCXO/OCXO input frequency
- D_{TCXO} : TCXO input doubler, 1 = disabled and 2 = enabled
- M : TCXO input divider (5 bits, 1 to 32)
- $P1$ = PLL primary post-divider (4 to 9, 11, 13)
- $PR_{TCXO-DPLL}$: TCXO-DPLL feedback prescaler divider (2 to 17)
- $INT_{TCXO-DPLL}$: TCXO-DPLL feedback divider integer value (30 bits, 1 to $2^{30}-1$)
- $NUM_{TCXO-DPLL}$: TCXO-DPLL feedback divider numerator value (40 bits, 0 to $2^{40}-1$)
- $DEN_{TCXO-DPLL}$: TCXO-DPLL feedback divider denominator value (fixed, 2^{40}) (2)

Equation 3 relates to the REF-DPLL.

$$F_{VCO} = (F_{INx} / Rx) \times P1 \times PR_{REF-DPLL} \times (INT_{REF-DPLL} + NUM_{REF-DPLL} / DEN_{REF-DPLL})$$

where

- F_{VCO} : APLL/VCO frequency
- F_{INx} : Reference input (0 to 3) or VCO loopback frequency (IN4 = VCO2, IN5 for VCO1)
- Rx : Reference input divider (16 bits, 1 to $2^{16}-1$) ($x = 0$ to 5)
- $PR_{REF-DPLL}$: REF-DPLL feedback prescaler divider (2 to 17)
- $INT_{REF-DPLL}$: REF-DPLL feedback divider integer value (30 bits, 1 to $2^{30}-1$)
- $NUM_{REF-DPLL}$: TCXO-DPLL feedback divider numerator value (40 bits, 0 to 0 to $2^{40}-1$)
- $DEN_{REF-DPLL}$: REF-DPLL feedback divider denominator value (40 bits, 1 to 2^{40}) (3)

Equation 4 relates to any reference inputs assigned to a DPLL to ensure a constant REF-TDC rate for proper input switchover.

$$F_{REF-TDC} = F_{IN0}/R0 = F_{IN1}/R1 = F_{IN2}/R2 = F_{IN3}/R3 \quad (4)$$

Equation 5, Equation 6, and Equation 7 relate to the output frequency according to the source selected by the output channel mux (CH_x_MUX).

$$F_{OUTx} = F_{XO} \text{ or } F_{REF} \text{ when XO or Ref Bypass is selected (OUT0 or OUT1 only)} \quad (5)$$

$$F_{OUTx} = F_{VCO} / (Pn \times DIVA_{OUTx}) \text{ when PLL post-divider is selected} \quad (6)$$

$$F_{OUTx} = F_{VCO} / (Pn \times DIVA_{OUTx} \times DIVB_{OUTx}) \text{ when PLL post-divider is selected (OUT0 or OUT7 only)}$$

where

- F_{REF} : TCXO, DPLL1 Ref, or DPLL2 Ref input frequency selected by REF_BYPASS_MUX
- Pn : P1 or P2 post divider value for PLL1 or PLL2
- $DIVA_{OUTx}$: Output divider value (20 bits, 1 to $2^{20}-1$)
- $DIVB_{OUTx}$: Output divider MSB value (11 bits, 1 to $2^{11}-1$) (7)

9.3.8.3 APLL XO Doubler

Each APLL has a frequency doubler on the XO input that can be enabled (default) to double the APLL PFD rate for improved phase noise and jitter performance within the APLL loop bandwidth.

9.3.8.4 APLL Phase Frequency Detector (PFD)

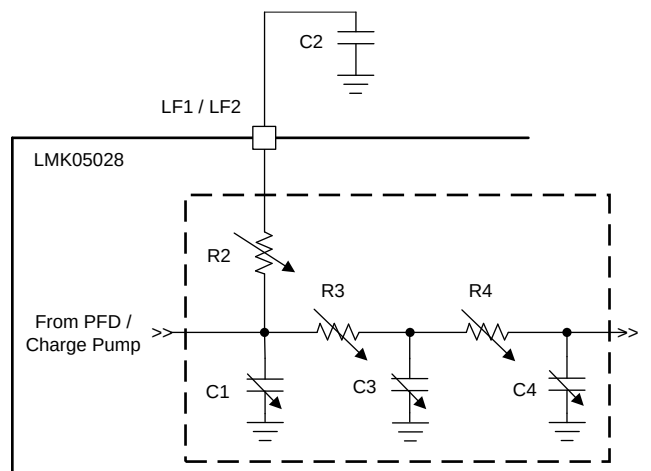
The PFD frequency of each APLL can operate from 10 MHz to 200 MHz, but the APLL performance is optimized for PFD frequencies at 96 MHz or higher.

9.3.8.5 APLL Charge Pump

Each PLL has programmable charge pump settings of 1.6 mA, 3.2 mA, 4.8 mA, or 6.4 mA.

9.3.8.6 APLL Loop Filter

Each APLL supports programmable loop bandwidth from 100 kHz to 1 MHz. The analog loop filter components, R2, C1, R3, C3, R4, and C4 can be configured through registers. C2 for each APLL is an external 0.1-μF capacitor on the LF1 or LF2 pins. Because each APLL operates in fractional mode during normal operation, the charge pump non-linearity should be reduced by configuring the bleed resistor. Figure 27 shows the APLL loop filter structure between the PFD/charge pump output and VCO input.



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Figure 27. Loop Filter Structure of Each APLL

9.3.8.7 APLL Fractional Feedback Divider (NDIV)

The fractional feedback divider (NDIV) of each APLL includes a 9-b integer portion (INT), 40-b numerator portion (NUM), and 40-b denominator portion (DEN). The total NDIV value is: $NDIV = INT + NUM / DEN$. The NDIV output sets the APLL PFD frequency, which should be equal to the XO doubler output frequency.

9.3.8.8 REF-DPLL Reference Divider (RDIV)

The reference clock input paths to each REF-DPLL features a 16-b reference divider (RDIV) for each clock input (IN0 to IN3). The output of each RDIV sets the frequencies to the reference input mux and the TDC rate of the REF-DPLL. There are also two additional RDIV for the internal VCO loopback clocks (IN4 and IN5) which could be used in cascaded DPLL configurations. IN4 refers to the VCO1 loopback clock to DPLL2 reference input, and IN5 refers to the VCO2 loopback clock to DPLL1 reference input.

9.3.8.9 TCXO Input Doubler (D) and Divider (MDIV)

The TCXO input features a frequency doubler followed by a 5-b divider (MDIV). The MDIV output is sent to both TCXO-DPLLs and sets the TDC rate for both TCXO-DPLLs if used in the configuration.

9.3.8.10 REF-DPLL and TCXO-DPLL Time-to-Digital Converter (TDC)

Each REF-DPLL and TCXO-DPLL TDC operates up to 30 MHz. The TDC resolution is fine enough to achieve in-band phase noise of -102 dBc/Hz at 100-Hz offset for a 122.88-MHz output. The REF-DPLL TDC rate is: $REF-TDC = F_{INX} / RDIVx$. The TCXO-DPLL TDC rate is: $TCXO-TDC = F_{TCXO} \times D / MDIV$, where $D = 1$ (doubler disabled) or 2 (enabled).

9.3.8.11 REF-DPLL and TCXO-DPLL Loop Filter

Each REF-DPLL and TCXO-DPLL supports programmable loop bandwidth from 10 mHz to 4 kHz and can achieve jitter peaking below 0.1 dB. The jitter transfer characteristic of each DPLL attenuates the noise of its respective input clock at -60 dB/decade slope above its configured loop bandwidth.

In 2-loop mode with the REF-DPLL, the TCXO-DPLL is bypassed and the REF-DPLL loop filter output directly modulates the APLL NDIV MASH engine to steer the APLL VCO into lock with the selected REF-DPLL input.

In 2-loop mode with the TCXO-DPLL, the REF-DPLL is not used and the TCXO-DPLL loop filter output directly modulates the APLL NDIV MASH engine to steer the APLL VCO into lock with the TCXO input.

In 3-loop mode, the REF-DPLL loop filter output modulates the TCXO-DPLL FB_DIV MASH engine, and the TCXO-DPLL loop filter output correspondingly modulates the APLL NDIV MASH engine to steer the APLL VCO into lock with the selected REF-DPLL input.

9.3.8.12 REF-DPLL and TCXO-DPLL Feedback Dividers (FB_PRE_DIV, FB_DIV)

The feedback path of each REF-DPLL and TCXO-DPLL has an feedback prescaler (FB_PRE_DIV) followed by a fractional feedback divider (FB_DIV). The FB_PRE_DIV divides its PLL primary post divider (P1) by a programmable value from 2 to 17 and outputs the prescaler clock to the FB_DIV. The FB_DIV of each REF-DPLL and TCXO-DPLL includes a 30-b integer portion (INT), 40-b numerator portion (NUM), and 40-b denominator portion (DEN). The total FB_DIV value is: $FB_DIV = INT + NUM / DEN$. The FB_DIV output sets the TDC rate to the respective DPLL.

9.3.8.13 PLL VCO Post Dividers (P1, P2)

Each PLL has a primary (P1) and secondary (P2) VCO post divider for more flexible clock frequency generation. Each post divider supports divide by 4 to 9, 11, or 13 from the VCO frequency. Each post divider frequency for PLL1 and PLL2 is distributed to the output block where it can be selected by any output channel mux. The P1 post divider output for each PLL is also fed-back to their respective REF-DPLL and TCXO-DPLL feedback divider paths to close the loops.

Once the P1 divider and DPLL fractional feedback dividers have been configured for closed-loop operation, the P1 divider should not be changed dynamically without also changing the DPLL feedback dividers to maintain the original TDC rates. A software PLL reset is required after changing any PLL post divider value.

9.3.8.14 VCO Calibration

Each PLL's VCO must be calibrated to ensure that the clock outputs deliver optimal phase noise performance. Fundamentally, a VCO calibration establishes an optimal operating point within the tuning range of the VCO. While transparent to the user, the LMK05028 performs the following steps during a VCO calibration sequence:

1. **Normal Operation** – When the LMK05028 is in normal (operational) mode, the state of both the power-down pin (PDN) is high.
2. **Entering the reset state** - If the user wishes to restore all device defaults and initiate a VCO calibration sequence, then the host system must place the device in reset through the PDN pin, or through programming, or by removing and restoring device power. Pulling the PDN pin low or through programming places the device in the reset state.
3. **Exiting the reset state** – The device calibrates the VCO either by exiting the device reset state or through the device reset command initiated through the host interface. Exiting the reset state occurs automatically after power is applied, the system restores the state of the PDN, or both, or through programming from the low to high state. Exiting the reset state using this method causes the device defaults to be loaded or reloaded into the device register bank. Invoking a device reset through the register bit does not restore device defaults; rather, the device retains settings related to the current clock frequency plan. Using this method allows for a VCO calibration for a frequency plan other than the default state (that is, the device calibrates the VCO based on the settings contained within the registers). The nominal state of this bit is low. Writing this bit to a high state and then returning it to the low state invokes a device reset without restoring device defaults.
4. **Device stabilization** – After exiting the reset state as described in Step 3, the device monitors internal voltages and starts a reset timer. Only after internal voltages are at the correct level and the reset time has expired will the device initiate a VCO calibration. This ensures that the device power supplies and phase locked loops have stabilized prior to calibrating the VCO.
5. **VCO Calibration** – The LMK05028 calibrates the VCO. During the calibration routine, the device holds all outputs in reset so that they generate no spurious clock signals.

9.3.9 Output Channel Muxes

Each of the 6 output channels has an output mux. The output muxes for outputs 2 to 7 can select between the PLL1 and PLL2 post divider clocks. The output muxes for outputs 0 and 1 can select between PLL1 and PLL2 post divider clocks, XO input, or one of the reference bypass mux inputs.

9.3.9.1 Reference Bypass Mux

The reference bypass mux can select between the selected DPLL1 input, selected DPLL2 input, or TCXO input. These PLL bypass paths are intended for diagnostic purposes, and are not optimized for lowest additive phase noise or jitter.

9.3.10 Output Divider

Each of the 6 output channels has an output divider after the channel mux. Outputs 2 and 3 share an output divider, as do outputs 4 and 5. Outputs 0, 1, 6, and 7 have their own individual output dividers. The output divider is used to generate the final output clock frequency from the source selected by the output mux. Each output divider is powered from the same VDDO supply used for the clock output drivers.

Outputs 1 to 6 have 20-bit dividers that can support output frequencies from 2 kHz to 750 MHz. It is possible to configure the divider for higher clock frequencies, but the output voltage swing may fall out of specification due to signal attenuation depending on the configured output driver.

Outputs 0 and 7 each have cascaded 11-bit and 20-bit output dividers that can support output frequencies from 1 Hz (1 PPS) to 750 MHz. In this case, the total output divide value is the product of the cascaded divider values.

9.3.11 Clock Outputs

Each output can be configured through registers as Differential AC-coupled (AC-LVDS/CML/LVPECL), HCSL, or 2.5-V / 1.8-V LVCMOS clocks. Outputs 2 and 3 share an output supply (VDDO_23), as do outputs 4 and 5 (VDDO_45). Outputs 0, 1, 2, and 3 have individual output supplies (VDDO_0, VDDO_1, VDDO_6, and VDDO_7). Each output supply can be independently set to 1.8 V, 2.5 V, or 3.3 V for Differential or HCSL driver modes, or 1.8 V or 2.5 V for LVCMOS mode. Each channel has a dedicated LDO regulator to provide high power supply noise rejection (PSNR) and minimize supply-noise induced jitter and spurs.

The differential output stage uses a switched-current mode driver shown in . A programmable tail current of 4, 6, or 8 mA is used to achieve typical V_{OD} swings of 400 mV (AC-LVDS), 600 mV (AC-CML), or 800 mV (AC-LVPECL) across a 100- Ω differential load. Because this output driver is ground-referenced (V_{OL} near GND) and has low common-mode voltage, the output clock jitter performance or other AC or DC specifications are insensitive of the VDDO voltage. The differential output can be externally AC-coupled to LVDS, CML, or LVPECL receivers with internal or external termination and biasing. The differential drivers are internally biased and do not need any external pullup or pulldown resistors.

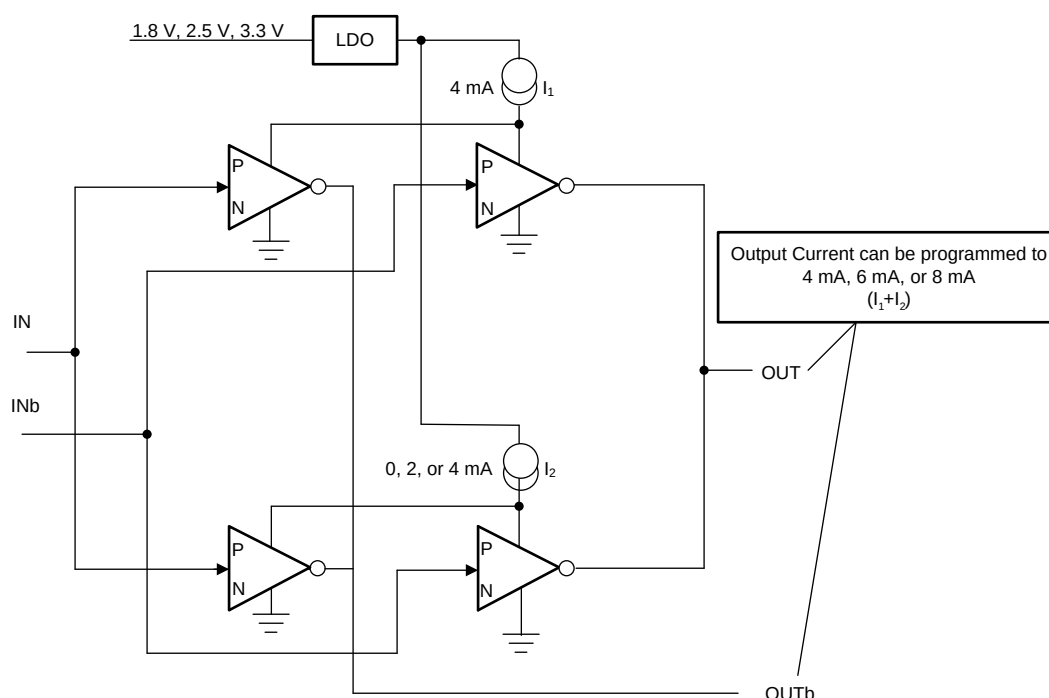


Figure 28. Structure of AC-LVDS, AC-CML, AC-LVPECL Differential Output Stage

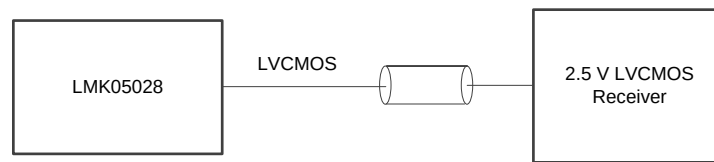
The HCSL output driver is open-drain type and can be DC coupled to HCSL receivers. The HCSL output has programmable 50-Ω source termination to ground internally. If the internal termination is disabled, the HCSL output should have external 50-Ω termination to ground at either the source or load side.

The LVCMOS outputs on each side (P and N) can be configured individually to be complementary or in-phase, or can be disabled (HiZ or static low). 1.8-V or 2.5-V LVCMOS outputs can be configured using VDDO of 1.8 V or 2.5 V, respectively.

Figure 29 and Figure 34 show recommendations for interfacing between clock outputs and LVCMOS, LVPECL, LVDS, CML, and HCSL receivers, respectively.

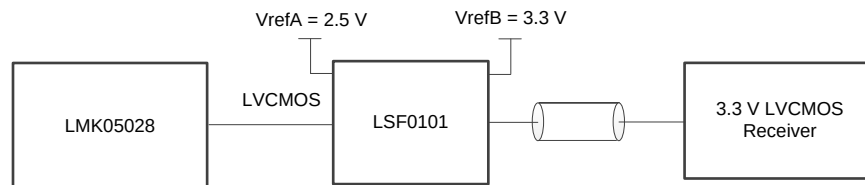
NOTE

If interfacing 2.5-V LVCMOS high-speed clock outputs with a 3.3-V LVCMOS receiver is desired, use a level-shifter like LSF0101 to convert the 2.5-V LVCMOS signal to a 3.3-V LVCMOS signal.



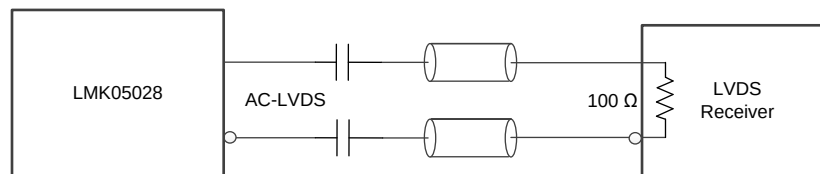
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Figure 29. Interfacing LMK05028's 2.5-V LVCMOS Output With 2.5-V LVCMOS Receiver



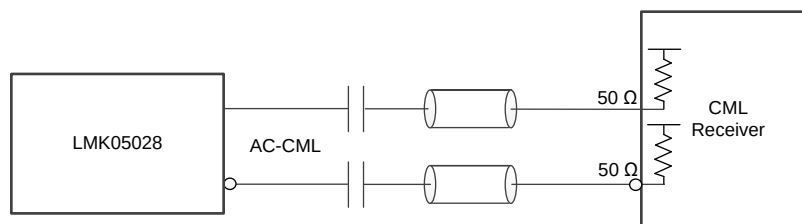
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Figure 30. Interfacing LMK05028's 2.5-V LVCMOS Output With 3.3-V LVCMOS Receiver



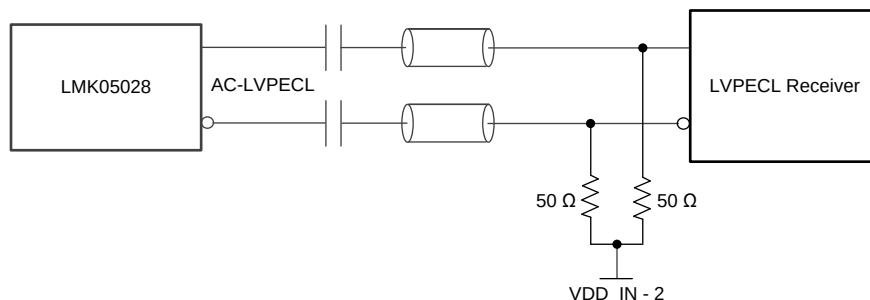
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Figure 31. Interfacing LMK05028's AC-LVDS Output With LVDS Receiver

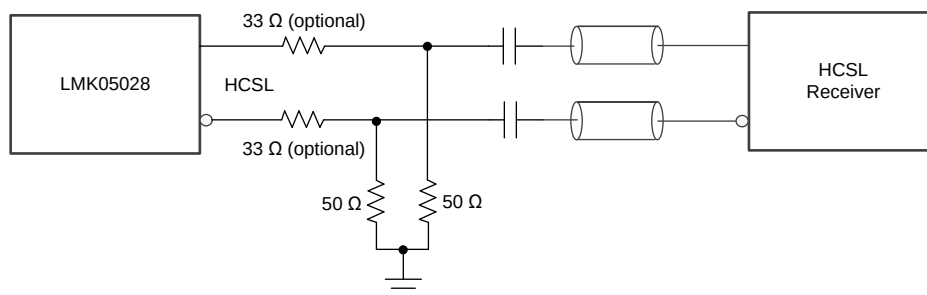


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Figure 32. Interfacing LMK05028's AC-CML Output With CML Receiver



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Figure 33. Interfacing LMK05028's AC-LVPECL Output With LVPECL Receiver


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Figure 34. Interfacing LMK05028's Output With HCSL Receiver

9.3.12 Output Synchronization

Each output divider and PLL post divider bank can be synchronized using the SYNC assertion signal for any divider that has their corresponding SYNC-enable bit set. The SYNC assertion signal can come from the external GPIO0 pin (active low) or the SYNC_SW register bit (active high). When SYNC is asserted, the SYNC-enabled dividers held are reset and clock outputs are muted. When SYNC is de-asserted, the clock outputs will start up with their initial phases synchronized or aligned. SYNC can also be used to mute any SYNC-enabled outputs to prevent output clocks from being distributed to down-stream devices, such as DSPs or FPGAs, until they are configured and ready to accept the incoming clock.

Table 6. Output Channel Synchronization

GPIO0 PIN	OUTPUT DIVIDER AND DRIVER STATE
0	Output driver(s) muted and output divider(s) reset
1	Normal output driver/divider operation as configured

9.4 Device Functional Modes

After device POR and initialization, each PLL core operates in one of the following modes depending on the clock input qualification and DPLL lock status:

9.4.1 Free-Run Mode

After device POR and initialization, the APLL in each PLL core locks to the qualified XO and no DPLL lock acquisition or synchronization has been initiated. The accuracy of the output clock is equal to the accuracy of the XO input clock. Neither the DPLL reference input nor TCXO/OCXO input are qualified yet. After the TCXO input is qualified, the TCXO-DPLL in each PLL core locks to it so the accuracy of the output clock is equal to the accuracy of the TCXO input clock. The reference input remains unqualified during free-run mode.

Device Functional Modes (continued)

9.4.2 Lock Acquisition Mode

Each DPLL constantly monitors its assigned inputs for a valid clock. When at least one valid clock is detected, the DPLL will exit free-run or holdover mode and initiate lock acquisition. The LMK05028 supports a fast lock feature where the loop bandwidth is set to wider than the nominal setting during lock acquisition to reduce the lock time. Once lock acquisition is done, the loop bandwidth is set to its nominal loop bandwidth setting.

9.4.3 Locked Mode

When a DPLL has completed lock acquisition, the PLL output clocks will be frequency and phase locked to its selected input clock. While the DPLL is locked, the output clocks will not be affected by frequency drift on the XO input or the TCXO input if the TCXO-DPLL is configured. Each DPLL has a programmable frequency and phase lock detector thresholds to indicate DPLL lock status, which can be observed through status pin or interrupt register bits.

9.4.4 Holdover Mode

If a tuning word history exists, the holdover frequency is the average frequency just prior to entry of the holdover. If no tuning word history exists, the holdover frequency is determined by the free-run tuning word register (user programmable). The initial holdover frequency accuracy depends on the loop bandwidth of the REF-DPLL and the time elapsed to compute a tuning word history. In general, the longer the historical average, the more accurate the initial holdover frequency (assuming the 0-ppm reference clock is drift-free). The stability of 0-ppm reference clock (XO or TCXO input) determines the long-term stability and accuracy of the holdover output frequency. Holdover mode flow chart is shown in [Figure 35](#).

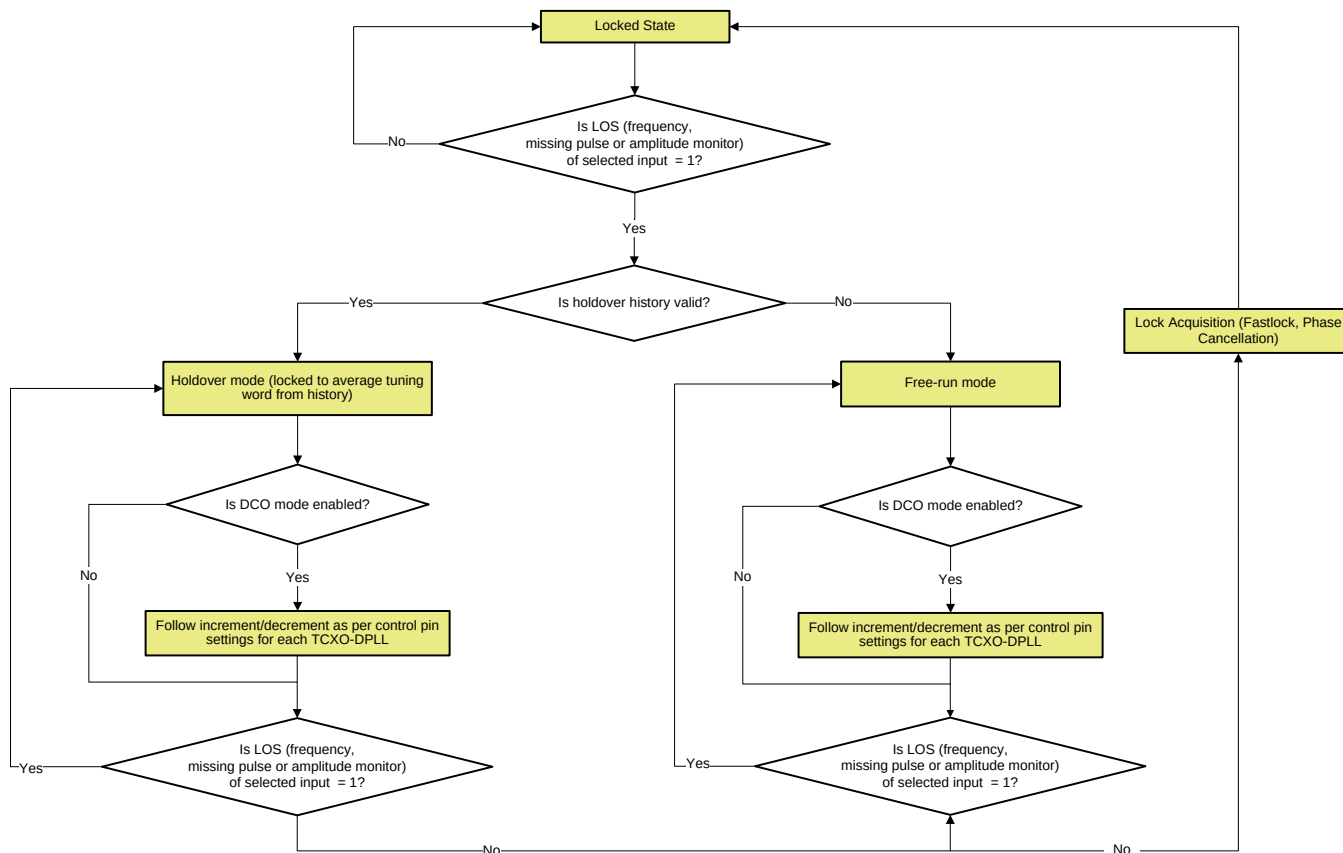


Figure 35. LMK05028 Holdover Flowchart

Device Functional Modes (continued)

9.4.5 Digitally-Controlled Oscillator (DCO) Mode

To support IEEE 1588 slave clock and other clock steering applications, each DPLL supports DCO mode to allow precise output clock frequency adjustment of less than 1 ppt per step. DCO mode can be enabled by register (DPLL_y_FDEV_EN bit) on either REF-DPLL or TCXO-DPLL loop when operating in locked mode. The DCO frequency step size can be programmed through the frequency deviation register (DPLL_y_FDEV bits), and the DCO frequency increment or decrement can be updated through software or pin control. DCO updates through software control are always available through I2C or SPI register write command (DPLL_y_FDEV_REG_UPDATE bit). Pin control must be enabled through registers. When pin control is enabled (GPIO[3:6]_FDEV_EN bits), the GPIO3 and GPIO4 pins allow DPLL1 DCO frequency increment (FINC) and decrement (FDEC) updates, and the GPIO5 and GPIO6 pins allow DPLL2 DCO FINC and FDEC updates, respectively. A rising edge on the FINC pin will increment the PLL output frequency by the programmed step size, while a rising edge on the FDEC pin will decrement it. The DCO update rate should be limited to 1 MHz or less.

9.4.5.1 DCO Frequency Step Size

Equation 8 shows the formula to compute the DPLL_y_FDEV register value required to meet the specified DCO frequency step size (in ppb) when DCO mode is enabled for the REF-DPLL (when DPLL_y_DCO_SEL_REF_TCXOB = 1).

$$\text{DPLL}_y\text{FDEV} = (\text{Reqd_ppb} / 1\text{E}9) \times \text{DEN}_{\text{REF-DPLL}} / (\text{F}_{\text{INX}} / \text{Rx}) \times \text{F}_{\text{VCO}} / (\text{P1} \times \text{PR}_{\text{REF-DPLL}})$$

where

- DPLL_y_FDEV: Frequency deviation value (38 bits, 0 to 2³⁸-1)
- Reqd_ppb: Required DCO frequency step size (in ppb)
- DEN_{REF-DPLL}: REF-DPLL feedback divider denominator value (40 bits, 1 to 1 to 2⁴⁰)
- F_{INX}: Reference input frequency (x = 0, 1, 2, 3)
- Rx: Reference input divider (16 bits, 1 to 1 to 2¹⁶-1) (x = 0, 1, 2, 3)
- F_{VCO}: APLL/VCO frequency
- P1 = PLL primary post-divider (4 to 9, 11, 13)
- PR_{REF-DPLL}: REF-DPLL feedback prescaler divider (2 to 17)

(8)

Equation 9 shows the formula to compute the DPLL_y_FDEV register value required to meet the specified DCO frequency step size (in ppb) when DCO mode is enabled for the TCXO-DPLL (when DPLL_y_DCO_SEL_REF_TCXOB = 0).

$$\text{DPLL}_y\text{FDEV} = (\text{Reqd_ppb} / 1\text{E}9) \times \text{DEN}_{\text{TCXO-DPLL}} / (\text{F}_{\text{TCXO}} / \text{M}) \times \text{F}_{\text{VCO}} / (\text{P1} \times \text{PR}_{\text{TCXO-DPLL}})$$

where

- Reqd_ppb: Required DCO frequency step size (in ppb)
- DEN_{TCXO-DPLL}: TCXO-DPLL feedback divider denominator value (fixed, 2⁴⁰)
- F_{TCXO}: TCXO/OCXO input frequency
- M: TCXO/OCXO input divider (5 bits, 1 to 32)
- PR_{TCXO-DPLL}: TCXO-DPLL feedback prescaler divider (2 to 17)

(9)

9.4.5.2 Direct-Write DCO Mode

An alternate method to update the DCO frequency is by directly writing the REF-DPLL or TCXO-DPLL feedback divider numerator (NUM) register for the corresponding DPLL through I2C or SPI write command.

9.5 Programming

The LMK05028 can start up in one of three modes depending on the 3-level input level sampled on the HW_SW_CTRL pin:

- HW_SW_CTRL = 0: EEPROM + I2C Mode (Soft pin mode)
- HW_SW_CTRL = F: EEPROM + SPI Mode (Soft pin mode)
- HW_SW_CTRL = 1: ROM + I2C Mode (Hard pin mode)

The selected device start-up mode determines the following:

- The memory bank (EEPROM or ROM) used to initialize the registers to configure all device blocks.

Programming (continued)

- The serial interface (I2C or SPI) used for register access.
- The logic pin functionality for control and status.

The I2C or SPI interface allows register access to configure the device after start-up and monitors its status. The register map configurations are the same for I2C and SPI.

Figure 36 shows the device start-up mode configurations. Table 2 shows the logic pin functions used to enter and operate in each device mode.

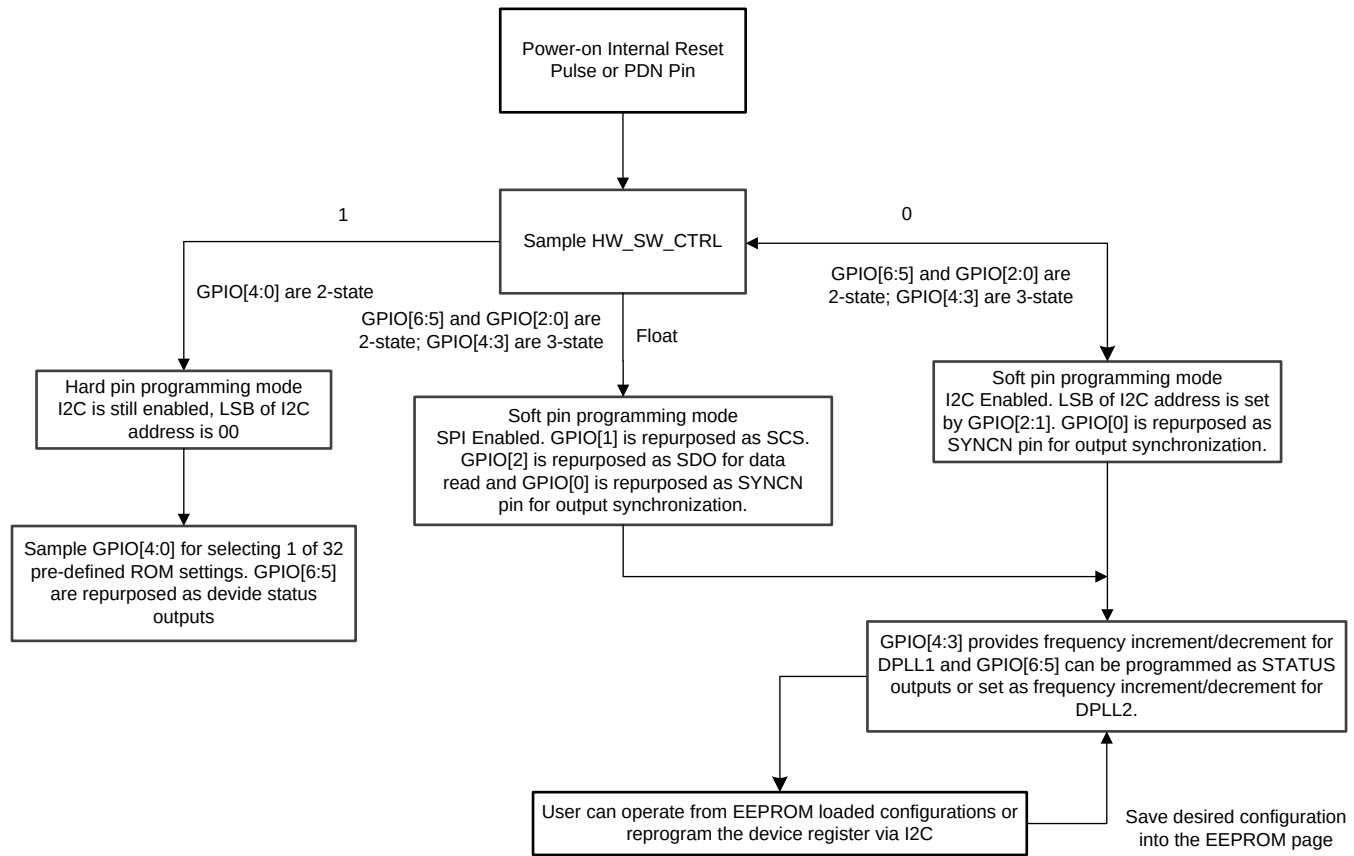


Figure 36. LMK05028 Programming Flow

9.5.1 Interface and Control

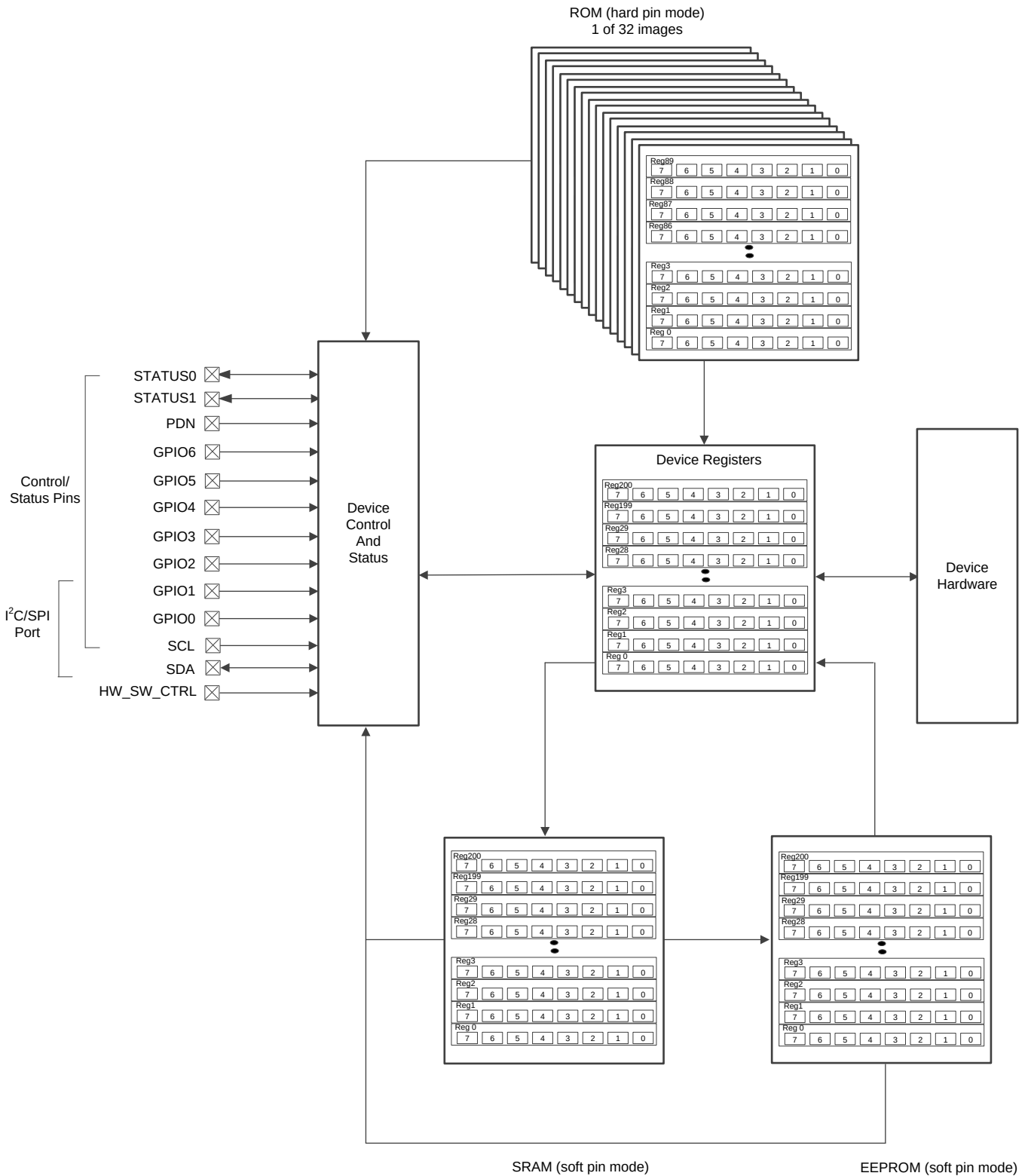
The system host (MCU, FPGA,) can use either I2C or SPI to access the register, SRAM, and EEPROM maps. The register and EEPROM map configurations are the same for I2C and SPI. The LMK05028 device blocks can be initially configured, controlled, and monitored through registers during normal operation (not when the PDN is low). The host can also control and monitor certain device parameters directly through the external logic control and status pins.

In the absence of a host, the LMK05028 can self-start from its on-chip EEPROM or ROM page depending on the state of HW_SW_CTRL pin. The EEPROM or ROM page is used to initialize the registers upon device POR. The EEPROM can be programmed and read-back through the register interface using I2C or SPI. The contents of ROM are fixed in hardware and cannot be modified.

Within the device registers, there are certain bits that have read or write access. Other bits are read-only (an attempt to write to a read-only bit will not change the state of the bit). Certain device registers and bits are reserved and should not be modified to avoid potential mis-operation of the device. Figure 37 shows the interface and control blocks within LMK05028 and the arrows refer to read and write access for the different embedded memories (SRAM, EEPROM, and ROM).

Programming (continued)

ADVANCE INFORMATION



NOTE: The internal ROM has 16 pages selectable by GPIO[3:0] pins in Hard pin mode (not 32 pages as shown).

Figure 37. Device Control, Register, and Memory Interfaces

Programming (continued)

9.5.2 I2C Serial Interface

When started in I2C mode (HW_SW_CTRL = 0 or 1), the LMK05028 operates as an I2C slave and supports bus rates of 100 kHz (standard mode) and 400 kHz (fast mode). Slower bus rates can work as long as the other I2C specifications are met. The I2C timing diagram is shown in [Figure 38](#).

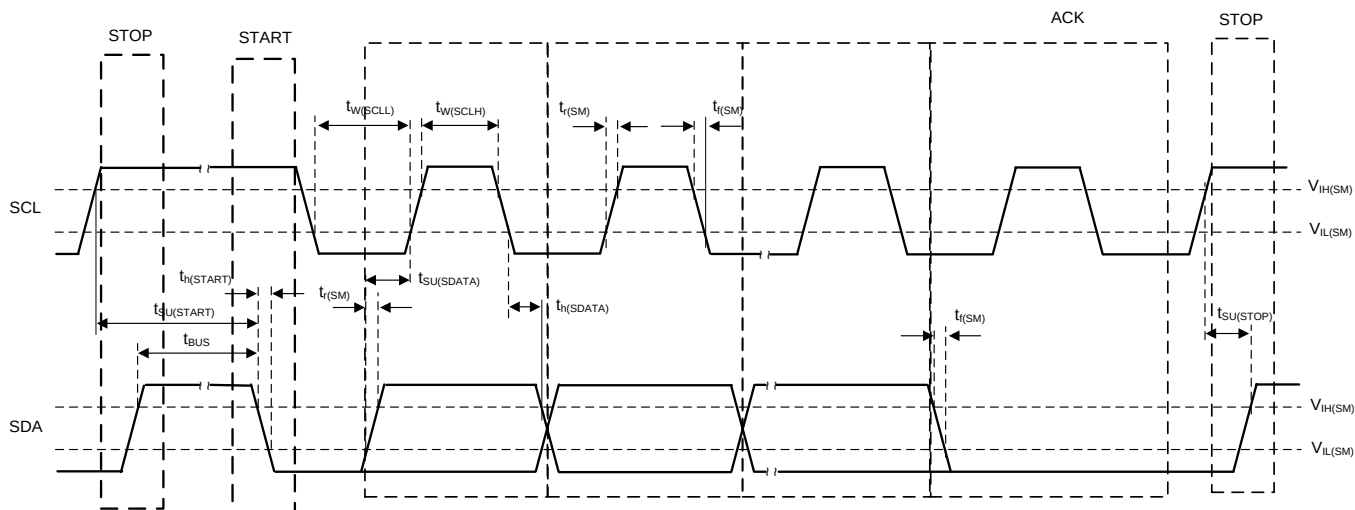


Figure 38. I2C Timing Diagram

In EEPROM mode, the LMK05028 can support up to 4 different I2C addresses depending on the GPIO[2:1] pins. The 7-bit I2C address is 11000xxb, where the two LSBs are determined by the GPIO[2:1] input levels sampled at device POR and the five MSBs (11000b) are initialized from EEPROM. In ROM mode, the two LSBs are fixed to 00b and the five MSBs are initialized from ROM.

A generic transaction is shown in [Figure 39](#).

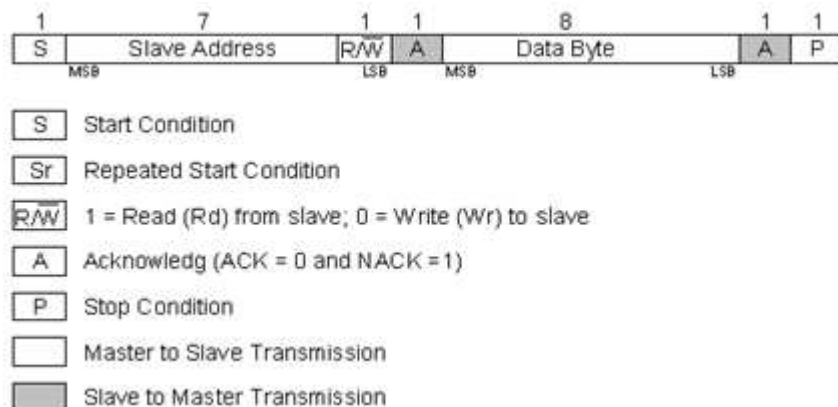


Figure 39. I2C Generic Programming Sequence

Programming (continued)

9.5.3 SPI Serial Interface

When started in SPI mode (HW_SW_CTRL = float), the LMK05028 uses a 4-wire SPI interface with SDI, SCL, SDO, and SCS signals. The host must present data to the device MSB first. A message includes a transfer direction bit (W/R), a 15-bit address field (A14 to A0), and an 8-bit data field (D7 to D0) as shown in Figure 40. The W/R bit is 0 for a SPI write and 1 for a SPI read.

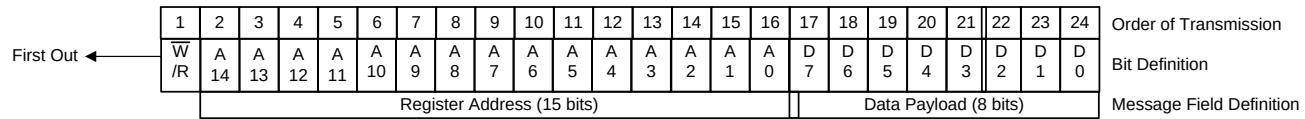


Figure 40. SPI Message Format

The SPI timing diagram is shown in Figure 41.

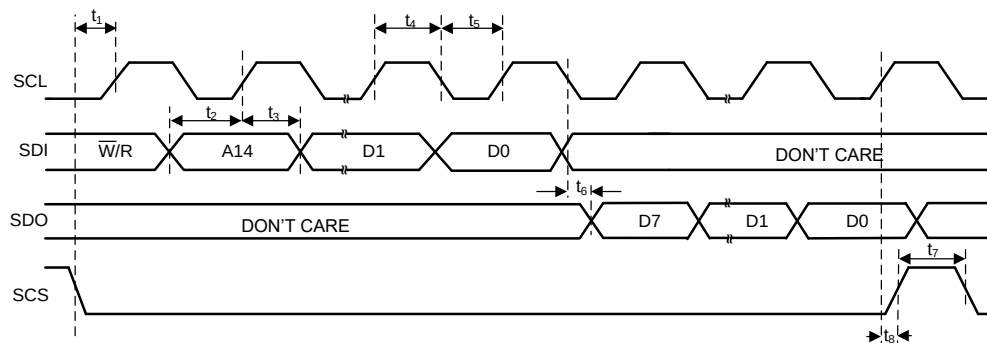


Figure 41. SPI Timing Parameters

9.5.4 EEPROM Programming Flow

After the configuration registers are programmed, the EEPROM can be programmed by the register writes in two steps: Write SRAM and Program EEPROM.

9.5.4.1 Write SRAM

The SRAM array is volatile *shadow* memory mapped to a subset of the active configuration registers that determine the device operation at POR or initialization. After the active registers have been programmed, they can be committed to the SRAM through the following sequence:

1. Write a 0 to REGCOMMIT_PG bits.
2. Write a 1 to REGCOMMIT bit (self-clearing). This transfers the active register data to the SRAM internally.

If the SRAM/EEPROM map data is already known, the SRAM can also be written directly *without modifying the active configuration registers* through the following sequence:

1. Write the 4 upper bits of the SRAM address to MEMADR[12:8] bits and write 8 lower bits of the SRAM address to MEMADR[7:0] bits.
2. Write the desired SRAM data byte to RAMDAT bits in the same I2C or SPI transaction and this data byte will be written at the SRAM address specified in the previous step. Any additional access that is part of the same transaction will cause the SRAM address to be auto-incremented and a subsequent write will take place to the next SRAM address. Access to SRAM will terminate at the end of current I2C or SPI transaction.

Programming (continued)

9.5.4.2 Program EEPROM

The EEPROM array is non-volatile memory mapped directly from the SRAM array. After the register settings have been committed to SRAM (see [Write SRAM](#)), the EEPROM can be programmed from SRAM through the following sequence:

1. Write EAh to NVMUNLK bits. This unlocks the EEPROM from protected state to allow programming.
2. Write a 1 to NVM_ERASE_PROG bits. This programs EEPROM from the entire SRAM contents. The total Erase/Program sequence takes about 230 ms.
3. Poll the NVMBUSY bit. The EEPROM programming is done when the NVMBUSY bit is cleared. The NVMCNT register value will be auto-incremented by 1 to reflect total number of EEPROM programming cycles completed.
4. (optional) Write 0h to NVMUNLK bits. This locks the EEPROM to protect against inadvertent programming.

On the next power-up or POR cycle, the device will self-start in Soft Pin mode from the newly programmed EEPROM configuration.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Device Start-Up Sequence

The device start-up sequence is shown in [Figure 42](#). In the case when VDDO_x is delayed until after the POR, the output channel is held in reset and its output(s) are muted when VDDO_x reaches acceptable value. Once VDDO_x reaches is ramped, the output channel is released from reset and outputs are unmuted without glitches.

Application Information (continued)

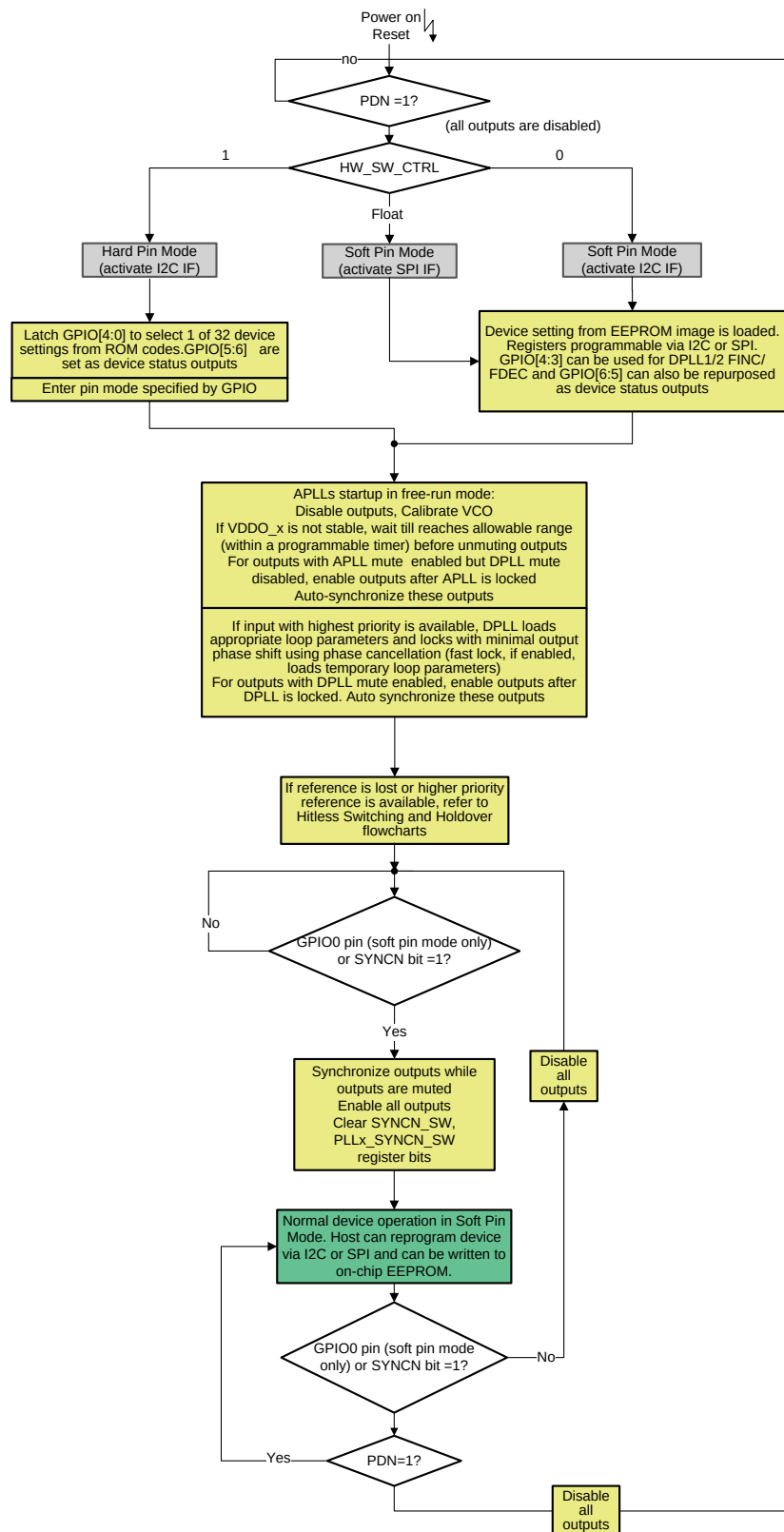


Figure 42. Device Start-Up Sequence

Application Information (continued)

10.1.2 Power Down (PDN) Pin

The PDN pin (active low) can be used for device power-down and used to initialize the POR sequence. When PDN is pulled low, the entire device is powered down and the serial interface is disabled. When PDN is pulled high, the device POR sequence is triggered to begin the device start-up sequence and normal operation as depicted in Figure 42.

Table 7. PDN Control

PDN PIN STATE	DEVICE OPERATION
0	Device is disabled
1	Normal operation

10.1.3 Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains

10.1.3.1 Mixing Supplies

The LMK05028 incorporates flexible power supply architecture. While all VDD core supplies should be powered by the same 3.3-V rail, the individual output supplies can be powered from separate 1.8-V, 2.5-V or 3.3-V rails. This can allow all output supplies at 1.8 V to minimize power consumption. It can also allow mixed output driver levels simultaneously, for example, a 2.5-V LVCMOS clock from a 2.5-V rail and other differential clocks from a 1.8-V rail.

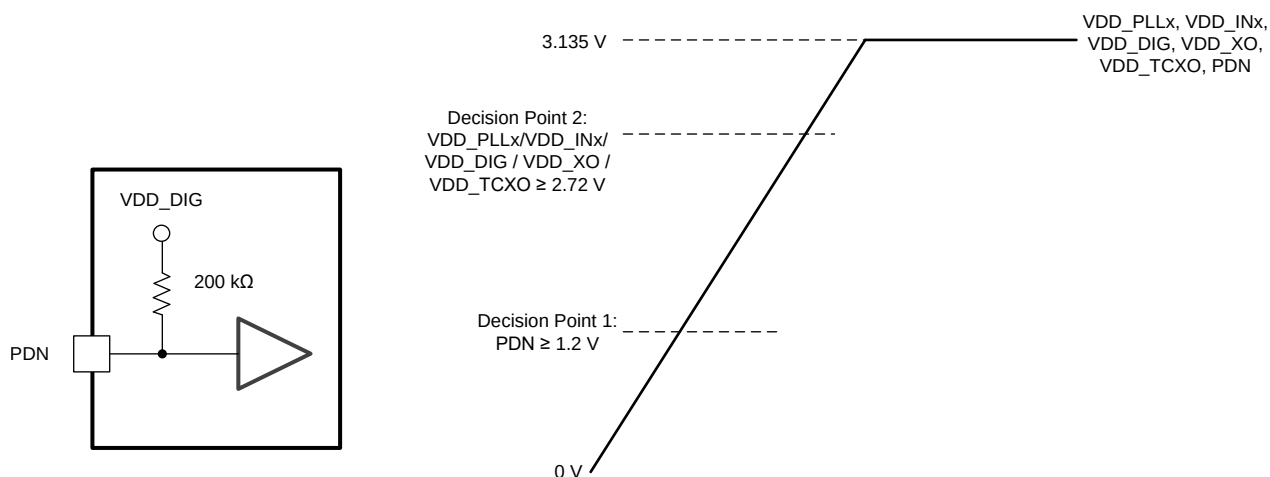
10.1.3.2 Power-On Reset (POR) Circuit

The LMK05028 integrates a built-in power-on reset (POR) circuit that holds the device in reset until all of the following conditions have been met:

- All VDD core supplies have ramped above 2.72 V
- PDN pin has ramped above 1.2 V (V_{IH})

10.1.3.3 Powering Up From a Single-Supply Rail

As long as all VDD core supplies are driven by the same 3.3-V supply rail that ramp in a monotonic manner from 0 V to 3.135 V, irrespective of the ramp time, then there is no requirement to add a capacitor on the PDN pin to externally delay the device power-up sequence. As shown in Figure 43, the PDN pin can be left floating or otherwise driven by a host controller for meeting the clock sequencing requirements in the system.


Figure 43. Recommendation for Power Up From a Single-Supply Rail

10.1.3.4 Power Up From Split-Supply Rails

If some VDD core supplies are driven from different supply rails, TI recommends starting the PLL calibration after all of the core supplies have settled at 3.135 V. This can be realized by delaying the PDN low-to-high transition. The PDN input incorporates a 200-k Ω resistor to VDD_DIG and as shown in Figure 44, a capacitor from the PDN pin to GND can be used to form a R-C time constant with the internal pullup resistor. This R-C time constant can be designed to delay the low-to-high transition of PDN until all the core supplies have settled at 3.135 V.

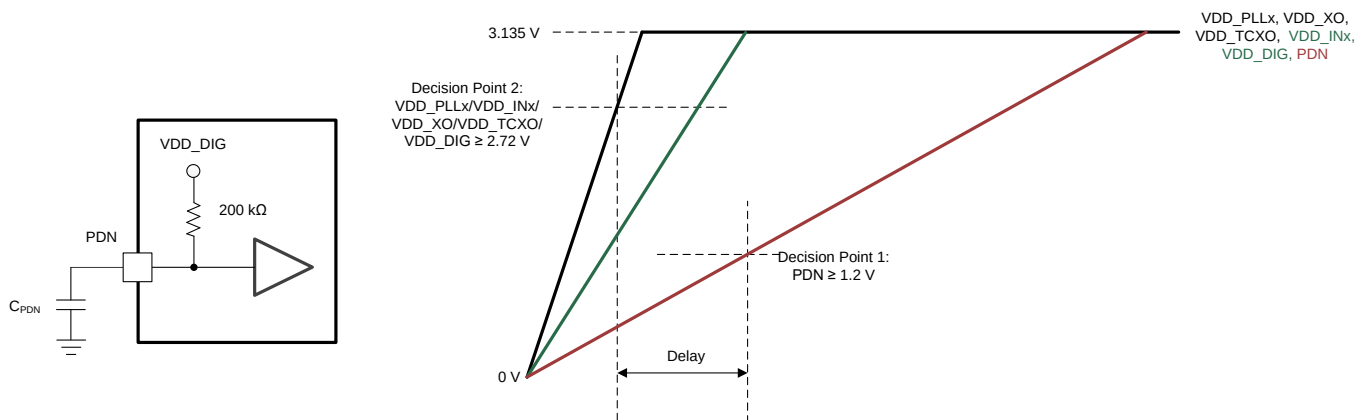


Figure 44. Recommendation for Power Up From Split-Supply Rails

10.1.3.5 Non-Monotonic or Slow Power-Up Supply Ramp

In case the VDD core supplies ramp with a non-monotonic manner or with a slow ramp time from 0 V to 3.135 V of over 100 ms, TI recommends starting the PLL calibration after all of the core supplies have settled at 3.135 V. This can be realized by delaying the PDN low-to-high transition in a manner similar to the condition shown in Figure 44.

10.2 Typical Application

Figure 45 shows a reference schematic to help implement the LMK05028 and its peripheral circuitry. Power filtering examples are given for the core supply pins and independent output supply pins. Single-ended LVCMOS, AC-coupled differential, and HCSL clock interface examples are shown for the various clock input and output pins. An external LVCMOS oscillator is driving a AC-coupled voltage divider network as an example to interface a 3.3-V LVCMOS output to the XO or TCXO input pin. The required external capacitors with the recommended values are shown. The logic I/O pins with external pullup or pulldown resistor options set the default input states. The I2C or SPI pins and other logic pins can be connected to a host device (not shown) to program and control the LMK05028 and monitor its status. This example assumes the device will start up from EEPROM mode with an I2C interface (HW_SW_CTRL = 0).

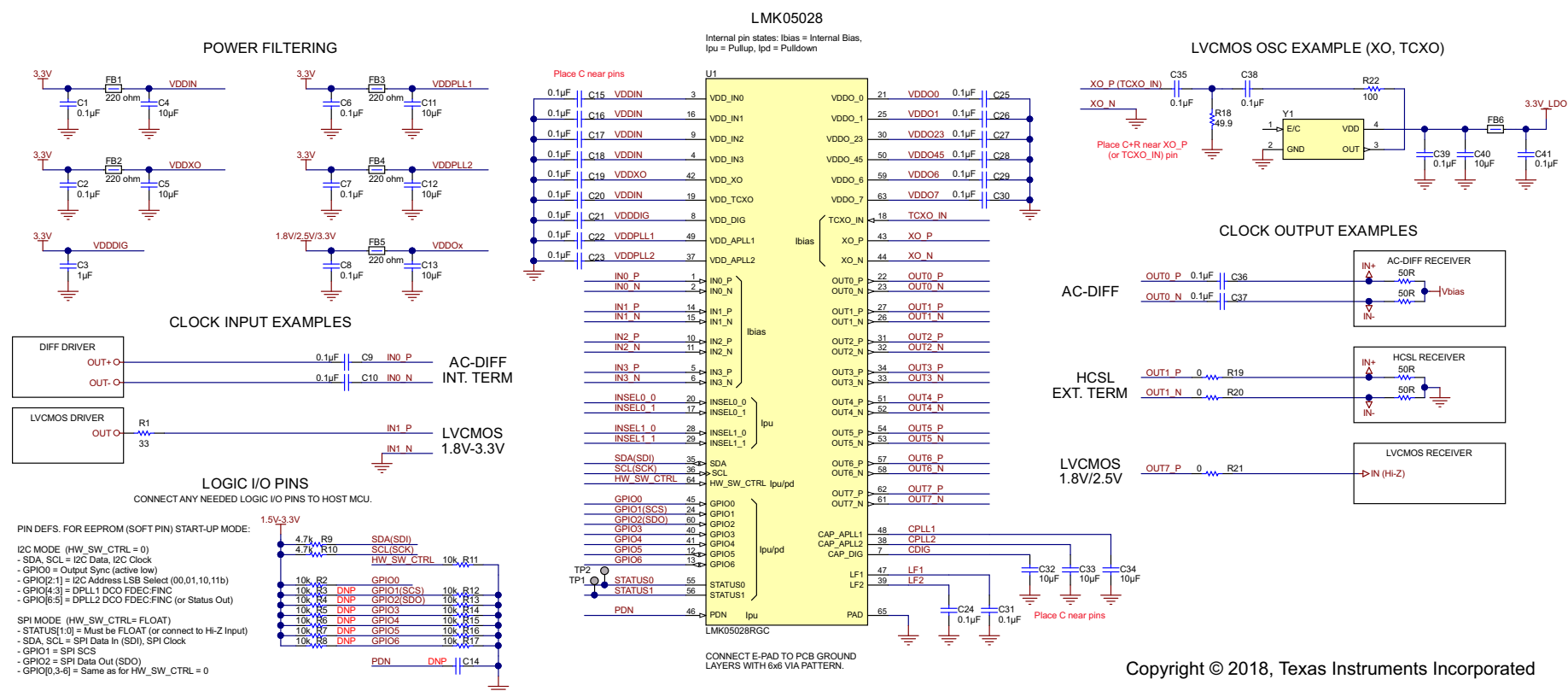


Figure 45. Reference Schematic Example

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10.2.1 Design Requirements

In a typical application, the following design parameters should be considered to implement the overall clock solution:

1. Device initial configuration: Host programmed or factory pre-programmed.
2. Device start-up mode and serial interface. Typically, this will be EEPROM + I2C or SPI mode.
3. XO frequency, signal type, and phase noise or jitter
4. TCXO frequency and stability if any of the following is required:
 - Standard-compliant frequency stability (such as SyncE, SONET/SDH, IEEE 1588)
 - Lowest possible close-in phase noise at offsets ≤ 100 Hz
 - Narrow DPLL bandwidth ≤ 10 Hz
5. For each PLL domain, determine the following:
 - Input clocks: frequency, buffer mode, priority, and input selection mode
 - Output clocks: frequency, buffer mode
 - DPLL loop mode, loop bandwidth, and *market segment*
 - DCO mode or Zero delay
6. Clock monitoring options
7. Status outputs and interrupt flag
8. Power supply rails

10.2.2 Detailed Design Procedure

In a typical application, TI recommends the following steps:

1. The LMK05028 GUI in TI's TICS Pro software has a step-by-step design flow to enter the design parameters, calculate the frequency plan for each PLL domain, and generate the register settings for the desired configuration. The register settings can be exported (as hex data) to enable host or factory programming.
 - If using a generic (non-custom) device, a host device can program the register settings through the serial interface after power-up and issue a soft-reset (by RESET_SW bit) to start the device. The host can also store the settings to the EEPROM to allow self-startup with these register settings on subsequent power-on reset cycles.
 - Alternatively, a LMK05028 setup file for TICS Pro (.tcs) can be sent to TI to request custom factory pre-programmed devices.
2. Tie the HW_SW_CTRL pin to 0 or float it (V_{IM}) to select EEPROM mode with I2C or SPI respectively. Determine the logic I/O pin assignments for control and status functions.
 - Connect I2C/SPI and logic I/O pins (1.8-V compatible levels) to the host device pins with the proper I/O direction and voltage levels.
3. Select a XO frequency by following [Oscillator Input \(XO_P/N\)](#).
 - Choose a XO with target phase jitter performance < 300 fs RMS (12 kHz to 20 MHz).
 - For a 3.3-V LVCMOS XO, follow the OSC clock interface example in [Figure 45](#). Power the OSC from a low-noise regulator.
 - Configure the XO input buffer and termination options through the registers.
4. If a TCXO/OCXO is needed, select the frequency by following [TCXO Input \(TCXO_IN\)](#).
 - Choose a TCXO/OCXO that meets the frequency stability (over operating conditions) and accuracy requirements required for the output clocks during free-run or holdover.
 - For a 3.3-V LVCMOS TCXO/OCXO, follow the OSC clock interface example in [Figure 45](#).
 - A (clipped) sinewave TCXO/OCXO with less than 1.2-V_{pp} swing can be simply AC-coupled to the input pin.
5. For each PLL domain, wire the clock I/O in the schematic and configure the device settings as follows:
 - Reference inputs: Follow the LVCMOS or differential clock input interface examples in [Figure 45](#).
 - Configure each reference input buffer mode through registers to match the driver interface requirements.
 - LVCMOS input mode should be used for input frequencies below 5 MHz.

- Configure the DPLL input selection modes and input priorities through the registers.
- Output clock assignment guidelines to minimize crosstalk and spurs:
 - OUT[4:7] bank requires at least one clock from the PLL1 domain. OUT[4:7] bank is preferred for PLL1 clocks.
 - OUT[0:3] bank requires at least one clock from the PLL2 domain if enabled. OUT[0:3] bank is preferred for PLL2 clocks.
 - Group identical output frequencies (or harmonic frequencies) on adjacent channels. Use the output pairs with a single divider (OUT2/3 or OUT4/5) if possible to minimize power.
 - Separate clock outputs when the difference of the two frequencies, $|F_{OUTx} - F_{OUTy}|$, falls within the jitter integration bandwidth (12 kHz to 20 MHz, for example). The two outputs should be separated by at least 4 static pins (power or logic) to minimize potential coupling, or consider placing them on separate output banks (which are on opposite sides of the chip).
 - Avoid or isolate any LVCMOS output (strong aggressor) from other jitter-sensitive differential output clocks. If a LVCMOS output is required, use dual complementary LVCMOS mode (+/- or -/+) with the unused LVCMOS output left floating with no trace. Furthermore, the output slew rate could also be slowed to Normal mode (CHx_SLEW_RATE bit) to reduce the coupling strength of an LVCMOS output.
 - If not all outputs pairs are used in the application, consider connecting OUT0 or OUT1 to a pair of RF coaxial test structures for testing purposes (such as SMA, SMP). OUT0 and OUT1 are capable of selecting a buffered copy of the XO clock or the Ref Bypass clock (either DPLL reference or TCXO input) as well as any PLL post-divider clock.
- Clock outputs: Follow the single-ended or differential clock output interface examples in [Figure 45](#).
 - Configure each clock output buffer mode through registers to match the receiver interface requirements.
 - Differential outputs should be AC-coupled and terminated or biased at the receiver inputs.
 - HCSL outputs should have 50-Ω termination to GND (at source or load side) unless the internal source termination is enabled by registers.
 - LVCMOS outputs have internal source termination to drive 50-Ω traces directly. LVCMOS V_{OH} level is determined by VDDO voltage (1.8 V and 2.5 V).
- Configure the DPLL loop mode.
 - 3-loop mode supports standards-compliant synchronization using a low-cost holdover TCXO/OCXO, very low loop bandwidths (≤ 10 Hz), or both. 3-loop mode also supports 1-PPS input synchronization.
 - 2-loop mode with REF-DPLL supports higher loop bandwidth (> 10 Hz) and relaxed holdover stability without a TCXO/OCXO.
 - 2-loop mode with TCXO-DPLL locks to a TCXO/OCXO input and typically used with DCO mode for external clock steering (such as IEEE 1588 PTP).
- Configure the REF-DPLL loop bandwidth.
 - The optimal bandwidth depends on the relative phase noise between the reference input and the XO (or the TCXO for 3-loop mode).
 - For 3-loop mode, the bandwidth is typically 10 mHz to 10 Hz to attenuate wander and support low wander generation because of the TCXO/OCXO.
 - For 2-loop mode, the bandwidth is typically 10 Hz or higher. Target a bandwidth below 300 Hz if the PLL VCO frequency is an integer multiple of the reference input frequency.
 - Below the loop bandwidth, the reference noise is added to the REF-TDC noise floor (and the XO noise in 2-loop mode). Above the loop bandwidth, the reference noise will be attenuated at 20 dB/decade.
- Configure the TCXO-DPLL loop bandwidth.
 - The optimal bandwidth depends on the relative phase noise between the TCXO/OCXO and the XO.
 - For 3-loop mode, the bandwidth should be at least 200x higher than the REF-DPLL bandwidth for loop stability.
 - For 2-loop mode with TCXO-DPLL, target a bandwidth below 300 Hz if the PLL VCO frequency is an integer multiple of the TCXO/OCXO frequency.
 - Below the loop bandwidth, the TCXO/OCXO noise is added to the TCXO-TDC noise floor. Above the loop bandwidth, the OCXO/TCXO noise will be attenuated at 20 dB/decade.

- Configure the *market segment* parameter in TICS Pro to optimize the DPLL according to the use case.
 - *SyncE/SONET*: TDC rate is targeted for approximately 400 kHz. Hitless switching is enabled. Supports SyncE/SONET and other use cases using a narrow loop bandwidth (≤ 10 Hz) in 3-loop mode with a TCXO/OCXO to set the frequency stability and wander performance.
 - *Wireless/BTS*: TDC rate is maximized for lowest in-band TDC noise contribution. Hitless switching is enabled. Supports wireless and other use cases where close-in phase noise is critical. This is used to achieve -102 dBc/Hz at 100-Hz offset for a 122.88-MHz output.
 - *OTN/JitterAtten*: TDC rate is targeted for approximately 1 MHz. Hitless switching is disabled. Supports OTN/OTU and traditional jitter cleaning use cases with wider bandwidths (> 10 Hz) in 2-loop mode and relaxed holdover frequency accuracy (no TCXO/OCXO).
 - If clock steering is needed (such as for IEEE 1588 PTP), configure DCO mode for the REF or TCXO loop and compute the DCO FDEV step size register by following [Digitally-Controlled Oscillator \(DCO\) Mode](#). To allow DCO frequency updates using the external control pins, enable the FINC/FDEC functionality on the needed GPIO pins by setting the appropriate register bits (GPIO[3:6]_FDEV_EN).
 - If deterministic input-to-output clock phase is needed, configure zero delay mode and select the output channel that needs to be phase-aligned with the input. For DPLL1, any output from the OUT[4:7] bank can be selected for zero-delay feedback. For DPLL2, any output from the OUT[0:3] bank can be selected for zero-delay feedback.
6. Configure the clock monitoring features (per input or per DPLL):
- *Amplitude monitor*: Set the LVCMOS input slew rate detected edge or the Differential input minimum amplitude to monitor input signal quality. Disable monitor for differential inputs below 5 MHz or else use LVCMOS input mode.
 - *Frequency monitor*: Set the valid and invalid thresholds (in ppm). Disable monitor for inputs < 2 kHz.
 - *Missing pulse monitor*: Set the late window threshold (T_{LATE}) to allow for the longest expected input clock period, including jitter and gapped input clock (if applicable). Disable monitor for inputs < 2 kHz.
 - *Runt pulse monitor*: Set the early window threshold (T_{EARLY}) to allow for the shortest expected input clock period, including jitter. Disable monitor for inputs < 2 kHz.
 - *Phase validation monitor*: Set the phase validation threshold to account for worst-case input peak-to-peak jitter, specified by number of periods of the 0-ppm reference clock (XO or TCXO input). Disable monitor for inputs ≥ 2 kHz.
 - *Validation timer*: Set the amount of time the reference input must be qualified by all enabled input monitors before the input is valid for selection.
 - *DPLL frequency lock and phase lock detectors*: Set the lock and unlock thresholds for each detector.
7. Configure each status output pin and interrupt flag, if needed.
- Select the desired status signal selection, driver mode (3.3-V LVCMOS or open-drain), and status polarity. Open-drain requires an external pullup resistor.
 - If the Interrupt is enabled and selected as a status output, set the mask for any interrupt flag to be ignored, set the interrupt flag polarity, and select the combinational gate logic (OR/AND) as desired.

10.3 Do's and Don'ts

- Power all VDD pins with proper supply decoupling and bypassing connect like shown in [Figure 45](#).
- Power down unused blocks through registers to minimize power consumption.
- Leave unused clock outputs floating and powered down through register control.
- Leave unused clock inputs floating.
- For EEPROM+SPI Mode: Leave HW_SW_CTRL and STATUS[1:0] pins floating during POR to ensure proper start-up. These pins have internal biasing to V_{IM} internally.
 - If HW_SW_CTRL or either STATUS pin is connected to an external device (MCU, FPGA), the external device must be configured with high-impedance input (no pullup or pulldown resistors) to avoid conflict with the internal bias to V_{IM} . If needed, external biasing resistors (10-k Ω pullup to 3.3 V and 3.75-k Ω pulldown) can be connected on each STATUS pin to bias the inputs to V_{IM} during POR.
- Use a low-noise, high-PSRR LDO regulator to power the external oscillators used to drive the XO and TCXO inputs. Typically, oscillator jitter performance is typically impacted by switching noise on its power supply.
- Include a dedicated serial port to the I2C or SPI pins of the LMK05028.
 - This allows off-board programming for device bring-up, debug, and diagnostics using TI's USB hardware

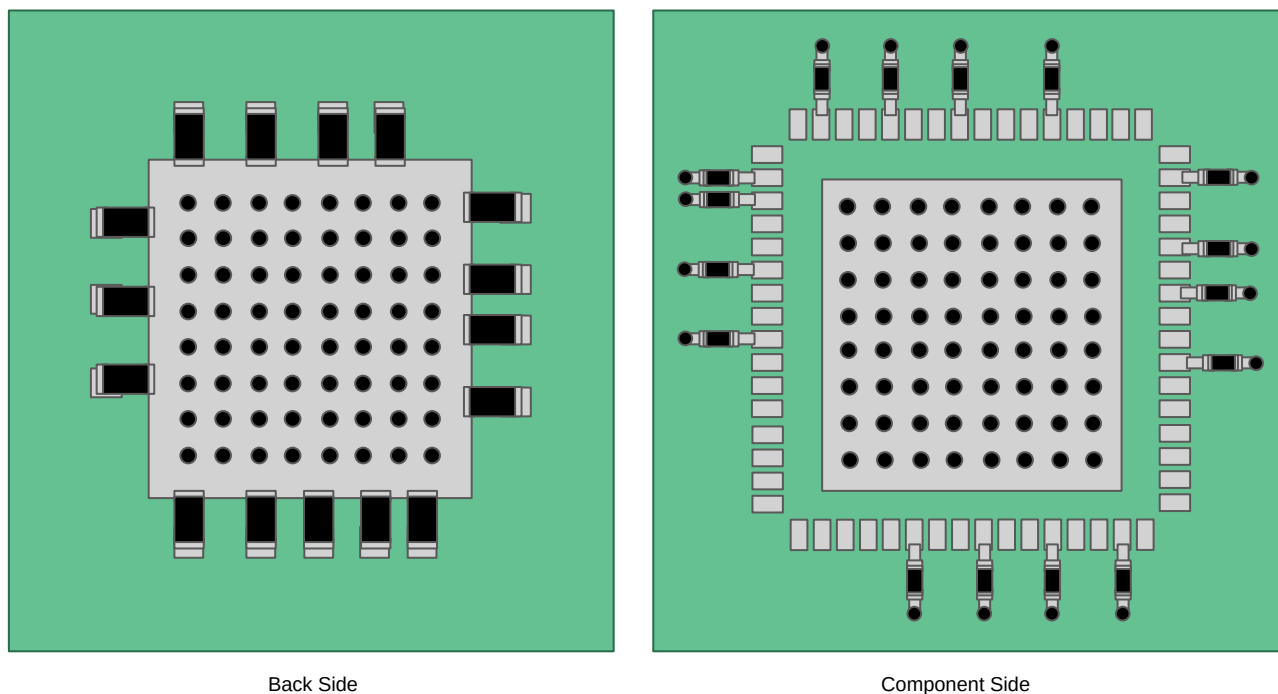
Do's and Don'ts (continued)

interface and software GUI tools.

11 Power Supply Recommendations

11.1 Power Supply Bypassing

Figure 46 shows two general placements of power supply bypass capacitors on either back side or component side. If the capacitors are mounted on the back side, 0402 components can be employed. For component side mounting, use 0201 body size capacitors to facilitate signal routing. A combination of component and back side placement can be used. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.



(Does not indicate actual location of LMK05028 supply pins)

Figure 46. Generalized Placement of Power Supply Bypass Capacitors

12 Layout

12.1 Layout Guidelines

- Isolate input, XO, TCXO, and output clocks from adjacent clocks with different frequencies and other nearby dynamic signals.
- Avoid impedance discontinuities on controlled-impedance 50-Ω single-ended (or 100-Ω differential) traces for clock and dynamic logic signals.
- Place bypass capacitors close to the VDD and VDDO pins on the same side as the LMK05028, or directly below the IC pins on the back side of the PCB. Larger decoupling capacitor values can be placed further away.
- Place external capacitors close to the CAP_x and LFX pins.
- Preferably use multiple vias to connect wide supply traces to the respective power islands or planes.
- Use at least 7x7 through-hole via pattern to connect the IC ground/thermal pad to the PCB ground planes.

12.2 Layout Example

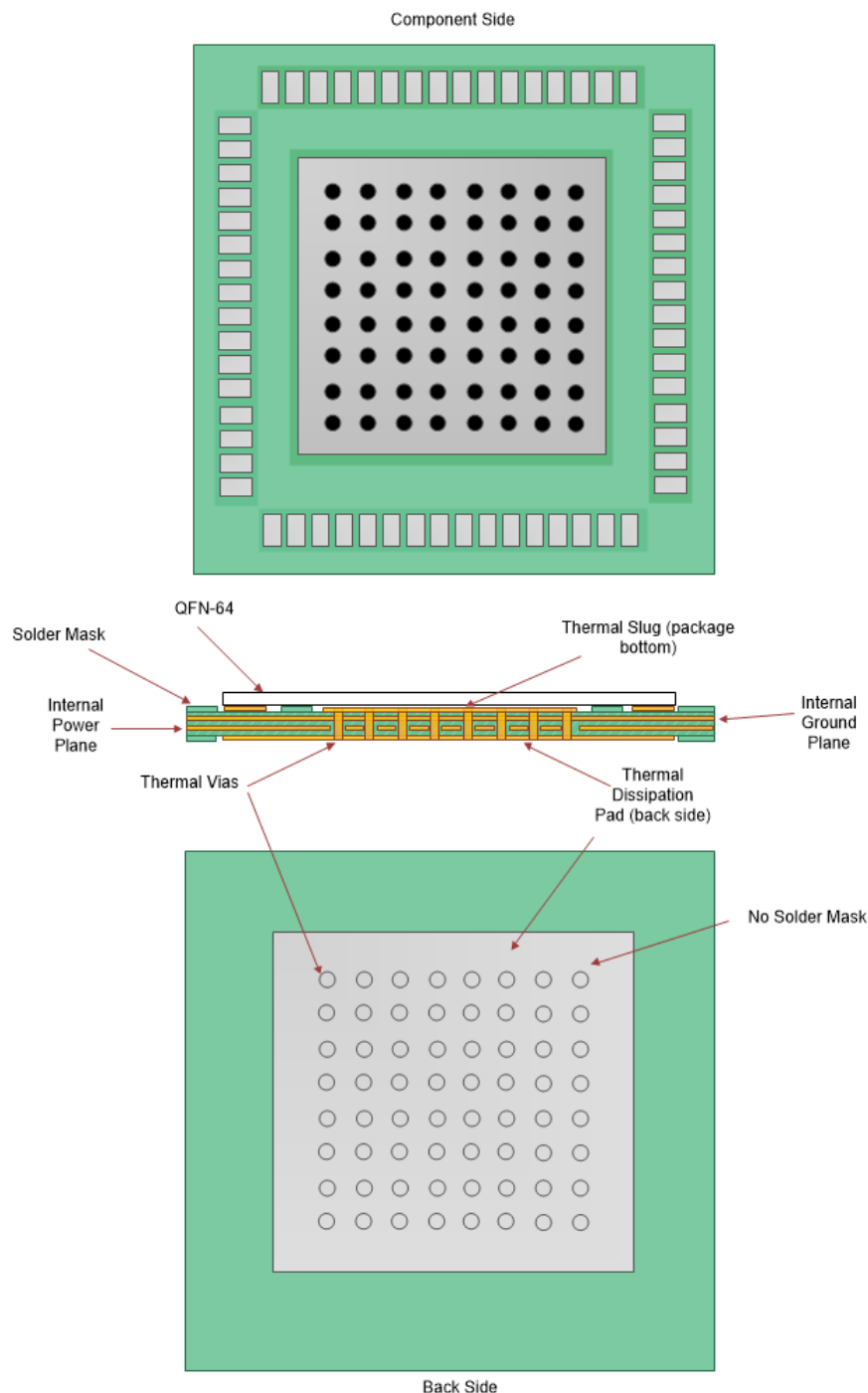


Figure 47. Recommended PCB Layout of LMK05028

12.3 Thermal Reliability

The LMK05028 is a high-performance device. To ensure good electrical and thermal performance, it is recommended to design a thermally-enhanced interface between the IC ground/thermal pad and the PCB ground using at least 7x7 through-hole via pattern connected to multiple PCB ground layers like shown in [Figure 47](#).

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

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13.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK05028RGCR	PREVIEW	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	K5028	
LMK05028RGCRN1	PREVIEW	VQFN	RGC	64	2500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	K5028N1	
LMK05028RGCT	PREVIEW	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	K5028	
LMK05028RGCTN1	PREVIEW	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	K5028N1	
P1LMK05028RGCT	ACTIVE	VQFN	RGC	64	250	TBD	Call TI	Call TI	-40 to 85	P1K5028	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

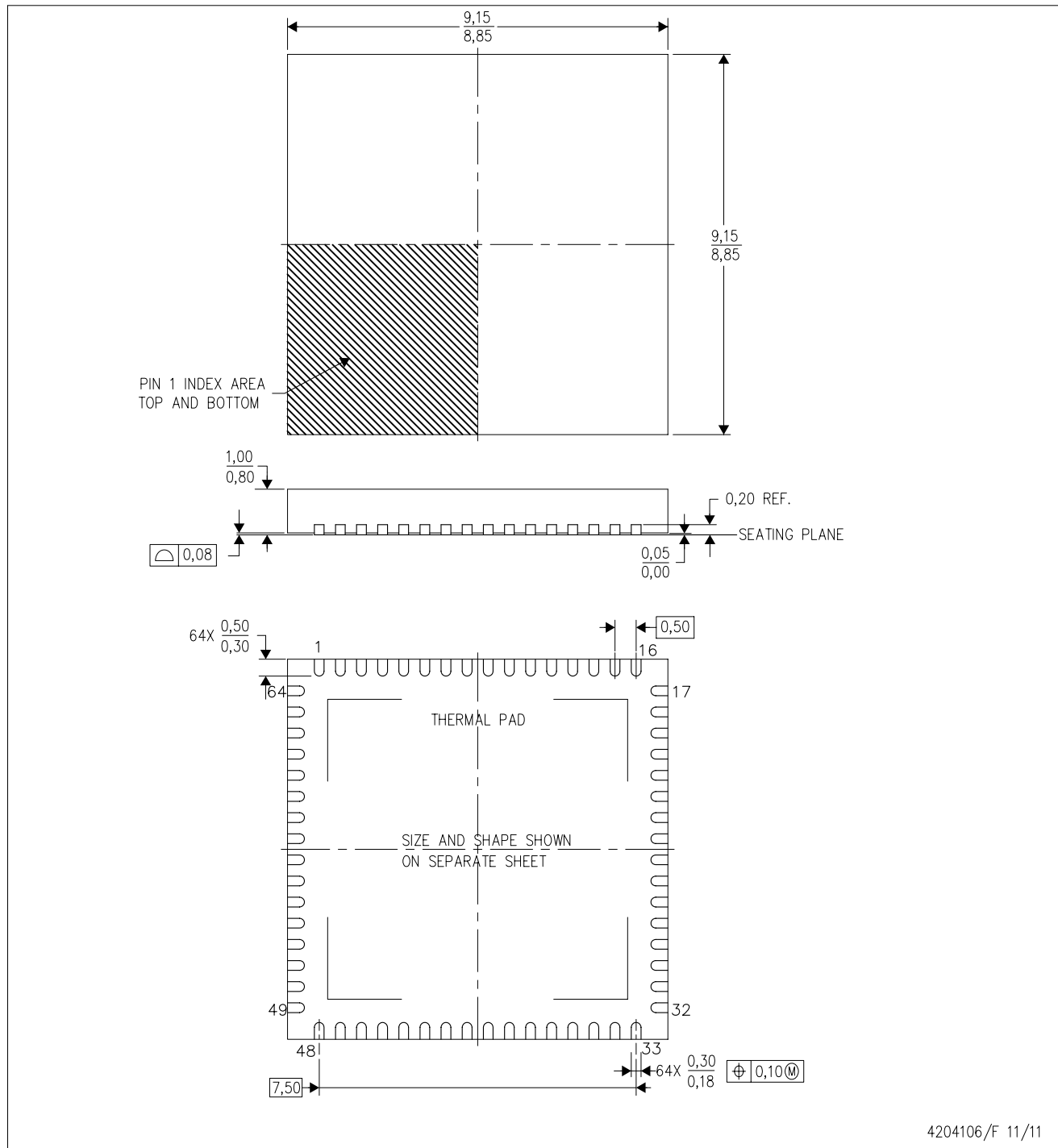
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



4204106/F 11/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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