Ordering number : ENN5841

Monolithic Linear IC

LA7615

Single-Chip NTSC Color TV IC

Overview

The LA7615 is an NTSC color TV IC that supports computer control over an I²C bus. In addition to improved quality and increased functionality in color TV products, this IC supports the development of a TV set product line in software and the simplification of end product design. The provision of an I²C bus means that this product can also respond to desires for increased total manufacturing productivity, including improved automation of computer controlled production lines.

Functions

- I²C bus control, VIF, SIF, Y, C, and deflection circuits integrated on a single chip.

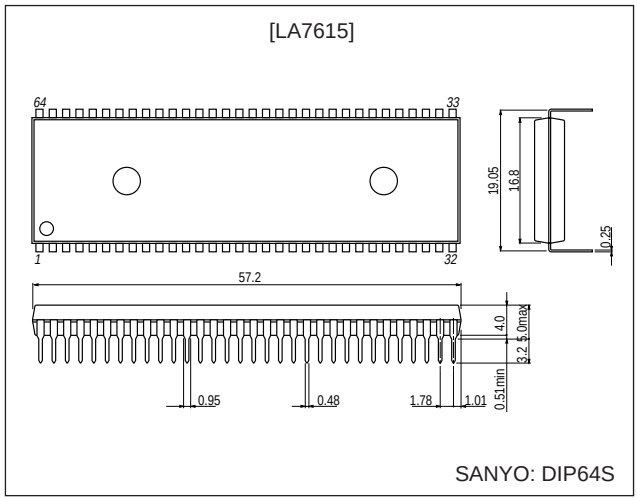
Features

- Pursuit of higher integration levels
  The LA7615 integrates VIF, SIF, luminance, chrominance, and deflection (horizontal and vertical synchronization) circuits, A/V switching, and power supply control on a single chip.
- Bus control for reduced external component counts and mechanical adjustment points
  All the LA7615 signal-processing circuits can be controlled and adjusted digitally over the I²C bus. All adjustments, both those required during manufacture and the user controls, can be controlled over the I²C bus, and both function selection and characteristics settings can be performed in software over the I²C bus. This increases flexibility in designing a product line of TV sets and also enhances productivity by allowing mixed production runs.
  While this device supports multifunction and good performance, it is also economical in that it achieves reduced power and reduced pin count.

Package Dimensions

unit: mm

3071-DIP64S



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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V2 max		9.6	V
	V17 max		9.6	V
	V32 max		9.6	V
	V60 max		9.6	V
Maximum supply current	I24 max		30	mA
Allowable power dissipation	Pd max	Ta ≤ 65°C	1.5	W
Operating temperature	Topr		–10 to +65	°C
Storage temperature	Tstg		–55 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V2		7.6	V
	V17		7.6	V
	V32		7.6	V
	V60		7.6	V
Recommended supply current	I24		24	mA
Operating supply voltage range	V2 op		7.3 to 7.9	V
	V17 op		7.3 to 7.9	V
	V32 op		7.3 to 7.9	V
	V60 op		7.3 to 7.9	V
Operating supply current range	I24 op		20 to 30	mA

Functional Description

<VIF/SIF Functions>

In addition to a PLL synchronous detection system, the IF block also adopts a split system in which the VIF signal and the SIF signal are processed separately.

- Low-level VCO
  The LA7615 achieves a significant reduction in beat generation due to interference by lowering the VCO oscillator level from that used in earlier ICs.
- Adjustment-free VCO coil implemented using bus control
  By compensating for manufacturing variations in the VCO coil using bus control, the LA7615 eliminates coil adjustment from the manufacturing line.
- Built-in 4.5 MHz trap
  The LA7615 incorporates an on-chip trap that also provides a video equalizer function. Thus the number of external trap, inductor, and capacitor components is reduced.
- Built-in SIF FM detector: 4.5 MHz quadrature detection
- The video signal and FM demodulated signal levels can be controlled from the serial bus.
  The improved precision associated with controlling the output level over the serial bus makes it easier to design the interface with the following stage.
- Built-in buzz canceler
  Allows high performance to be maintained even during stereo reception.
- Built-in video switch (INT/EXT(AUX) switching circuit)
  Built-in AUX input switching circuit means that the dedicated switching ICs required can be reduced. Also, the ability to control this switch from the serial bus makes it easier to design the peripheral wiring pattern.
- Dedicated IF video signal output pin
  The provision of this pin makes it easier to design end products that support PIP and similar features.

<Luminance and Chrominance Circuits>

These blocks have been designed to minimize the use of external components as much as possible. The filter circuits are now integrated on the same chip, and not only the adjustment circuits, but also the function selection and characteristics modifications functions can be controlled over the serial bus. As a result, basically all the signal processing from input to output can be performed with only the addition of the chrominance circuit VCO crystal and the APC filter circuit.

Furthermore, this IC also supports high image quality systems and responds to needs from a diverse range of end products.

- Two independent inputs for the luminance and chrominance signals and switching between the Y1/C1 and Y2/C2 inputs
- Video muting on/off switch
- Built-in filters (The filter f0 adjustment function can be used to select the filter characteristics.)
  Chrominance system: Bandpass filter (symmetric and asymmetric types)
  Luminance system: Color trap and delay line

<f0 Mode Selection>

Mode f0 =	Y signal		Chroma signal	
	Trap f0	*Total delay	BPF	*Total 500 ns delay
0	3.58 MHz	500 ns	Asymmetric (peaking type)	515 ns
1	4.2 MHz	510 ns	Symmetric	535 ns
2	5.0 MHz	520 ns		
3	10.0 MHz	265 ns	Bypass	265 ns

*: Reference values

<Luminance System Circuit>

- Built-in high image quality variable-type luminance system filter (color trap and delay line)
  Luminance filter mode selection (f0 adjustment)
  Four modes are provided: 3.58 MHz trap, 4.2 MHz trap, 5.0 MHz wide, and 10.0 MHz high band.
- Peaking (sharpness) control
  Aperture type control implemented using the delay line
  The emphasis frequency is automatically selected according to the f0 mode using the delay line.
  One of the four frequencies 2.2, 2.6, 3.0, or 4.9 MHz is emphasized according to which of the f0 modes (3.58 MHz trap, 4.2 MHz trap, 5.0 MHz wide, or 10.0 MHz high band) is used.
- Adaptive coring
  For low-level signals, the above peaking is suppressed to reduce the image contamination due to that peaking.
  The coring level is automatically adjusted according to the amplitude of the input signal.
- Black stretch circuit: Can be turned on or off under control of the serial bus interface.
- SYO (Selected luminance (Y) output)
  One of the Y1/Y2 inputs is selected, and that input signal is output as the sync separator circuit signal directly. However, the DC level of that signal is clamped at 1/2 VCC.
  Also, this signal can be used for closed captions or as a velocity modulation.
- Support for analog/digital OSD
  Amplitude level limiting is applied to digital input signals internally to the IC.
- Contrast and brightness controls
- ABL (automatic beam limiter)
  Three-pin system (IB IN, BRT ABL FILT, and CONTRAST ABL FILT pins), mode switching under control of serial bus data.
- R, G, and B output drive and bias adjustments
- Sub-bias (brightness) control
  The DC level of each of the R, G, and B signals can be adjusted over a 4-step (2-bit) range.

<Chrominance Circuit>

- Built-in chrominance bandpass filter
  Chrominance system filter mode selection: bandpass filter peaking/symmetric type selection and chrominance bandpass filter bypass on/off setting
- Auto Flesh: Flesh tone correction (on/off)
- Overload (on/off)
  Limits the saturation of the color when the ratio of the burst and color signals is large, i.e. when the color is highly saturated.
- Color phase and saturation controls
- Demodulation angle: 104°

<Deflection Circuits>
Dedicated sync separator circuit input pin
The horizontal deflection circuit adopts a dual AFC circuit, and the horizontal oscillator uses the 32fH (503 kHz) pulse signal as the horizontal decrement counter clock.
The following are the main settings for the horizontal output system that can be controlled over the serial bus interface. These settings support even more efficient end product design.
- AFC gain (first loop gain control)
- APC gain (second loop gain control)
- Horizontal duty cycle
- Horizontal phase

*: The vertical deflection circuit adopts a decrement counter system, and provides constantly adjustment-free and stable vertical synchronization for any type of signal, from TV on air, to weak reception conditions, to VCR signals. Furthermore, this circuit uses an internal capacitor to implement a ramp generator, and allows the corrections described later in this document to be applied to correct image distortion and other problems due to manufacturing variations in the TV tube itself.

<Horizontal Circuit Functions>
- High-stability adjustment-free horizontal oscillator that uses a ceramic oscillator element
- Dual AFC circuit
- Multi-mode control of the AFC gain (first loop gain)
- Horizontal duty and phase controls
- Geometrical distortion correction: East-west DC (horizontal size)
  - East-west amplitude (horizontal pin-cushion distortion correction)
  - Corner pin
    - East-west corner 1
    - East-west corner 2
  - Tilt adjustment
- Sync killer

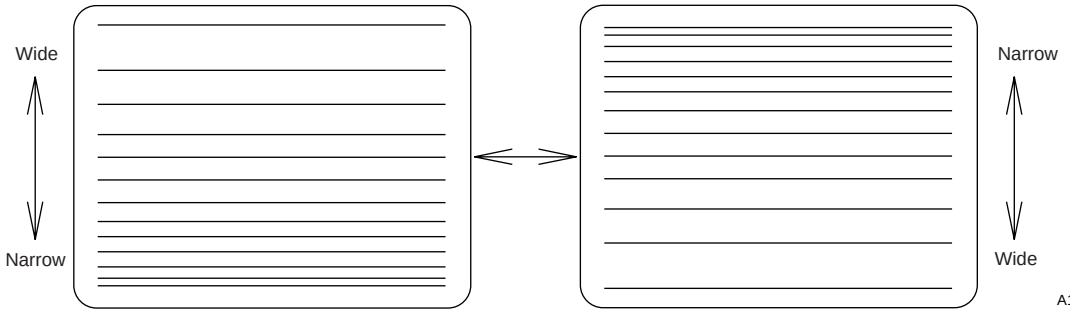
<Vertical Circuit Functions>
- Forcible non-standard mode support (standard mode: 262.5 H)
- Vertical size/linearity and vertical DC (vertical position) adjustments, vertical S-curve correction
- V-comp adjustment (Corrects for changes in the vertical size due to variations in the luminance.)
- Vertical killer

<Power System>
PWM circuits have come to be widely used in TV set power supplies in recent years. This IC integrates parts of the power supply circuit (the pulse generator and its control system) and allows the supply voltage (high B) to be adjusted over the serial bus.

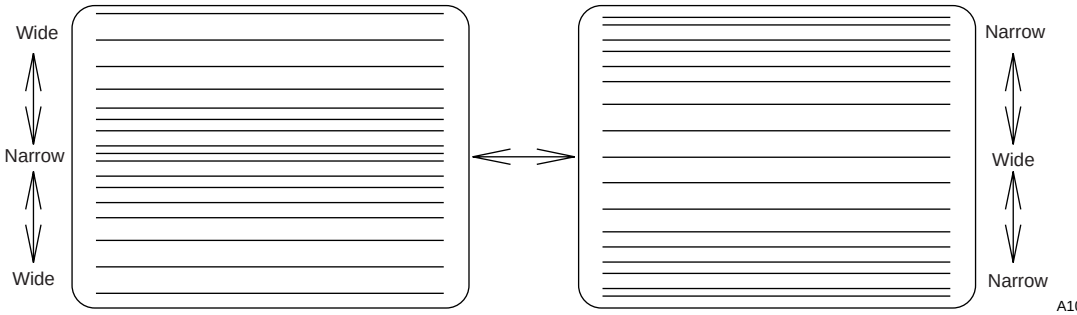
Bus Control

General Functions	
ON/OFF SW	1 bit
Video muting switch	1 bit
VIF/SIF	
Video signal switching	1 bit
RF AGC delay	6 bits
IF AGC SW	1 bit
PLL tuning	7 bits
APC detector adjustment	6 bits
AFT defeat switch	1 bit
Noise inverter defeat switch	1 bit
Video level	3 bits
Sound 4.5 MHz trap	4 bits
FM level	4 bits
F0 fast (FM detection speed)	1 bit
Luminance/Chrominance Systems	
Y/C input selection (one of two inputs) switch	1 bit
Luminance (Y) F0 adjustment (filter control)	2 bits
Chrominance signal bandpass filter mode switch	1 bit
Chrominance signal bandpass filter bypass switch	1 bit
Black stretch on/off switch	1 bit
Peaking (sharpness) control	5 bits
Coring on/off switch	1 bit
Auro flesh on/off	1 bit
Overload switch	1 bit
Contrast control	6 bits
Brightness control	6 bits
Tint control	7 bits
Saturation control	7 bits
RGB bias adjustment	6 bits each
RGB bias adjustment	7 bits each
Sub-brightness control	2 bits each
Brightness ABL operating point control	3 bits
Brightness ABL mode defeat switch	1 bit each
Emergency ABL defeat switch	1 bit
Deflection System	
AFC gain (sync killer)	2 bits
APC gain	2 bits
Horizontal duty adjustment	2 bits
Horizontal phase adjustment	4 bits
Geometrical distortion correction	
EAST-WEST DC	5 bits
EAST-WEST AMPLITUDE	4 bits
East-west corner 1/2	3 bits each
Tilt adjustment	4 bits
Vertical linearity adjustment	4 bits
Vertical S-curve correction	4 bits
Vertical size adjustment	7 bits
Vertical DC adjustment	6 bits
Standard/nonstandard mode switch	1 bit
VERTICAL KILL	1 bit
V-COMP adjustment	3 bits
DAC REF. (+B TRIM)	4 bits
Others: Status Register	
POWER ON RESET	1 bit
X-ray protection switch	1 bit
Horizontal lock detection	1 bit
AFT and RF AGC status discrimination	2 bits each

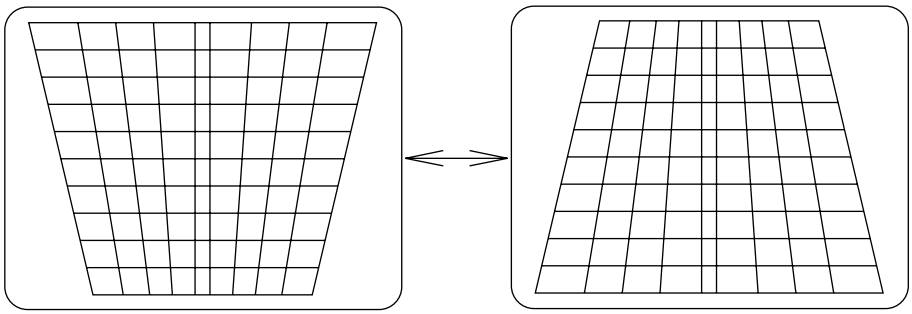
Vertical Linearity



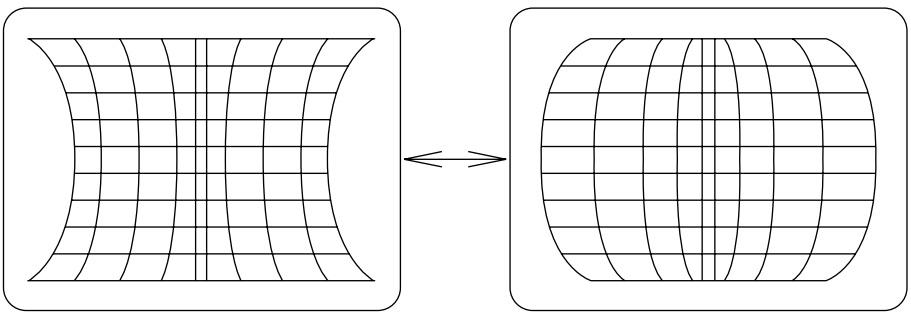
Vertical S-Curve Correction



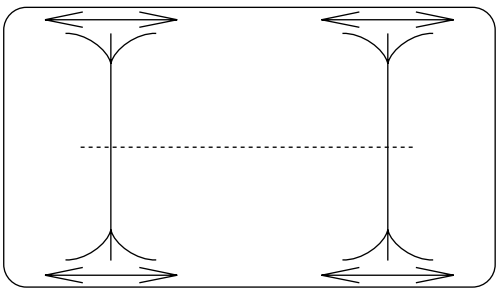
Tilt



East-West Amp



Corner Pin



The distortion correction operation is symmetric left to right.

Bus : Control Register Bit Allocation Map

Control Register Bit Allocations

IC address		Sub address		MSB	Data bits						LSB
IC Add7 → Add0		¥ Add7 → Add0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1011	1010	0000	0000	1			On/Off		Video mute	AFC gain/sync kill (b1)	(b0)
			0001	1		APC gain (b1)	(b0)	B+ trim (b3)	(b2)	(b1)	(b0)
			0010	1		Hor duty cycle (b1)	(b0)	Horizontal phase (b3)	(b2)	(b1)	(b0)
			0011	1	BNI defeat	RF AGC delay (b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			0100	1	IF AGC defeat	AFT defeat	FM level (b4)	(b3)	(b2)	(b1)	(b0)
			0101	1	VCO free running (b6)	(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			0110	1	4.5 MHz trap (b3)	(b2)	(b1)	(b0)	(b2)	(b1)	(b0)
			0111	1	Video switch	IF APC offset adjust. (b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			1000	1	Vertical kill	Vertical DC (b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			1001	1	Countdown mode (b1)	(b0)	East-west DC (b4)	(b3)	(b2)	(b1)	(b0)
			1010	1				East-west amp (b3)	(b2)	(b1)	(b0)
			1011	1	Vertical comp. (b2)	(b1)	(b0)	East-west tilt (b3)	(b2)	(b1)	(b0)
			1100	1	Vertical size (b6)	(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			1101	1				Vertical linearity (b3)	(b2)	(b1)	(b0)
			1110	1			FM mode switch	Vertical S-correction (b3)	(b2)	(b1)	(b0)
			1111	1		East-west bottom corner (b2)	(b1)	(b0)	East-west top corner (b2)	(b1)	(b0)

Bits are transmitted in this order ➔

Bus : Control Register Bit Allocation Map

Control Register Bit Allocations (cont)

IC address		Sub address		MSB	Data bits						LSB
IC Add7 → 0		Add7 → Add0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1011	1010	0001	0000	1	Red bias						
					(b6)	(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			0001	1	Green bias						
					(b6)	(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			0010	1	Blue bias						
					(b6)	(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			0011	1		Red drive					
						(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			0100	1		Green drive					
						(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			0101	1		Blue drive					
						(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			0110	1	Blue sub bias		Red sub bias		Green sub bias		Y/C
					(b1)	(b0)	(b1)	(b0)	(b1)	(b0)	switch
			0111	1		Brightness control					
						(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			1000	1		Pix control					
						(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			1001	1		Coring	Peaking control				
						switch	(b4)	(b3)	(b2)	(b1)	(b0)
			1010	1		F0 select		Chroma	Auto	Chrom	Over
						(b1)	(b0)	BPF	flesh	bypass	load
			1011	1	Tint control						
					(b6)	(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			1100	1	Color control						
					(b6)	(b5)	(b4)	(b3)	(b2)	(b1)	(b0)
			1101	1		ABL	Mid Stp	EMG	Bright ABL threshold		
						defeat	defeat	defeat	(b2)	(b1)	(b0)
			1110	1	Test register 1				Test register 2		
					(b3)	(b2)	(b1)	(b0)	(b2)	(b1)	(b0)
			1111	1	Test regster 3				Black Stretch	Blanking	Reserved
					(b3)	(b2)	(b1)	(b0)	defeat	defeat	

Bits are transmitted in this order →

Table 8 : Status Register Bit Allocation Map

Status Register Bit Allocations

IC address		Sub address		MSB	Data bits						LSB
IC Add7 → Add0		Add7 → Add0		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1011	1010	0001	0000	Pon	XRay	Horiz lock	On/off	AFT status		RF AGC status	
			0001	1	1	1	1	1	1	1	1

Bus : Control Register Truth Table

Control Register Truth Table

Register	0 HEX	1 HEX	2 HEX	3 HEX
On/off	Off	On	na	na
Video mute	Active	Mute	na	na
AFC gain/sync Kill	Sync Kill	Low gain (auto mode)	Mid gain	High gain
BNI defeat	Enable BNI	Defeat	na	na
IF AGC defeat	Enable AGC	Defeat	na	na
AFT defeat	Enable AFT	Defeat	na	na
Video switch	IF video	Aux video	na	na
Vertical Kill	Vertical active	Vertical Killed	na	na
Countdown mode	Standard	Non-standard	50 Hz	48 Hz
FM mode switch	Normal	Fast	na	na
Y/C switch	Y1/C1 IN	Y2/C2 IN	na	na
Coring switch	Defeat	Enable	na	na
F0 select	3.58 Trap	4.20 Trap	5.00 APF	10.0 APF
Chrom BPF	Symmetrical	Peaker	na	na
Autoflesh	Off	On	na	na
Chroma bypass	BPF	Bypass	na	na
Over load	Off	Active	na	na
Bright ABL defeat	Enable	Defeat	na	na
Bright mid stop defeat	Enable	Defeat	na	na
Emergency ABL defeat	Enable	Defeat	na	na
Black Str defeat	Enable	Defeat	na	na
Blanking defeat	Enable	Defeat	na	na

Bus : Status Register Truth Table

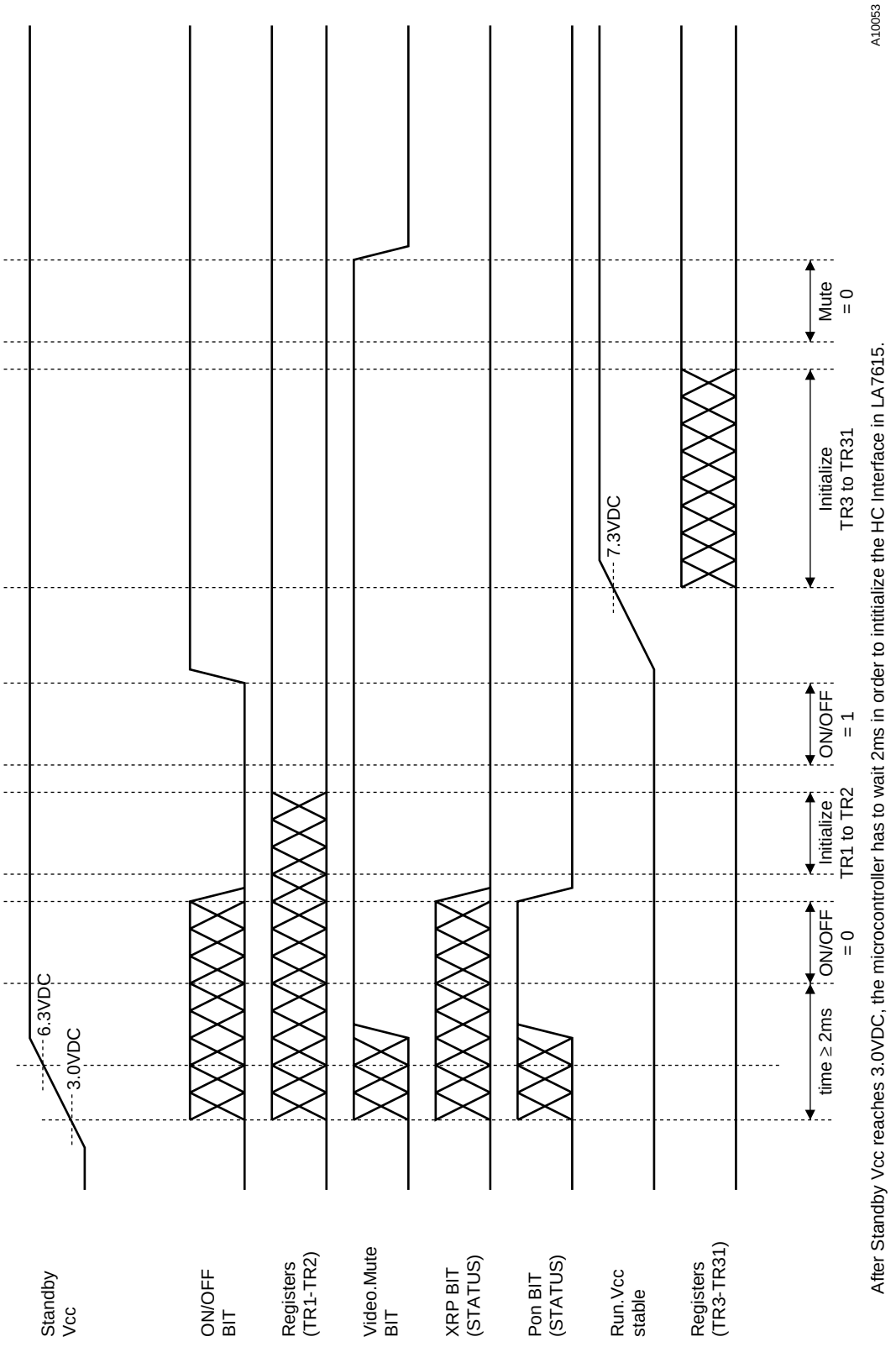
Status Register Truth Table

Register	0 HEX	1 HEX	2 HEX	3 HEX
POR	Inactive	Low standby detected	na	na
XRP	Inactive	XRP fault detected	na	na
Horizontal lock	Locked	Unlocked	na	na
On/off	Off	On	na	na
AFT	IF frequency in high	IF frequency in range	na	IF frequency is low
RF AGC	RF AGC voltage is Low.	RF AGC voltage is in range.	na	RF AGC voltage is High.

Initial Condition

Function	
On/off	1 HEX
Video mute	0 HEX
AFC gain & sync Kill	1 HEX
APC gain	3 HEX
B+ trim	8 HEX
Horizontal duty	1 HEX
Horizontal phase	8 HEX
BNI defeat	0 HEX
RF AGC delay	20 HEX
IF AGC defeat	0 HEX
AFT defeat	0 HEX
FM level	10 HEX
IF VCO free running	40 HEX
4.5 trap	8 HEX
Video level	4 HEX
Video switch	0 HEX
IF APC offset	20 HEX
Vertical Kill	0 HEX
Vertical DC	20 HEX
Countdown mode	0 HEX
East/west DC	10 HEX
East/west amplitude	8 HEX
Vertical comp.	0 HEX
East/west tilt	8 HEX
Vertical size	40 HEX
Vertical linearity	8 HEX
FM mode switch	0 HEX
Vertical S-correction	8 HEX
East/west bottom	0 HEX
East/west top corner	0 HEX
Red bias	00 HEX
Green bias	00 HEX
Blue bias	00 HEX
Red drive	3F HEX
Green drive	3F HEX
Blue drive	3F HEX
Blue sub bias	2 HEX
Red sub bias1	2 HEX
Green sub bias	2 HEX
Y/C switch	0 HEX
Brightness control	20 HEX
Pix control	20 HEX
Coring switch	0 HEX
Peaking control	00 HEX
F0 select	1 HEX
Chroma BPF	0 HEX
Autoflesh	0 HEX
Chroma bypass	0 HEX
Over load	0 HEX
Tint control	40 HEX
Color control	40 HEX
Bright ABL defeat	0 HEX
Bright mid stop	0 HEX
Emergency ABL defeat	0 HEX
Bright ABL threshold	0 HEX
Test registers 1, 2, 3	0 HEX
Black strech defeat	1 HEX
Blanking defeat	0 HEX

Power Up Sequence <Reference>



After Standby Vcc reaches 3.0VDC, the microcontroller has to wait 2ms in order to intitialize the HC Interface in LA7615.

Electrical Characteristics at Ta = 25°C, V_{CC} = V2 = V17 = V32 = V60 = 7.6 V, I_{CC} = I24 = 24 mA

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Circuit Voltages and Currents]						
Horizontal supply voltage	HV_{CC}		7.2	7.6	8	V
IF power supplly current (V2)	I2 (IFI_{CC})	IF AGC : 5 V	28	43	58	mA
Vertical supply current (V17)	I17 ($DEFI_{CC}$)		10	13	16	mA
Video/chrominance supply current (V32)	I32 (YCI_{CC})		65	85	105	mA
FM supply current (V60)	I60 (FMI_{CC})		5.5	8.5	11.5	mA
[VIF Block]						
No signal AFT output voltage	V14	With no input signal	2.8	3.8	4.8	Vdc
No signal video output voltage	V53	With no input signal	4.7	4.9	5.1	Vdc
APC pull-in range (U)	f_{PU}	After APC, PLL, and D/A converter adjustment	1			MHz
APC pull-in range (L)	f_{PL}	After APC, PLL, and D/A converter adjustment	1			MHz
Maximum RF AGC voltage	V_{4H}	CW = 91 dBμ, DAC = 0	7.7	8.2	9.0	Vdc
Minimum RF AGC voltage	V_{4L}	CW = 91 dBμ, DAC = 63	0	0.2	0.4	Vdc
RF AGC Delay Pt (@DAC = 0)	RF_{AGC0}	DAC = 0	96			dBμ
RF AGC Delay Pt (@DAC = 63)	RF_{AGC63}	DAC = 63			86	dBμ
Maximum AFT output voltage	V_{14H}	CW = 93 dBμ, frequency change	6.2	6.5	7.6	Vdc
Minimum AFT output voltage	V_{14L}	CW = 93 dBμ, frequency change	0.5	0.9	1.2	Vdc
AFT detection sensitivity	Sf	CW = 93 dBμ, frequency change	33	25	17	mV/kHz
4.5 MHz attenuation	T_{RAP}	V100 kHz/V4.5 MHz		–35	–32	dB
Video output amplitude	V_O53	93 dBμ, 87.5% Video MOD	1.8	2	2.2	Vp-p
Synchronizing signal tip level	$V53_{TIP}$	93 dBμ, 87.5% Video MOD	2.4	2.6	2.8	Vdc
Input sensitivity	V_{IN}	Output –3 dB		43	46	dBμ
Vide/sync ratio (@100 dBμ)	V/S	100 dBμ, 87.5% Video MOD	2.4	2.5	3	
Differential gain	DG	93 dBμ, 87.5% Video MOD		2	10	%
Differential phase	DP	93 dBμ, 87.5% Video MOD		2	10	deg
Video signal-to-noise ratio	S/N	CW = 93 dBμ	55	58		dB
920 kHz beat level	I920	V3.58 MHz/V920 kHz		–57	–50	dB
[SIF Block]						
[1st.SIF]						
4.5 MHz conversion gain	SG_G		21	26	31	dB
4.5 MHz output level	SV_O		91	96	101	dB
First SIF maximum input	SV_M		–1	0	+1	dB
[SIF Block]						
FM detection output voltage	S_{OADJ}		414	424	434	mVrms
FM limiting sensitivity	S_{LS}				50	dBμ
FM detector output bandwidth	S_F		50		100k	Hz
FM detector output distortion	S_{THD}				1	%
AM rejection ratio	S_{AMR}		40			dB
SIF. Signal-to-noise ratio	S_{SN}		74			dB
[Chrominance Block]						
ACC amplitude characteristics 1	ACC_M1	Input: +6 dB/0 dB, 0 dB = 40 IRE	0.8	1.0	1.2	times
ACC amplitude characteristics 2	ACC_M2	Input: –14 dB/0 dB	0.8	1.0	1.1	times
B-Y/Y amplitude ratio	CLR_{BY}		75	100	120	%
Color control characteristics 1	CLR_{MN}	Color: max/normal	1.7	2.0	2.3	times
Color control characteristics 2	CLR_{MN}	Color: max/min	33	40	50	dB
Color control sensitivity	CLR_{SE}		1	2	4	%/bit
Tint center	TIN_{CEN}	TINT NOM	–10		+5	deg
Tint control max	TIN_{MAX}	TINT max	30	45	60	deg
Tint control min	TIN_{MIN}	TINT min	–60	–45	–30	deg
Tint control sensitivity	TIN_{SE}		0.7		2.0	deg/bit
Demodulated output ratio: B-Y/R-Y	BR		1.06	1.19	1.32	
Demodulated output ratio: G-Y/R-Y	GR		0.34	0.40	0.46	

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Demodulation angle B-Y/R-Y	AN_{GBR}		99	104	109	deg
Demodulation angle G-Y/R-Y	ANGGR		–146	–136	–127	deg
Killer operating point	KILL	0 dB = 40IRE	–32	–26	–22	dB
Chrominance V_{CO} free-running frequency	$CV_{CO}F$	Deviation from 3.579545 MHz	–250		+250	Hz
Chrominance pull-in range (+)	PUL_{IN+}		350			Hz
Chrominance pull-in range (–)	PUL_{IN-}				–350	Hz
Auto Flesh characteristics: 73°	AF_{073}		8	20	30	deg
Auto Flesh characteristics: 118°	AF_{118}		–7	0	+7	deg
Auto Flesh characteristics: 163°	AF_{163}		–30	–20	–8	deg
Overload characteristics 1	OVL1		3.2		4.7	
Overload characteristics 2	OVL2		4.2		6.8	
Overload characteristics 3	OVL3		4.5		8.5	
[Chrominance Bandpass Filter Block]						
Peaking amplitude characteristics: 3.08 MHz	C_{PE308}	Referenced to 3.48 MHz	–5	–3	–1	dB
Peaking amplitude characteristics: 3.88/3.28 MHz	C_{PE}	Referenced to 3.28 MHz	–0.5	+1.5	+3.5	dB
Peaking amplitude characteristics: 4.08/3.08 MHz	C_{PE05}	Referenced to 3.08 MHz	–5.0	2.5	–1	dB
Bandpass amplitude characteristics: 3.08 MHz	C_{BP308}	Referenced to 3.48 MHz	–5	–3	–1	dB
Bandpass amplitude characteristics: 3.88/3.28 MHz	C_{BP}	Referenced to 3.28 MHz	–2	0	+2	dB
Bandpass amplitude characteristics: 4.08/3.08 MHz	C_{BP05}	Referenced to 3.08 MHz	–2.5	0	+2.5	dB
[Video Block]						
Video overall gain (at maximum contrast)	CONT63		10	12	14	dB
Contrast adjustment characteristics (normal/max)	CONT32		–7.5	–6.0	–4.5	dB
Contrast adjustment characteristics (min/max)	CONT0		–15	–12	–9	dB
Video frequency characteristics: f0 = 3	Y_{f03}		–6.0	–3.5	0.0	dB
Chrominance trap level: f0 = 0	C_{trap}			–23	–15	dB
DC restoration	C_{lampG}		95	100	105	%
Luminance delay: f0 = 1	Y_{DLY}		480	505	530	ns
Maximum black stretch gain	BKSTmax		12	16	20	IRE
Black stretch threshold (40 IRE Δblack)	$BKST_{TH}$		–2	0	+2	IRE
Sharpness variation range (normal)	Sharp16		4	6	8	dB
(max)	Shaprp31		9.0	11.5	14.0	dB
(min)	Shapr0		–6.0	–3.5	–1.0	dB
Horizontal/vertical blanking output level	RGB_{BLK}		1.4	1.7	2.0	V
[OSD Block]						
OSD fast switch threshold	FS_{TH}		1.7	1.9	2.2	V
RGB output level: red	R_{OSDH}		120	165	200	IRE
RGB output level: green	G_{OSDH}		70	120	140	IRE
RGB output level: blue	B_{OSDH}		85	120	155	IRE
Analog OSD output level	R_{RGB}		1.12	1.4	1.68	Ratio
Gain matching Linearity	LR_{RGB}		45	50	60	%

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Analog OSD green output level	G_{RGB}		0.8	1.0	1.2	Ratio
Gain matching Linearity	LG_{RGB}		45	50	60	%
Analog OSD blue output level	B_{RGB}		0.8	1.0	1.2	Ratio
Gain matching Linearity	LB_{RGB}		45	50	60	%
[RGB Output (cutoff and drive) Block]						
Brightness control (normal)	BRT32		2.0	2.35	2.7	V
High brightness (max)	BRT63		15	20	25	IRE
Low brightness (min)	BRT60		–25	–20	–5	IRE
Cutoff control (min)	Vbias0		1.6	2.0	2.4	V
(bias control) (max)	Vbias128		2.8	3.2	3.6	V
Cutoff contrad Resolution	Vbiassns		3	4	6	mV/bit
Sub-bias control resolution	Vsbiassns		160	220	280	mV/bit
Drive adjustment: maximum output	RGBout63		2.4	3.0	3.6	Vp-p
Output attenuation	RGBout0		7	9	11	dB
[Deflection Block]						
Sync separator circuit sensitivity	S_{sync}			10	15	IRE
Horizontal free-running frequency deviation	Δf_H		15.634	15.734	15.834	kHz
Horizontal pull-in range	$f_{H\ PULL}$		±400			Hz
Horizontal output pulse width @0	Hduty0	ON time, Hduty : 0	36.0	37.5	39.0	µs
Horizontal output pulse width @1	Hduty1	ON time, Hduty : 1	34.3	35.8	37.5	µs
Horizontal output pulse width @2	Hduty2	ON time, Hduty : 2	32.5	34.0	35.5	µs
Horizontal output pulse width @3	Hduty3	ON time, Hduty : 3	30.5	32.0	33.5	µs
Horizontal output pulse saturation voltage	$V_H$sat				0.4	V
Horizontal output pulse phase	HPH_{CEN}		9.5	10.5	11.5	µs
Horizontal position adjustment range	HPHrange	4 bits		±2		µs
Horizontal position adjustment maximum variation	HPHstep				350	ns
X-ray protection circuit operating voltage	V_{XRAY}		2.7	3.0	3.3	V
POR circuit operating voltage	V_{POR}		5.5	6.3	6.7	V
[Vertical Screen Size Adjustment]						
Vertical ramp output amplitude @64	Vsize64	V_{SIZE} : 1000000	1.44	1.74	2.04	Vp-p
Vertical ramp output amplitude @0	Vsize0	V_{SIZE} : 0000000	0.72	1.02	1.32	Vp-p
Vertical ramp output amplitude @127	Vsize127	V_{SIZE} : 1111111	2.14	2.44	2.64	Vp-p
[High Voltage Dependency Vertical Size Correction]						
Vertical size correction @3	Vsizecomp	V_{COMP} : 11	0.96	0.97	0.98	ratio
[Vertical Screen Position Adjustment]						
Vertical ramp DC voltage @32	Vdc32	V_{DC} : 1000000	3.686	3.876	4.484	Vdc
Vertical ramp DC voltage @0	Vdc0	V_{DC} : 0000000	3.344	3.557	3.762	Vdc
Vertical ramp DC voltage @63	Vdc63	V_{DC} : 1111111	4.104	4.294	4.484	Vdc
Vertical linearity @8	Vlin8	V_{LIN} : 1000	0.93	0.985	1.04	ratio
Vertical linearity @0	Vlin0	V_{LIN} : 0000	0.77	0.84	0.92	ratio
Vertical linearity @15	Vlin15	V_{LIN} : 1111	1.13	1.18	1.25	ratio
Vertical S-curve correction @8	VScor8	V_S : 1000	0.77	0.84	0.92	ratio
Vertical S-curve correction @0	VScor0	V_S : 0000	0.92	1.00	1.08	ratio
Vertical S-curve correction @15	VScor15	V_S : 1111	0.62	0.72	0.78	ratio

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Horizontal Size Adjustment]						
East/west DC voltage @16	EWdc16	EW_{DC} : 10000	3.60	4.00	4.40	Vdc
East/west DC voltage @0	EWdc0	EW_{DC} : 00000	2.70	3.05	3.40	Vdc
East/west DC voltage @31	EWdc31	EW_{DC} : 11111	4.80	5.10	5.40	Vdc
[Pin cushion Distortion Correction]						
East/west parabola amplitude @8	EWamp8	EW_{AMP} : 1000	0.58	0.73	0.88	Vp-p
East/west parabola amplitude @0	EWamp0	EW_{AMP} : 0000	0.15	0.30	0.45	Vp-p
East/west parabola amplitude @15	EWamp15	EW_{AMP} : 1111	0.95	1.15	1.35	Vp-p
[Trapezoidal Distortion Correction]						
East/west parabola tilt @8	EWtilt4	EW_{TILT} : 1000	–0.14	0	+0.14	V
East/west parabola tilt @0	EWtilt0	EW_{TILT} : 0000	–0.37	–0.23	–0.09	V
East/west parabola tilt @15	EWtilt7	EW_{TILT} : 1111	0.09	0.23	0.37	V
[Corner Distortion Correction]						
East/west parabola corner, top	EWcorTOP	COR_{TOP} : 111-000	0.15	0.25	0.35	V
East/west parabola corner, bottom	EWcorTOP	COR_{BOTTOM} : 111-000	0.15	0.25	0.35	V
[Sandcastle Output]						
Burst gate pulse peak value	V_{BGP}		5.0	5.7	6.5	V
Burst gate pulse phase	Td_{BGP}		4.6	5.1	5.6	µs
Burst gate pulse width	PW_{BGP}		2.35	2.85	3.35	µs
Blanking pulse peak value	V_{BLK}		3.4	3.9	4.4	V
[D/A Converter Output]						
Pin 30 D/A converter voltage @0	$V_{DAC}0$	+B TRIM : 0000	2.75	3.00	3.25	V
Pin 30 D/A converter voltage @8	$V_{DAC}8$	+B TRIM : 1000	3.15	3.40	3.65	V
Pin 30 D/A converter voltage @15	$V_{DAC}15$	+B TRIM : 1111	3.55	3.80	4.05	V

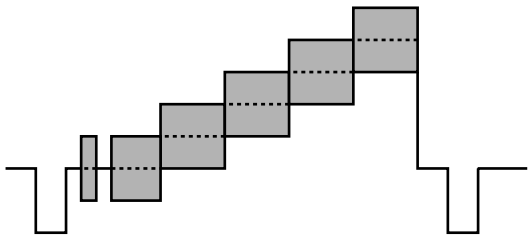
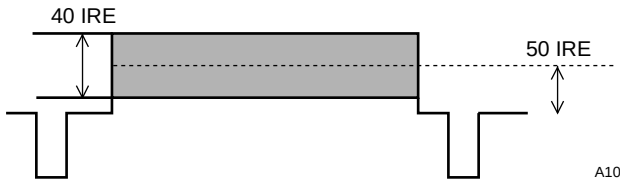
Circuit Voltage and Current Test Conditions at Ta = 25°C, $V_{CC} = V_2 = V_{17} = V_{32} = V_{60} = 7.6$ V, $I_{CC} = I_{24} = 24$ mA

Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
[Circuit Voltage and Current]					
Horizontal supply voltage	HV_{CC}	(24)		Apply a 24-mA current to pin 24 and measure the voltage on pin 24 at that time.	Initial
IF current drain (pin 2)	I_2 (IFI_{CC})	2	No signal	Apply 7.6 V to pin 2 and measure the DC current (in mA) that flows into the IC. (With 5 V applied to the IF AGC)	Initial
Vertical current drain (pin 17)	I_{17} ($DEFI_{CC}$)	17		Apply 7.6 V to pin 17 and measure the DC current (in mA) that flows into the IC.	Initial
Video, chrominance, current drain (pin 32)	I_{32} (YCV_{CC})	32		Apply 7.6 V to pin 32 and measure the DC current (in mA) that flows into the IC.	Initial
FM power supply current (pin 60)	I_{60} (FMV_{CC})	60	No signal	Apply 7.6 V to pin 60 and measure the DC current (in mA) that flows into the IC.	Initial

VIF Block - Input Signals and Test Conditions

1. All input signals are input to VIF IN in the test circuit diagram.
2. The input signal voltages are all taken to be the voltage at VIF IN in the test circuit diagram.
3. The signals and their levels are as follows.

Input signal

Input signal	Waveform	Condition
SG1		45.75 MHz
SG2		42.17 MHz
SG3		41.25 MHz
SG4		Variable frequency
SG5		45.75 MHz 87.5% video modulation 10-step waveform (subcarrier: 3.58 MHz)
SG6		45.75 MHz 87.5% video modulation Sweep signal (APL: 50 IRE, sweep signal level: 40 IRE)
SG7		45.75 MHz 87.5% video modulation Flat field signal

4. Before testing, adjust the D/A converter in the order presented below.

Parameter	Test point	Input signal	Adjustment
APC DAC	⑭	No signal, with pin 11 connected to ground	Set the pin 14 DC voltage to be as close to 3.8 V as possible.
PLL DAC	⑭	SG1, 93 dBμ	Set the pin 14 DC voltage to be as close to 3.8 V as possible.
Video level DAC	㊸	SG7, 93 dBμ	Set the pin 53 output level to be 2.0 ±0.2 Vpp.
Trap	㊸	SG6, 93 dBμ	Lower the D/A converter from its maximum (15) and set the circuit so that the 4.5 MHz component is at least –32 dB below the 100 kHz component.

(Test Conditions)

Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
[VIF Block]					
No signal AFT output voltage	V14	14	No signal	Connect the pin 11 to ground and measure the pin 14 DC voltage.	The adjusted values from item 4.
No signal video output voltage	V53	53	No signal	Connect the pin 11 to ground and measure the pin 53 DC voltage.	The adjusted values from item 4.
APC pull-in range (U), (L)	f_{PU}, f_{PL}	53	SG4 93 dBμ	Monitor pin 53 with an oscilloscope, and modify SG4 to have a frequency higher than 45.75 MHz so that the PLL goes to the unlocked state. (Beating should appear at this point.) Gradually decrease the SG4 frequency until the PLL circuit locks, and measure the lock frequency. Also, and modify SG4 to have a frequency lower than 45.75 MHz so that the PLL goes to the unlocked state. Gradually increase the SG4 frequency until the PLL circuit locks, and measure the lock frequency.	The adjusted values from item 4.
Maximum RF AGC voltage	$V4_H$	4	SG1 91 dBμ	Set the RF AGC D/A converter to 0 and measure the pin 4 DC voltage.	The adjusted values from item 4.
Minimum RF AGC voltage	$V4_L$	4	SG1 91 dBμ	Set the RF AGC D/A converter to 63 and measure the pin 4 DC voltage.	The adjusted values from item 4.
Video output amplitude	V_O53	53	SG7 93 dBμ	Monitor the pin 53 with an oscilloscope, and measure the peak-to-peak value of the waveform.	The adjusted values from item 4.
RF AGC Delay Pt (@DAC = 0)	$RF_{AGC}0$	4	SG1	Set the RF AGC D/A converter to 0 and determine the input level such that the pin 4 DC voltage becomes 3.8 ±0.5 V.	The adjusted values from item 4.
RF AGC Delay Pt (@DAC = 63)	$RF_{AGC}63$	4	SG1	Set the RF AGC D/A converter to 63 and determine the input level such that the pin 4 DC voltage becomes 3.8 ±0.5 V.	The adjusted values from item 4.
Input sensitivity	V_{IN}	53	SG7	Monitor the pin 53 with an oscilloscope, and measure the peak-to-peak value of the waveform. Gradually decrease the input level and determine the input level such that the output goes down to a level lower than the video amplitude (V_O 53) by –3 dB.	The adjusted values from item 4.
Video/Sync ratio (@100 dBμ)	V/S	53	SG7 100 dBμ	Monitor the pin 53 with an oscilloscope, and measure the peak-to-peak values of the sync waveform (Vs) and the luminance signal (Vy) to determine the ratio Vy/Vs.	The adjusted values from item 4.
Differential gain	DG	53	SG5 93 dBμ	Measure the pin 53 with a vectorscope.	The adjusted values from item 4.
Differential phase	DP	53	SG5 93 dBμ	Measure the pin 53 with a vectorscope.	The adjusted values from item 4.
Video signal-to-noise ratio	S/N	53	SG1 93 dBμ	Pass the noise voltage signal generated at pin 53 through a 4 to 10 MHz bandpass filter and measure that signal(V_{sn}) with an rms voltmeter. Determine the value of the formula 20log(1.43/Vsn).	The adjusted values from item 4.
Synchronizing signal tip level	V53 TIP	53	SG1 93 dBμ	Measure the pin 53 DC voltage.	The adjusted values from item 4.
4.5 MHz attenuation	TRAP	53	SG6 93 dBμ	Measure the values of the 100 kHz and 4.5 MHz components and determine their ratio.	The adjusted values from item 4.
920 kHz beat level	I920	53	SG1 SG2 SG3	Input the 93 dBμ SG1 signal, and measure the pin 11 DC voltage (V11). Mix the three signals SG1 = 87 dBμ, SG2 = 82 dBμ, and SG3 = 63 dBμ, and input that signal to VIF IN. Apply the voltage V11 to pin 11 using an external power supply. Measure the difflerence of the 3.58 MHz and 920 kHz components using a spectrum analyzer.	The adjusted values from item 4.
Maximum AFT output voltage	$V14_H$	14	SG4 93 dBμ 44.75 MHz	Measure the pin 14 DC voltage.	
Minimum AFT output voltage	$V14_L$	14	SG4 93 dBμ 46.75 MHz	Measure the pin 14 DC voltage.	
AFT detection sensitivity	Sf	14	SG4 93 dBμ	Gradually change the SG4 frequency and determined the frequency change Δf required to change the pin 14 DC voltage from 2.5 V to 5.0 V. Sf = 2500/Δf [mV/kHz]	

First SIF Block - Input Signals and Test Conditions

For each of the test items, set up the following conditions unless otherwise specified.

1. PIF.IN: 45.75 MHz, 93 dBμ, CW
2. Bus control conditions: Set the following 4 items to their adjusted values.
   (See the VIF block test description for details on the adjustment procedure.)
   - APC DET.ADJ
   - PLL tuning
   - 4.5 MHz trap
   - Video level
3. Apply the input signal to the pin 12, using a signal with a frequency of 41.25 MHz CW.

Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
4.5 MHz conversion gain	SC_G	59	60 dBμ	Measure the pin 59 output 4.5 MHz component (mV rms). Let SV1 be this measured value and perform the following calculation. $SC_G = 20 \times \log(SV1 \times 1000) - 60$ [dB]	
4.5 MHz output level	SV_O	59	88 dBμ	Measure the pin 59 output 4.5 MHz component (mV rms). Let SV2 be this measured value and perform the following calculation. $SC_O = 20 \times \log(SV2 \times 1000)$ [dB]	
First SIF maximum input	SV_M	59	96 dBμ	Measure the pin 59 output 4.5 MHz component (mV rms). Let SV3 be this measured value and perform the following calculation. $SC_M = 20 \times \log(SV3/SV1)$ [dB]	

SIF Block - Input Signals and Test Conditions

For each of the test items, set up the following conditions unless otherwise specified.

1. Connect pin 13 (SIF AGC) to ground.
2. Bus control conditions: IF.AGC.SW = 1.
3. SW:IF1 = off
4. Apply the input signal to pin 61. The carrier frequency should be 4.5 MHz.

Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
FM detector output voltage	SO_{ADJ}	5	90 dBμ, fm = 1 kHz, FM = ±25 kHz	Adjust the D/A converter (FM.LEVEL) so that the pin 5 FM detector output 1 kHz component is as close to 424 mV rms as possible. Measure the output (mV rms) at that time. Let SV1 be the measured value at this time.	
FM limiting sensitivity	SLS	5	fm = 1 kHz, FM = ±25 kHz	Determine the input level (dBμ) such that the pin 5 FM detector output 1 kHz component is down –3 dB from SV1.	FM.LEVEL = adjusted value.
FM detector output bandwidth	SF	5	90 dBμ, FM ±25 kHz	Determine the modulation frequency bandwidth (Hz) for a –3 dB drop in the pin 5 FM detector output 1 kHz component with respect to SV1.	FM.LEVEL = adjusted value.
FM detector output distortion	S_{THD}	5	90 dBμ, fm = 1 kHz, FM ±25 kHz	Determine the distortion in the pin 5 FM detector output 1 kHz component.	FM.LEVEL = adjusted value.
AM rejection ratio	S_{AMR}	5	90 dBμ, fm = 1 kHz, AM = 30%	Measure (in mV rms) the pin 5 FM detector output 1 kHz component. Let SV2 be the measured value at this time and perform the following calculation. $S_{AMR} = 20 \times \log(SV1/SV2)$ [dB]	FM.LEVEL = adjusted value.
SIF signal-to-noise ratio	S_{SN}	5	90 dBμ, CW	Set the SW:IF1 switch to the on state. Measure the noise level (mV rms) on pin 5. Let SV3 be the measured value at this time and perform the following calculation. $S_{SN} = 20 \times \log(SV1/SV3)$ [dB]	FM.LEVEL = adjusted value.

Video Block - Input Signals and Test Conditions

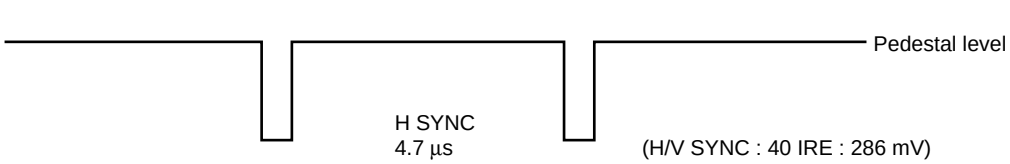
[Input Signals]

<C_{IN} input signal>

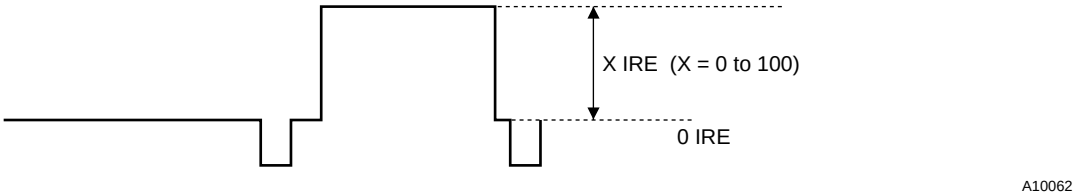
*: chrominance burst signal: 40 IRE

<Y_{IN} input signal>

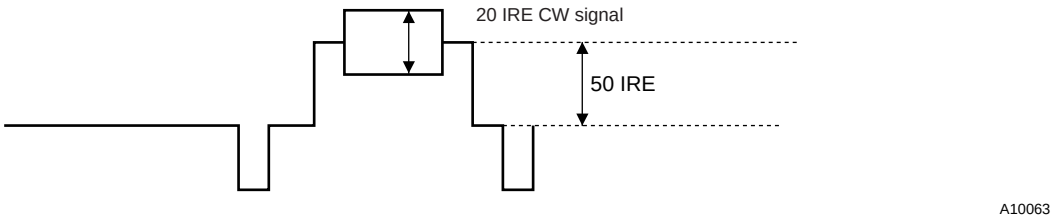
0 IRE signal (L-0): NTSC standard synchronizing signal



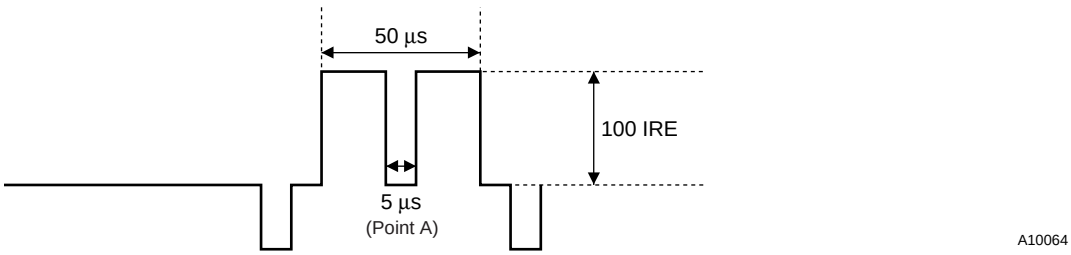
X IRE signal (L-X)



CW signal (L-CW)

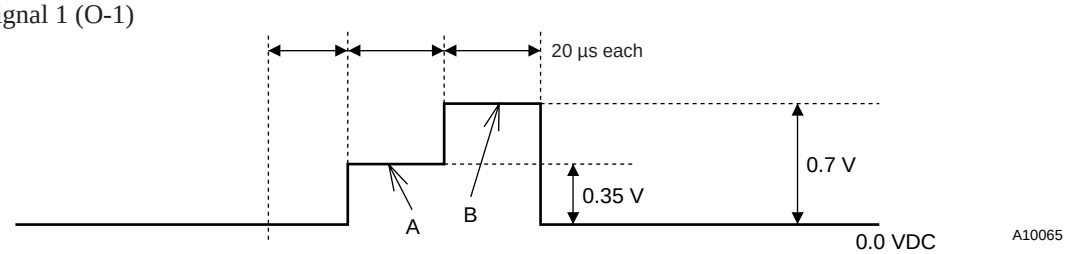


Black stretch 0 IRE signal (L-BK)

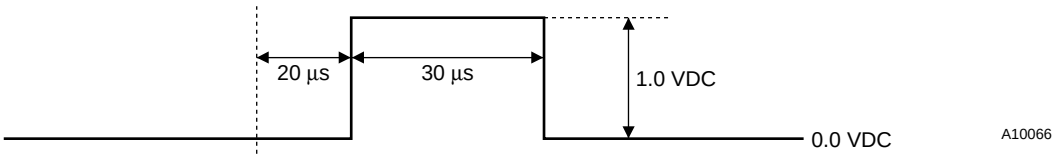


<R/G/B IN input signal>

RGB input signal 1 (O-1)



RGB input signal 2 (O-2)



(Test Conditions)

Parameter	Symbol	Test point	Input signal	Test procedure	Bus bits/input signal
[Video Block]					
Overall video gain (at maximum contrast)	CONT63	38	L-50	Measure the output signal 50 IRE amplitude (CNT_{HB} Vp-p) and calculate CONT63 = 20log(CNT_{HB}/0.357).	TR24: Contrast 111111
Contrast adjustment characteristics (normal/max)	CONT32	38	L-50	Measure the output signal 50 IRE amplitude (CNT_{CB} Vp-p) and calculate CONT32 = 20log(CNT_{CB}/0.357).	
Contrast adjustment characteristics (normal/max)	CONT0	38	L-50	Measure the output signal 50 IRE amplitude (CNT_{LB} Vp-p) and calculate CONT0 = 20log(CNT_{LB}/0.357).	TR24: Contrast 000000
Video frequency characteristics f0 = 1 (sharp 0)	Yf03	38	L-CW	With the input signal CW = 100 kHz, measure the amplitude of the CW signal in the output signal ($PEAK_{DC}$ Vp-p).	TR26: F0 Adjust 01
f0 = 3 (sharp 15)				With the input signal CW = 10 MHz, measure the amplitude of the CW signal in the output signal (F03 Vp-p).	TR26: F0 Adjust 11 TR25: Sharpness 01111
				Calculate Yf3 = 20log(F03/$PEAK_{DC}$).	
Chrominance trap level f0 = 0 (sharp 0)	Ctrap	38	L-CW	With the input signal CW = 3.58 MHz, measure the amplitude of the CW signal in the output signal (F00 Vpp).	TR26: F0 Adjust 00
				Calculate Ctrap = 20·log(F00/$PEAK_{DC}$).	
DC restoration	ClampG	38	L-0	Measure the output signal 0 IRE DC level (BRTPL (V)).	TR23: Brightness 000000 TR24: Contrast 111111
			L-100	Measure the output signal 0 IRE DC level (DRVPH (V)) and the 100 IRE amplitude (DRV_H Vpp). Calculate ClampG = 100 × (1 + ($DRVP_H$ – BRTPL)/DRV_H)).	TR23: Brightness 000000 TR24: Contrast 111111
Luminance delay f0 = 1	Y_{DLY}	38	L-50	Measure the time difference (amount of delay) between the rise of the input signal 50 IRE amplitude, and rise of the output signal 50 IRE amplitude.	
Maximum black stretch gain	BKSTmax	38	L-BK	Measure the 0 IRE DC level at point A in the output signal when the black stretch function is defeated (black stretch off). (BKST1 (V))	TR31: BKST Defeat 1
				Measure the 0 IRE DC level at point A in the output signal when the black stretch function is on. (BKST2 (V))	TR31: BKST Defeat 0
				Calculate BKSTmax = 2 × 50 × (BKST1 – BKST2)/CNT_{HB}.	
Black stretch threshold Δblack(40 IRE Δblack)	$BKST_{TH}\Delta$	38	L-40	Measure the 40 IRE DC level in the output signal when the black stretch function is on. (BKST3 (V))	TR31: BKST Defeat 0
				Measure the 40 IRE DC level in the output signal when the black stretch function is defeated (black stretch off). (BKST4 (V))	TR31: BKST Defeat 1
				Calculate $BKST_{TH}\Delta$ = 50 × (BKST4 – BKST3)/CNT_{HB}.	
Sharpness (peaking) variability characteristics (normal)	Sharp16	38	L-CW	With the input signal CW = 2.2 MHz, measure the amplitude of the CW signal in the output signal (F00S16 Vp-p).	TR26: F0 Adjust 00 TR25: Sharpness 10000
				Calculate Sharp16 = 20log(F00S16/$PEAK_{DC}$).	
(maximum)	Sharp31		L-CW	With the input signal CW = 2.2 MHz, measure the amplitude of the CW signal in the output signal (F00S31 Vp-p).	TR25: Sharpness 11111
				Calculate Sharp31 = 20log(F00S31/$PEAK_{DC}$).	
(minimum)	Sharp0		L-CW	With the input signal CW = 2.2 MHz, measure the amplitude of the CW signal in the output signal (F00S0 Vp-p).	TR25: Sharpness 00000
				Calculate Sharp0 = 20log(F00S0/$PEAK_{DC}$).	
Horizontal/vertical blanking output level	RGB_{BLK}	38	L-100	Measure the DC level of the output signal during the blanking period (RGB_{BLK} (V)).	

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Parameter	Symbol	Test point	Input signal	Test procedure	Bus bits/input signal
[OSD Block]					
OSD fast switching threshold	FS_{TH}	38	L-0 O-2	Gradually increase the pin 39 voltage starting at 1.5 V, and determine the pin 39 voltage at the point where the output signal switches to the OSD signal.	Pin 42: Apply signal O-2.
RGB red output level	R_{OSDH}	36	L-50	Measure the 50 IRE amplitude in the output signal. (CNT_{CR} Vp-p).	
			L-0 O-2	Measure the OSD output amplitude (OSD_{HR} Vp-p).	Pin 39: Apply 3.5 V. Pin 40: Apply signal O-2.
				Calculate $R_{OSDH} = 50 \times (OSD_{HR}/CNT_{CR})$.	
RGB green output level	G_{OSDH}	37	L-50	Measure the 50 IRE amplitude in the output signal. (CNT_{CG} Vp-p).	
			L-0 O-2	Measure the OSD output amplitude (OSD_{HG} Vpp).	Pin 39: Apply 3.5 V. Pin 41: Apply signal O-2.
				Calculate $G_{OSDH} = 50 \times (OSD_{HG}/CNT_{CG})$.	
RGB blue output level	B_{OSDH}	38	L-50	Measure the 50 IRE amplitude in the output signal. (CNTCB Vp-p).	
			L-0 O-2	Measure the OSD output amplitude (OSD_{HB} Vp-p).	Pin 39: Apply 3.5 V. Pin 42: Apply signal O-2.
				Calculate $B_{OSDH} = 50 \times (OSD_{HB}/CNT_{CB})$.	
Analog OSD red output level		36	L-0 O-1	Measure the amplitudes at point A (the 0.35 V component of the input signal O-1) and point B (the 0.7 V component of the input signal O-1) in the output signal and record these as RGB_{LR} and RGB_{HR} (Vp-p) respectively.	Pin 39: Apply 3.5 V. Pin 40: Apply signal O-1.
Gain matching	R_{RGB}			Calculate $R_{RGB} = RGB_{LR}/CNT_{CR}$.	
Linearity	LR_{RGB}			Calculate $LR_{RGB} = 100 \times (RGB_{LR}/RGB_{HR})$.	
Analog OSD green output level		37	L-0 O-1	Measure the amplitudes at point A (the 0.35 V component of the input signal O-1) and point B (the 0.7 V component of the input signal O-1) in the output signal and record these as RGB_{LG} and RGB_{HG} (Vp-p) respectively.	Pin 39: Apply 3.5 V. Pin 34: Apply signal O-1.
Gain matching	G_{RGB}			Calculate $G_{RGB} = RGB_{LG}/CNT_{CG}$.	
Linearity	LG_{RGB}			Calculate $LG_{RGB} = 100 \times (RGB_{LG}/RGB_{HG})$.	
Analog OSD blue output level		38	L-0 O-1	Measure the amplitudes at point A (the 0.35 V component of the input signal O-1) and point B (the 0.7 V component of the input signal O-1) in the output signal and record these as RGB_{LB} and RGB_{HB} (Vp-p) respectively.	Pin 39: Apply 3.5 V. Pin 41: Apply signal O-1.
Gain matching	B_{RGB}			Calculate $B_{RGB} = RGB_{LB}/CNT_{CB}$.	
Linearity	LB_{RGB}			Calculate $LB_{RGB} = 100 \times (RGB_{LB}/RGB_{HB})$.	
[RGB Output Block] (Cutoff and Drive Blocks)					
Brightness control (normal)	BRT32	36 37 38	L-0	Measure the output signal 0 IRE DC levels of the R output (pin 36), G output (pin 37), and B output (pin 38) and record these as $BRTPC_R$, $BRTPC_G$, and $BRTPC_B$ (V), respectively.	TR24: Contrast 111111
				Calculate $BRT63 = (BRTPC_R + BRTPC_G + BRTPC_B)/3$.	
(maximum)	BRT63	38		Measure the output signal 0 IRE DC level of the B output (pin 38) ($BRTPH_B$).	TR23: Brightness 111111
				Calculate $BRT63 = 50 \times (BRTPH_B - BRTPC_B) / CNTH_B$.	
(minimum)	BRT0			Measure the output signal 0 IRE DC level of the B output (pin 38) ($BRTPL_B$).	TR23: Brightness 000000
				Calculate $BRT0 = 50 \times (BRTPL_B - BRTPC_B) / CNTH_B$.	

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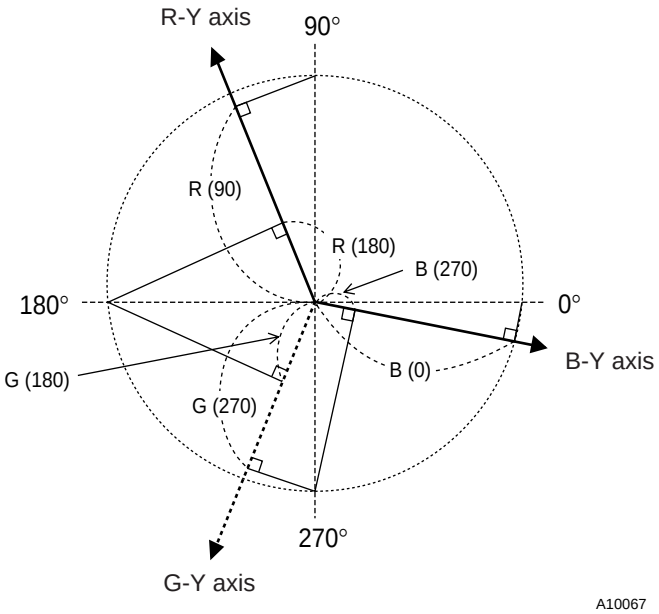
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Parameter	Symbol	Test point	Input signal	Test procedure	Bus bits/input signal
[RGB Output Block] (Cutoff and Drive Blocks)					
Bias (cutoff) control (minimum)	Vbias0	36 37 38	L-50	Measure the output signal 0 IRE DC levels of the R output (pin 36), G output (pin 37), and B output (pin 38) and record these as Vbias0* (V), where * : R, G, and B, respectively.	TR24: CONTRAST 111111 TR22: SUB-BIAS R, G, B 000000
(maximum)	Vbias128			Measure the output signal 0 IRE DC levels of the R output (pin 36), G output (pin 37), and B output (pin 38) and record these as Vbias128* (V), where * : R, G, and B, respectively.	TR16: R BIAS 111111 TR: G BIAS 111111 TR18: B BIAS 111111 TR24: CONTRAST 111111 TR22: SUB-BIAS R, G, B 111111
Bias (cutoff) control resolution	Vbiassns			Measure the output signal 0 IRE DC levels of the R output (pin 36), G output (pin 37), and B output (pin 38) and record these as BAS80* (V), where * : R, G, and B, respectively.	TR16: R BIAS 1010000 TR17: G BIAS 1010000 TR18: B BIAS 1010000 TR24: CONTRAST 111111
				Measure the output signal 0 IRE DC levels of the R output (pin 36), G output (pin 37), and B output (pin 38) and record these as BAS48* (V), where * : R, G, and B, respectively.	TR16: R BIAS 0110000 TR17: G BIAS 0110000 TR18: B BIAS 0110000 TR24: CONTRAST 11111
				Vbiassns * = (BAS80 * – BAS48 *)/32	
Sub-bias control resolution	Vsbiassns		L-50	Measure the output signal 0 IRE DC levels of the R output (pin 36), G output (pin 37), and B output (pin 38) and record these as SBTPM* (V), where * : R, G, and B, respectively.	TR22: SUB-BIAS R, G, B 101010
				Vsbiassns * = (BRTPC * – SBTPM *)	
Maximum drive adjustment output	RGBout63	36 37 38	L-100	Measure the output signal 100 IRE DC amplitudes of the R output (pin 36), G output (pin 37), and B output (pin 38) and record these as DRV_H* (Vpp), where * : R, G, and B, respectively.	TR24: CONTRAST 111111 TR23: Brightness 000000
Output attenuation	RGBout0			Measure the output signal 100 IRE DC amplitudes of the R output (pin 36), G output (pin 37), and B output (pin 38) and record these as DRV_L* (Vpp), where * : R, G, and B, respectively.	TR24: CONTRAST 111111 TR23: Brightness 000000 TR19: R DRIVE 000000 TR20: G DRIVE 000000 TR21: B DRIVE 000000
				RGBout0 * = 20 log(DRV_H */DRV_L *)	

Chrominance Block - Input Signals and Test Conditions

For each of the test items, set up the following conditions unless otherwise specified.

1. VIF and SIF blocks: No signal
2. Deflection block: Input a horizontal/vertical composite sync signal and verify that the deflection block is locked on the synchronizing signal. (See the section on input signals and test conditions for the deflection block.)
3. Bus control conditions: All conditions set to their initial values, unless otherwise specified.
4. Connect a crystal oscillator circuit to pin 16. Adjust the impedance (Z) of the series capacitance and resistance as shown below.
   Z = 0 deg @ 3.579545 MHz ±10 Hz
   –40 ±1 deg @3.579345 MHz
5. Luminance (Y) input: No signal
6. Chrominance (C) input: Input the signal to the C1IN pin (pin 51).
7. The method for calculating the demodulation angle is shown below.
   B-Y axis angle = tan – 1 (B(0)/B(270)) + 270°
   R-Y axis angle = tan – 1 (R(180)/R(90)) + 90°
   G-Y axis angle = tan – 1 (G(270)/G(180)) + 180°

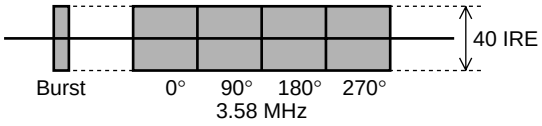


8. The method for calculating the AF angle is shown below.
   BR · · · · The B-Y/R-Y demodulation output ratio
   θ· · · · · · ANGBR: the B-Y/R-Y demodulation angle

$$AFXXX = \tan - 1 \left\{ \frac{R - Y/B - Y \times BR - \cos\theta}{\sin\theta} \right\}$$

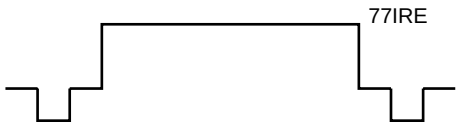
[Input Signal]

C-1



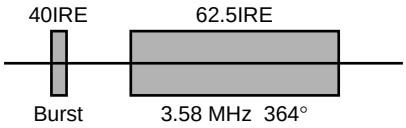
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X IRE signal (L-X)



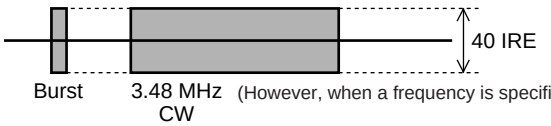
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C-2



A10070

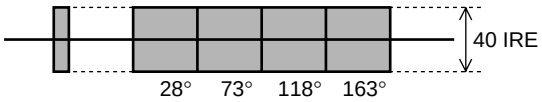
C-3



(However, when a frequency is specified, that frequency is to be used.)

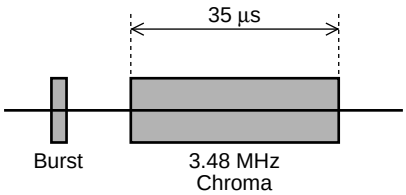
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C-4



A10072

C-5



A10073

(Test Conditions)

Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
[Chrominance Block]					
ACC amplitude characteristics 1	ACC_M1	Bout 38	C-1 0 dB +6 dB	Measure the output amplitude when the chrominance input is set to 0 dB and the output amplitude when the input is reduced by – 6 dB, and calculate the ratio. ACC_M1 = 20log(+6 dB data/0 dB data)	
ACC amplitude characteristics 2	ACC_M2	Bout 38	C-1 –14 dB	Measure the output amplitude when the chrominance input is set to –14 dB and calculate the ratio. ACC_M2 = 20log(–14 dB data/0 dB data)	
B-Y/Y amplitude ratio	CLR_{BY}	38	Y_{IN}: L77 C-1: No signal	Measure the luminance (Y) output level(V1).	
			C-2	Next, apply a signal to the C_{IN} input (with only a sync applied to the Y input) and measure the output level (V2). Calculate the following formula. $CLR_{BY} = 100 \times (V2/V1) + 15\%$	
Color control characteristics 1	CLR_{MN}	38	C-3	Measure V1: the output amplitude when the color control is maximum, and V2: the output amplitude when the color control is normal (Color control: 1000000) and calculate CLR_{MN} = V1/V2.	TR28: Color Control 1111111 1000000
Color control characteristics 2	CLR_{MM}	38	C-3	Measure V3: the output amplitude when the color control is minimum and calculate CLR_{MM} = 20·log(V1/V3).	TR28: Color Control 0000000
Color control sensitivity	CLR_{SE}	38	C-3	Measure V4: the output amplitude when the color control is 90, and V5: the output amplitude when the color control is 38. Calculate the following formula. $CLR_{SE} = 100 \times (V4 – V5) / (V2 \times 52)$	TR28: Color Control 1011010 Color Ctontrol 0100110
Tint center	TIN_{CEN}	38	C-1	Measure each section of the output waveform and calculate the angle of the B-Y axis.	TR27: TINT 0111111
Tint control (max)	TIN_{MAX}	38	C-1	Measure each section of the output waveform and calculate the angle of the B-Y axis. Calculate the following formula. TIN_{MAX} = (the B-Y axis angle) – TIN_{CEN}	TR27: TINT 1111111
Tint control (min)	TIN_{MIN}	38	C-1	Measure each section of the output waveform and calculate the angle of the B-Y axis. Calculate the following formula. TIN_{MIN} = (the B-Y axis angle) – TIN_{CEN}	TR27: TINT 0000000
Tint control sensitivity	TIN_{SE}	38	C-1	Measure A1: the angle when the tint control is 85, and A2: the angle when the tint control is 42. Calculate the following formula. TIN_{SE} = (A1 – A2)/43	TR27: TINT 1010101 0101010
Demodulation output ratio B-Y/R-Y	BR	38 36	C-3	Measure Vb: the B_{OUT} output amplitude and Vr: the R_{OUT} output amplitude, and calculate BR = Vb/Vr.	TR28: Color Control 1000000
Demodulation output ratio G-Y/R-Y	GR	37	C-3	Measure Vg: the G_{OUT} output amplitude and calculate GR = Vg/Vr.	TR28: Color Control 1000000

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Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
Demodulation angle B-Y/R-Y	ANG_{BR}	38 36	C-1	Measure the B_{OUT} and R_{OUT} output levels and calculate the angle between the B-Y and R-Y axes. Calculate ANG_{BR} = (R-Y angle) – (B-Y angle).	
Demodulation angle G-Y/R-Y	ANG_{GR}	37	C-1	Measure the GOUT output level and calculate the angle between the G-Y and R-Y axes. Calculate ANG_{GR} = (R-Y angle) – (G-Y angle).	
Killer operating point	KILL	38	C-3	Gradually decrease the amplitude of the input signal and measure the input level when the output level falls less than 150 mVpp.	
Chrominance VCO free-running frequency	C_{VCOF}	16	CIN No signal	Measure the oscillator frequency f and calculate the following formula. C_{VCOF} = f – 3579545 (Hz)	
Chrominance pull-in range (+)	PUL_{IN}^{+}	38	C-1	Gradually decrease the input signal subcarrier frequency starting at 3.579545 MHz + 1000 Hz, and measure frequency at the point the output waveform locks.	
Chrominance pull-in range (–)	PUL_{IN}^{-}	38	C-1	Gradually raise the input signal subcarrier frequency starting at 3.579545 MHz – 1000 Hz, and measure frequency at the point the output waveform locks.	
Auto Flesh characteristics 73°	AF073	38 36	C-4	With Auto Flesh = 0, measure the level that corresponds to a B_{OUT} and R_{OUT} output waveform of 73° and calculate the angle AF073A. With Auto Flesh = 1, measure the angle AF073B in the same manner. Calculate the following formula. AF073 = AF073B – AF073A	TR26: Auto Flesh : **** 0 ** TR26: Auto Flesh : **** 1 **
Auto Flesh characteristics 118°	AF118	38 36	C-4	With Auto Flesh = 0, measure the level that corresponds to a B_{OUT} and R_{OUT} output waveform of 118° and calculate the angle AF118A. With Auto Flesh = 1, measure the angle AF118B in the same manner. Calculate the following formula. AF118 = AF118B – AF118A	TR26: Auto Flesh : **** 0 ** TR26: Auto Flesh : **** 1 **
Auto Flesh characteristics 163°	AF163	38 36	C-4	With Auto Flesh = 0, measure the level that corresponds to a B_{OUT} and R_{OUT} output waveform of 163° and calculate the angle AF163A. With Auto Flesh = 1, measure the angle AF163B in the same manner. Calculate the following formula. AF163 = AF163B – AF163A	TR26: Auto Flesh : **** 0 ** TR26: Auto Flesh : **** 1 **
Overload characteristics 1	OVL1	36	C-5	Measure V1: the output amplitude when the input signal burst level is set to 40 IRE and the chrominance level is set to 8 IRE, and V2: the output amplitude when the input signal burst level is set to 40 IRE and the chrominance level is set to 40 IRE. Calculate the following formula. OVL1 = V2/V1	TR26: OverLoad : ****** 1

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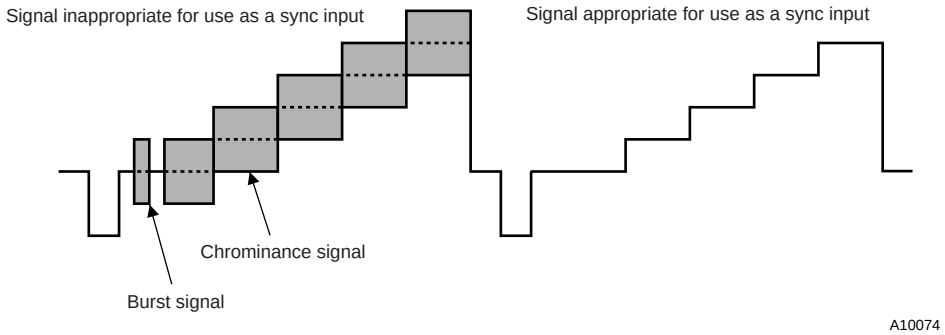
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Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
Overload characteristics 2	OVL2	36	C-5	Measure V3: the output amplitude when the input signal burst level is set to 40 IRE and the chrominance level is set to 80 IRE. Calculate the following formula. OVL2 = V3/V1	TR26: Overload ******1
Overload characteristics 3	OVL3	36	C-5	Measure V4: the output amplitude when the input signal burst level is set to 20 IRE and the chrominance level is set to 80 IRE. Calculate the following formula. OVL3 = V4/V1	TR26: Overload ******1
[Chrominance Bandpass Filter Characteristics]					
Peaking amplitude characteristics: 3.08 MHz	CPE308	38	C-3	Measure V0: the output amplitude. Next, set the input chrominance signal (CW) frequency to 3.08 MHz and measure V1: the output amplitude. Calculate the following formula. CPE308 = 20log(V1/V0)	TR26: CHR.BPF: ***1***
Peaking amplitude characteristics: 3.88/3.28 MHz	CPE	38	C-3	Measure V2: the output amplitude when the input chrominance signal (CW) frequency is 3.28 MHz, and V3: the output amplitude when the input chrominance signal (CW) frequency is 3.88 MHz. Calculate the following formula. CPE = 20log(V3/V2)	TR26: CHR.BPF: ***1***
Peaking amplitude characteristics: 4.08/3.08 MHz	CPE05	38	C-3	Measure V4: the output amplitude when the input chrominance signal (CW) frequency is 4.08 MHz. Calculate the following formula. CPE05 = 20log(V4/V1)	TR26: CHR.BPF: ***1***
Bandpass amplitude characteristics: 3.08 MHz	CBE308	38	C-3	Measure V5: the output amplitude. Next, measure V6: the output amplitude when the input chrominance signal (CW) frequency is set to 3.08 MHz. Calculate the following formula. CPE308 = 20log(V6/V5)	TR26: CHR.BPF: ***0***
Bandpass amplitude characteristics: 3.88/3.28 MHz	CBE	38	C-3	Measure V7: the output amplitude when the input chrominance signal (CW) frequency is 3.28 MHz, and V8: the output amplitude when the input chrominance signal (CW) frequency is 3.88 MHz. Calculate the following formula. CPE = 20log(V8/V7)	TR26: CHR.BPF: ***0***
Bandpass amplitude characteristics: 4.08/3.08 MHz	CBE05	38	C-3	Measure V9: the output amplitude when the input chrominance signal (CW) frequency is set to 4.08 MHz. Calculate the following formula. CPE05 = 20log(V9/V6)	TR26: CHR.BPF: ***0***

Deflection Block - Input Signals and Test Conditions

For each of the test items, set up the following conditions unless otherwise specified.

1. VIF and SIF blocks: No signal
2. Luminance (Y) input and chrominance (C) input: No signal
3. Sync input: Horizontal/vertical composite sync signal (DC offset: 3.8 V, 40 IRE. Other timing and other parameters must conform to the FCC broadcast standards.)
   Caution: There must be no burst or chrominance signal under the pedestal level.



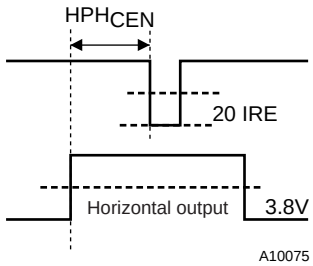
4. Bus control conditions: All conditions set to their initial values, unless otherwise specified.
5. The delay time from the rise of the horizontal output (the pin 26 output) to the rise of the F.B.P IN (pin 27 input) must be 9 µs.
6. The pin 18 (the vertical size correction circuit input pin) voltage must be V_{CC} (7.6 V).
7. Pin 28 (the x-ray protection circuit input pin) must be connected to ground.

Notes:

Perform the following operations if the horizontal output pulse signal was stopped.

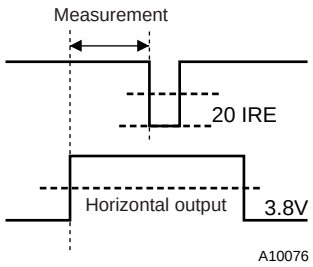
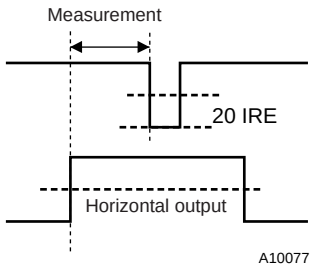
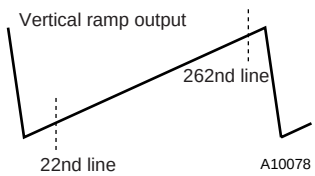
1. Set the bus on/off bit to off (0) temporarily, and then set it to on (1) again.
   (If the x-ray protection circuit and/or the PON-RES circuit operate, an IC internal latch circuit will be set. The on/off bit must be set to off (0) to reset that latch circuit, even if the horizontal output signal is not output. Since the PON-RES circuit operates when the horizontal supply voltage rises, the on/off bit must be set to off (0).)

2. Note on video muting
   If the horizontal output pulse signal was stopped, after performing the operation described in paragraph 1 above, clear the video muting bit to 0.
   (This is because the video muting bit is forcibly set to 1 when the on/off bit is set to 0 or when either the x-ray protection circuit or the PON-RES circuit operate. This also applies at power on.)

Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
[Deflection Block]					
Sync separator circuit sensitivity	Ssync	44	SYNC IN: horizontal and vertical synchronizing signal	Gradually decrease the level of the synchronizing signal input to SYNC IN (pin 44) and measure the level of the synchronizing signal when the synchronization is unlocked.	
Horizontal free-running frequency deviation	Δf_H	26	SYNC IN: no signal	Connect the pin 26 output (Hout) to a frequency counter and measure the horizontal free-running frequency. Calculate the following formula. Δf_H = <measured value> – 15.743 kHz	
Horizontal pull-in range	f_H PULL	44	SYNC IN: horizontal and vertical synchronizing signal	Monitor the horizontal synchronizing signal input to SYNC IN (pin 44) and the pin 26 output (Hout) with an oscilloscope. Vary the frequency of the horizontal synchronizing signal and measure the pull-in range.	
Horizontal output pulse width @0	Hduty 0	26	SYNC IN: horizontal and vertical synchronizing signal	Measure the low-level period in the pin 26 horizontal pulse waveform.	HDUTY: 00
Horizontal output pulse width @1	Hduty 1	26	SYNC IN: horizontal and vertical synchronizing signal	Measure the low-level period in the pin 26 horizontal pulse waveform.	HDUTY: 01
Horizontal output pulse width @2	Hduty 2	26	SYNC IN: horizontal and vertical synchronizing signal	Measure the low-level period in the pin 26 horizontal pulse waveform.	
Horizontal output pulse width @3	Hduty 3	26	SYNC IN: horizontal and vertical synchronizing signal	Measure the low-level period in the pin 26 horizontal pulse waveform.	HDUTY: 11
Horizontal output pulse saturation voltage	$V_H$sat	26	SYNC IN: horizontal and vertical synchronizing signal	Measure the voltage during low-level period in the pin 26 horizontal pulse waveform.	
Horizontal output pulse phase	HPH_{CEN}	26 44	SYNC IN: horizontal and vertical synchronizing signal	Measure the delay time from the rise of the pin 26 horizontal output pulse waveform to the fall of the SYNC IN horizontal synchronizing signal. 	

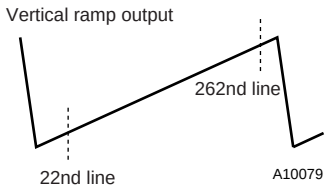
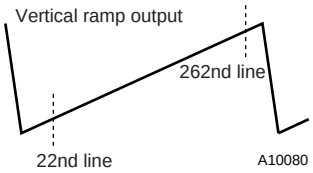
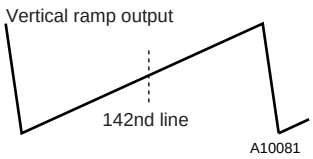
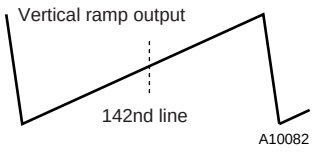
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Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
Horizontal position adjustment range	HPHrange	26 44	SYNC IN: horizontal and vertical synchronizing signal	Measure the delay time from the rise of the pin 26 horizontal output pulse to the fall of SYNC IN horizontal synchronizing signal with H_{PHASE} set to both 0 and 15 and calculate the difference with respect to HPH_{CEN}. 	H_{PHASE}: 0000 H_{PHASE}: 1111
Maximum horizontal position adjustment variability	HPHstep	26 44	SYNC IN: horizontal and vertical synchronizing signal	Measure the delay time from the rise of the pin 26 horizontal output pulse to the fall of SYNC IN horizontal synchronizing signal while varying H_{PHASE} from 0 to 15, and measure the amount of variation at each step. Find the step with the largest value of the data. 	H_{PHASE}: 0000 to H_{PHASE}: 1111
X-ray protection circuit operating voltage	VX_{RAY}	26 28	SYNC IN: horizontal and vertical synchronizing signal	Connect a DC voltage source to pin 28, and gradually increase that voltage starting at 0 V. Measure the pin 28 DC voltage at the point the pin 26 horizontal output pulse stops.	
POR circuit operating voltage	V_{POR}	(24) 26	SYNC IN: horizontal and vertical synchronizing signal	Replace the current source connected to pin 24 with a DC voltage source, and gradually decrease the voltage starting at 7.3 V. Measure the pin 24 DC voltage at the point the pin 26 horizontal output pulse stops.	
[Vertical Screen Size Adjustment]					
Vertical ramp output amplitude @64	Vsize64	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltages at the 22nd line and at the 262nd line. Calculate the following formula. Vsize64 = Vline262 – Vline22 	

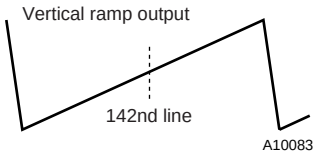
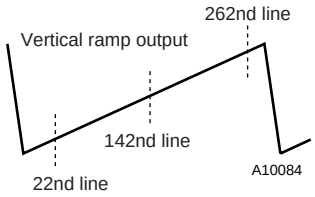
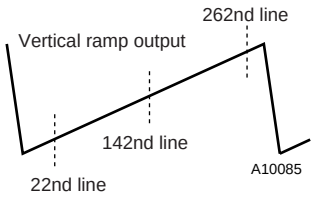
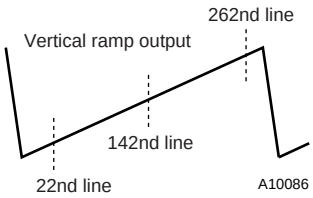
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Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
Vertical ramp output amplitude @0	Vsize0	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltages at the 22nd line and at the 262nd line. Calculate the following formula. Vsize0 = Vline262 – Vline22 	V_{SIZE}: 0000000
Vertical ramp output amplitude @127	Vsize127	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltages at the 22nd line and at the 262nd line. Calculate the following formula. Vsize0 = Vline262 – Vline22 	V_{SIZE}: 1111111
[High-Voltage Dependency Vertical Size Correction]					
Vertical size correction @7 (maximum)	Vsizecomp	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltages at the 22nd line and at the 262nd line. Calculate Va from the following formula. Va = Vline262 – Vline22 Next, apply 3.8 V to pin 18, and once again measure the voltages at the 22nd line and at the 262nd line. Calculate Vb from the following formula. Vb = Vline262 – Vline22 Finally, calculate Vsizecomp from the following formula. Vsizecomp = (Va – Vb)/Va × 100	V_{COMP}: 111
[Vertical Screen Position Adjustment]					
Vertical ramp DC voltage @32	Vdc32	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltage at the 142nd line. 	
Vertical ramp DC voltage @0	Vdc0	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltage at the 142nd line. 	V_{DC}: 000000

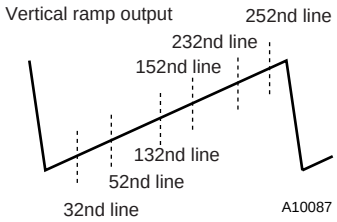
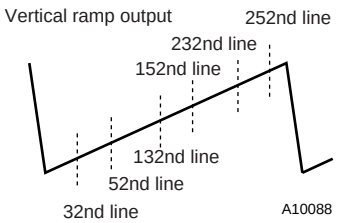
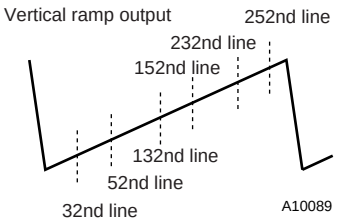
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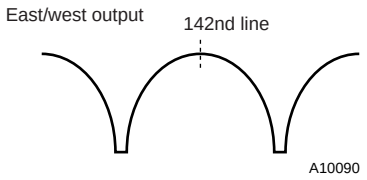
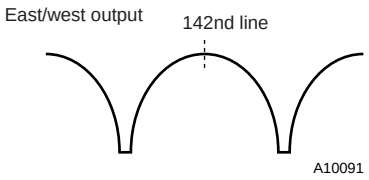
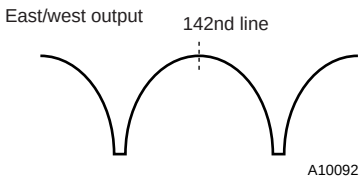
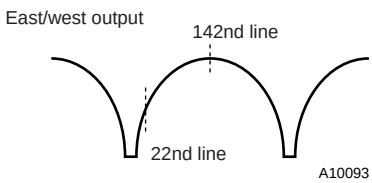
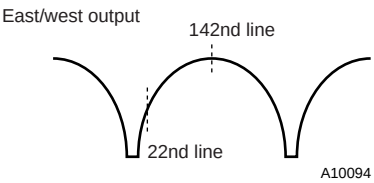
Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
Vertical ramp DC voltage @63	Vdc63	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltage at the 142nd line. 	V_{DC}: 111111
Vertical linearity @8	Vlin8	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltages at the 22nd line, the 142nd line, and the 262nd line. Let Va, Vb, and Vc be these measurements, and calculate the following formula. Vline8 = (Vb – Va)/(Vc – Va) 	
Vertical linearity @0	Vlin0	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltages at the 22nd line, the 142nd line, and the 262nd line. Let Va, Vb, and Vc be these measurements, and calculate the following formula. Vline0 = (Vb – Va)/(Vc – Va) 	VLIN: 0000
Vertical linearity @15	Vlin15	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltages at the 22nd line, the 142nd line, and the 262nd line. Let Va, Vb, and Vc be these measurements, and calculate the following formula. Vline15 = (Vb – Va)/(Vc – Va) 	VLIN: 1111

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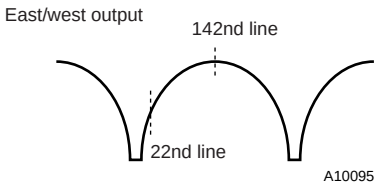
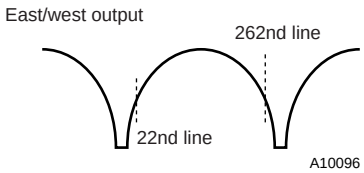
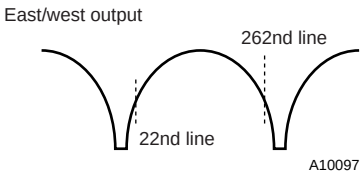
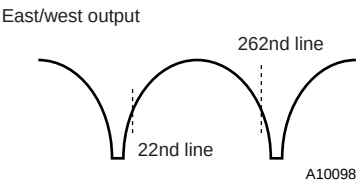
Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
Vertical S-curve correction @8	VScor8	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltages at the 32nd line, the 52nd line, the 132nd line, the 152nd line, the 232nd line, and the 252nd line. Let Va, Vb, Vc, Vd, Ve, and Vf be these measurements, and calculate the following formula. VScor8 = 0.5[(Vb – Va) + (Vf – Ve)] / (Vd – Vc) 	VS: 1000
Vertical S-curve correction @0	VScor0	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltages at the 32nd line, the 52nd line, the 132nd line, the 152nd line, the 232nd line, and the 252nd line. Let Va, Vb, Vc, Vd, Ve, and Vf be these measurements, and calculate the following formula. VScor0 = 0.5[(Vb – Va) + (Vf – Ve)] / (Vd – Vc) 	
Vertical S-curve correction @15	VScor15	19	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 19 vertical ramp output and measure the voltages at the 32nd line, the 52nd line, the 132nd line, the 152nd line, the 232nd line, and the 252nd line. Let Va, Vb, Vc, Vd, Ve, and Vf be these measurements, and calculate the following formula. VScor15 = 0.5[(Vb – Va) + (Vf – Ve)] / (Vd – Vc) 	VS: 1111

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Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
[Horizontal Size Adjustment]					
East/west DC voltage @16	EWdc16	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltage at the 142nd line. 	
East/west DC voltage @0	EWdc0	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltage at the 142nd line. 	EW_{DC}: 00000
East/west DC voltage @31	EWdc31	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltage at the 142nd line. 	EW_{DC}: 11111
[Pin-Cushion Distortion Correction]					
East/west parabola amplitude @8	EWamp8	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltages at the 22nd line and at the 142nd line. Let Va and Vb be these measurements, and calculate the following formula. EWamp8 = Vb – Va 	
East/west parabola amplitude @0	EWamp0	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltages at the 22nd line and at the 142nd line. Let Va and Vb be these measurements, and calculate the following formula. EWamp0 = Vb – Va 	EW_{AMP}: 0000

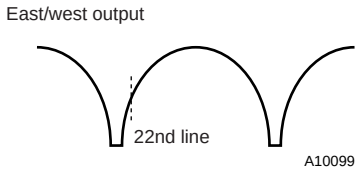
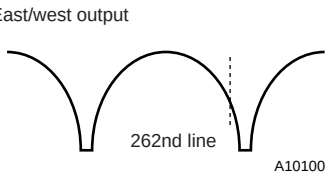
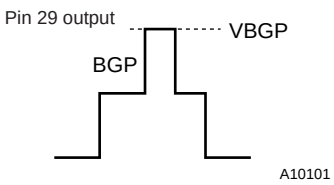
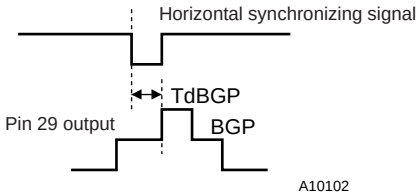
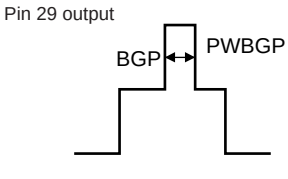
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Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
East/west parabola amplitude @15	EWamp15	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltages at the 22nd line and at the 142nd line. Let Va and Vb be these measurements, and calculate the following formula. EWamp15 = Vb – Va 	EW_{AMP}: 1111
[Trapezoidal Distortion Correction]					
East/west parabola tilt @8	EWtilt8	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltages at the 22nd line and at the 262nd line. Let Va and Vb be these measurements, and calculate the following formula. EWamp8 = Va – Vb 	
East/west parabola tilt @0	EWtilt0	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltages at the 22nd line and at the 262nd line. Let Va and Vb be these measurements, and calculate the following formula. EWtilt0 = Va – Vb 	EW_{TILT}: 0000
East/west parabola tilt @15	EWtilt15	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltages at the 22nd line and at the 262nd line. Let Va and Vb be these measurements, and calculate the following formula. EWtilt15 = Va – Vb 	EW_{TILT}: 1111

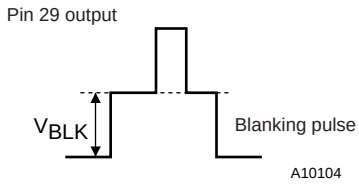
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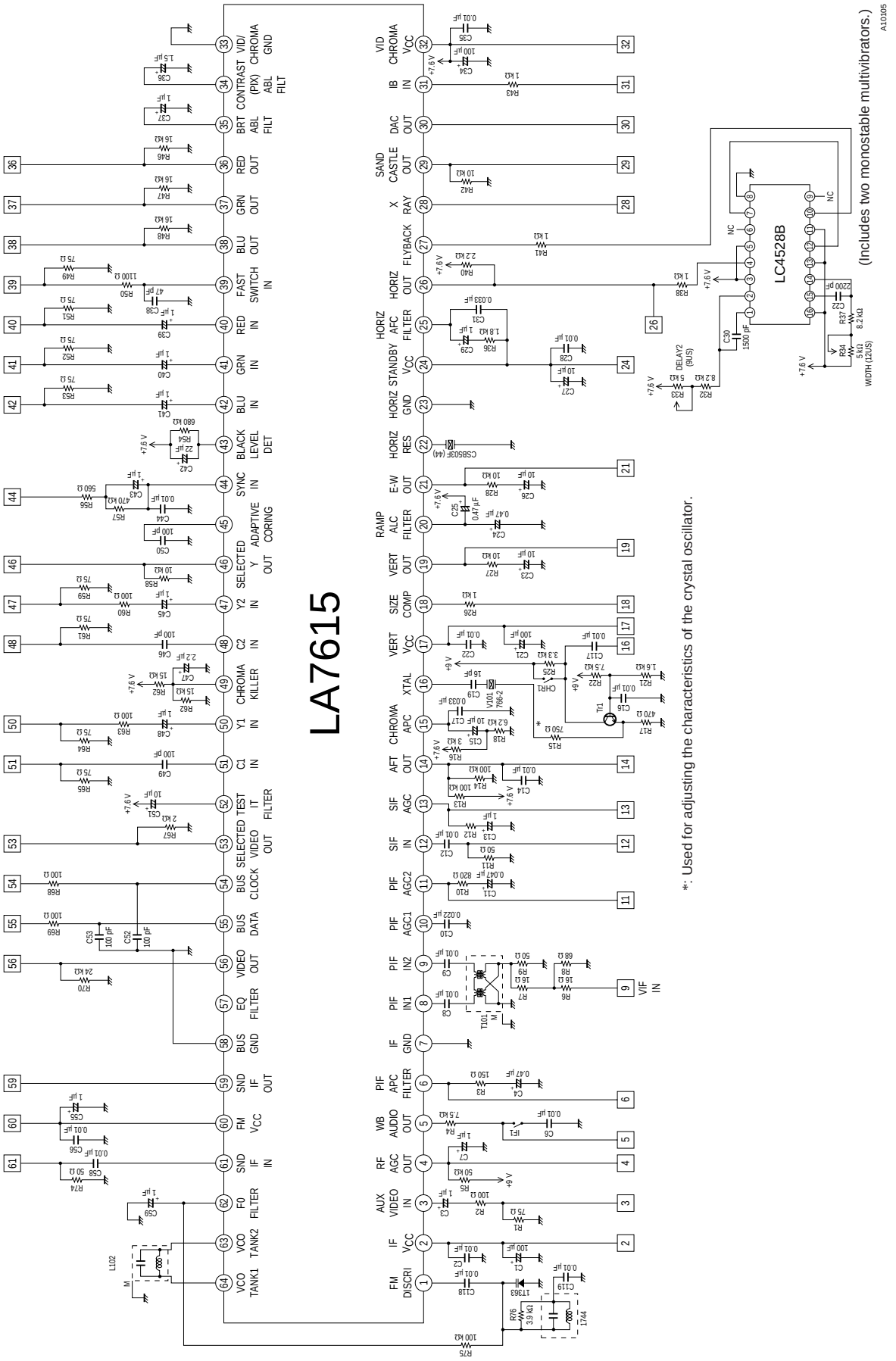
Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
[Corner Distortion Correction]					
East/west parabola corner: Top	EWcortop	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltage at the 22nd line under the conditions with COR_{TOP} set to 111 and to 000. Let Va and Vb be these measurements. Calculate the following formula. EWcortop = Va – Vb 	$CORT_{OP}$: 111-000
East/west parabola corner: Bottom	EWcorbot	21	SYNC IN: horizontal and vertical synchronizing signal	Monitor the pin 21 east/west output (parabola waveform output) and measure the voltage at the 262nd line under the conditions with COR_{BOT} set to 111 and to 000. Let Va and Vb be these measurements. Calculate the following formula. EWcorbot = Va – Vb 	CORBOTTOM: 111-000
[Sandcastle Output]					
Burst gate pulse peak value	V_{BGP}	29	SYNC IN: horizontal and vertical synchronizing signal	Measure the pin 29 output burst gate pulse peak value. 	
Burst gate pulse phase	Td_{BGP}	29 44	SYNC IN: horizontal and vertical synchronizing signal	Measure the delay time from the rise of the horizontal synchronizing signal to the rise of the pin 29 burst gate pulse. 	
Burst gate pulse width	PW_{BGP}	29	SYNC IN: horizontal and vertical synchronizing signal	Measure the width of the pin 29 burst gate pulse. 	

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Parameter	Symbol	Test point	Input signal	Test procedure	Bus condition
Blanking pulse peak value	V_{BLK}	29	SYNC IN: horizontal and vertical synchronizing signal	Measure the peak value of the pin 29 output blanking pulse. 	
[D/A Converter Output]					
Pin 30 D/A converter output voltage @0	$V_{DAC}0$	30		Measure the pin 30 D/A converter output DC voltage.	$+B_{TRIM}$: 0000
Pin 30 D/A converter output voltage @8	$V_{DAC}8$	30		Measure the pin 30 D/A converter output DC voltage.	
Pin 30 D/A converter output voltage @15	$V_{DAC}15$	30		Measure the pin 30 D/A converter output DC voltage.	$+B_{TRIM}$: 1111

Test Circuit Diagram



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