Integrated Circuit Systems, Inc.

# ICS843001-21

## FEMTOCLOCKS™ CRYSTAL-TO-3.3V LVPECL FREQUENCY SYNTHESIZER

## GENERAL DESCRIPTION

The ICS843001-21 is a a highly versatile, low phase noise LVPECL Synthesizer which can generate low jitter reference clocks for a variety of communications applications and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. The dual crystal interface allows the synthesizer to support up to two communications standards in a given application (i.e. 1GB Ethernet with a 25MHz crystal and 1Gb Fibre Channel using a 25.5625MHz crystal). The rms phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET and 10Gb Ethernet. The ICS843001-21 is packaged in a small 24-pin TSSOP package.

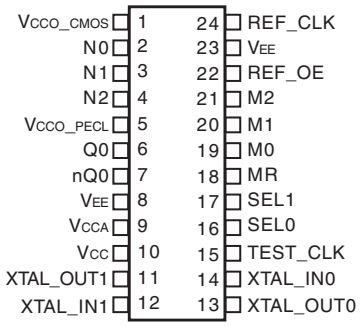
## FEATURES

- One 3.3V LVPECL output pair and one LVCMOS output
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 560MHz - 700MHz
- Supports the following applications: SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz): 0.80ps (typical)

| Offset | Noise Power |
|---|---|
| 100Hz | -60.3 dBc/Hz |
| 1kHz | -88.5 dBc/Hz |
| 10kHz | -111.9 dBc/Hz |
| 100kHz | -113.0 dBc/Hz |

- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

## PIN ASSIGNMENT




**ICS843001-21**
**24-Lead TSSOP**
4.40mm x 7.8mm x 0.92mm
package body
**G Package**
Top View

## BLOCK DIAGRAM

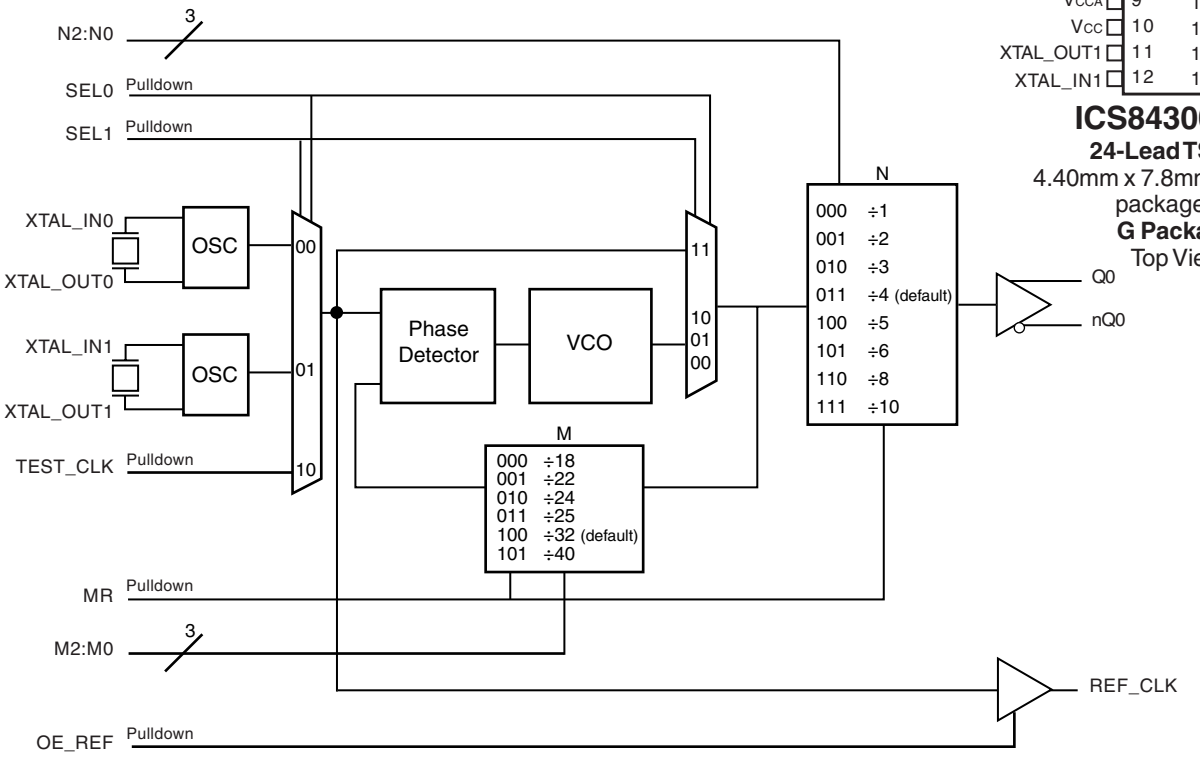


**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | $V_{CCO\_CMOS}$ | Power | | Output supply pin for LVCMOS output. |
| 2, 3 | N0, N1 | Input | Pullup | Output divider select pins. Default ÷4. LVCMOS/LVTTL interface levels. |
| 4 | N2 | Input | Pulldown | |
| 5 | $V_{CCO\_LVPECL}$ | Power | | Output supply pin for LVPECL output. |
| 6, 7 | Q0, nQ0 | Ouput | | Differential output pair. LVPECL interface levels. |
| 8, 23 | $V_{EE}$ | Power | | Negative supply pin. |
| 9 | $V_{CCA}$ | Power | | Analog supply pin. |
| 10 | $V_{CC}$ | Power | | Core supply pin. |
| 11<br>12 | XTAL_OUT1,<br>XTAL_IN1 | Input | | Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input. |
| 13<br>14 | XTAL_OUT0,<br>XTAL_IN0 | Input | | Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input. |
| 15 | TEST_CLK | Input | Pulldown | LVCMOS/LVTTL clock input. |
| 16, 17 | SEL0, SEL1 | Input | Pulldown | Input MUX select pins. LVCMOS/LVTTL interface levels. |
| 18 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q0 to go low and the inverted output nQ0 to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 19, 20 | M0, M1 | Input | Pulldown | Feedback divider select pins. Default ÷32. LVCMOS/LVTTL interface levels. |
| 21 | M2 | Input | Pullup | |
| 22 | REF_OE | Input | Pulldown | Reference clock output enable. Default Low. LVCMOS/LVTTL interface levels. |
| 24 | REF_CLK | Output | | Reference clock output. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{out}$ | Output Impedance | | | 7 | | Ω |

**TABLE 3A. COMMON CONFIGURATIONS TABLE**

| Input Reference Clock | M Divider Value | N Divider Value | VCO (MHz) | Output Frequency (MHz) | Application |
|---|---|---|---|---|---|
| 27 | 22 | 8 | 594 | 74.25 | HDTV |
| 24.75 | 24 | 8 | 594 | 74.25 | HDTV |
| 14.8351649 | 40 | 8 | 593.4066 | 74.1758245 | HDTV |
| 19.44 | 32 | 4 | 622.08 | 155.52 | SONET |
| 19.44 | 32 | 8 | 622.08 | 77.76 | SONET |
| 19.44 | 32 | 1 | 622.08 | 622.08 | SONET |
| 19.44 | 32 | 2 | 622.08 | 311.04 | SONET |
| 19.53125 | 32 | 4 | 625 | 156.25 | 10 GigE |
| 25 | 25 | 5 | 625 | 125 | 1 GigE |
| 25 | 25 | 10 | 625 | 62.5 | 1 GigE |
| 25 | 24 | 6 | 600 | 100 | PCI Express |
| 25 | 24 | 4 | 600 | 150 | SATA |
| 25 | 24 | 8 | 600 | 75 | SATA |
| 26.5625 | 24 | 6 | 637.5 | 106.25 | Fibre Channel 1 |
| 26.5625 | 24 | 3 | 637.5 | 212.5 | 4 Gig Fibre Channel |
| 26.5625 | 24 | 4 | 637.5 | 159.375 | 10 Gig Fibre Channel |
| 31.25 | 18 | 3 | 562.5 | 187.5 | 12 Gig Ethernet |

**TABLE 3B. PROGRAMMABLE M OUTPUT DIVIDER FUNCTION TABLE**

| Inputs | | | M Divider Value | Input Frequency | |
|---|---|---|---|---|---|
| M2 | M1 | M0 | | Minimum | Maximum |
| 0 | 0 | 0 | 18 | 31.1 | 38.9 |
| 0 | 0 | 1 | 22 | 25.5 | 31.8 |
| 0 | 1 | 0 | 24 | 23.3 | 29.2 |
| 0 | 1 | 1 | 25 | 22.4 | 28.0 |
| 1 | 0 | 0 | 32 | 17.5 | 21.9 |
| 1 | 0 | 1 | 40 | 14.0 | 17.5 |

**TABLE 3C. PROGRAMMABLE N OUTPUT DIVIDER FUNCTION TABLE**

| Inputs | | | N Divide Value |
|---|---|---|---|
| N2 | N1 | N0 | |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 8 |
| 1 | 1 | 1 | 10 |

**TABLE 3D. BYPASS MODE FUNCTION TABLE**

| Inputs | | Reference | PLL Mode |
|---|---|---|---|
| SEL1 | SEL0 | | |
| 0 | 0 | XTAL0 | Active |
| 0 | 1 | XTAL1 | Active |
| 1 | 0 | TEST_CLK | Active |
| 1 | 1 | TEST_CLK | Bypass |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$ (LVPECL) | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Outputs, $V_O$ (LVCMOS) | -0.5V to $V_{CCO}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 70°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCO\_PECL, \_CMOS}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 170 | mA |
| $I_{CCA}$ | Analog Supply Current | | | | 11 | mA |
| $I_{CCO\_PECL, \_CMOS}$ | Output Supply Current | | | | 8 | mA |

**TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | SEL0, SEL1, OE_REF, MR, M0:M2, N0:N2 | | -0.3 | | 0.8 | V |
| | | TEST_CLK | | -0.3 | | 1.3 | V |
| $I_{IH}$ | Input High Current | TEST_CLK, SEL0, SEL1, OE_REF, MR, M0, M1, N2 | $V_{CC} = V_{IN}$ = 3.465V | | | 150 | µA |
| | | M2, N0, N1 | $V_{CC} = V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | TEST_CLK, SEL0, SEL1, OE_REF, MR, M0, M1, N2 | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | M2, N0, N1 | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{OH}$ | Output High Voltage; NOTE 1 | | REF_CLK | 2.6 | | | V |
| $V_{OL}$ | Output Low Voltage: Note 1 | | REF_CLK | | | 0.5 | V |

NOTE 1: Output terminated with 50Ω to $V_{CCO\_CMOS}$/2. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit Diagram".

**TABLE 4C. LVPECL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO}$ - 1.4 | | $V_{CCO}$ - 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO}$ - 2.0 | | $V_{CCO}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO\_PECL}$ - 2V.

**TABLE 5. CRYSTAL CHARACTERISTICS**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | MHz |
| Frequency | | 12 | | 40 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

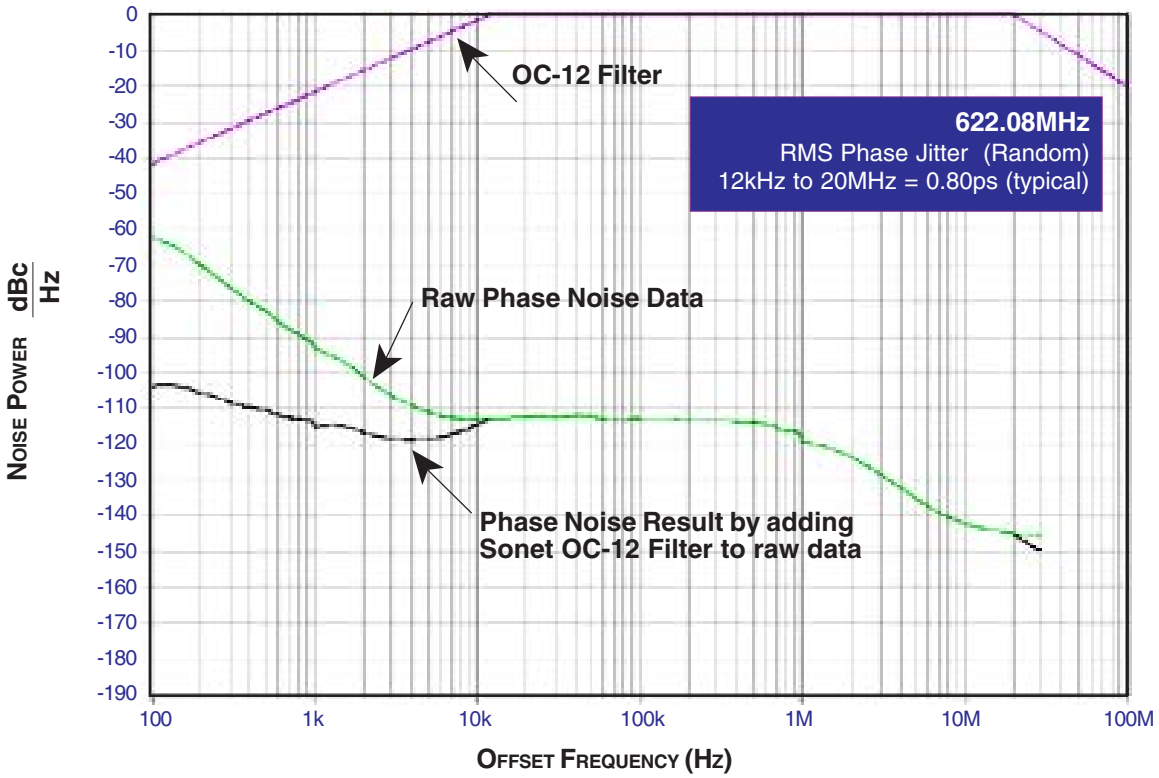
NOTE: Characterized using an 18pF parallel resonant crystal.

**TABLE 6. AC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

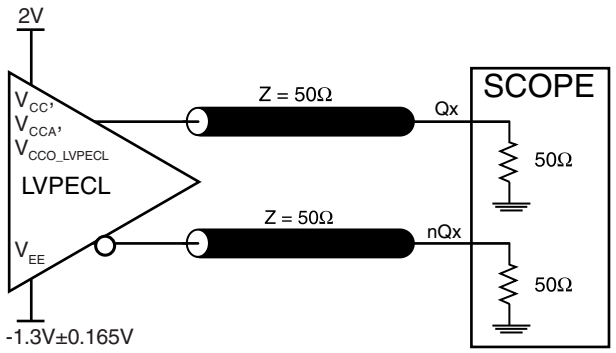
| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | | | 56 | | 700 | MHz |
| $t_{PD}$ | Propagation Delay, NOTE 1 | TEST_CLK to REF_CLK | | 2.3 | | 2.8 | ns |
| *t*jit(Ø) | RMS Phase Jitter, (Random); NOTE 2, 3 | | 622.08MHz (12kHz - 20MHz) | | 0.80 | | ps |
| $f_{VCO}$ | PLL VCO Lock Range | | | 560 | | 700 | MHz |
| $t_R$ / $t_F$ | Output Rise/Fall Time | LVPECL | 20% to 80% | 200 | | 500 | ps |
| | | LVCMOS | 20% to 80% | 300 | | 800 | ps |
| odc | Output Duty Cycle | LVPECL | | 45 | | 55 | % |
| | | LVCMOS | | 44 | | 56 | % |

NOTE 1: Measured from the $V_{CC}$/2 of the input to $V_{CCO\_CMOS}$/2 of the output.
NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

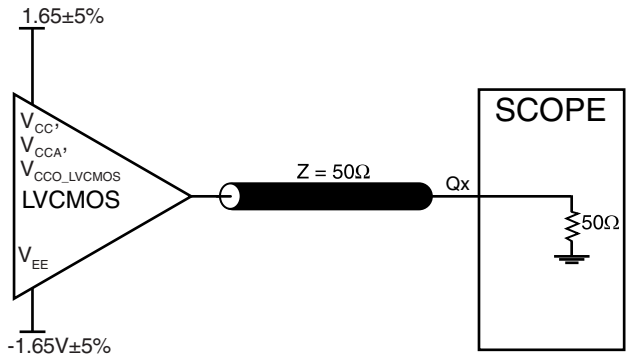
## TYPICAL PHASE NOISE AT 622.08MHZ



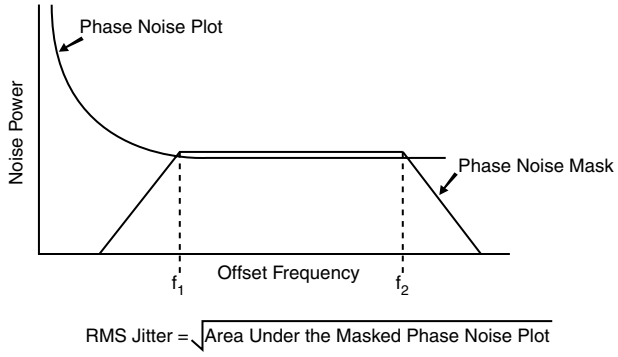
# PARAMETER MEASUREMENT INFORMATION



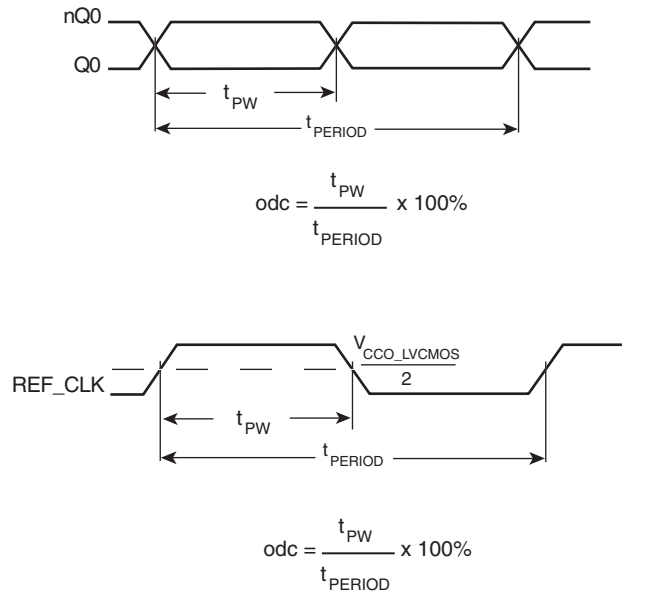

**3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT**



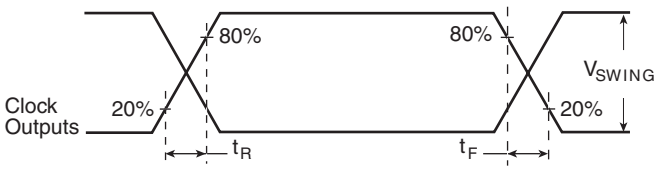

**3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT**



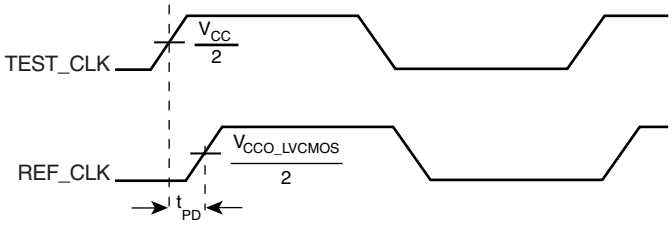

**RMS PHASE JITTER**




**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**




**OUTPUT RISE/FALL TIME**




**PROPAGATION DELAY**

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843001-21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$, $V_{CCA}$, and $V_{CCO\_x}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each $V_{CCA}$. The 10Ω resistor can also be replaced by a ferrite bead.

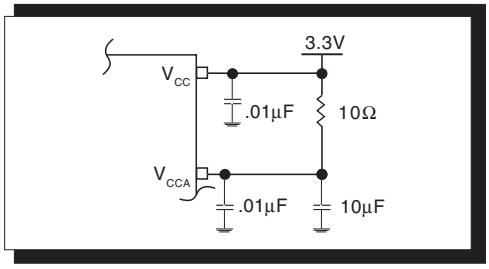



**FIGURE 1. POWER SUPPLY FILTERING**

## CRYSTAL INPUT INTERFACE

The ICS843001-21 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 19.44MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

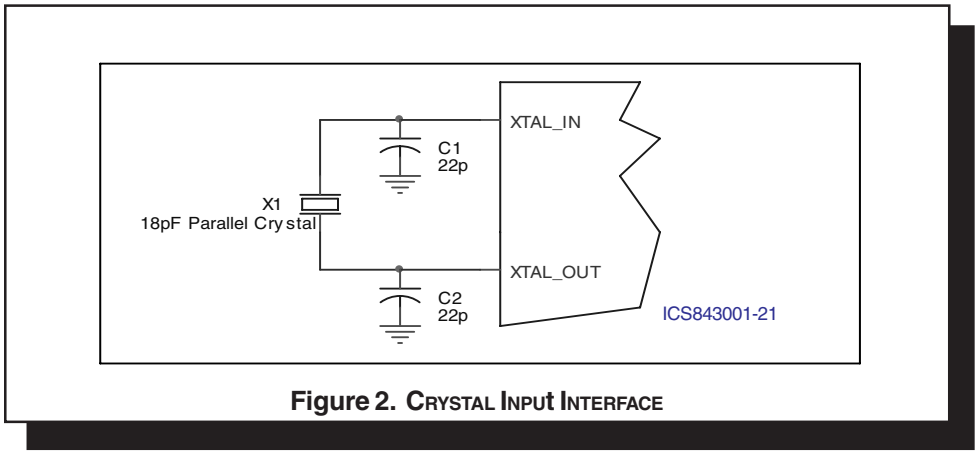



**Figure 2. CRYSTAL INPUT INTERFACE**

## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

**CRYSTAL INPUT:**
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

**TEST_CLK INPUT:**
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

**LVCMOS CONTROL PINS:**
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### OUTPUTS:

**LVCMOS OUTPUT:**
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

**LVPECL OUTPUT**
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

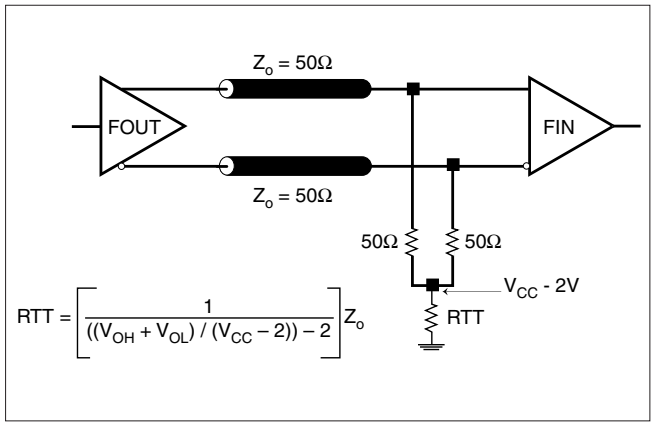



**FIGURE 3A. LVPECL OUTPUT TERMINATION**

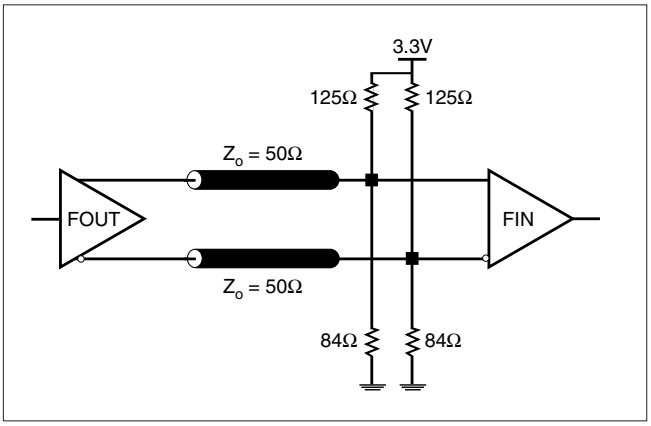



**FIGURE 3B. LVPECL OUTPUT TERMINATION**

# POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843001-21. Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the ICS843001-21 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.
**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 170mA = **589.05mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

**Total Power$_{_MAX}$** (3.465V, with all outputs switching) = 589.05mW + 30mW = **619.05mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.619W * 65°C/W = 110.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 7. THERMAL RESISTANCE $\theta_{JA}$ FOR 24-PIN TSSOP, FORCED CONVECTION**

| $\theta_{JA}$ by Velocity (Meters per Second) | | | |
|---|---|---|---|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 70°C/W | 65°C/W | 62°C/W |

*3. Calculations and Equations.*
The purpose of this section is to derive the power dissipated into the load.
LVPECL output driver circuit and termination are shown in *Figure 4.*

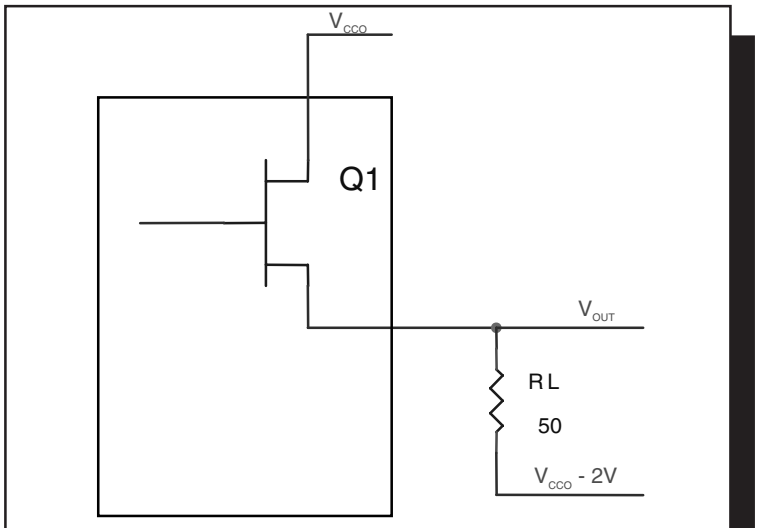



**FIGURE 4. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC}$ - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

# RELIABILITY INFORMATION

**TABLE 8. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 24 LEAD TSSOP**

| $\theta_{JA}$ by Velocity (Meters per Second) | | | |
|---|---|---|---|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 70°C/W | 65°C/W | 62°C/W |

**TRANSISTOR COUNT**

The transistor count for ICS843001-21 is: 4057

## PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

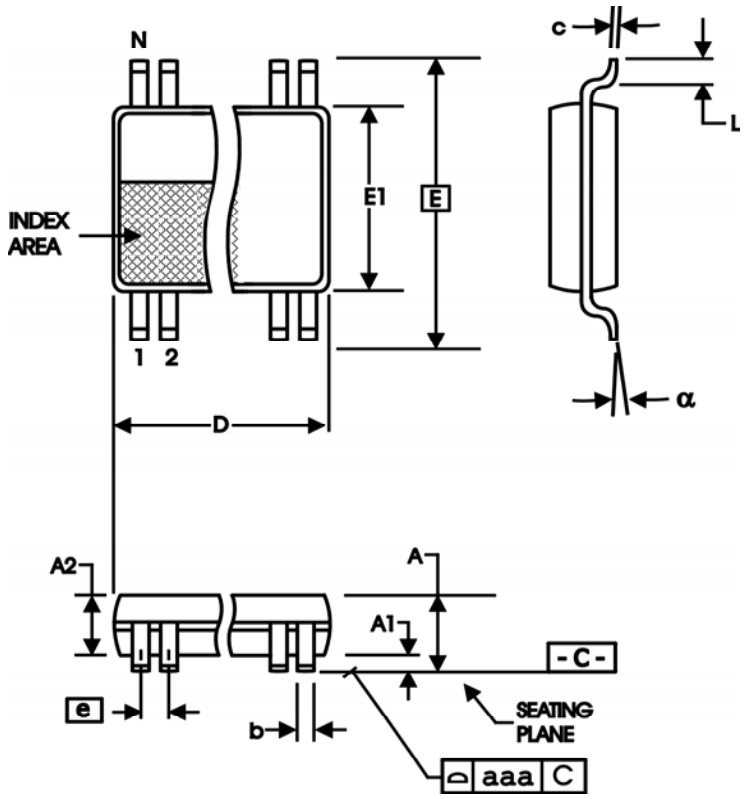



**TABLE 9. PACKAGE DIMENSIONS**

| SYMBOL | Millimeters | |
|---|---|---|
| | Minimum | Maximum |
| N | 24 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 7.70 | 7.90 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

**TABLE 10. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| ICS843001AG-21 | ICS843001A21 | 24 Lead TSSOP | tube | 0°C to 70°C |
| ICS843001AG-21T | ICS843001A21 | 24 Lead TSSOP | 2500 tape & reel | 0°C to 70°C |
| ICS843001AG-21LF | ICS843001A21L | 24 Lead "Lead-Free" TSSOP | tube | 0°C to 70°C |
| ICS843001AG-21LFT | ICS843001A21L | 24 Lead "Lead-Free" TSSOP | 2500 tape & reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

| REVISION HISTORY SHEET | | | | |
|---|---|---|---|---|
| **Rev** | **Table** | **Page** | **Description of Change** | **Date** |
| A | | 1 | Features Section - added Lead-Free bullet. | 2/8/05 |
| | T10 | 14 | Ordering Information table - added Lead-Free marking. | |
| A | T3C | 3 | Programmable N Output Divider Function Table - corrected heading from *M Divide Value* to *N Divide value.* | 10/26/05 |
| | | 9 | Added *Recommendations for Unused Input and Output Pins.* | |
| | T10 | 10 | Ordering Information Table - added lead-free note. | |
| | | | | |