

TPS3840 Nano Power, High Input Voltage Supervisor With $\overline{\text{MR}}$ and Programmable Delay

1 Features

- Wide Operating Voltage : 1.5 V to 10 V
- Nano Supply Current : 350 nA (Typical)
- Fixed Threshold Voltage ($V_{\text{IT-}}$)
 - Threshold From 1.6 V to 4.9 V in 0.1-V steps
 - High Accuracy: 1% (Typical)
 - Built-in Hysteresis ($V_{\text{IT+}}$)
 - $1.6 \text{ V} < V_{\text{IT-}} \leq 3.1 \text{ V} = 100 \text{ mV}$ (Typical)
 - $3.2 \text{ V} \leq V_{\text{IT-}} < 4.9 \text{ V} = 200 \text{ mV}$ (Typical)
- Reset Time Delay (t_{D}): Capacitor-Based Programmable
 - Minimum Time Delay: 80 μs (Maximum) Without Capacitor
- Active-Low Manual Reset ($\overline{\text{MR}}$)
- Three Output Topologies:
 - TPS3840DL: Open-Drain, Active-Low ($\overline{\text{RESET}}$)
 - TPS3840PL: Push-Pull, Active-Low ($\overline{\text{RESET}}$)
 - TPS3840PH: Push-Pull, Active-High (RESET)
- Wide Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Package: SOT23-5 (DBV)

2 Applications

- Grid Infrastructure: Circuit Breaker, Smart Meter, Other Monitoring and Protection Equipment
- Factory Automation: Field Transmitter, PLC.
- Building Automation: Fire Safety, Smoke Detector, and HVAC
- Electronic Point of Sale
- Portable, Battery-Powered systems

3 Description

The TPS3840 family of voltage supervisors or reset ICs can operate at high voltage levels while maintaining very low quiescent current across the whole V_{DD} and temperature range. TPS3840 offers best combination of low power consumption, high accuracy and low propagation delay ($t_{\text{p_HL}} = 30 \mu\text{s}$ typical).

Reset output signal is asserted when the voltage at VDD drops below the negative voltage threshold ($V_{\text{IT-}}$) or when manual reset is pulled to a low logic ($V_{\overline{\text{MR_L}}}$). Reset signal is cleared when V_{DD} rise above $V_{\text{IT-}}$ plus hysteresis ($V_{\text{IT+}}$) and manual reset ($\overline{\text{MR}}$) is floating or above $V_{\overline{\text{MR_H}}}$ and the reset time delay (t_{D}) expires. Reset time delay can be programmed by connecting a capacitor between CT pin and ground. For a fast reset CT pin can be left floating.

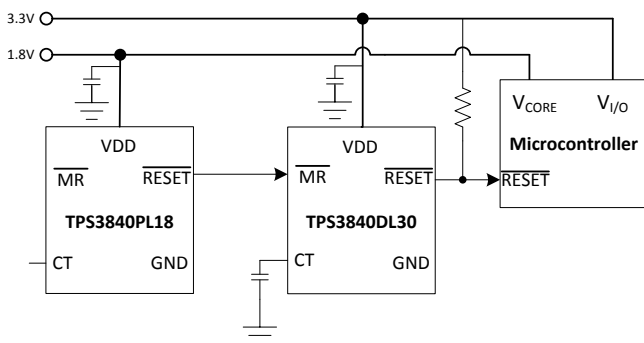
Additional features: Low power-on reset voltage (V_{POR}), built-in glitch immunity protection for $\overline{\text{MR}}$ and VDD, built-in hysteresis, low open-drain output leakage current ($I_{\text{LKG(OD)}}$). TPS3840 is a perfect voltage monitoring solution for industrial applications and battery-powered / low power applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3840	SOT-23 (5) (DBV)	2.90 mm x 1.60 mm

(1) For package details, see the mechanical drawing addendum at the end of the data sheet.

Typical Application Circuit



TPS3840 Typical Supply Current

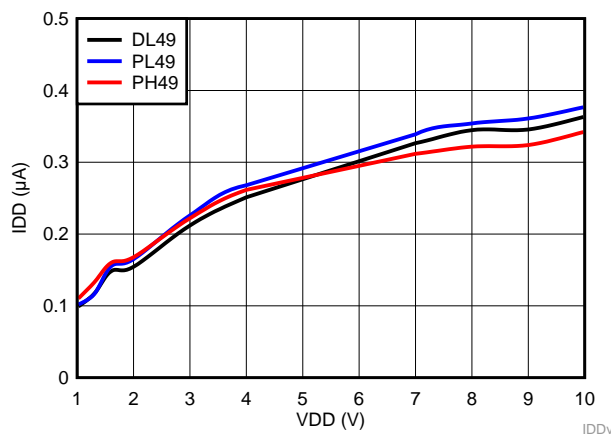


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2018	*	Initial release

5 Device Comparison Table

Device Comparison Table shows the variants planned to release at RTM, however other voltages from [Table 3](#) at the end of datasheet can be sample upon request, please contact TI sales representative for details.

PART NUMBER	OUTPUT TOPOLOGY	THRESHOLD (V_{it}) (V)	HYSTERESIS (mV)
TPS3840DL20 ⁽¹⁾	Open-Drain, Active-Low	2	100
TPS3840PL25 ⁽²⁾	Push-Pull, Active-Low	2.5	100
TPS3840PL28 ⁽²⁾	Push-Pull, Active-Low	2.8	100
TPS3840PH30 ⁽³⁾	Push-Pull, Active-High	3.0	100
TPS3840DL27 ⁽¹⁾	Open-Drain, Active-Low	2.7	100
TPS3840DL29 ⁽¹⁾	Open-Drain, Active-Low	2.9	100

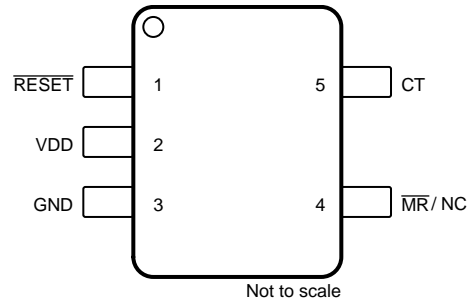
(1) TPS3840DL: Open-Drain, Active-Low ($\overline{\text{RESET}}$)

(2) TPS3840PL: Push-Pull, Active-Low ($\overline{\text{RESET}}$)

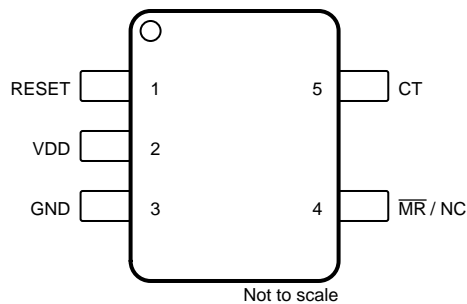
(3) TPS3840PH: Push-Pull, Active-High ($\overline{\text{RESET}}$)

6 Pin Configuration and Functions

**DBV Package
5-Pin WSON
TPS3840PL, TPS3840DL Top View**



**DBV Package
5-Pin WSON
TPS3840PH Top View**



Pin Functions

PIN		I/O	DESCRIPTION	
NAME	TPS3840PL, TPS3840DL			TPS3840PH
RESET	N/A	1	O	Active-High Output Reset Signal: This pin is driven high when either the $\overline{\text{MR}}$ pin is driven to a logic low or VDD voltage falls below the negative voltage threshold (V_{IT-}). RESET remains high (asserted) for the delay time period (t_D) after both $\overline{\text{MR}}$ is floating or above $V_{\overline{\text{MR}}_L}$ and VDD voltage rise above V_{IT+} .
$\overline{\text{RESET}}$	1	N/A	O	Active-Low Output Reset Signal: This pin is driven logic low when either the $\overline{\text{MR}}$ pin is driven to a logic low or VDD voltage falls below the negative voltage threshold (V_{IT-}). $\overline{\text{RESET}}$ remains low (asserted) for the delay time period (t_D) after both $\overline{\text{MR}}$ is floating or above $V_{\overline{\text{MR}}_L}$ and VDD voltage rise above V_{IT+} .
VDD	2	2	I	Input Supply Voltage. TPS3840 monitors VDD voltage
GND	3	3	–	Ground
$\overline{\text{MR}}$ / NC	4	4	I	Manual Reset. Pull this pin to a logic low ($V_{\overline{\text{MR}}_L}$) to assert a reset signal in the output pin. After the $\overline{\text{MR}}$ pin is left floating or pull to $V_{\overline{\text{MR}}_H}$ the output goes to the nominal state after the reset delay time (t_D) expires. $\overline{\text{MR}}$ can be left floating when not in use. NC stands for "No Connection" or floating.
CT	5	5	–	Capacitor Time Delay Pin. The CT pin offers a user-programmable delay time. Connect an external capacitor on this pin to adjust time delay. When not in use leave pin floating for the smallest fixed time delay.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted⁽¹⁾

		MIN	MAX	UNIT
Voltage	VDD	-0.3	12	V
	$\overline{\text{RESET}}$ (TPS3840PL)	-0.3	$V_{\text{DD}} + 0.3$	
	RESET (TPS3840PH)	-0.3	$V_{\text{DD}} + 0.3$	
	$\overline{\text{RESET}}$ (TPS3840DL)	-0.3	12	
	$\overline{\text{MR}}$ ⁽²⁾	-0.3	12	
	CT	-0.3	5.5	
Current	$\overline{\text{RESET}}$ pin and RESET pin		± 70	mA
Temperature ⁽³⁾	Operating junction temperature, T_{J}	-40	125	°C
	Storage, T_{stg}	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) If the logic signal driving MR is less than V_{DD} , then additional current flows into V_{DD} and out of MR. V_{MR} should not be higher than V_{DD} .
- (3) As a result of the low dissipated power in this device, it is assumed that $T_{\text{J}} = T_{\text{A}}$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{\text{(ESD)}}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Input supply voltage	1.5		10	V
$V_{\overline{\text{RESET}}}, V_{\text{RESET}}$	$\overline{\text{RESET}}$ pin and RESET pin voltage	0		10	V
$I_{\overline{\text{RESET}}}, I_{\text{RESET}}$	$\overline{\text{RESET}}$ pin and RESET pin current	0		± 5	mA
T_{J}	Junction temperature (free air temperature)	-40		125	°C
$V_{\overline{\text{MR}}}$ ⁽¹⁾	Manual reset pin voltage	0		V_{DD}	V

- (1) If the logic signal driving MR is less than V_{DD} , then additional current flows into V_{DD} and out of MR. V_{MR} should not be higher than V_{DD} .

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3840	UNIT
		DBV (SOT23-5)	
		5 PINS	
$R_{\theta\text{JA}}$	Junction-to-ambient thermal resistance	187.5	°C/W
$R_{\theta\text{JC(top)}}$	Junction-to-case (top) thermal resistance	109.2	°C/W
$R_{\theta\text{JB}}$	Junction-to-board thermal resistance	92.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	35.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	92.5	°C/W
$R_{\theta\text{JC(bot)}}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

At $1.5\text{ V} \leq V_{DD} \leq 10\text{ V}$, $CT = \overline{MR} = \text{Open}$, \overline{RESET} pull-up resistor ($R_{pull-up}$) = 100 k Ω to VDD, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage		1.5		10	V
V_{IT-}	Negative-going input threshold accuracy ⁽¹⁾	-40°C to 125°C	-2.5	1	2.5	%
		-40°C to 105°C	-1.5	1	1.5	%
V_{HYS}	Hysteresis on V_{IT-} pin	$V_{IT-} = 1.6\text{ V to }3.1\text{ V}$	75	100	125	mV
		$V_{IT-} = 3.2\text{ V to }4.9\text{ V}$	150	200	250	mV
I_{DD}	Supply current into VDD pin	$V_{DD} = 1.5\text{ V} < V_{DD} < 10\text{ V}$ $V_{DD} > V_{IT+}$ ⁽²⁾ $T_A = -40^\circ\text{C to }125^\circ\text{C}$		0.35	1	μA
		$V_{DD} = 1.5\text{ V} < V_{DD} < 5.5\text{ V}$ $V_{DD} > V_{IT+}$ ⁽²⁾ $T_A = -40^\circ\text{C to }85^\circ\text{C}$		350	500	nA
$V_{\overline{MR}_L}$	Manual reset logic low input ⁽³⁾				300	mV
$V_{\overline{MR}_H}$	Manual reset logic high input ⁽³⁾		$0.8V_{DD}$			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance			100		k Ω
R_{CT}	CT pin internal resistance			500		k Ω
VARIANT-SPECIFIC PARAMETERS						
V_{POR}	TPS3840PL (Push-Pull Active-Low)	Power on Reset Voltage ⁽⁴⁾	$V_{OL(max)} = 200\text{ mV}$ $I_{OUT(Sink)} = 200\text{ nA}$		300	mV
V_{OL}		Low level output voltage	$1.5\text{ V} < V_{DD} < 5\text{ V}$ $V_{DD} < V_{IT-}$ $I_{OUT(Sink)} = 2\text{ mA}$		200	mV
V_{OH}		High level output voltage	$1.5\text{ V} < V_{DD} < 5\text{ V}$ $V_{DD} > V_{IT+}$ ⁽²⁾ $I_{OUT(Source)} = 2\text{ mA}$	$0.8V_{DD}$		V
V_{OH}		High level output voltage	$5\text{ V} < V_{DD} < 10\text{ V}$ $V_{DD} > V_{IT+}$ ⁽²⁾ $I_{OUT(Source)} = 5\text{ mA}$	$0.8V_{DD}$		V
V_{POR}	TPS3840PH (Push-Pull Active-High)	Power on Reset Voltage ⁽⁴⁾	$V_{OH}, I_{OUT(Source)} = 500\text{ nA}$		920	mV
V_{OL}		Low level output voltage	$1.5\text{ V} < V_{DD} < 5\text{ V}$ $V_{DD} > V_{IT+}$ ⁽²⁾ $I_{OUT(Sink)} = 2\text{ mA}$		200	mV
V_{OL}		Low level output voltage	$1.5\text{ V} < V_{DD} < 5\text{ V}$ $V_{DD} > V_{IT+}$ ⁽²⁾ $I_{OUT(Sink)} = 5\text{ mA}$		200	mV
V_{OH}		High level output voltage	$1.5\text{ V} < V_{DD} < 5\text{ V}, V_{DD} < V_{IT-}$ $I_{OUT(Source)} = 2\text{ mA}$	$0.8V_{DD}$		V
V_{POR}	TPS3840DL (Open-Drain)	Power on Reset Voltage ⁽⁴⁾	$V_{OL(max)} = 0.2\text{ V}$ $I_{OUT(Sink)} = 5.6\text{ uA}$		900	mV
V_{OL}		Low level output voltage	$1.5\text{ V} < V_{DD} < 5\text{ V}$ $V_{DD} < V_{IT-}$ $I_{OUT(Sink)} = 2\text{ mA}$		200	mV
$I_{lkq(OD)}$		Open-Drain output leakage current	\overline{RESET} pin in High Impedance, $V_{DD} = V_{RESET} = 5.5\text{ V}$ $V_{IT+} < V_{DD}$		90	nA

(1) V_{IT-} threshold voltage range from 1.6 V to 4.9 V in 100 mV steps, for released versions see Device Voltage Thresholds table.

(2) $V_{IT+} = V_{HYS} + V_{IT-}$.

(3) If the logic signal driving \overline{MR} is less than VDD, then additional current flows into VDD and out of \overline{MR} .

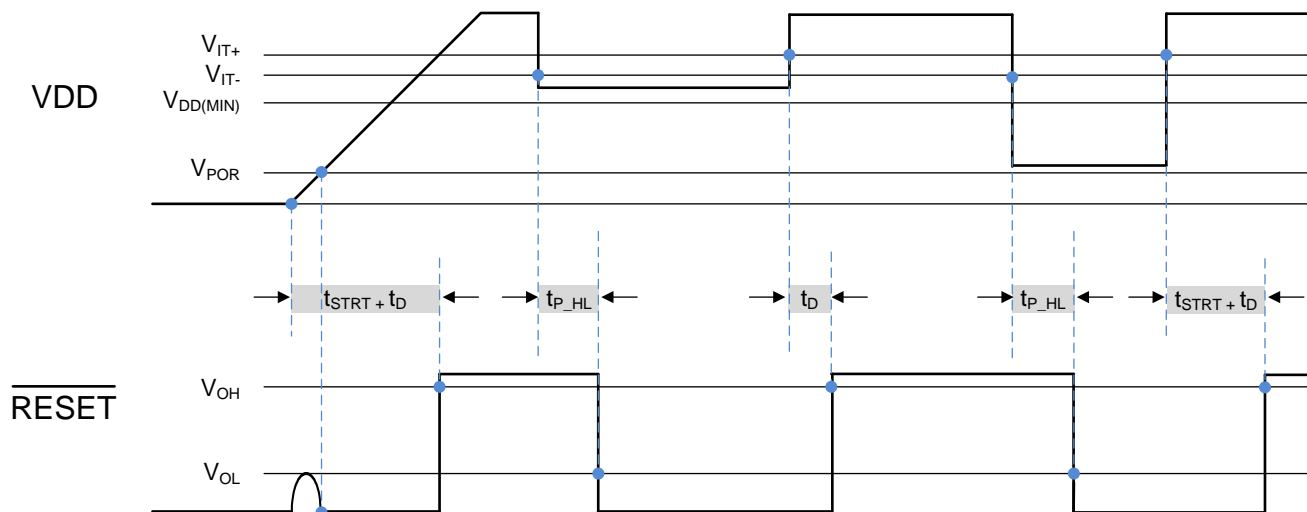
(4) V_{POR} is the minimum V_{DD} voltage level for a controlled output state. V_{DD} slew rate $\leq 100\text{mV}/\mu\text{s}$.

7.6 Timing Requirements

At $1.5\text{ V} \leq V_{DD} \leq 10\text{ V}$, $CT = \overline{MR} = \text{Open}$, \overline{RESET} pull-up resistor ($R_{pull-up}$) = 100 k Ω to V_{DD} , output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup Delay ⁽¹⁾	CT pin open	TBD	220	TBD	μs
t_{P_HL}	Propagation detect delay for V_{DD} falling below V_{IT-}	$V_{DD} = V_{IT+}$ to $(V_{IT-}) - 10\%$ ⁽²⁾		30	50	μs
t_D	Reset time delay	CT pin = open			80	μs
		CT pin = 10 nF		6.2		ms
		CT pin = 1 μF		619		ms
t_{GL_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive ⁽³⁾		10		μs
t_{MR_PW}	\overline{MR} pin pulse duration to initiate reset			300		ns
t_{MR_RES}	Propagation delay from \overline{MR} low to reset	$V_{DD} = 4.5\text{ V}$, $\overline{MR} < V_{\overline{MR_L}}$		700		ns
t_{MR_tD}	Delay from release \overline{MR} to deassert reset	$V_{DD} = 4.5\text{ V}$, $\overline{MR} = V_{\overline{MR_L}}$ to $V_{\overline{MR_H}}$		t_D		ms

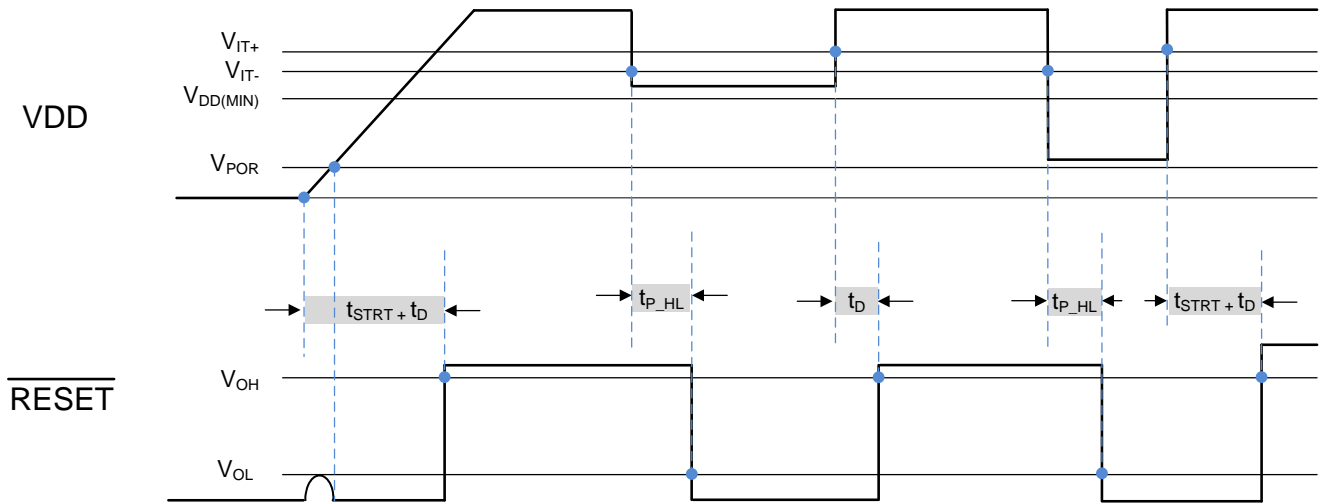
- (1) When V_{DD} starts from less than the specified minimum V_{DD} and then exceeds V_{IT-} , reset is release after the startup delay (t_{STRT}), a capacitor at CT pin will add t_D delay to t_{STRT} time
- (2) t_{P_HL} measured from threshold trip point (V_{IT-}) to V_{OL} for active low variants and V_{OH} for active high variants.
- (3) Overdrive % = $[(V_{DD}/V_{IT-}) - 1] \times 100\%$



- (1) $t_{D (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, V_{DD} slew rate = 100 mV / μs .
- (2) Open-Drain timing diagram assumes pull-up resistor is connected to \overline{RESET}

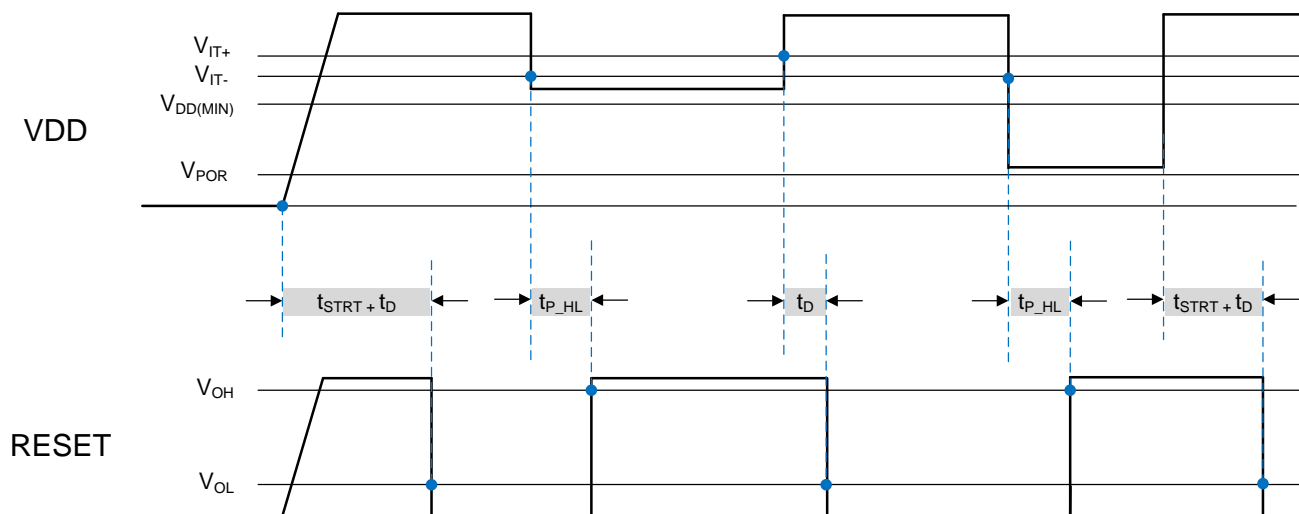
Figure 3. Timing Diagram TPS3840DL (Open-Drain Active-Low)

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- (3) t_D (no cap) is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin, then t_D programmed time will be added to the startup time. VDD slew rate = 100 mV / μ s.

Figure 4. Timing Diagram TPS3840PL (Push-Pull Active-Low)



- (4) t_D (no cap) is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin, then t_D programmed time will be added to the total startup time. VDD slew rate = 100 mV / μ s.

Figure 5. Timing Diagram TPS3840PH (Push-Pull Active-High)

7.7 Typical Characteristics

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $R_{pull-up} = 100\text{ k}\Omega$, $C_{Load} = 50\text{ pF}$, unless otherwise noted.

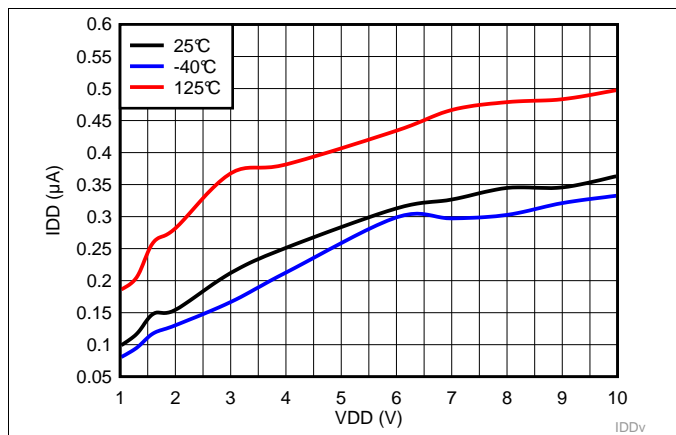


Figure 6. Supply Current vs Supply Voltage for TPS3840DL49

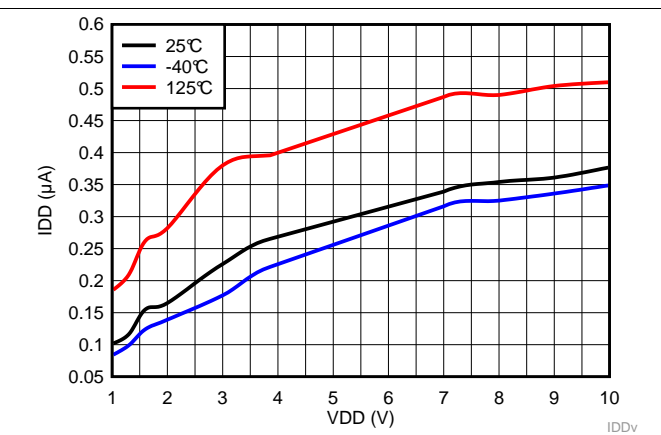


Figure 7. Supply Current vs Supply Voltage for TPS3840PL49

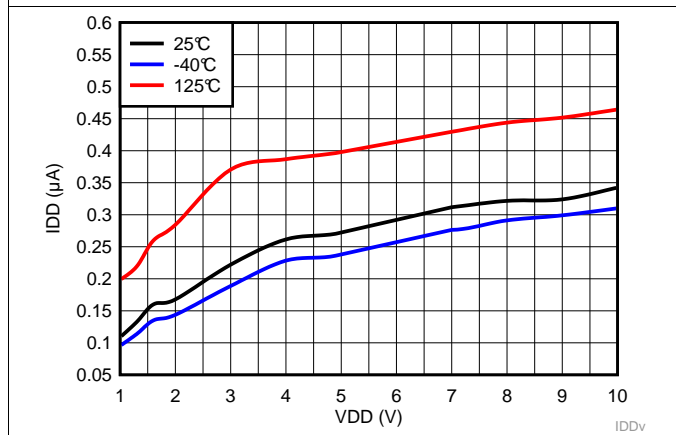


Figure 8. Supply Current vs Supply Voltage for TPS3840PH49

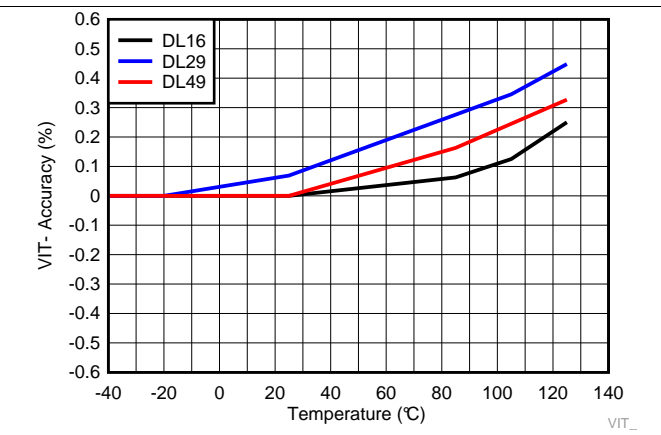


Figure 9. Negative-going Input Threshold Accuracy over Temperature for TPS3840DLXX

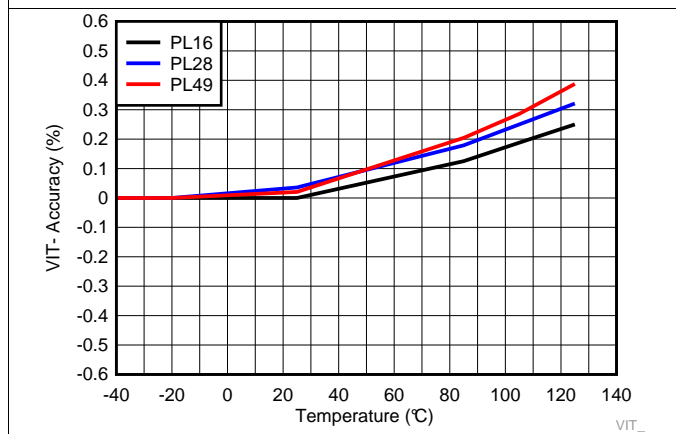


Figure 10. Negative-going Input Threshold Accuracy over Temperature for TPS3840PLXX

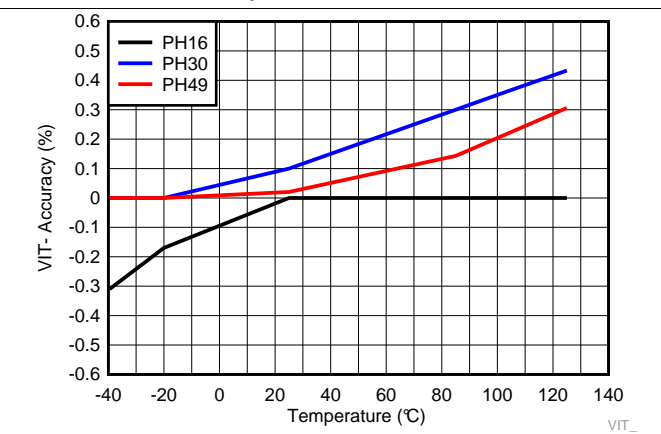


Figure 11. Negative-going Input Threshold Accuracy over Temperature for TPS3840PHXX

ADVANCE INFORMATION

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $R_{pull-up} = 100\text{ k}\Omega$, $C_{Load} = 50\text{ pF}$, unless otherwise noted.

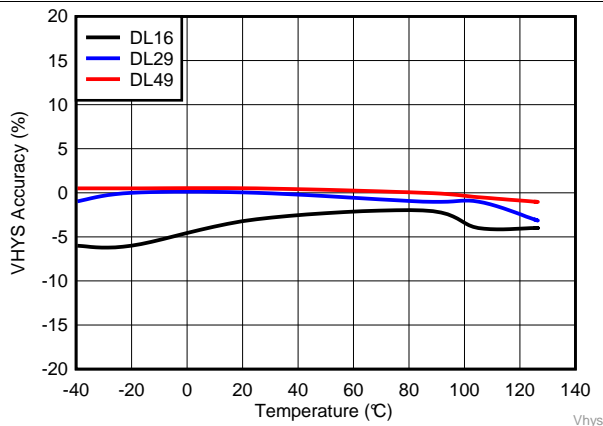


Figure 12. Input Threshold V_{IT} . Hysteresis Accuracy for TPS3840DLXX

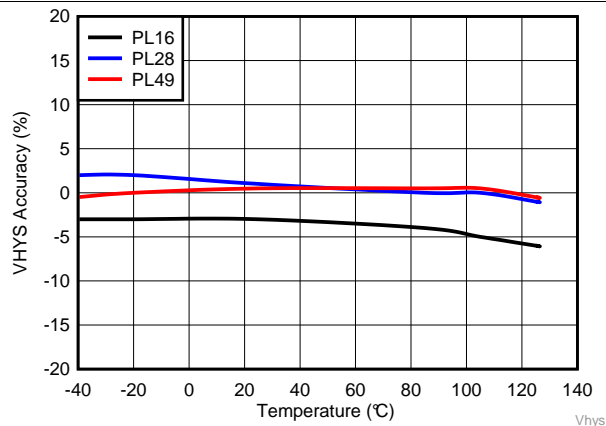


Figure 13. Input Threshold V_{IT} . Hysteresis Accuracy for TPS3840PLXX

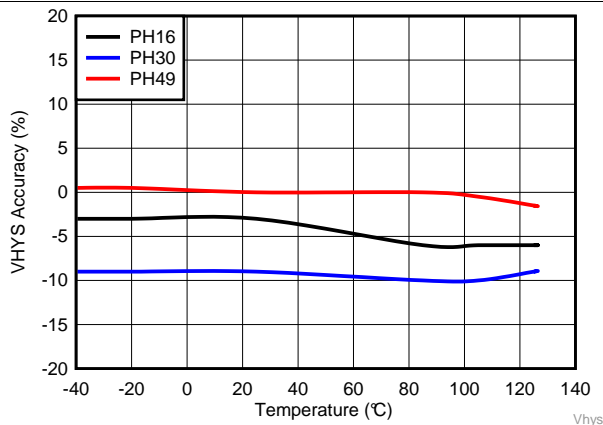


Figure 14. Input Threshold V_{IT} . Hysteresis Accuracy for TPS3840PHXX

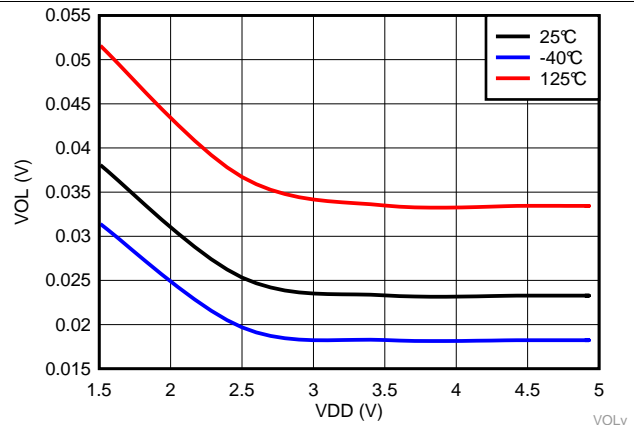


Figure 15. Low Level Output Voltage over Temperature for TPS3840DL49

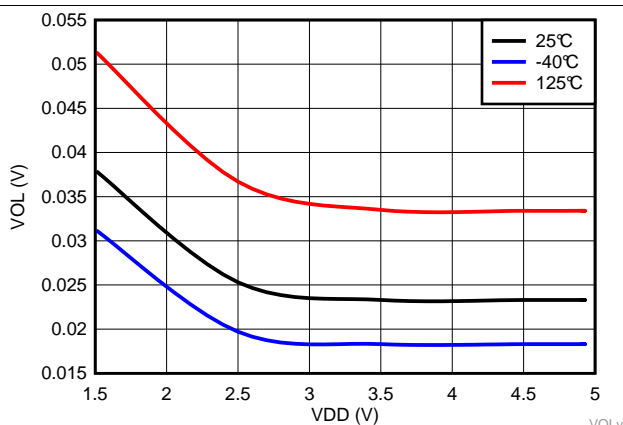


Figure 16. Low Level Output Voltage over Temperature for TPS3840PL49

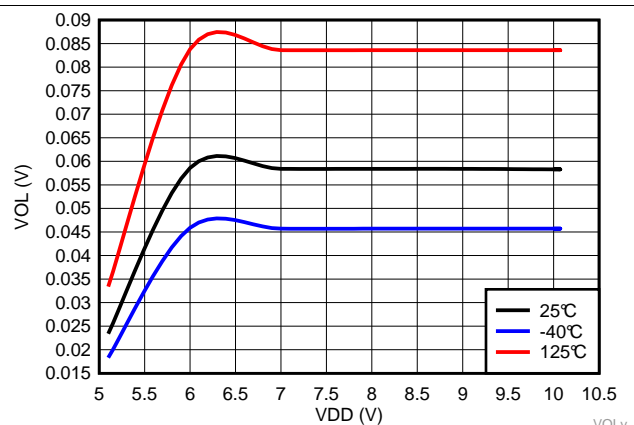


Figure 17. Low Level Output Voltage over Temperature for TPS3840PH49

ADVANCE INFORMATION

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $R_{\text{pull-up}} = 100\text{ k}\Omega$, $C_{\text{Load}} = 50\text{ pF}$, unless otherwise noted.

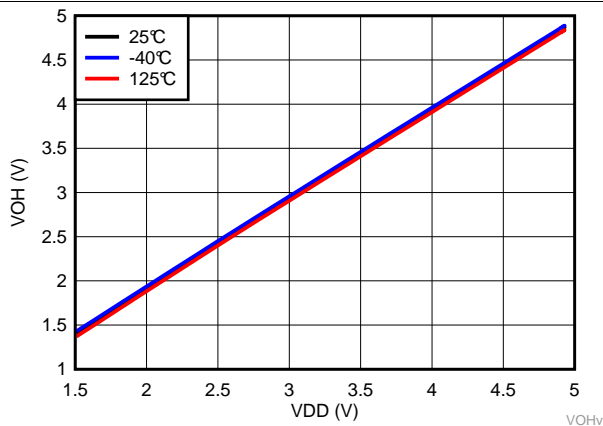


Figure 18. High Level Output Voltage over Temperature for TPS3840PL49

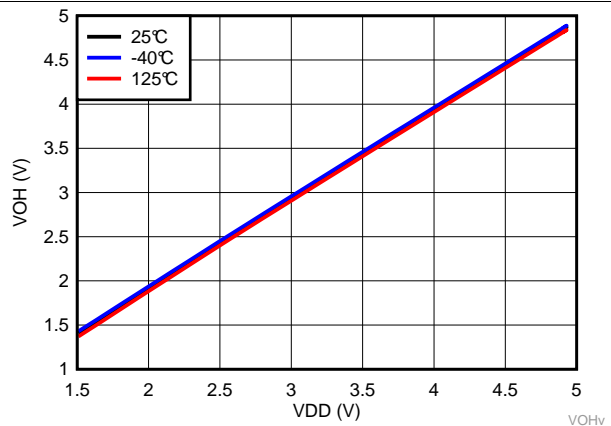


Figure 19. High Level Output Voltage over Temperature for TPS3840PH49

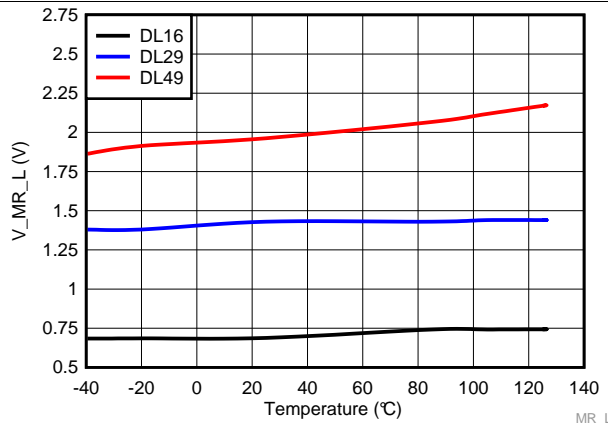


Figure 20. Manual Reset Logic Low Voltage Threshold over Temperature for TPS3840DLXX

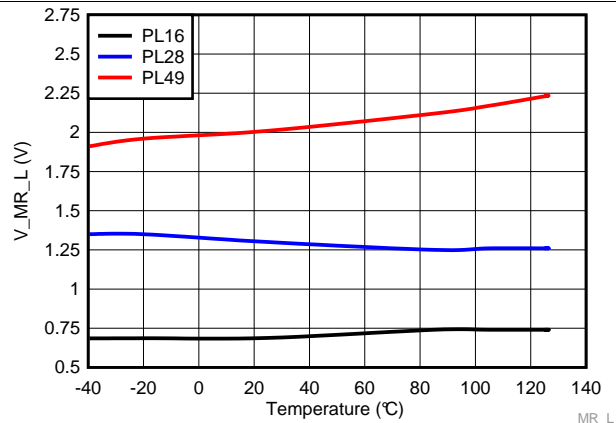


Figure 21. Manual Reset Logic Low Voltage Threshold over Temperature for TPS3840PLXX

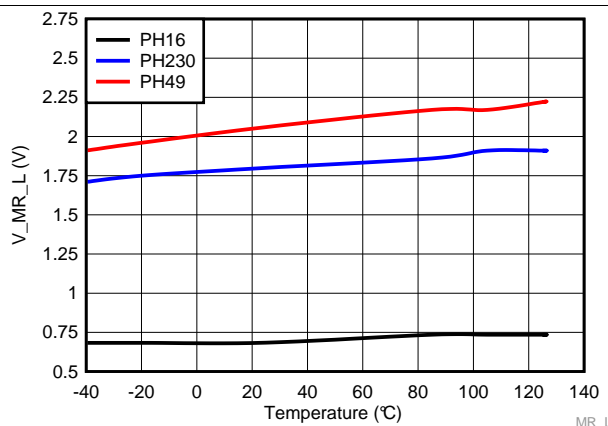


Figure 22. Manual Reset Logic Low Voltage Threshold over Temperature for TPS3840PHXX

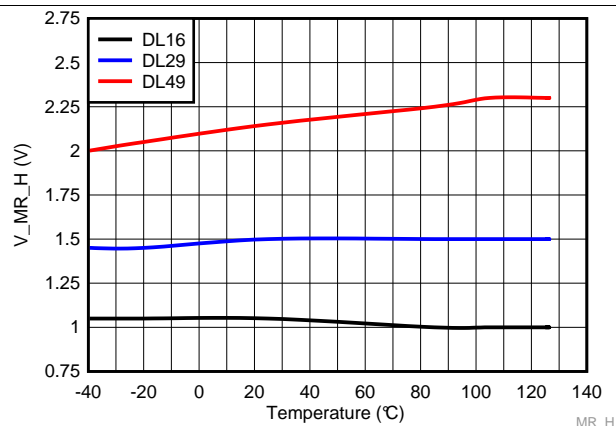


Figure 23. Manual Reset Logic High Voltage Threshold over Temperature for TPS3840DLXX

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $R_{pull-up} = 100\text{ k}\Omega$, $C_{Load} = 50\text{ pF}$, unless otherwise noted.

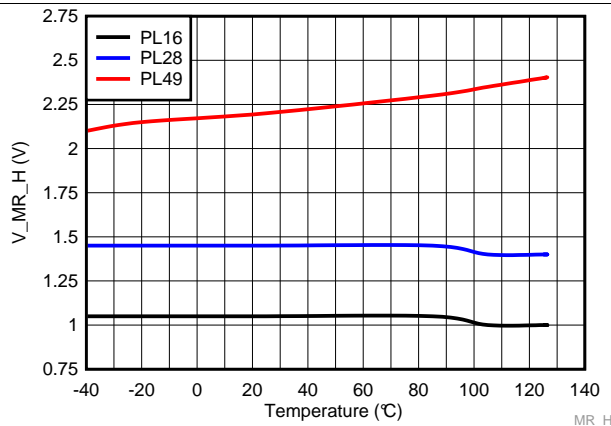


Figure 24. Manual Reset Logic High Voltage Threshold over Temperature for TPS3840PLXX

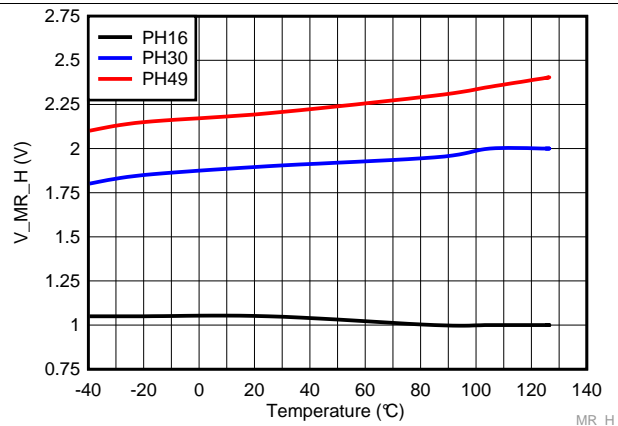


Figure 25. Manual Reset Logic High Voltage Threshold over Temperature for TPS3840PHXX

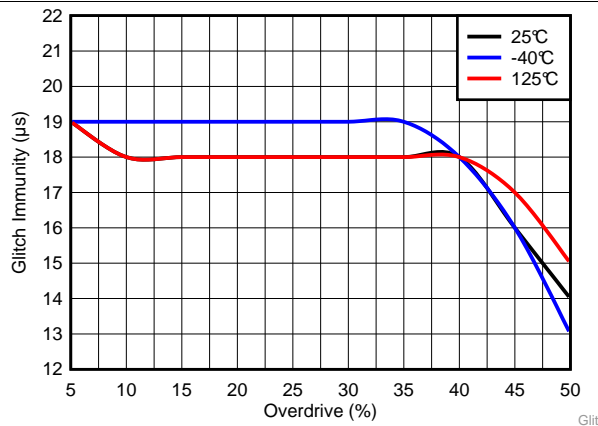


Figure 26. Glitch Immunity on V_{IT} vs Overdrive (Data Taken with TPS3840PL28)

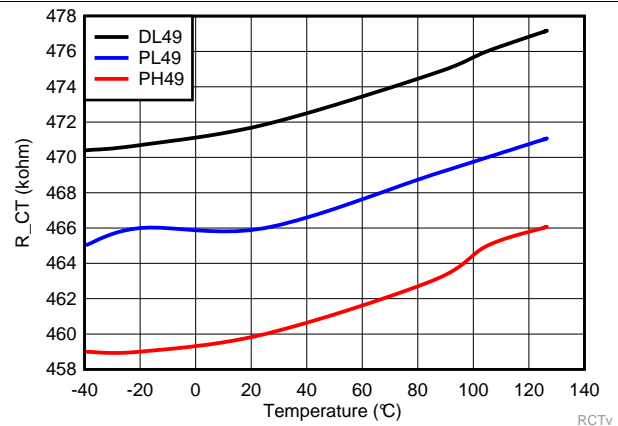


Figure 27. CT Pin Internal Resistance over Temperature

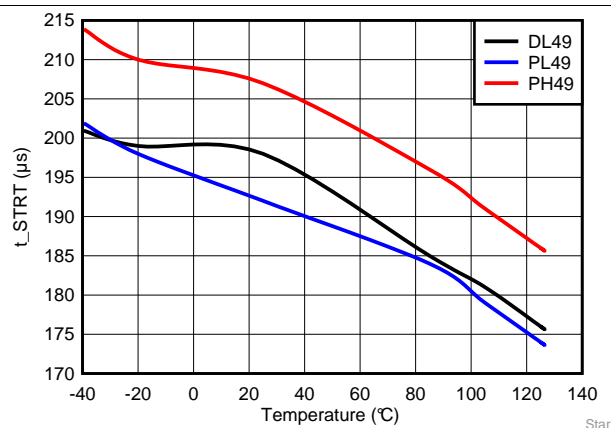


Figure 28. Startup Delay over Temperature

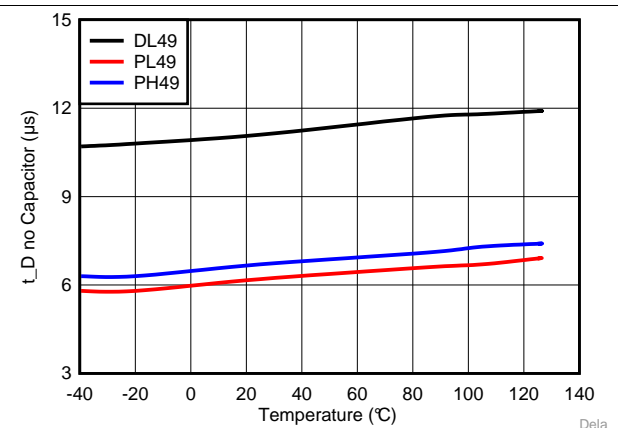


Figure 29. Reset Time Delay with No Capacitor over Temperature

ADVANCE INFORMATION

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $R_{pull-up} = 100\text{ k}\Omega$, $C_{Load} = 50\text{ pF}$, unless otherwise noted.

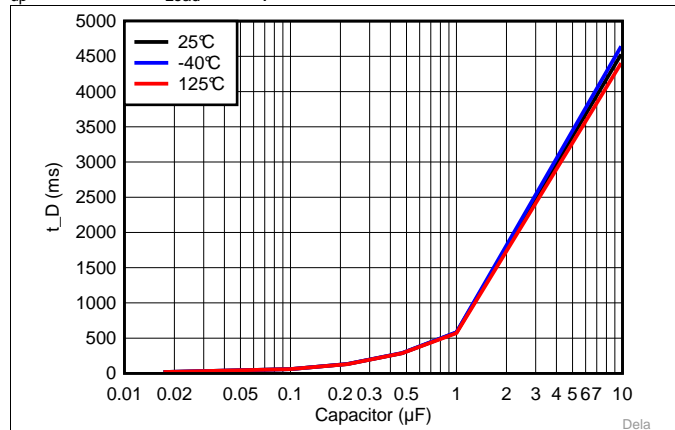


Figure 30. Reset Time Delay vs Capacitor Value (Data Taken with TPS3840PL16)

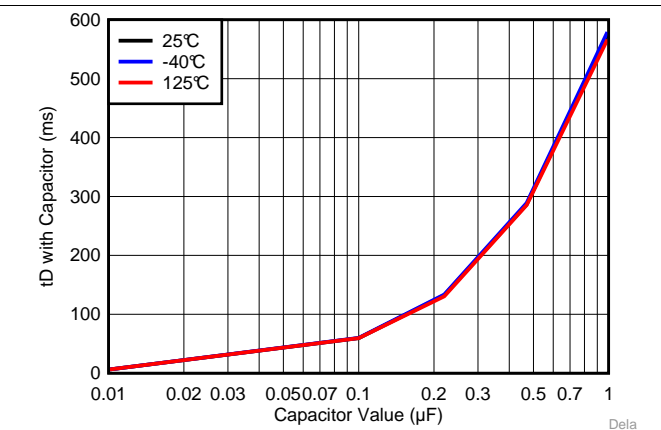


Figure 31. Reset Time Delay vs Small Capacitor Values (Data Taken with TPS3840PL16)

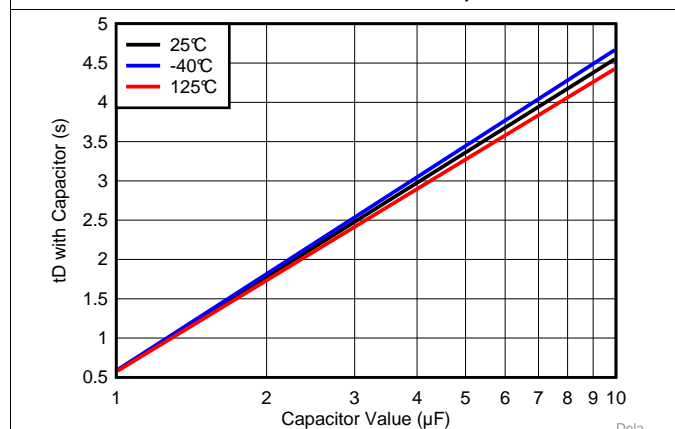


Figure 32. Reset Time Delay vs Large Capacitor Values (Data Taken with TPS3840PL16)

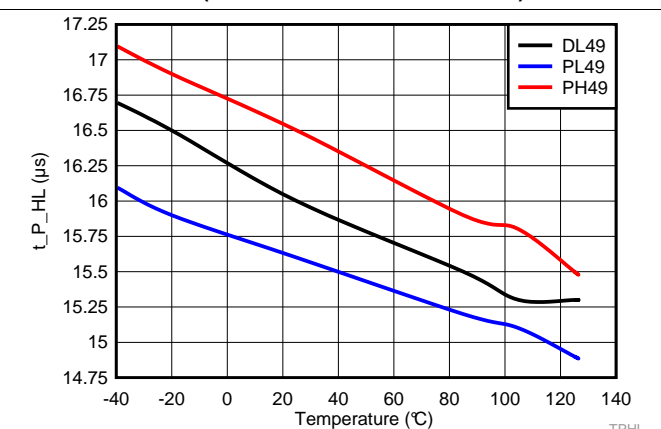


Figure 33. Propagation Detect Time Delay for VDD Falling Below V_{IT-} (High-to-Low) over Temperature

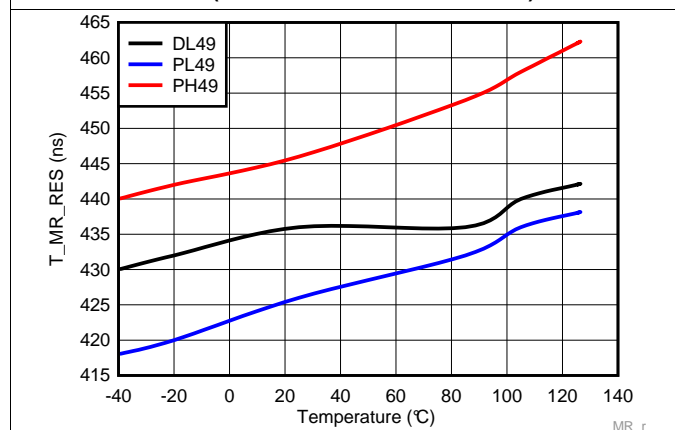


Figure 34. Propagation Time Delay from \overline{MR} Asserted to Reset over Temperature

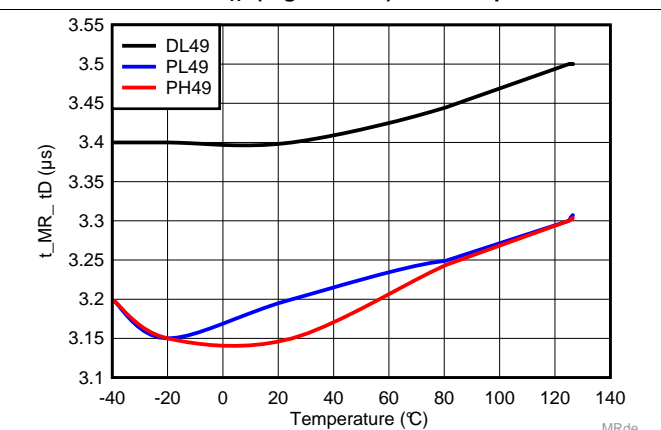


Figure 35. Propagation Time Delay from \overline{MR} Release to Deasserted Reset over Temperature

ADVANCE INFORMATION

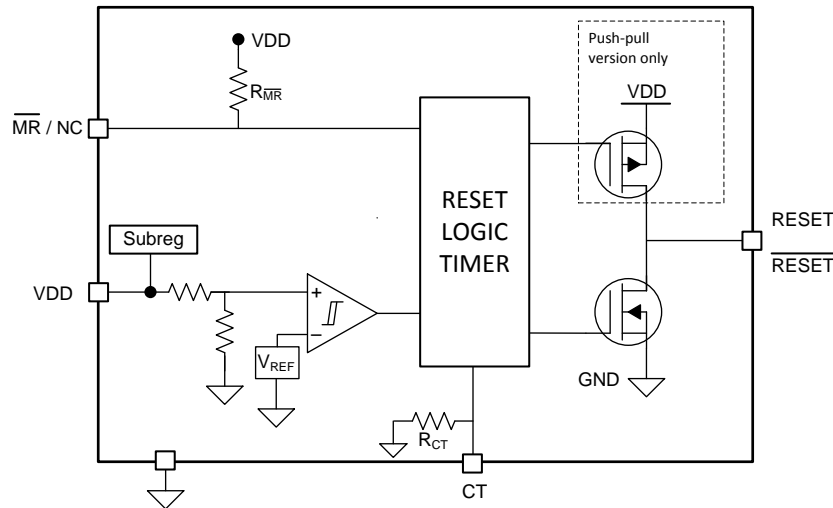
8 Detailed Description

8.1 Overview

The TPS3840 is a family of wide VDD and nano-quiescent current voltage detectors with fixed threshold voltage. TPS3840 features include programmable reset time delay using external capacitor, active-low manual reset, 1% typical monitor threshold accuracy with hysteresis and glitch immunity.

Fixed negative threshold voltages (V_{IT}) can be factory set from 1.6 V to 4.9 V (see the [Device Comparison Table](#) for available options). TPS3840 is available in SOT-23 5 pin industry standard package.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the internal bandgap, internal regulator, state machine, buffers and other control logic blocks. Good design practice involve placing a 0.1 uF to 1 uF bypass capacitor at VDD input for noisy applications to ensure enough charge is available for the device to power up correctly.

Feature Description (continued)

8.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below V_{IT-} , the output reset is asserted. When the voltage at the VDD pin goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

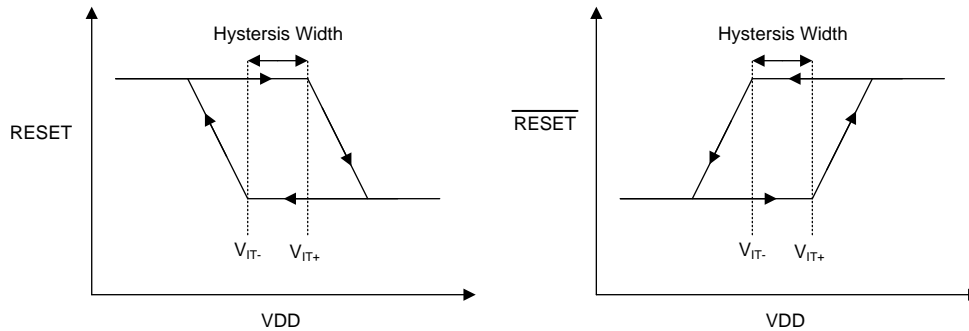


Figure 36. Hysteresis Diagram

8.3.1.2 VDD Transient Immunity

The TPS3840 is immune to quick voltage transients or excursion on VDD. Sensitivity to transients depends on both pulse duration and overdrive. Overdrive is defined by how much VDD deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 1.

$$\text{Overdrive} = | (V_{DD} / V_{IT-} - 1) \times 100\% | \quad (1)$$

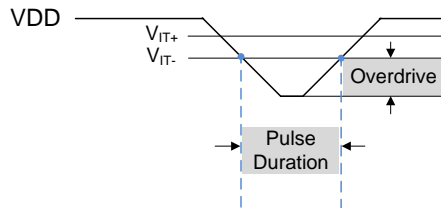


Figure 37. Overdrive vs Pulse Duration

8.3.2 User-Programmable Reset Time Delay

The reset time delay can be set to a minimum value of 80 μs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 μF delay capacitor. The reset time delay (t_D) can be programmed by connecting a capacitor no larger than 10 μF between CT pin and GND.

The relationship between external capacitor (C_{CT_EXT}) at CT pin and the time delay is given by Equation 2.

$$t_D = -\ln(0.29) \times R_{CT} \times C_{CT_EXT} + t_{D(\text{no cap})} \quad (2)$$

Equation 2 is simplified to Equation 3 by plugging R_{CT} and $t_{D(\text{no cap})}$ given in *Electrical Characteristics* section :

$$t_D = 618937 \times C_{CT_EXT} + 80\mu\text{s} \quad (3)$$

Equation 4 solves for external capacitor value (C_{CT_EXT})

$$C_{CT_EXT} = (t_D - 80\mu\text{s}) \div 618937 \quad (4)$$

The recommended maximum delay capacitor for the TPS3840 is limited to 10 μF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay capacitor will begin charging from a voltage above zero and the reset delay will be shorter than expected. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault.

Feature Description (continued)

8.3.3 Manual Reset ($\overline{\text{MR}}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a processor GPIO or other logic circuits to initiate a reset. A logic low on $\overline{\text{MR}}$ with pulse duration longer than $t_{\text{MR_RES}}$ will cause reset output to assert. After $\overline{\text{MR}}$ returns to a logic high ($V_{\text{MR_H}}$) and VDD is above $V_{\text{IT+}}$, reset is deasserted after the user programmed reset time delay (t_{D}) expires.

If $\overline{\text{MR}}$ is not controlled externally, then $\overline{\text{MR}}$ can be left disconnected. If the logic signal controlling $\overline{\text{MR}}$ is less than VDD, then additional current flows from VDD into $\overline{\text{MR}}$ internally. For minimum current consumption, drive $\overline{\text{MR}}$ to either VDD or GND. V_{MR} should not be higher than VDD voltage.

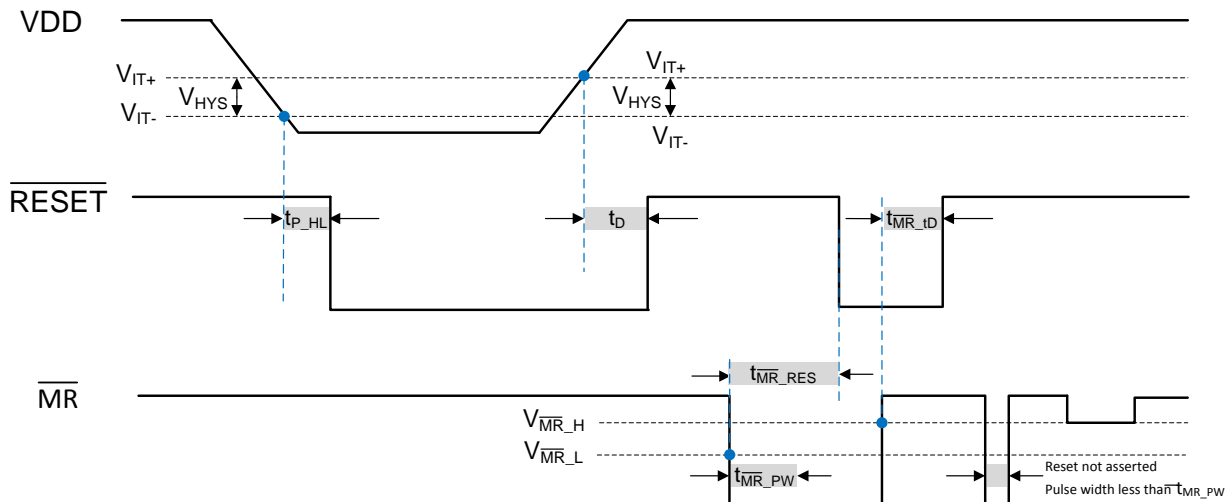


Figure 38. Timing Diagram $\overline{\text{MR}}$ and $\overline{\text{RESET}}$ (TPS3840DL)

8.3.4 Output Logic

8.3.4.1 $\overline{\text{RESET}}$ Output, Active-Low

$\overline{\text{RESET}}$ (Active-Low) applies to TPS3840DL (Open-Drain) and TPS3840PL (Push-Pull) hence the "L" in the device name. $\overline{\text{RESET}}$ remains high (deasserted) as long as VDD is above the negative threshold ($V_{\text{IT-}}$) and the $\overline{\text{MR}}$ pin is floating or above $V_{\text{MR_H}}$. If VDD falls below the negative threshold ($V_{\text{IT-}}$) or if $\overline{\text{MR}}$ is driven low, then $\overline{\text{RESET}}$ is asserted.

When $\overline{\text{MR}}$ is again logic high or floating and VDD rise above $V_{\text{IT+}}$, the delay circuit will hold $\overline{\text{RESET}}$ low for the specified reset time delay (t_{D}). When the reset time delay has elapsed, the $\overline{\text{RESET}}$ pin goes back to logic high voltage (V_{OH}).

The TPS3840DL (Open-Drain) version, denoted with "D" in the device name, requires a pull-up resistor to hold $\overline{\text{RESET}}$ pin high. Connect the pull-up resistor to the desired pull-up voltage source and $\overline{\text{RESET}}$ can be pulled up to any voltage up to 10 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value determines the actual V_{OL} , the output capacitive loading, and the output leakage current ($I_{\text{LKG(OD)}}$).

The Push-Pull variants (TPS3840PL and TPS3840PH), denoted with "P" in the device name, does not require a pull-up resistor

8.3.4.2 RESET Output, Active-High

RESET (active-high), denoted with no bar above the pin label, applies only to TPS3840PH push-pull active-high version. RESET remains low (deasserted) as long as VDD is above the threshold ($V_{\text{IT-}}$) and the manual reset signal ($\overline{\text{MR}}$) is logic high or floating. If VDD falls below the negative threshold ($V_{\text{IT-}}$) or if $\overline{\text{MR}}$ is driven low, then RESET is asserted driving the RESET pin to high voltage (V_{OH}).

When $\overline{\text{MR}}$ is again logic high and VDD is above $V_{\text{IT+}}$ the delay circuit will hold RESET high for the specified reset time delay (t_{D}). When the reset time delay has elapsed, the RESET pin goes back to low voltage (V_{OL})

8.4 Device Functional Modes

Table 1 summarizes the various functional modes of the device. Logic high is represented by "H" and logic low is represented by "L".

Table 1. Truth Table

VDD	$\overline{\text{MR}}$	RESET	$\overline{\text{RESET}}$
$V_{\text{DD}} < V_{\text{POR}}$	Ignored	Undefined	Undefined
$V_{\text{POR}} < V_{\text{DD}} < V_{\text{IT-}}^{(1)}$	Ignored	H	L
$V_{\text{DD}} \geq V_{\text{IT-}}$	L	H	L
$V_{\text{DD}} \geq V_{\text{IT-}}$	H	L	H
$V_{\text{DD}} \geq V_{\text{IT-}}$	Floating	L	H

(1) When V_{DD} falls below $V_{\text{DD(MIN)}}$, undervoltage-lockout (UVLO) takes effect and output reset is held asserted until V_{DD} falls below V_{POR} .

8.4.1 Normal Operation ($V_{\text{DD}} > V_{\text{DD(min)}}$)

When VDD is greater than $V_{\text{DD(min)}}$, the reset signal is determined by the voltage on the VDD pin with respect to the trip point ($V_{\text{IT-}}$) and the logic state of $\overline{\text{MR}}$.

- $\overline{\text{MR}}$ high: the reset signal corresponds to VDD with respect to the threshold voltage.
- $\overline{\text{MR}}$ low: in this mode, the reset is asserted regardless of the threshold voltage.

8.4.2 VDD Between VPOR and $V_{\text{DD(min)}}$

When the voltage on VDD is less than the $V_{\text{DD(min)}}$ voltage, and greater than the power-on-reset voltage (V_{POR}), the reset signal is asserted.

8.4.3 Below Power-On-Reset ($V_{\text{DD}} < V_{\text{POR}}$)

When the voltage on VDD is lower than V_{POR} , the device does not have enough bias voltage to internally pull the asserted output low or high and reset voltage level is undefined.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

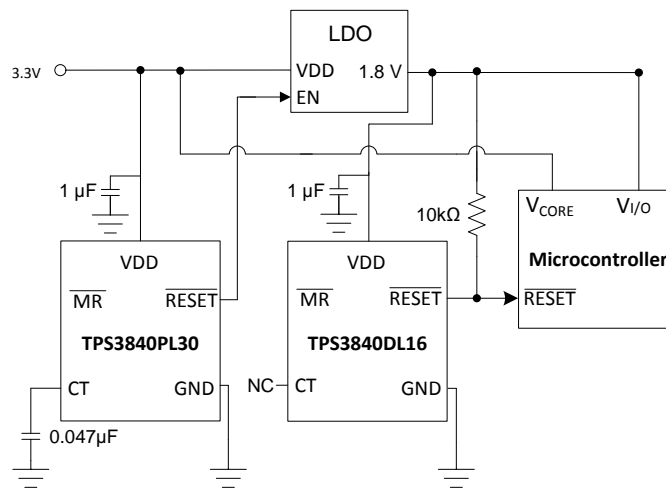
9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

9.2.1 Design 1: Dual Rail Monitoring with Power-up Sequencing

A typical application for the TPS3840 is voltage rail monitoring and power-up sequencing as shown in Figure 39. The TPS3840 can be used to monitor any rail above 1.6 V. In this design application, two TPS3840 devices monitor two separate voltage rails and sequences the rails upon power-up. The TPS3840PL30 is used to monitor the 3.3-V main power rail and the TPS3840DL16 is used to monitor the 1.8-V rail provided by the LDO for other system peripherals. The RESET output of the TPS3840PL30 is connected to the ENABLE input of the LDO. A reset event is initiated on either voltage supervisor when the VDD voltage is less than V_{IT} or when MR is driven low by an external source.



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Figure 39. TPS3840 Voltage Rail Monitor and Power-Up Sequencer Design Block Diagram

9.2.1.1 Design Requirements

This design requires voltage supervision on two separate rails: 3.3-V and 1.8-V rails. The voltage rail needs to sequence upon power up with the 3.3-V rail coming up first followed by the 1.8-V rail at least 25 ms after.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Two Rail Voltage Supervision	Monitor 3.3-V and 1.8-V rails	Two TPS3840 devices provide voltage monitoring with 1% accuracy with device options available in 0.1 V variations
Voltage Rail Sequencing	Power up the 3.3-V rail first followed by 1.8-V rail 25 ms after	The CT capacitor on TPS38240PL28 is set to 0.047 μF for a reset time delay of 29 ms typical
Output logic voltage	3.3-V Open-Drain	3.3-V Open-Drain
Maximum device current consumption	1 μA	Each TPS3840 requires 350 nA typical

9.2.1.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TPS3840 can monitor any voltage between 1.6 V and 10 V and is available in 0.1 V increments. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to choose. In this example, the first TPS3840 triggers when the 3.3-V rail falls to 3.0 V. The second TPS3840 triggers a reset when the 1.8-V rail falls to 1.6 V. The secondary constraint for this application is the reset time delay that must be at least 25 ms to allow the microprocessor, and all other devices using the 3.3-V rail, enough time to startup correctly before the 1.8-V rail is enabled via the LDO. Because a minimum time is required, the user must account for capacitor tolerance. For applications with ambient temperatures ranging from -40°C to $+125^{\circ}\text{C}$, C_{CT} can be calculated using R_{CT} and solving for C_{CT} in Equation 2. Solving Equation 2 for 25 ms gives a minimum capacitor value of 0.04 μF which is rounded up to a standard value 0.047 μF to account for capacitor tolerance.

A 1- μF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the Open-Drain device variants and is calculated to maintain the $\overline{\text{RESET}}$ current within the ± 5 mA limit found in the *Recommended Operating Conditions*: $R_{\text{Pull-up}} = V_{\text{Pull-up}} \div 5 \text{ mA}$. For this design, a standard 10-k Ω pull-up resistor is selected to minimize current draw when $\overline{\text{RESET}}$ is asserted. Keep in mind the lower the pull-up resistor, the higher V_{OL} . The $\overline{\text{MR}}$ pin can be connected to an external signal if desired or left floating if not used due to the internal pull-up resistor to VDD.

9.2.1.3 Application Curves

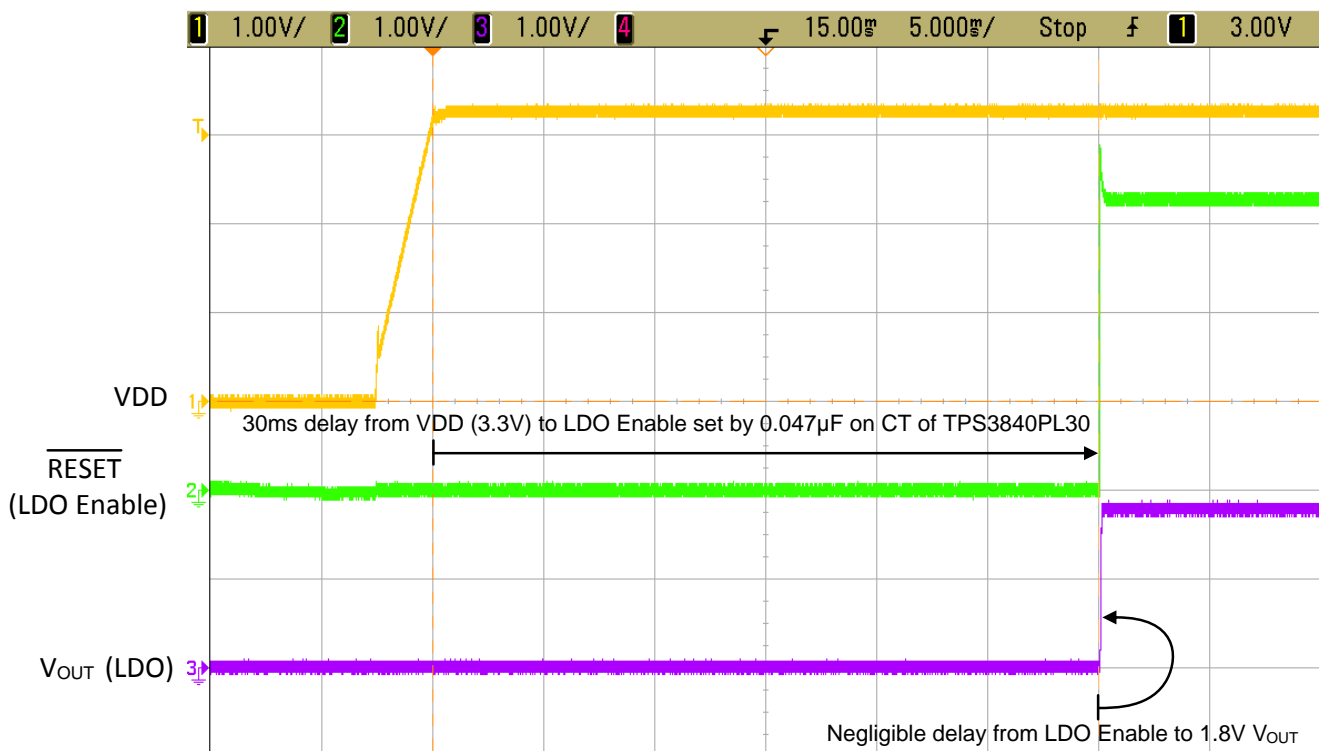


Figure 40. Startup Sequence Highlighting the Delay Between 3.3V and 1.8V Rails

9.2.2 Design 2: Battery Voltage and Temperature Monitor

A typical application for the TPS3840 is battery voltage and temperature monitoring. The TPS3840 is offered in active-low or active-high output topologies meaning the device can be used as an undervoltage monitor as shown in Figure 39 or overvoltage monitor as shown in Figure 42. The TPS3840 can be used to monitor any rail above 1.6 V. In this design application, a TPS3840DL30 monitors the 3.3-V battery voltage rail and triggers a reset fault condition if the battery voltage falls below 3 V and TPS3840PH30 monitors a 2.8-V battery and triggers a reset at 3.1 V due to the 100 mV hysteresis for the rising input trigger. Both designs monitor the battery temperature and trigger a fault if the battery temperature falls outside of a defined window temperature range by utilizing the TMP303. The TMP303 device is a temperature switch that monitors the battery temperature and sends a signal to the manual reset pin on the TPS3840 if the battery temperature is out of range.

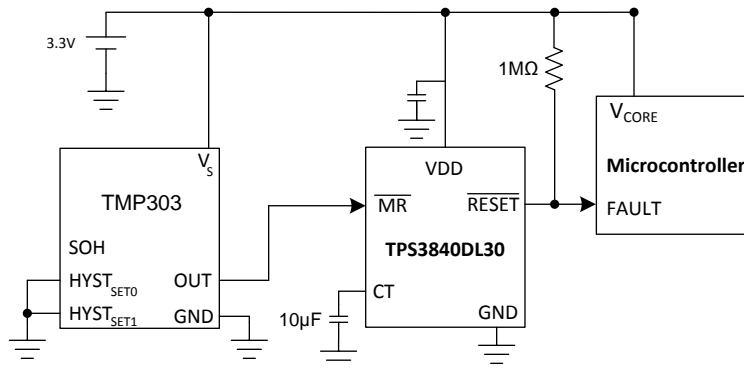


Figure 41. Low Battery Voltage and Window Temperature Monitoring Solution

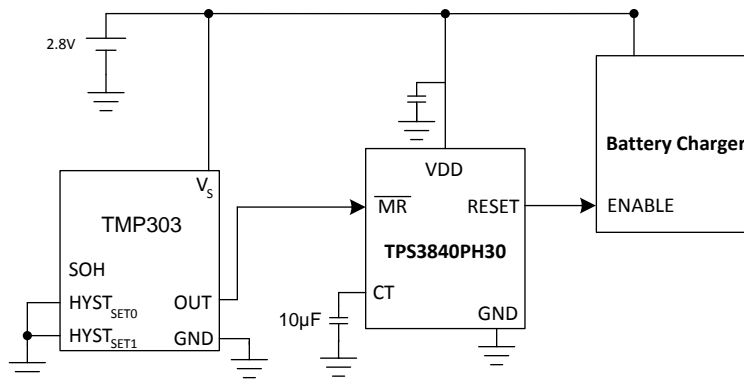


Figure 42. Overvoltage and Window Temperature Monitoring Solution

9.2.2.1 Design Requirements

This design requires voltage and temperature supervision on a battery voltage rail and the requirements may differ depending on if undervoltage or overvoltage monitoring is required. For this design, both requirements are considered to show the flexibility of the TPS3840 device. For the undervoltage requirement, the fault occurs when the battery voltage drops below 3 V or when the battery temperature is outside the range from 0°C to 60°C. For the overvoltage requirement, the fault occurs when the battery voltage rises above 3.1 V or when the battery temperature is outside the range from 0°C to 60°C. Note that if using two TPS3840 devices for both undervoltage and overvoltage monitoring on the same battery, only one single TMP303 temperature monitoring device is required.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Battery Voltage Supervision	Monitor 3.3-V battery for undervoltage condition	TPS3840 provides voltage monitoring with 1% accuracy with device options available in 0.1 V variations. TPS3840DL30 triggers a reset when VDD falls below 3 V. TPS3840PH30 triggers a reset when VDD rises above 3 V plus hysteresis setting the overvoltage threshold to 3.1 V.
	Monitor 2.8-V battery for overvoltage condition	
Battery Temperature Supervision	Monitor battery temperature between 0°C and 60°C with 1°C resolution	TMP303A monitors temperature within 0°C to 60°C with 1°C resolution
Output Topology	Undervoltage: Active-Low, Open-Drain	TPS3840 is offered in Active-Low Open-drain, Active-Low Push-Pull, and Active-High Push-Pull topologies
	Overvoltage: Active-High, Push-Pull	
Maximum device current consumption	10 μ A	TPS3840 requires 350 nA (typical) and TMP303 requires 3.5 μ A (typical)
Delay when returning from fault condition	Delay of at least 6 seconds when returning from the fault to prevent operation in fault conditions	$C_{CT} = 10 \mu$ F sets 6.18 second delay

9.2.2.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the battery supply voltage. The TPS3840 can monitor any voltage between 1.6 V and 10 V and is available in 0.1 V increments. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to choose. In this example, the TPS3840DL30 triggers when the 3.3-V rail falls to 3 V and the TPS3840PH30 triggers when the 2.8-V rail rises to 3.1 V. The secondary constraint for this application is the battery temperature monitoring accomplished by the TMP303. Typical Lithium Ion battery discharge temperature range is 0°C to 60°C. The TMP303 triggers a fault to the $\overline{\text{MR}}$ pin of the TPS3840 whenever the temperature is outside of the temperature range. The TMP303 offers 1°C resolution to meet the high resolution requirement. The last constraint is the $\overline{\text{RESET}}/\text{RESET}$ time delay set by C_{CT} . For applications with ambient temperatures ranging from -40°C to +125°C, C_{CT} can be calculated using R_{CT} and solving for C_{CT} in Equation 2. By choosing a standard 10% capacitor value of 10 μ F ensures the $\overline{\text{RESET}}/\text{RESET}$ time delay will be at least 6 seconds. Note: active-low devices use the output label $\overline{\text{RESET}}$ and active-high devices use the output label RESET.

A 0.1- μ F decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the Open-Drain device variants and is calculated to maintain the $\overline{\text{RESET}}$ current within the ± 5 mA limit found in the *Recommended Operating Conditions*: $R_{\text{pull-up}} = V_{\text{pull-up}} \div 5 \text{ mA}$. For this design, a 1-M Ω pull-up resistor is selected to minimize current draw when $\overline{\text{RESET}}$ is asserted and to prevent the battery from unnecessary discharge. Keep in mind the lowering the pull-up resistor, increases V_{OL} and I_{OUT} . The $\overline{\text{MR}}$ pin is used for a second fault condition provided by the temperature switch.

9.2.3 Design 3: Fast Start Undervoltage Supervisor with Level-shifted Input

A typical application for the TPS3840 is a fast startup undervoltage supervisor that operates with an input power supply higher than the recommended maximum of 10 V through the use of a resistor divider at the input as shown in Figure 43. The TPS3840 can be used to monitor any rail above 1.6 V and only requires maximum 500 μ s upon startup before the device can begin monitoring a voltage. In this design application, a TPS3840 monitors a 12-V rail and triggers a reset fault condition if the voltage rail voltage drops below 10 V using a TPS3840 device with V_{IT} of 4.9 V. This design also accounts for a wide input range in the case the 12-V rail rises higher, the resistor divider is set so that the voltage at the VDD pin never exceeds 10 V. TPS3840 is available in both active-low and active-high topologies providing the flexibility to monitor undervoltage or overvoltage with either output logic. This design uses the active-low, open-drain TPS3840DL49 variant so that when the undervoltage condition occurs, that is when the voltage at VDD pin falls below the voltage threshold set by the external resistor divider, the output transitions to logic-low and can be used to flag an undervoltage condition or used to connect to the ENABLE of the next device to shut it off as a logic low on an ENABLE pin typically disables the device. In this design, the output of the TPS3840 simply connects to a MCU to flag an undervoltage condition.

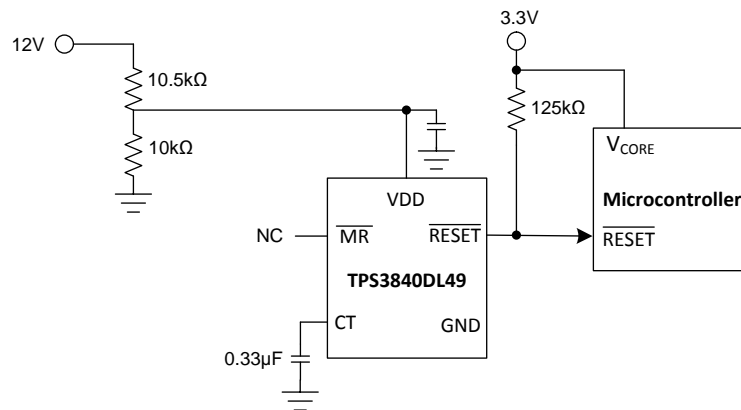


Figure 43. Fast Start Undervoltage Supervisor with Level-shifted Input

9.2.3.1 Design Requirements

This design requires voltage supervision on a 12-V power supply voltage rail with possibility of the 12-V rail rising up as high as 18 V. The undervoltage fault occurs when the power supply voltage drops below 10 V.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Power Rail Voltage Supervision	Monitor 12-V power supply for undervoltage condition, trigger a undervoltage fault at 10 V.	TPS3840 provides voltage monitoring with 1% accuracy with device options available in 0.1 V variations. The TPS3840 monitors voltages above 1.6 V.
Maximum Input Power	Operate with power supply input up to 18 V.	The TPS3840 limits VDD to 10 V but can monitor voltages higher than the maximum VDD voltage with the use of an external resistor divider.
Output logic voltage	3.3-V Open-Drain	3.3-V Open-Drain
Maximum device current consumption	35 µA when power supply is at 18 V maximum	TPS3840 requires 350 nA (typical) and the external resistor divider will also consume current. There is a tradeoff between current consumption and voltage monitor accuracy but generally set the resistor divider to consume 100 times current into VDD.
Voltage Monitor Accuracy	Typical voltage monitor accuracy of 2.5%. This allows the voltage threshold to range between 11.75 V and 10.25 V.	The TPS3840 has 1% typical voltage monitor accuracy. By decreasing the ratio of resistor values, the resistor divider will consume more current but the accuracy will increase. The resistor tolerance also needs to be accounted for.
Delay when returning from fault condition	RESET delay of at least 200 ms when returning from a undervoltage fault.	C _{CT} = 0.33 µF sets 204 ms delay

9.2.3.2 Detailed Design Procedure

The primary constraint for this application is monitoring a 12-V rail while preventing the VDD pin on TPS3840 from exceeding the recommended maximum of 10 V. This is accomplished by sizing the resistor divider so that when the 12-V rail drops to 10 V, the VDD pin for TPS3840 will be at 4.9 V which is the V_{IT-} threshold for triggering a undervoltage condition for TPS3840DL49 as shown in Equation 5.

$$V_{\text{rail_trigger}} = V_{\text{IT-}} \times (R_{\text{bottom}} \div (R_{\text{top}} + R_{\text{bottom}})) \tag{5}$$

where V_{rail_trigger} is the trigger voltage of the rail being monitored, V_{IT-} is the falling threshold on the VDD pin of TPS3840, and R_{top} and R_{bottom} are the top and bottom resistors of the external resistor divider. V_{IT-} is fixed per device variant and is 4.9 V for TPS3840DL49. Substituting in the values from Figure 43, the undervoltage trigger threshold for the rail is set to 10.045 V.

Since the undervoltage trigger of 10 V on the rail corresponds to 4.9 V undervoltage threshold trigger of the TPS3840 device, there is plenty of room for the rail to rise up while maintaining less than 10 V on the VDD pin of the TPS3840. Equation 6 shows the maximum rail voltage that still meets the 10 V maximum at the VDD pin for TPS3840.

$$V_{\text{rail_max}} = 10 \times (10,000 \div (10,500 + 10,000)) = 20.5 \text{ V} \quad (6)$$

This means the monitored voltage rail can go as high as 20.5 V and still not violate the recommended maximum for the VDD pin on TPS3840. This is useful when monitoring a voltage rail that has a wide range that may go much higher than the nominal rail voltage such as in this case with the specification that the 12-V rail can go as high as 18 V.

9.2.4 Design 4: Voltage Monitor with Back-up Battery Switchover

A typical application for the TPS3840 is to monitor a voltage rail and switch the power to a back-up battery if the main supply is in undervoltage condition. Because systems that utilize a back-up battery tend to require low quiescent current, TPS3840 serves as the perfect solution as this device only requires 350 nA typically. The TPS3840 monitors the main power rail via the VDD pin and when the main power rail falls, the $\overline{\text{RESET}}$ output asserts causing a switch to close on the back-up battery rail. The diodes provide an ORing logic function to prevent reverse leakage and to allow either rail to connect to the output depending on the status of the main voltage rail.

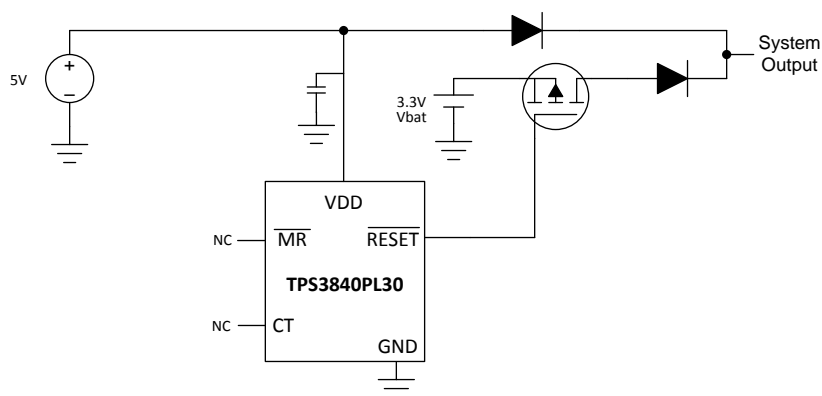


Figure 44. Voltage Monitor with Back-up Battery Switchover Solution

9.2.4.1 Design Requirements

This design requires voltage supervision on a 5-V main supply voltage rail and when the main rail fails, switch to a back-up battery supply to prevent complete power loss in the system. The System Output must remain above 1.8 V even when the main supply completely fails. The design requires less than 500 nA of total current consumption and must prevent battery leakage when the battery is not being used. When the system is using the back-up battery and the main supply voltage rail comes back up, the system must switch back to the main power supply in less than 100 μs to save battery power.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Main Supply Voltage Supervision	Monitor 5-V main supply for undervoltage condition. When main supply drops below 3 V, switch to back-up battery.	TPS3840 provides voltage monitoring with 1% accuracy with device options available in 0.1 V variations. This design uses TPS3840PL30 to set the undervoltage trigger at 3 V.
Back-up Battery Switchover	When undervoltage occurs on the main supply voltage rail, switch to the back-up battery.	When undervoltage occurs on the main supply rail, the PMOS switch closes allowing the back-up battery to connect to the system output. The diodes prevent reverse leakage and allow either power supply to connect to the system output.
Main Power Supply to Back-up Battery Switch Response Time	No more than 50 μs to switch to the back-up battery when the main power supply falls to undervoltage condition.	TPS3840 provides a propagation delay for VDD falling below the undervoltage threshold (t_{p_HL}) of 50 μs maximum to meet the requirement.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Back-up Battery to Main Power Supply Switch Back Response Time	Less than 100 μ s when switching from back-up battery back to main power supply when undervoltage condition is removed.	By leaving $\overline{\text{MR}}$ disconnected, the $\overline{\text{RESET}}$ delay is set to a maximum of 80 μ s to meet the requirement.
Device Current Consumption	500 nA	TPS3840 requires 350 nA (typical)
System Output Voltage	System Output must remain above 1.8 V in all cases	When the main 5-V rail is connected, the System Output will be the rail voltage minus a diode voltage drop so at least 3 V - 0.7 V ~ 2.3 V. When the voltage rail drops below 3 V, the back-up battery switches into the system and the System Output becomes the battery voltage minus a diode voltage drop so 3.3 V - 0.7 V ~ 2.6 V. The threshold at which the battery switches into the system directly depends on the TPS3840 variant chosen.

9.2.4.2 Detailed Design Procedure

The primary constraints for this application are choosing the correct device variant for the monitored voltage and deciding the preferred solution to switch the back-up battery in and out of the system. For this design, the TPS3840PL30 provides an active-low, push-pull output topology that turns on the PFET when the 5-V rail monitored by VDD drops to 3.0 V. The diodes logically OR the power supply with the back-up battery and prevents reverse current leakage. Using this solution, the System Output remains above 1.8 V in all circumstances unless both the 5-V rail and back-up battery fail. The System Output voltage will follow the 5-V rail minus a diode drop until the 5-V rail drops to 3 V then the back-up battery switches into the system providing 3.3 V minus a diode drop to the System Output. When the 5-V rail comes back above 3.1 V accounting for hysteresis, the PFET turns off to disconnect the back-up battery from the system. Since this design disconnects the battery when not being used, this solution maximizes battery life.

9.2.5 Application Curve: TPS3840EVM

These application curves are taken with the [TPS3840EVM](#). Please see the [TPS3840EVM User Guide](#) for more information.

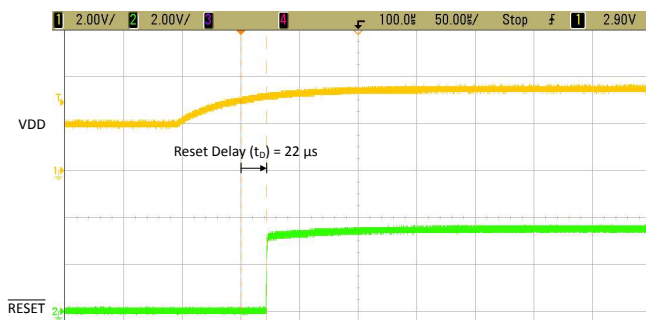


Figure 45. TPS3840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with No Capacitor

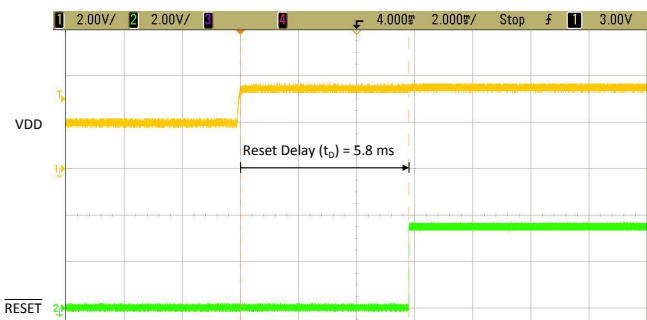


Figure 46. TPS3840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with 0.01- μ F Capacitor

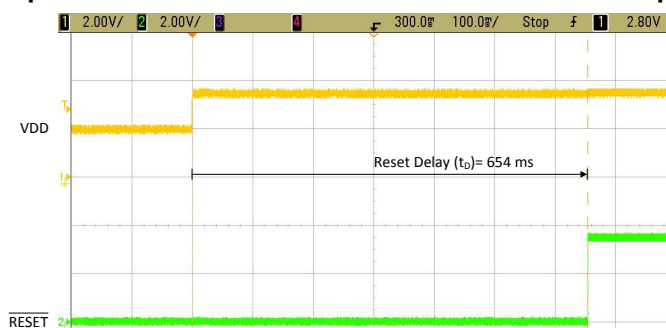


Figure 47. TPS3840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with 1- μ F Capacitor

10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.5 V and 10 V. TI recommends an input supply capacitor between the VDD pin and GND pin. This device has a 12-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 12 V, additional precautions must be taken.

11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a minimum 0.1- μ F ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the rest time delay is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a >0.1- μ F ceramic capacitor as near as possible to the VDD pin.
- If a C_{CT} capacitor is used, place these components as close as possible to the CT pin. If the CT pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin to <5 pF.
- Place the pull-up resistors on $\overline{\text{RESET}}$ pin as close to the pin as possible.

11.2 Layout Example

The layout example in shows how the TPS3840 is laid out on a printed circuit board (PCB) with a user-defined delay.

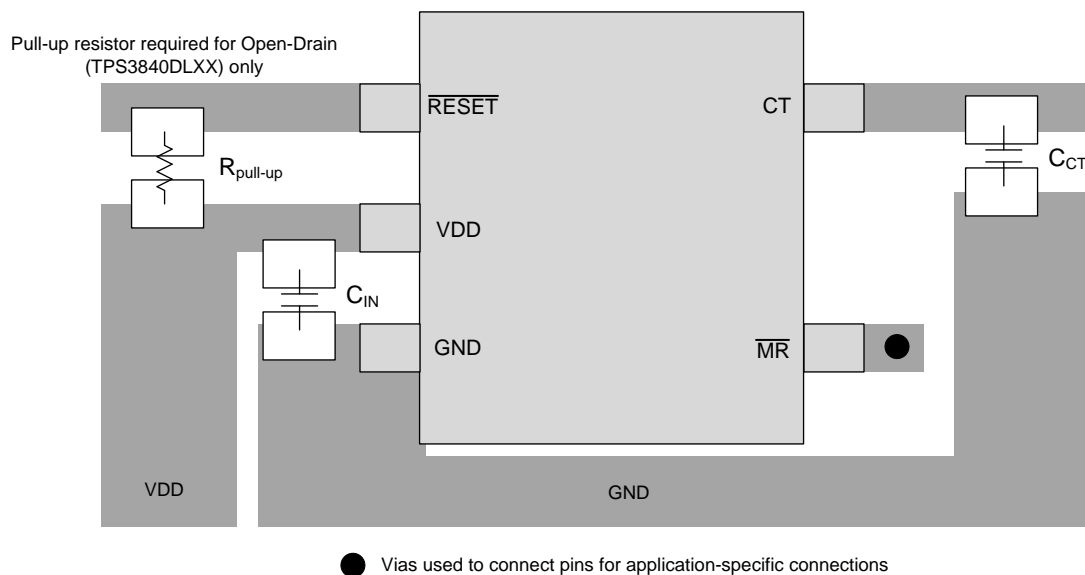


Figure 48. TPS3840 Recommended Layout

12 Device and Documentation Support

12.1 Device Nomenclature

Table 2 shows how to decode the function of the device based on its part number

Table 2. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE
Engineering Prototype pre-release sample	P	Engineering Prototype Sample
Part number	TPS3840	TPS3840
Variant code (Output Topology)	DL	Open-Drain, Active-Low
	PH	Push-Pull, Active-High
	PL	Push-Pull, Active-Low
Detect Voltage Option	## (two characters)	Example: 12 stands for 1.2 V threshold
Package	DBV	SOT23-5
Reel	R	Large Reel

Table 3 shows the possible variants of the TPS3840. Contact Texas Instruments for details and availability of other options shown; minimum order quantities apply.

Table 3. Device Threshold

Product			Voltage Threshold (V _{IT})	Hysteresis (V _{HYST})
Open-Drain, Active-Low	Push-Pull, Active-Low	Push-Pull, Active-High	Typ (V)	Typ (V)
TPS3840DL16	TPS3840PL16	TPS3840PH16	1.6	0.100
TPS3840DL17	TPS3840PL17	TPS3840PH17	1.7	0.100
TPS3840DL18	TPS3840PL18	TPS3840PH18	1.8	0.100
TPS3840DL19	TPS3840PL19	TPS3840PH19	1.9	0.100
TPS3840DL20	TPS3840PL20	TPS3840PH20	2.0	0.100
TPS3840DL21	TPS3840PL21	TPS3840PH21	2.1	0.100
TPS3840DL22	TPS3840PL22	TPS3840PH22	2.2	0.100
TPS3840DL23	TPS3840PL23	TPS3840PH23	2.3	0.100
TPS3840DL24	TPS3840PL24	TPS3840PH24	2.4	0.100
TPS3840DL25	TPS3840PL25	TPS3840PH25	2.5	0.100
TPS3840DL26	TPS3840PL26	TPS3840PH26	2.6	0.100
TPS3840DL27	TPS3840PL27	TPS3840PH27	2.7	0.100
TPS3840DL28	TPS3840PL28	TPS3840PH28	2.8	0.100
TPS3840DL29	TPS3840PL29	TPS3840PH29	2.9	0.100
TPS3840DL30	TPS3840PL30	TPS3840PH30	3.0	0.100
TPS3840DL31	TPS3840PL31	TPS3840PH31	3.1	0.100
TPS3840DL32	TPS3840PL32	TPS3840PH32	3.2	0.200
TPS3840DL33	TPS3840PL33	TPS3840PH33	3.3	0.200
TPS3840DL34	TPS3840PL34	TPS3840PH34	3.4	0.200
TPS3840DL35	TPS3840PL35	TPS3840PH35	3.5	0.200
TPS3840DL36	TPS3840PL36	TPS3840PH36	3.6	0.200
TPS3840DL37	TPS3840PL37	TPS3840PH37	3.7	0.200
TPS3840DL38	TPS3840PL38	TPS3840PH38	3.8	0.200
TPS3840DL39	TPS3840PL39	TPS3840PH39	3.9	0.200
TPS3840DL40	TPS3840PL40	TPS3840PH40	4.0	0.200
TPS3840DL41	TPS3840PL41	TPS3840PH41	4.1	0.200
TPS3840DL42	TPS3840PL42	TPS3840PH42	4.2	0.200

Table 3. Device Threshold (continued)

Product			Voltage Threshold (V_{IT-})	Hysteresis (V_{HYST})
Open-Drain, Active-Low	Push-Pull, Active-Low	Push-Pull, Active-High	Typ (V)	Typ (V)
TPS3840DL43	TPS3840PL43	TPS3840PH43	4.3	0.200
TPS3840DL44	TPS3840PL44	TPS3840PH44	4.4	0.200
TPS3840DL45	TPS3840PL45	TPS3840PH45	4.5	0.200
TPS3840DL46	TPS3840PL46	TPS3840PH46	4.6	0.200
TPS3840DL47	TPS3840PL47	TPS3840PH47	4.7	0.200
TPS3840DL48	TPS3840PL48	TPS3840PH48	4.8	0.200
TPS3840DL49	TPS3840PL49	TPS3840PH49	4.9	0.200

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS3840DL20DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS3840DL27DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS3840DL29DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS3840PH30DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS3840PL25DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS3840PL28DBVR	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS3840DL20DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS3840DL27DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS3840DL29DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS3840PH30DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS3840PL25DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS3840PL28DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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