UNIVERSAL DEMULTIPLEXER/ DECODER

SY100S370

FEATURES

- **Max. propagation delay of 1200ps**
- **I_{EE} min. of –92mA**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75KΩ input pull-down resistors**
- **60% faster than National or Signetics**
- **Approximately 40% lower power than Fairchild**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 24-pin CERPACK and 28-pin PLCC packages**

DESCRIPTION

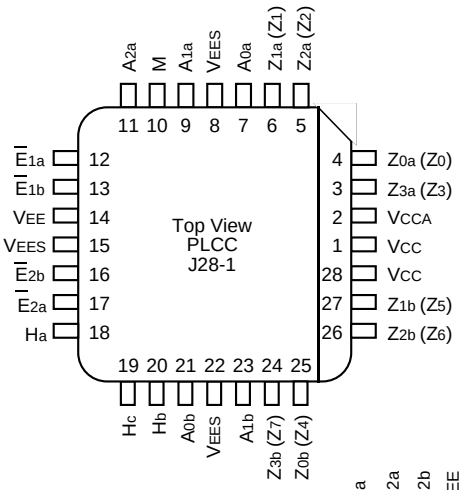
The SY100S370 is a universal demultiplexer/decoder that can be used as either a dual 1-of-4 decoder or as a single 1-of-8 decoder and is designed for use in high-performance ECL systems. The Mode control (M) input determines the function. In the dual 1-of-4 mode, each 4-input group has a pair of active-LOW Enable ($\overline{E}$) inputs. The Enable pins are assigned such that in the single 1-of-8 mode they can be tied together in pairs to result in two active-LOW Enable inputs. $\overline{E}_{1a}$ will be tied to $\overline{E}_{1b}$ and $\overline{E}_{2a}$ to $\overline{E}_{2b}$.

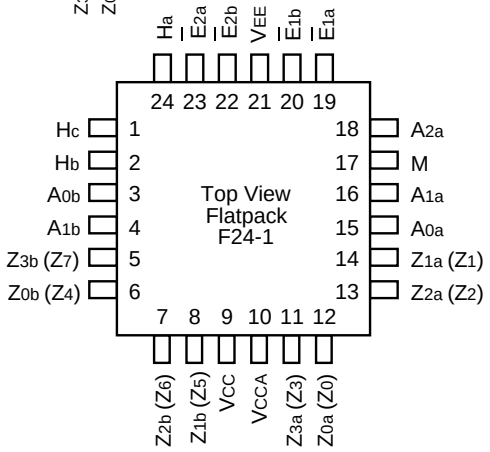
The auxiliary inputs (H_n) are used to determine whether the outputs are active-HIGH or active-LOW. The address inputs for the dual 1-of-4 mode are A_{0a}, A_{1a}, A_{0b}. A_{2a} is unused. In the 1-of-8 mode, the address inputs are A_{0a}, A_{1a}, A_{2a}. The inputs on the device have 75KΩ pull-down resistors.

PIN NAMES

Pin	Function
A_{na}, A_{nb}	Address Inputs (n = 0,1,2)
$\overline{E}_{na}$, $\overline{E}_{nb}$	Enable Inputs (n = 1,2)
M	Mode Control Input
H_a	$Z_0 – Z_3$ ($\overline{Z}_{0a} – \overline{Z}_{3a}$) Polarity Select Input
H_b	$Z_4 – Z_7$ ($\overline{Z}_{0b} – \overline{Z}_{3b}$) Polarity Select Input
H_c	Common Polarity Select Input
$Z_0 – Z_7$	Single 1-of-8 Data Outputs
Z_{na}, Z_{nb}	Dual 1-of-4 Data Outputs (n = 1...4)
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

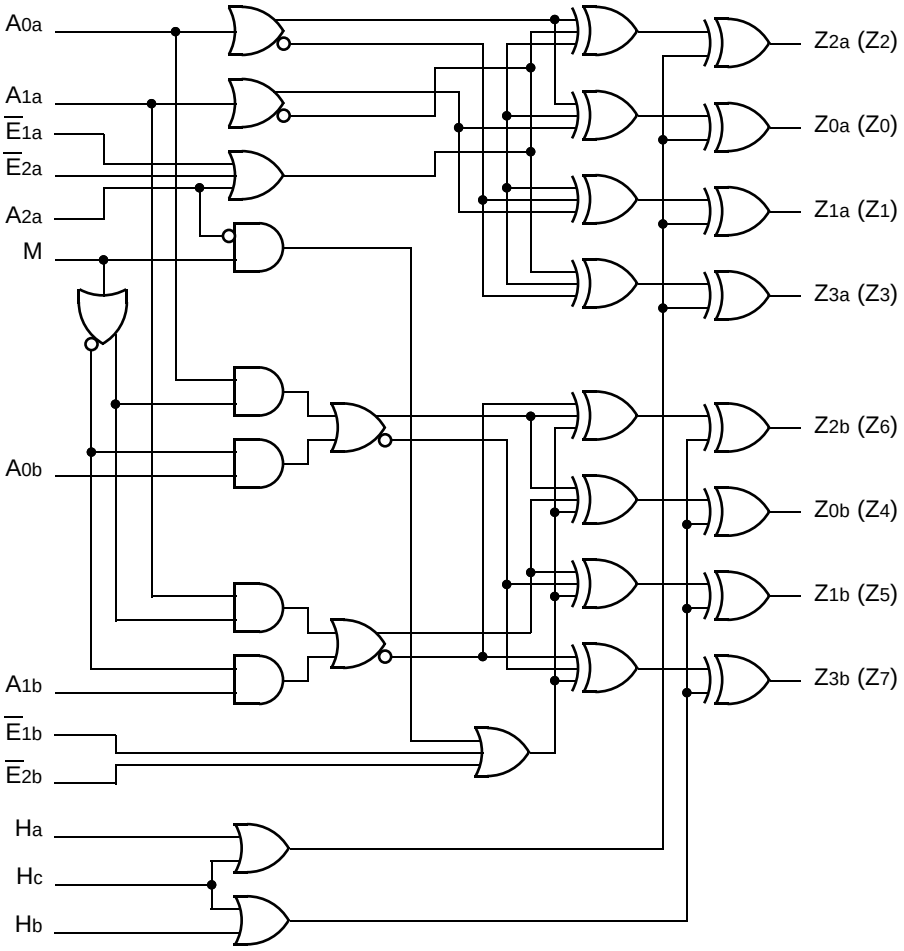
PIN CONFIGURATIONS





Rev.: G Amendment: /0
Issue Date: July, 1999

BLOCK DIAGRAM



TRUTH TABLES[1]

Dual 1-of-4 Mode (M = A_{2a} = H_c = LOW)											
Inputs				Active HIGH Outputs (H_a and H_b Inputs HIGH)				Active LOW Outputs (H_a and H_b Inputs LOW)			
$\overline{E}_{1a}$,$\overline{E}_{1b}$	$\overline{E}_{2a}$,$\overline{E}_{2b}$	A_{1a},A_{1b}	A_{0a},A_{0b}	Z_{0a},Z_{0b}	Z_{1a},Z_{1b}	Z_{2a},Z_{2b}	Z_{3a},Z_{3b}	Z_{0a},Z_{0b}	Z_{1a},Z_{1b}	Z_{2a},Z_{2b}	Z_{3a},Z_{3b}
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

Single 1-of-8 Mode (M = HIGH; A_{0b} = A_{1b} = H_a = H_b = LOW)												
Inputs					Active HIGH Outputs* (H_c Input HIGH)							
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   * for H_c = LOW, output states are complemented
   $\overline{E}_1$ = $\overline{E}_{1a}$ and $\overline{E}_{1b}$ wired; $\overline{E}_2$ = $\overline{E}_{2a}$ and $\overline{E}_{2b}$ wired

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current Hc, A0a, A1a, A2a All Others	 — —	 — —	 310 250	µA	V_{IN} = V_{IH} (Max.)
I_{EE}	Power Supply Current	–92	–73	–46	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

CERPACK

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

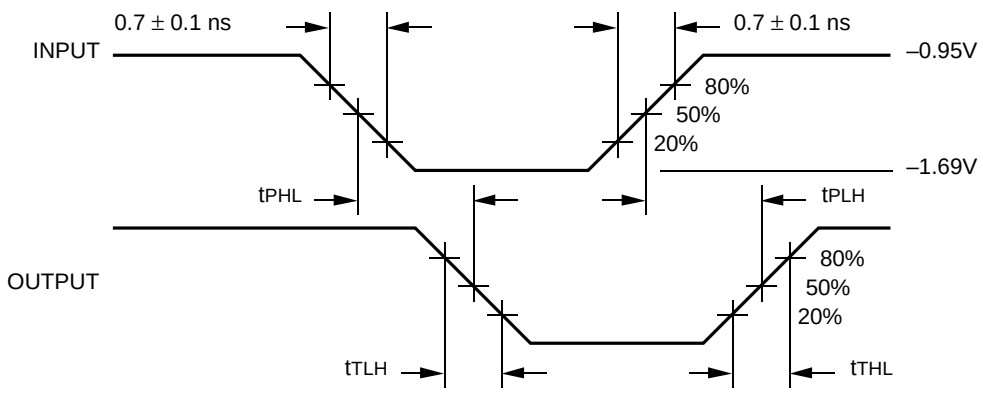
Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	300	1300	300	1300	300	1300	ps	
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	500	1600	500	1600	500	1600	ps	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	500	1600	500	1600	500	1600	ps	
t_{PLH} t_{PHL}	Propagation Delay M to Output	600	2100	600	2100	600	2100	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

PLCC

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	300	1200	300	1200	300	1200	ps	
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	500	1500	500	1500	500	1500	ps	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	500	1500	500	1500	500	1500	ps	
t_{PLH} t_{PHL}	Propagation Delay M to Output	600	2100	600	2100	600	2100	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	

TIMING DIAGRAM



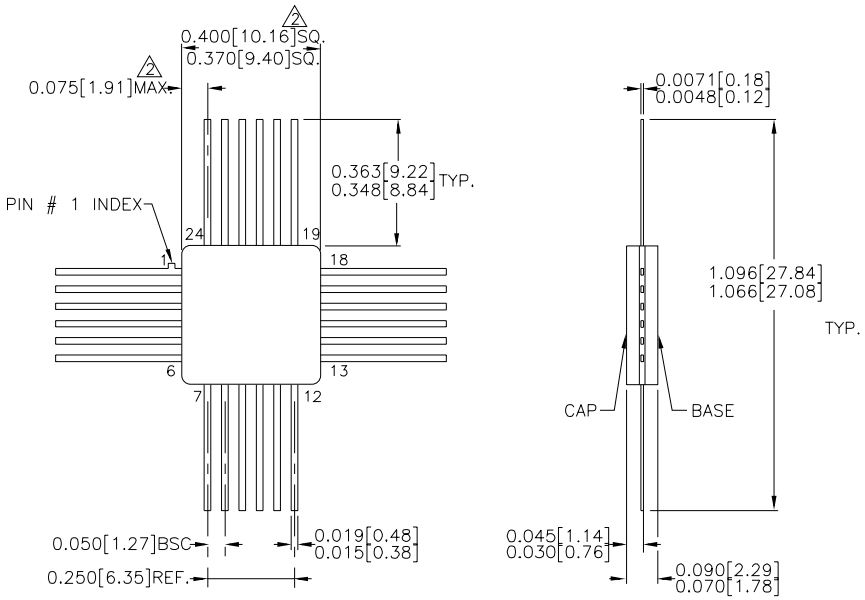
Propagation Delay and Transition Times

NOTE:
V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S370FC	F24-1	Commercial
SY100S370JC	J28-1	Commercial
SY100S370JCTR	J28-1	Commercial

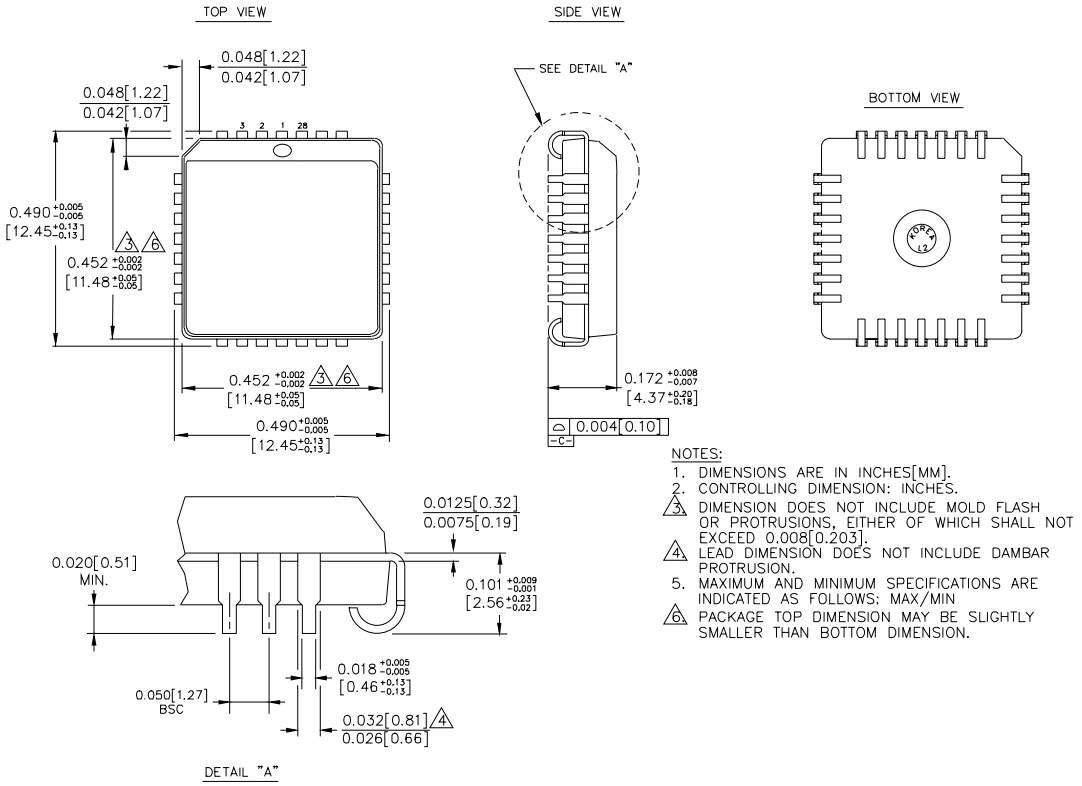
24 LEAD CERPACK (F24-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

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28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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