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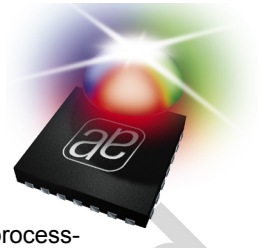
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AS3676

Flexible Lighting Management (CP, DCDC, 13 Current Sinks, ADC, LED Test, LDO, DLS and Ambient Light sensing)



1 General Description

The AS3676 is a highly-integrated CMOS Power and Lighting Management Unit for mobile telephones, and other 1-cell Li+ or 3-cell NiMH powered devices.

The AS3676 incorporates one Step Up DC/DC Converter for white backlight LEDs, one high-power Charge Pump, one Analog-to-Digital Converter, 13 current sinks, LED in-circuit function test, a two wire serial interface, and control logic all onto a single device. It supports **ambient light sensor** processing and a Dynamic Luminance Scaling (**DLS**) input. Output voltages and output currents are fully programmable.

The AS3676 is part of the austriamicrosystems AS3675, AS3687/87XM and AS3689 lighting management unit family. It is software compatible to AS3687/87XM and AS3689 and pin and software compatible to AS3675.

2 Key Features

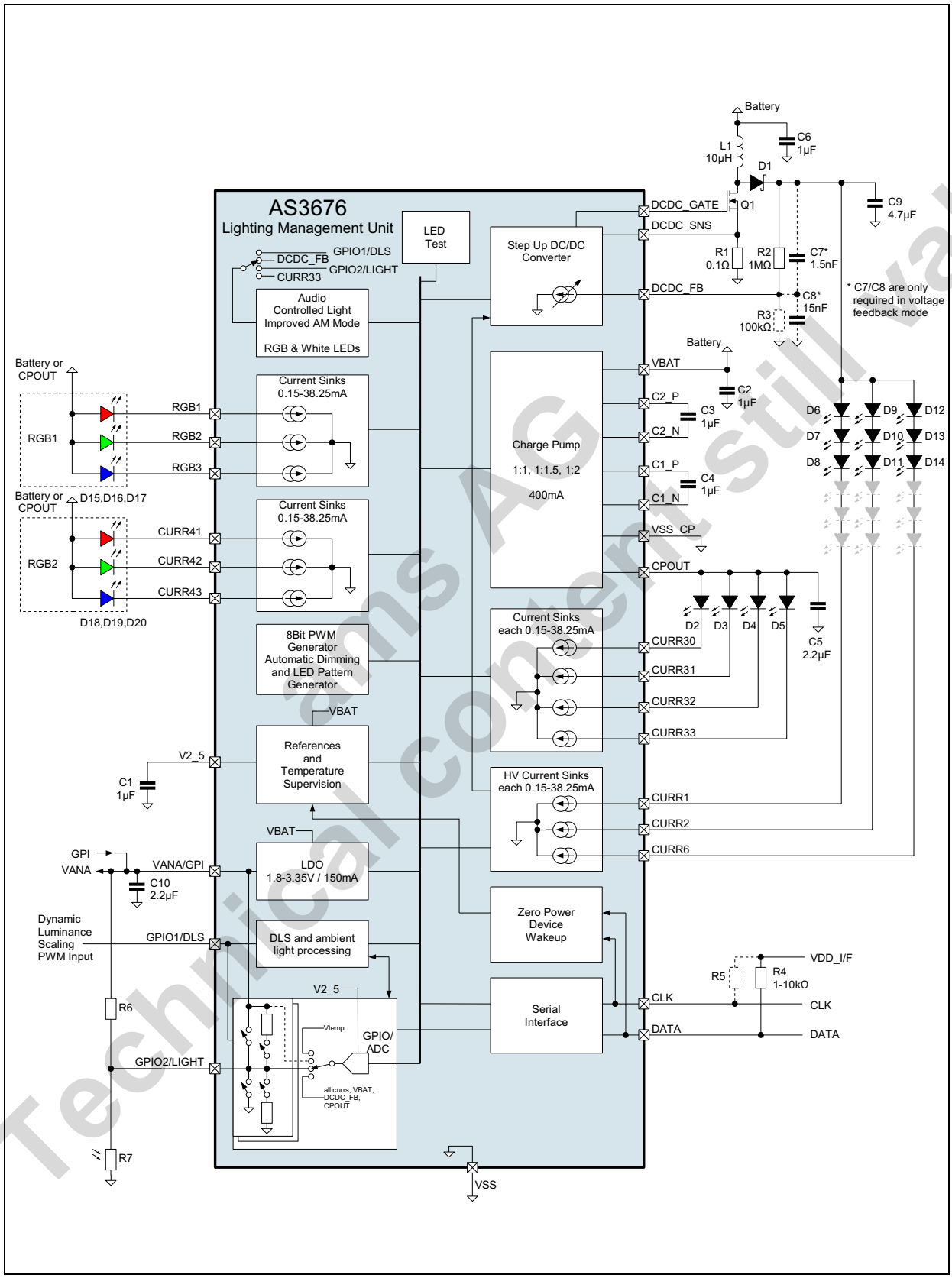
- High-Efficiency Step Up DC/DC Converter
  - Up to 26V/50mA for White LEDs
  - Programmable Output Voltage with External Resistors and Serial Interface
  - Over voltage Protection
- High-Efficiency High-Power Charge Pump
  - 1:1, 1:1.5, and 1:2 Mode
  - Automatic Up Switching (can be disabled and 1:2 mode can be blocked)
  - Output Current up to 400mA/500mA pulsed
  - Efficiency up to 95%
  - Very Low effective Resistance (2.5Ω typ. in 1:1.5)
  - Only 4 External Capacitors Required: 2 x 1µF Flying Capacitors, 2 x 2.2µF Input/Output Capacitors
  - Supports LCD White Backlight LEDs, or RGB LEDs
- 13 Current Sinks
  - All 13 current sinks fully Programmable (8-bit) from: 0.15mA to 38.5mA (up to 75.6mA for CURR30...CURR33)
  - Three current sinks are High Voltage capable (CURR1, CURR2, CURR6)
  - Programmable Hardware Control (Strobe, and Preview or PWM)
  - Selectively Enable/Disable Current Sinks
  - Dynamic Luminance Scaling (DLS) support to improve backlight operating time (can adjust any current source)
  - Light Sensor input with internal hardware processing to control backlight according to ambient light using 3 groups - any current source can select one of the groups or no light sensor control
- Internal PWM Generation
  - 8 Bit resolution
  - Autonomous Logarithmic up/down dimming
- Led Pattern Generator
  - Autonomous driving for Fun RGB LEDs
  - Support indicator LEDs
- 10-bit Successive Approximation ADC
  - 27µs Conversion Time
  - Selectable Inputs: VANA/GPI, GPIO1/DLS, GPIO2/LIGHT, all current sources, VBAT, CPOUT, DCDC_FB
  - Internal Temp. Measurement
  - Light Sensor input with Java support (JSR-256): read ADC processed value
- Support for automatic LED testing (open and shorted LEDs can be identified)
- Strobe Timeout protection
  - Up to 1600ms
  - Three different timing modes
- Two General Purpose Inputs/Output
  - GPIO1/DLS, GPIO2/LIGHT
  - Digital Input, Digital Output using VANA/GPI supply and Tristate
  - GPIOs Programmable Pull-Up/Down
- Programmable LDO
  - 1.8 to 3.35V, 150mA
  - Programmable via Serial Interface
- Standby LDO always on
  - Regulated 2.5V max. output 10mA
  - 3µA Quiescent Current
- Audio can be used to drive RGB LED(s)
  - Color and Brightness depends on audio amplitude
- Wide Battery Supply Range: 3.0 to 5.5V
- Two Wire Serial Interface Control
- Over current and Thermal Protection
- WL-CSP30 3x2.5mm, 0.5mm pitch Package

3 Applications

Power- and lighting-management for mobile telephones and other 1-cell Li+ or 3-cell NiMH powered devices.

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Figure 1. AS3676 Block Diagram



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4 Pinout

Table 1. Pin Description for AS3676

Pin Number	Pin Name	Type	Description
A1	GPIO1/DLS	AIO	Digital Luminance Scaling PWM input and General Purpose Input Output 1
A2	VANA/GPI	AIO	LDO Output/General Purpose Input
A3	C2_N	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
A4	C1_P	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
A5	CPOUT	AO	Output voltage of the Charge Pump; connect a ceramic capacitor of 1µF (±20%).
A6	DATA	DIO	Serial interface data input/output.
B1	GPIO2/LIGHT	AIO	Ambient Light Sensor input and General Purpose Input Output 2
B2	VSS_CP	GND	Ground Pad for Charge Pump
B3	C1_N	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
B4	C2_P	AIO	Charge Pump flying capacitor; connect a ceramic capacitor of 500nF to this pin.
B5	DCDC_GATE	AO	DCDC gate driver.
B6	CLK	DI	Clock input for serial interface.
C1	CURR41	AI	Analog current sink input
C2	RGB3	AI	Analog current sink input
C3	VSS	GND	Ground pad
C4	VBAT	S	Supply pad. Connect to battery.
C5	CURR30	AI	Analog current sink input, intended for activity icon LED
C6	DCDC_SNS	AI	Sense input of shunt resistor for Step Up DC/DC Converter.
D1	CURR43	AI	Analog current sink input
D2	RGB1	AI	Analog current sink input
D3	CURR33	AI	Analog current sink input, intended for activity icon LED
D4	CURR31	AI	Analog current sink input, intended for activity icon LED
D5	CURR2	AI_HV	Analog current sink input (intended for Keyboard backlight)
D6	DCDC_FB	AI	DCDC feedback. Connect to resistor string.
E1	CURR42	AI	Analog current sink input
E2	RGB2	AI	Analog current sink input
E3	CURR32	AI	Analog current sink input, intended for activity icon LED
E4	CURR6	AI_HV	Analog current sink input (intended for Keyboard backlight)
E5	CURR1	AI_HV	Analog current sink input (intended for Keyboard backlight)
E6	V2_5	AO3	Output voltage of the Low-Power LDO; always connect a ceramic capacitor of 1µF (±20%) or 2.2µF (+100%/-50%).

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4.1 Pin Definitions

Table 2. Pin Type Definitions

Type	Description
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
AIO	Analog Pad
AI	Analog Input
AI_HV	High-Voltage (26V) Pin
AO3	Analog Output (3.3V)
S	Supply Pad
GND	Ground Pad

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5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 4, “Operating Conditions,” on page 6 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
V_{IN_HV}	26V Pins	-0.3	26	V	Applicable for high-voltage current sink pins CURR1, CURR2, CURR6
V_{IN_MV}	5V Pins	-0.3	7.0	V	Applicable for 5V pins VBAT, CURR30-33, CURR41-43, RGB1-3, C1_N, C2_N, C1_P, C2_P, CPOUT, DCDC_FB, DCDC_GATE, CLK, DATA;
V_{IN_LV}	3.3V Pins	-0.3	5.0	V	Applicable for 3.3V pins V2_5; DCDC_SNS, GPIO1/DLS, GPIO2/LIGHT, VANA/GPI
	Input Pin Current	-25	+25	mA	At 25ºC, Norm: JEDEC 17
T_{strg}	Storage Temperature Range	-55	125	ºC	
I_{IN}	Humidity	5	85	%	Non-condensing
V_{ESD}	Electrostatic Discharge	-2000	2000	V	Norm: MIL 883 E Method 3015
Pt	Total Power Dissipation		0.75	W	TA = 70 ºC, Tjunc_max = 125ºC
T_{BODY}	Peak Body Temperature		260	ºC	T = 20 to 40s, in accordance with IPC/JEDEC J-STD 020.
MSL	Moisture Sensitivity Level	MSL 1			Represents a max. floor life time of unlimited

6 Electrical Characteristics

Table 4. Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
General Operating Conditions						
V_{HV}	High Voltage	Applicable for high-voltage current sink pins $CURR_1$, CURR2 and CURR6.	0.0		26.0	V
V_{BAT}	Battery Voltage	Pin VBAT	3.0	3.6	5.5	V
V_{PERI}	Periphery Supply Voltage	For serial interface pins.	1.5		5.5	V
V_{2_5}	Voltage on Pin V2_5	Internally generated	2.4	2.5	2.6	V
T_{AMB}	Operating Temperature Range		-30	25	85	ºC
I_{ACTIVE}	Battery current	Normal Operating current (see Operating Modes on page 80)		110		µA
$I_{STANDBY}$	Standby Mode Current	Current consumption in standby mode. Only 2.5V regulator on, interface active		8	13	µA
$I_{SHUTDOWN}$	Shutdown Mode Current	interface inactive (CLKand DATA set to 0V)		0.1	3	µA

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7 Typical Operating Characteristics

Figure 2. DCDC Step Up Converter: Efficiency of +15V, Step Up to 15V vs. Load Current at VBAT=*3.8V*

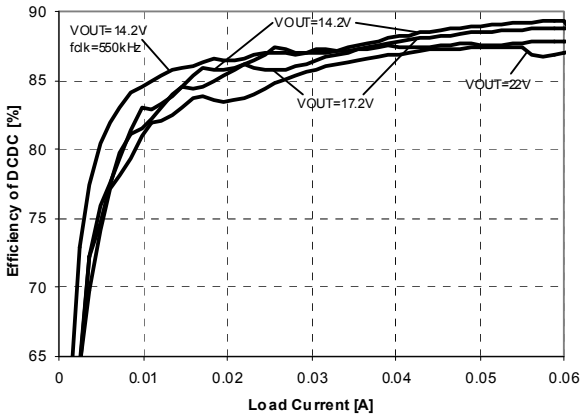


Figure 3. Charge Pump: Efficiency vs. VBAT

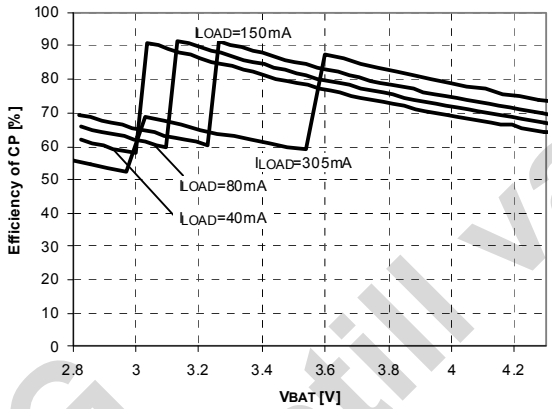


Figure 4. Charge Pump: Battery Current vs. VBAT

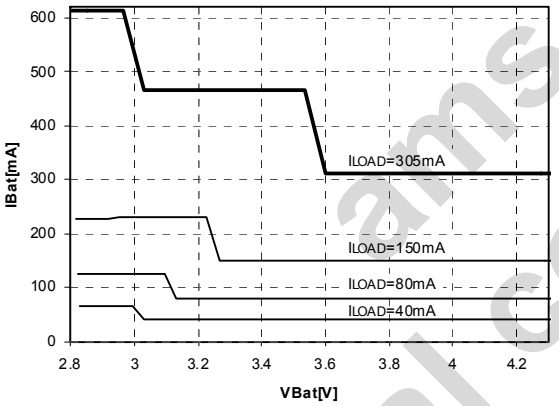


Figure 5. Current Sink CURR1 vs. V(CURRx)

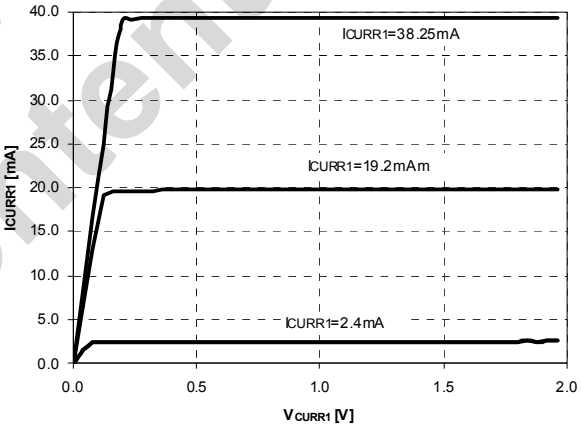
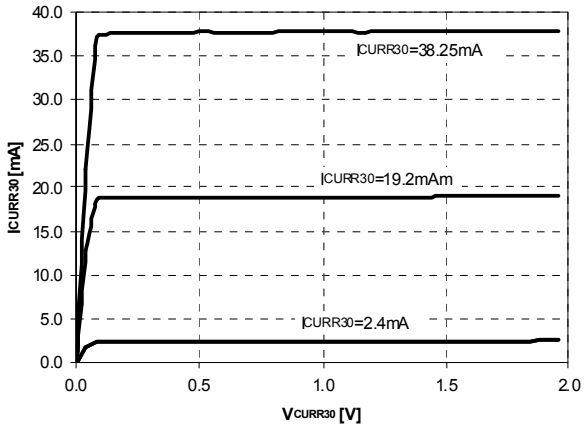


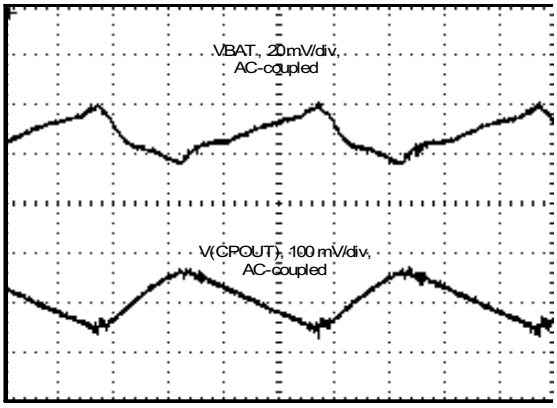
Figure 6.

Figure 7. Current Sink CURR3x vs. VBAT



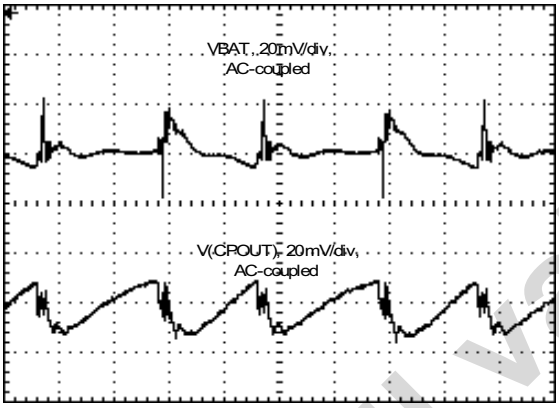
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Figure 8. Charge Pump Input and Output Ripple 1:1.5 Mode, 100mA load



250ns/div
Measured with battery (3.8V) on demoboard

Figure 9. Charge Pump Input and Output Ripple 1:2 Mode, 100mA load



250ns/div
Measured with battery (3.0V) on demoboard

VBAT = 3.6V, T_A = +25ºC (unless otherwise specified).

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8 Detailed Description

8.1 Analog LDO

The LDO is a general purpose LDO and the output pin connected to VANA/GPI. The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF ±20% (X5R) or 2.2µF +100/-50%(Z5U). The low ESR of these capacitors ensures low output impedance at high frequencies. The low impedance of the power transistor enables the device to deliver up to 150mA even at nearly discharged batteries without any decrease in performance.

The LDO is off by default after start-up.

Figure 10. Analog LDO Block Diagram

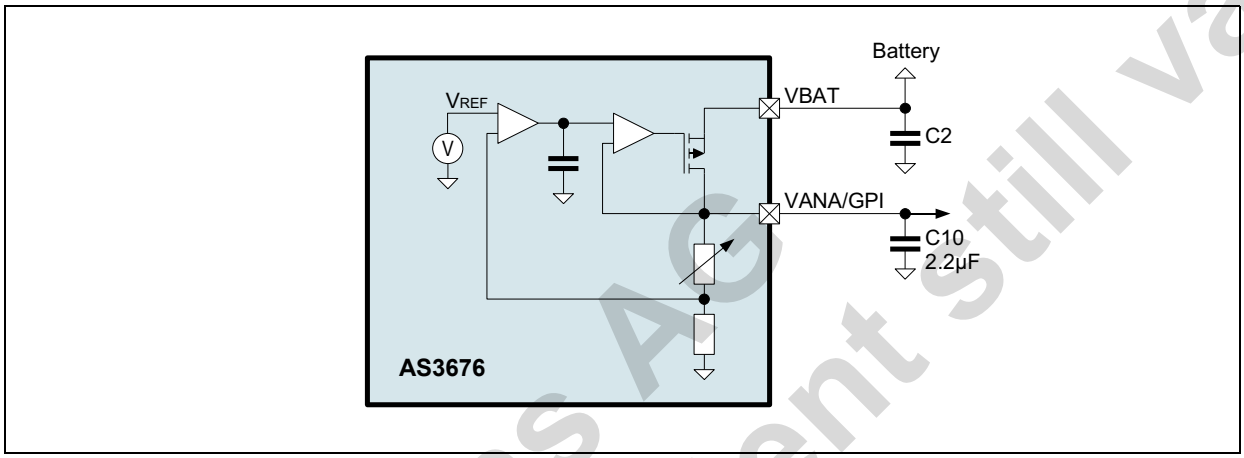


Table 5. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{BAT}	Supply Voltage Range		3.0		5.5	V
R_{ON}	On Resistance	@150mA, full operating temperature range			1.0	Ω
$V_{DROPOUT}$	Dropout Voltage	@150mA			150	mV
		@50mA			50	mV
I_{ON}	Supply Current	Without load		50		µA
		With 150mA load		150		
I_{OFF}	Shutdown Current	Without load			100	nA
t_{start}	Start-up Time				200	µs
V_{out_tol}	Output Voltage Tolerance		-3		+3	%
V_{OUT}	Output Voltage	V_{BAT} = 3.0V and I_{OUT}=150mA	1.8		2.85	V
		Full Programmable Range; V_{BAT} > V_{OUT}+ 150mV and I_{OUT}<=150mA	1.8		3.35	V
I_{LIMIT} [1]	LDO Current Limit	Pin VANA/GPI. LDO acts as current source if the output current exceeds I_{LIMIT}.	300	450 [2]		mA

1. Not production tested – guaranteed by design and laboratory verification
2. During startup of the LDO the current limit is half the value of I_{LIMIT}

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8.1.1 LDO Registers

Table 6. Reg. control Register

Addr: 00		Reg. control			
		This register enables/disables the LDOs, Charge Pumps, Charge Pump LEDs, current sinks, the Step Up DC/DC Converter, and low-power mode.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	ldo_on	0	R/W	0	Analog LDO is switched off
				1	Analog LDO is switched on

Table 7. LDO Voltage Register

Addr: 07h		LDO Voltage			
		This register sets the output voltage (VANA/GPI) for the LDO.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4:0	ldo_voltage	00000b	R/W	Controls LDO voltage selection.	
				00000b	1.8V
				...	LSB=50mV
				11111b	3.35V

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8.2 Step Up DC/DC Converter

The Step Up DC/DC Converter is a high-efficiency current mode PWM regulator, providing output voltage up to e.g. 25V/50mA[1]. A constant switching-frequency results in a low noise on the supply and output voltages.

Figure 11. Step Up DCDC Converter Block Diagram Option: Current Feedback with Over voltage protection

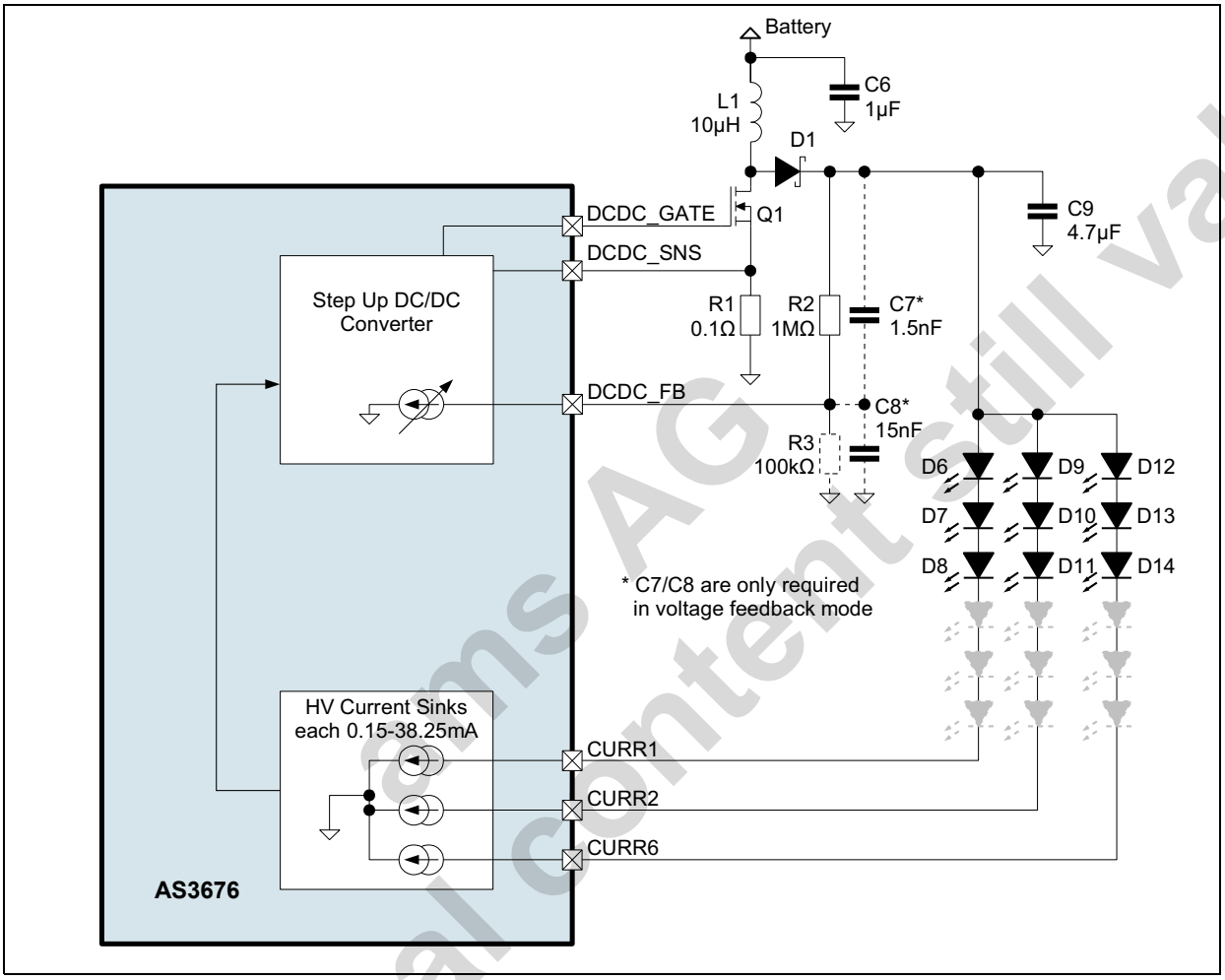


Table 8. Step Up DC/DC Converter Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IVDD	Quiescent Current	Pulse skipping mode.		140		µA
VFB1	Feedback Voltage for External Resistor Divider	For constant voltage control. *step_up_res* = 1	1.20	1.25	1.30	V
VFB2	Feedback Voltage for Current Sink Regulation	on CURR1, CURR2 or CURR6 in regulation. *step_up_res* = 0	0.4	0.5	0.6	V

1. The AS3676 internal driver structure allows output voltage higher than 25V. The Over voltage Protection in Current Feedback Mode (see page 13) or Voltage Feedback (see page 14) should be set to fit to the external components used (maximum voltage rating of Q1, C9 and D1).

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Table 8. Step Up DC/DC Converter Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DCDC_FB}	Additional Tuning Current at Pin DCDC_FB and over voltage protection	Adjustable by software using Register DCDC control1 1µA step size (0-31µA) $V_{PROTECT}$ = 1.25V + I_{DCDC_FB} * R_2	0		31	µA
	Accuracy of Feedback Current at full scale		-6		6	%
V_{rsense_max}	Current Limit Voltage at R_1	e.g., 1.32A for 0.1Ω sense resistor R_1.	92	132	170	mV
		For fixed startup time of 500us	50	66	86	
		If step_up_lowcur= 1	60	86	114	
R_{SW}	Switch Resistance	ON-resistance of external switching transistor.			1	Ω
I_{LOAD}	Load Current	At 26V output voltage	0		50	mA
f_{IN}	Switching Frequency	Internally trimmed	0.9	1	1.1	MHz
C_{OUT}	Output Capacitor	Ceramic, ±20%. Use nominal 4.7µF capacitors to obtain at least 0.7µF under all conditions (voltage dependence of capacitors)	0.7	4.7		µF
L	Inductor	Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency.	7	10	13	µH
t_{MIN_ON}	Minimum on Time		90	140	190	ns
MDC	Maximum Duty Cycle		90			%
Vripple	Voltage ripple >20kHz	Cout=4.7µF,Iout=0..45mA, VBAT=3.0...4.2V			160	mV
	Voltage ripple <20kHz				40	mV
Efficiency	Efficiency	Iout=20mA,Vout=17V,VBAT=3.8V		85		%

To ensure soft startup of the dcdc converter, the over current limits are reduced for a fixed time after enabling the dcdc converter. The total startup time for an output voltage of e.g. 26V is less than 2ms. If C7 and C8 are mounted and the bit step_up_prot is set, the total startup time can exceed 2ms.

Note: If the DCDC converter is only used in current feedback mode (CURR1, CURR2 or CURR6 - and not used for a constant voltage source), the capacitors C7 and C8 can be removed.

8.2.1 Feedback Selection

Register DCDC control1 and DCDC control2 selects the type of feedback for the Step Up DC/DC Converter.

The feedback for the DC/DC converter can be selected either by current sinks (CURR1, CURR2, CURR6) or by a voltage feedback at pin DCDC_FB. If the register bit step_up_fb_auto is set, the feedback path is automatically selected between CURR1, CURR2 and CURR6 (the lowest voltage of these current sinks is used).

Setting step_up_fb enables feedback on the pins CURR1, CURR2 or CURR6. The Step Up DC/DC Converter is regulated such that the required current at the feedback path can be supported. (Bit step_up_res should be set to 0 in this configuration)

Note: Always choose the path with the highest voltage drop as feedback to guarantee adequate supply for the other (unregulated) paths or enable the register bit step_up_fb_auto.

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8.2.2 Over voltage Protection in Current Feedback Mode

The over voltage protection in current feedback mode (step_up_fb = 01, 10 or 11 or step_up_fb_auto = 1) works as follows: Only resistor R2 and C7/C8[2] is soldered and R3 is omitted. An internal current source (sink) is used to generate a voltage drop across the resistor R2. If then the voltage on DCDC_FB is above 1.25V and step_up_prot=1, the DCDC is momentarily disabled to avoid too high voltages on the output of the DCDC converter. When the voltage on DCDC_FB drops below 1.25V, the DCDC automatically resumes operation.

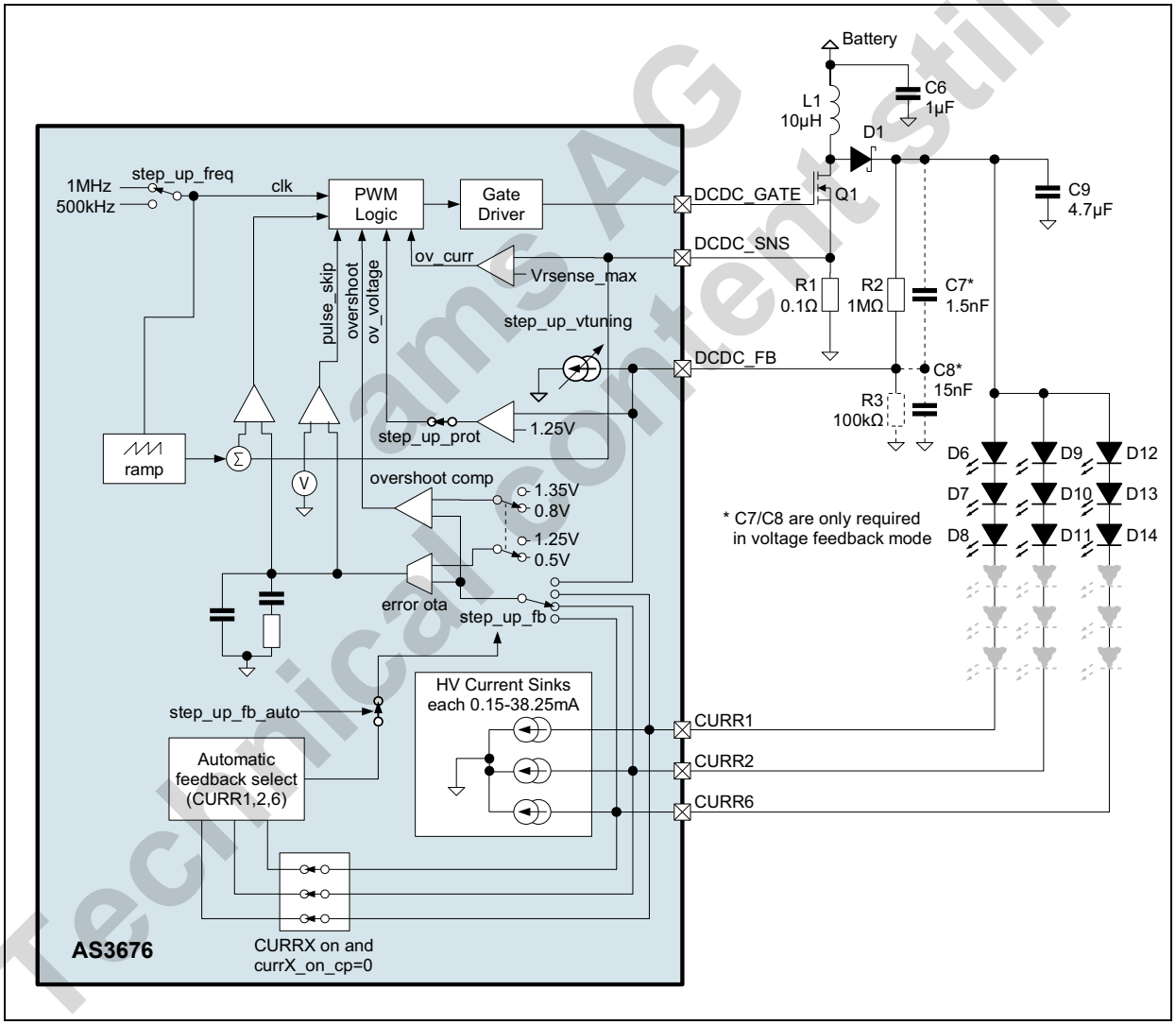
The protection voltage can be calculated according to the following formula:

$$V_{PROTECT} = 1.25V + I_{DCDC_FB} * R_2 \qquad \text{(EQ 1)}$$

Note: The voltage on the pin DCDC_FB is limited by an internal protection diode to VBAT + one diode forward voltage (typ. 0.6V).

If the over voltage protection is not used in current feedback mode, connect DCDC_FB to ground.

Figure 12. Step Up DC/DC Converter Detail Diagram; Option: Regulated Output Current, Feedback is automatically selected between CURR1, CURR2, CURR6 (step_up_fb_auto=1); over voltage protection is enabled (step_up_prot=1); 1MHz clock frequency (step_up_frequ=0)



2. If the DCDC converter is only used in current feedback mode (CURR1, CURR2 or CURR6 - and not used for a constant voltage source), the capacitors C7 and C8 can be removed.

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8.2.3 Voltage Feedback

Setting bit step_up_fb (see page 15) = 00 enables voltage feedback at pin DCDC_FB. Capacitors C7 and C8 have to be soldered in this operating mode.

The output voltage is regulated to a constant value, given by (Bit step_up_res should be set to 1 in this configuration)

$$U_{Step\ up_out} = (R2+R3)/R3 * 1.25 + I_{DCDC_FB} * R2 \quad (EQ\ 2)$$

If R3 is not used, the output voltage is by (Bit step_up_res should be set to 0 in this configuration)

$$U_{Step\ up_out} = 1.25 + I_{DCDC_FB} * R2 \quad (EQ\ 3)$$

Where:

$U_{Step\ up_out}$ = Step Up DC/DC Converter output voltage

$R2$ = Feedback resistor R2

$R3$ = Feedback resistor R3

I_{DCDC_FB} = Tuning current at ball DCDC_FB; 0 to 31µA

Table 9. Voltage Feedback Example Values

I_{DCDC_FB}	$U_{Step\ up_out}$	$U_{Step\ up_out}$
µA	**R2 = 1MΩ, R3 not used**	**R2 = 500kΩ, R3 = 50kΩ**
0	-	13.75
1	-	14.25
2	-	14.75
3	-	15.25
4	-	15.75
5	6.25	16.25
6	7.25	16.75
7	8.25	17.25
8	9.25	17.75
9	10.25	18.25
10	11.25	18.75
11	12.25	19.25
12	13.25	19.75
13	14.25	20.25
14	15.25	20.75
15	16.25	21.25
…	…	…
30	31.25	28.75
31	32.25	29.25

Note: The voltage on CURR1, CURR2 and CURR6 must not exceed 26V (see page 25)

8.2.4 PCB Layout Hints

To ensure good EMC performance of the DCDC converter, keep its external power components C6, R1, L1, Q1, D1 and C9 close together. Connect the ground of C6, R1 and C9 locally together and connect this with a short path to AS3676 VSS. This ensures that local high-frequency currents will not flow to the battery.

8.2.5 Unused DCDC converter

If the DCDC converter is not used, connect DCDC_SNS to GND. DCDC_FB[3] and DCDC_GATE can be left open.

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8.2.6 Step up Registers

Table 10. Reg. control Register

Addr: 00		Reg. control			
		This register enables/disables the Charge Pump and the Step Up DC/DC Converter.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
3	step_up_on	0	R/W	Enable the step up converter	
				0b	Disable the Step Up DC/DC Converter
				1b	Enable the Step Up DC/DC Converter

Table 11. DCDC control1 Register

Addr: 21h		DCDC control1			
		This register controls the Step Up DC/DC Converter.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	step_up_frequ	0	R/W	Defines the clock frequency of the Step Up DC/DC Converter.	
				0	1MHz
				1	500kHz
2:1	step_up_fb	00	R/W	Controls the feedback source if step_up_fb_auto = 0	
				00	DCDC_FB enabled (external resistor divider). Set step_up_fb=00 (DCDC_FB)
				01	CURR1 feedback enabled (feedback via LEDs)
				10	CURR2 feedback enabled (feedback via LEDs)
				11	CURR6 feedback enabled (feedback via LEDs)
7:3	step_up_vtuning	00000	R/W	Defines the tuning current at pin DCDC_FB.	
				00000	0 µA
				00001	1 µA
				00010	2 µA
				....	
				10000	15 µA
				.....	
				11111	31 µA

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3. DCDC_FB can be used as a general purpose ADC input (see Analog-to-Digital Converter on page 65)

Table 12. DCDC control2 Register

Addr: 22h		DCDC control2			
		This register controls the Step Up DC/DC Converter and low-voltage current sinks CURR3x.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	step_up_res	0	R/W	Gain selection for Step Up DC/DC Converter	
				0	Select 0 if Step Up DC/DC Converter is used with current feedback (CURR1, CURR2, CURR6) or if DCDC_FB is used with current feedback only – R2, C7, C8 connected, R3 not used
				1	Select 1 if DCDC_FB is used with external resistor divider using 2 resistors: R2 and R3
1	skip_fast	0	R/W	Step Up DC/DC Converter output voltage at low loads, when pulse skipping is active	
				0	Accurate output voltage, more ripple
				1	Elevated output voltage, less ripple
2	step_up_prot	1	R/W	Step Up DC/DC Converter protection	
				0	No over voltage protection
				1	Over voltage protection on pin DCDC_FB enabled voltage limitation =1.25V on DCDC_FB
3	step_up_lowcur	0	R/W	Step Up DC/DC Converter coil current limit	
				0	Normal current limit
				1	Current limit reduced by approx. 33%
7	step_up_fb_auto	0	R/W	0	step_up_fb selects the feedback of the DCDC converter
				1	If step_up_fb is not DCDC_FB (00), then feedback is automatically chosen within the current sinks CURR1, CURR2 and CURR6. Only those are used for this selection, which are enabled (currX_mode must not be 00) and not connected to the charge pump (currX_on_cp must be 0).

8.3 Charge Pump

The Charge Pump uses two external flying capacitors C3, C4 to generate output voltages higher than the battery voltage. There are three different operating modes of the charge pump itself:

- 1:1 Bypass Mode
  - Battery input and output are connected by a low-impedance switch
  - battery current = output current.
- 1:1.5 Mode
  - The output voltage is up to 1.5 times the battery voltage (without load), but is limited to VCPOUTmax all the time
  - battery current = 1.5 times output current.
- 1:2 Mode
  - The output voltage is up to 2 times the battery voltage (without load), but is limited to VCPOUTmax all the time
  - battery current = 2 times output current

As the battery voltage decreases, the Charge Pump must be switched from 1:1 mode to 1:1.5 mode and eventually in 1:2 mode in order to provide enough supply for the current sinks. Depending on the actual current the mode with best overall efficiency can be automatically or manually selected:

Examples:

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- Battery voltage = 3.7V, LED dropout voltage = 3.5V. The 1:1 mode will be selected and there is 200mV drop on the current sink and on the Charge Pump switch. Efficiency 95%.
- Battery voltage = 3.5V, LED dropout voltage = 3.5V. The 1:1.5 mode will be selected and there is 1.5V drop on the current sink and 250mV on the Charge Pump. Efficiency 66%.

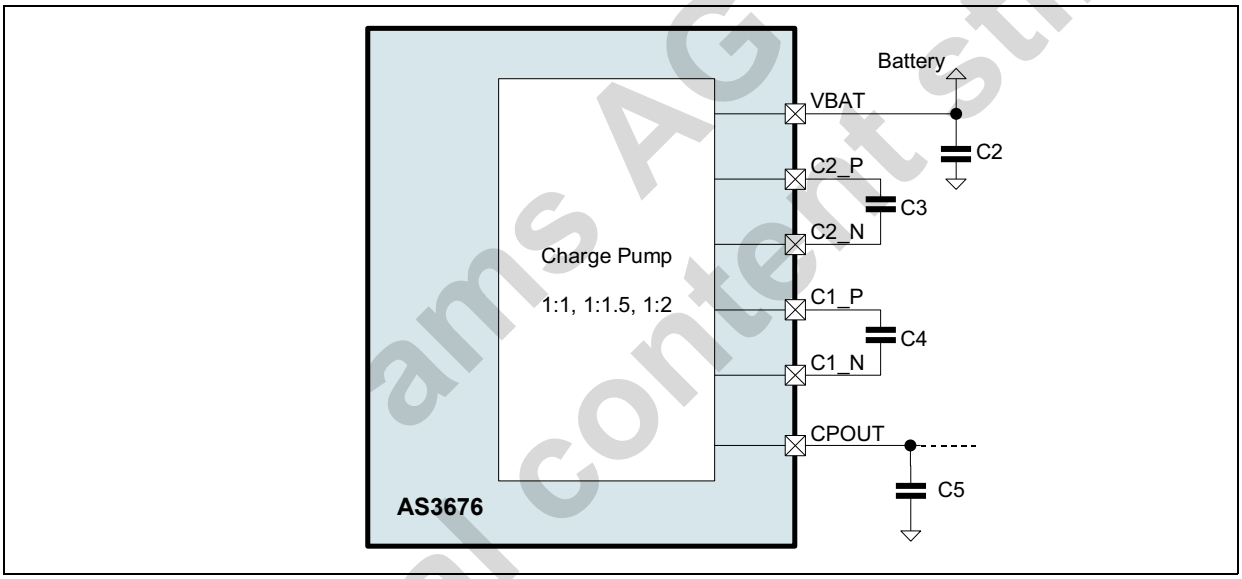
The efficiency is dependent on the LED forward voltage given by:

$$Eff=(V_LED*Iout)/(Uin*Iin) \quad (EQ\ 4)$$

The charge pump mode switching can be done manually or automatically with the following possible software settings:

- Automatic up all modes allowed (1:1, 1:1.5, 1:2)
  - Start with 1:1 mode
  - Switch up automatically 1:1 to 1:1.5 to 1:2
- Automatic up, but only 1:1 and 1:1.5 allowed
  - Start with 1:1 mode
  - Switch up automatically only from 1:1 to 1:1.5 mode; 1:2 mode is not used
- Manual
  - Set modes 1:1, 1:1.5, 1:2 by software

Figure 13. Charge Pump Pin Connections



The Charge Pump requires the external components listed in the following table:

Table 13. Charge Pump External Components

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_2	External Decoupling Capacitor	Ceramic low-ESR capacitor between pins VBAT and VSS.		1.0		µF
C_3, C_4	External Flying Capacitor (2x)	Ceramic low-ESR capacitor between pins C1_P and C1_N, between pins C2_P and C2_N and between VBAT and VSS		1.0		µF
C_5	External Storage Capacitor	Ceramic low-ESR capacitor between pins CPOUT and VSS, pins CPOUT and VSS. Use nominal 2.2µF capacitors (size 0603)		2.2		µF

Note: The connections of the external capacitors C2, C3, C4 and C5 should be kept as short as possible.

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The maximum voltage on the flying capacitors C3 and C4 is VBAT.

Table 14. Charge Pump Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICPOUT	Output Current Continuous	Depending on PCB layout	0.0		400	mA
	Output Current Pulsed	max. 200ms V_{CPOUT}= VBAT * CP_{MODE} – I_{LOAD} * R_{CP}	0.0		500	mA
VCPOUTmax	Output Voltage	Internally limited, Including output ripple			5.6	V
η	Efficiency	Including current sink loss; ICPOUT < 100mA.	60		90	%
ICP1_1.5	Power Consumption without Load fclk = 1 MHz	1:1.5 Mode		3.4		mA
ICP1_2		1:2 Mode		3.8		
Rcp1_1	Effective Charge Pump Output Resistance (Open Loop, fclk = 1MHz)	1:1 Mode; VBAT ≥ 3.5V		0.57		Ω
Rcp1_1.5		1:1.5 Mode; VBAT ≥ 3.3V		2.65		
Rcp1_2		1:1.2 Mode; VBAT ≥ 3.1V		3.25		
fclk Accuracy	Accuracy of Clock Frequency		-10		10	%
currhv_switch	CURR1, 2, 6 minimum voltage	If the voltage drops below this threshold, the charge pump will use the next available mode (1:1 -> 1:1.5 or 1:1.5 -> 1:2)			0.45	V
currlv_switch	CURR30-33, RGB1-3, CURR41-3, minimum voltage				0.2	V
	CURR30-33 0-75.6mA range for strobe if curr3x_strobe_high= 1				0.4	V
t_{deb}	CP automatic up-switching debounce time	cp_start_debounce=0		240		µsec
		After switching on CP (cp_on set to 1), if cp_start_debounce=1		2000		µsec

8.3.1 Charge Pump Mode Switching

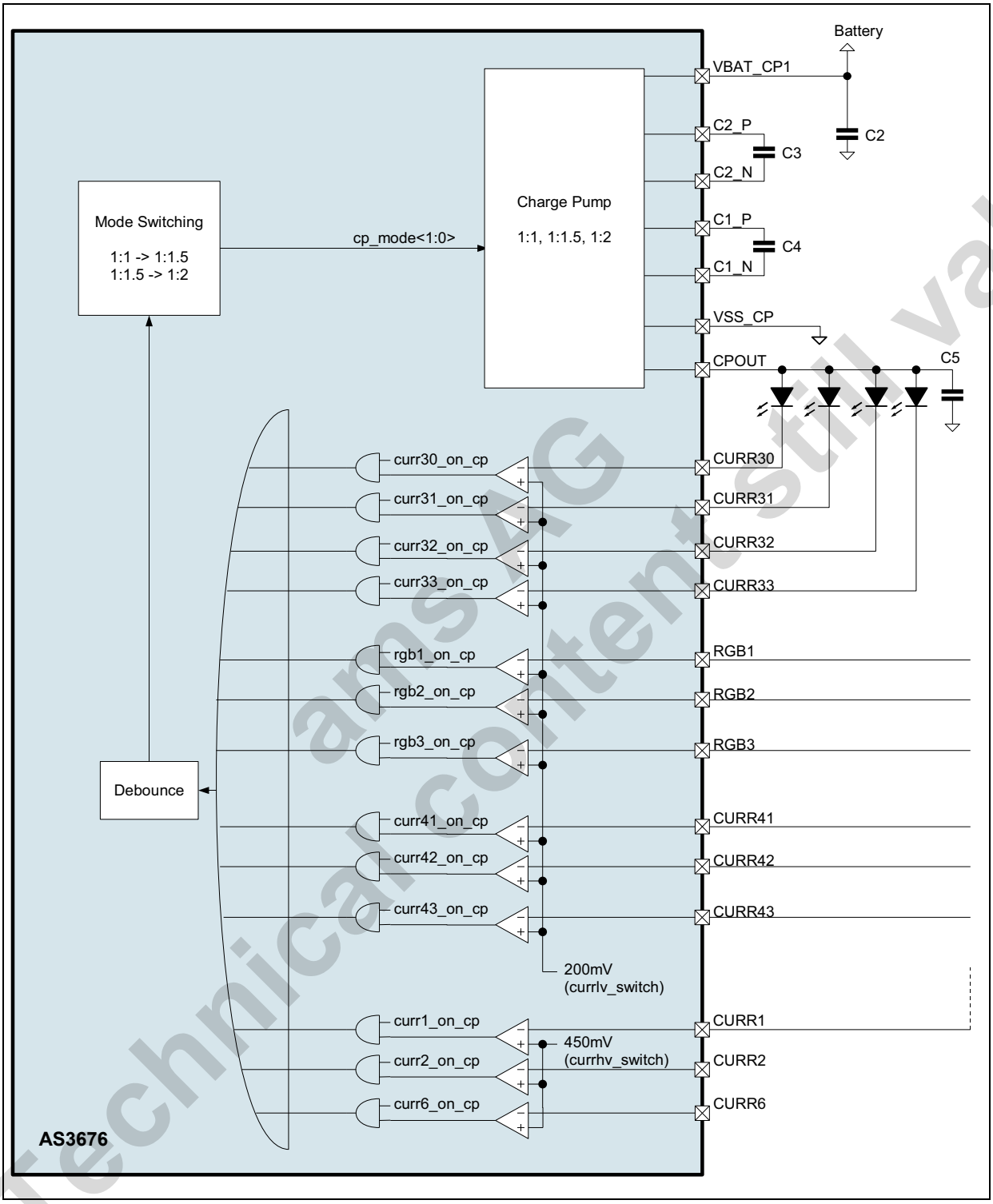
If automatic mode switching is enabled (cp_mode_switching (see page 20) = 00 or cp_mode_switching = 01) the charge pump monitors the current sinks, which are connected via a led to the output CPOUT. To identify these current sources (sinks), the registers CP mode Switch1 and CP mode Switch2 (register bits curr30_on_cp (see page 21) … curr33_on_cp, rgb1_on_cp … rgb3_on_cp, curr1_on_cp, curr2_on_cp, curr41_on_cp … curr43_on_cp and curr6_on_cp) should be setup before starting the charge pump (cp_on (see page 20) = 1). If any of the voltage on these current sources drops below the threshold (currlv_switch, currhv_switch), the next higher mode is selected after the debounce time.

To avoid switching into 1:2 mode (battery current = 2 times output current), set cp_mode_switching = 01.

If the currX_on_cp=0 and the according current sink is connected to the charge pump, the current sink will be functional, but there is no up switching of the charge pump, if the voltage compliance is too low for the current sink to supply the specified current.

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Figure 14. Automatic Mode Switching



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8.3.2 Soft Start

An implemented soft start mechanism reduces the inrush current. Battery current is smoothed when switching the charge pump on and also at each switching condition. This precaution reduces electromagnetic radiation significantly.

8.3.3 Unused Charge Pump

If the charge pump is not used, capacitors C3, C4 and C5 can be removed. The pins C1_P, C1_N, C2_P, C2_N and CPOUT should be left open and keep register cp_on and cp_auto_on at 0 (default value).

8.3.4 Charge Pump Registers

Table 15. Reg. control Register

Addr: 00h		Reg. control			
		This register controls the Charge Pump.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2	cp_on	0	R/W	0	Set Charge Pump into 1:1 mode (off state) unless cp_auto_on is set
				1	Enable manual or automatic mode switching

Table 16. CP control Register

Addr: 23h		CP control			
		This register enables/disables the Charge Pump and the Step Up DC/DC Converter.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	cp_clk	0	R/W	Clock frequency selection.	
				0	1 MHz
				1	500 kHz
2:1	cp_mode	00b	R/W	Charge Pump mode (in manual mode sets this mode, in automatic mode reports the actual mode used)[1]	
				00	1:1 mode
				01	1:1.5 mode
				10	1:2 mode
				11	NA
4:3	cp_mode_switching	00b	R/W	Set the mode switching algorithm	
				00	Automatic Mode switching; 1:1, 1:1.5 and 1:2 allowed
				01	Automatic Mode switching; only 1:1 and 1:1.5 allowed
				10	Manual Mode switching; register cp_mode defines the actual charge pump mode used
				11	Reserved
5	cp_start_debounce	0	R/W	0	Mode switching debounce timer is always 240µs
				1	Upon startup (cp_on set to 1) the mode switching debounce time is first started with 2ms then reduced to 240µs
6	cp_auto_on	0	R/W	0	Charge Pump is switched on/off with cp_on
				1	Charge Pump is automatically switched on if a current sink, which is connected to the charge pump (defined by registers CP Mode Switch 1 & 2) is switched on

1. Direct switching from 1:1.5 mode into 1:2 in manual mode and vice versa is not allowed. Always switch over 1:1 mode.

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Table 17. CP mode Switch1 Register

Addr: 24h		CP mode Switch1			
		Setup which current sinks are connected (via leds) to the charge pump; if set to '1' the correspond current source (sink) is used for automatic mode selection of the charge pump			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	curr30_on_cp	0	R/W	0	current Sink CURR30 is not connected to charge pump
				1	current sink CURR30 is connected to charge pump
1	curr31_on_cp	0	R/W	0	current Sink CURR31 is not connected to charge pump
				1	current sink CURR31 is connected to charge pump
2	curr32_on_cp	0	R/W	0	current Sink CURR32 is not connected to charge pump
				1	current sink CURR32 is connected to charge pump
3	curr33_on_cp	0	R/W	0	current Sink CURR33 is not connected to charge pump
				1	current sink CURR33 is connected to charge pump
4	rgb1_on_cp	0	R/W	0	current Sink RGB1 is not connected to charge pump
				1	current sink RGB1 is connected to charge pump
5	rgb2_on_cp	0	R/W	0	current Sink RGB2 is not connected to charge pump
				1	current sink RGB2 is connected to charge pump
6	rgb3_on_cp	0	R/W	0	current Sink RGB3 is not connected to charge pump
				1	current sink RGB3 is connected to charge pump

Table 18. CP mode Switch2 Register

Addr: 25h		CP mode Switch2			
		Setup which current sinks are connected (via LEDs) to the charge pump; if set to '1' the correspond current source (sink) is used for automatic mode selection of the charge pump			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	curr1_on_cp	0	R/W	0	current Sink CURR1is not connected to charge pump
				1	current sink CURR1 is connected to charge pump
1	curr2_on_cp	0	R/W	0	current Sink CURR2 is not connected to charge pump
				1	current sink CURR2 is connected to charge pump
2	curr41_on_cp	0	R/W	0	current Sink CURR41 is not connected to charge pump
				1	current sink CURR41 is connected to charge pump
3	curr42_on_cp	0	R/W	0	current Sink CURR42 is not connected to charge pump
				1	current sink CURR42 is connected to charge pump

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Table 18. CP mode Switch2 Register (Continued)

Addr: 25h		CP mode Switch2			
		Setup which current sinks are connected (via LEDs) to the charge pump; if set to '1' the correspond current source (sink) is used for automatic mode selection of the charge pump			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	curr43_on_cp	0	R/W	0	current Sink CURR43 is not connected to charge pump
				1	current sink CURR43 is connected to charge pump
7	curr6_on_cp	0	R/W	0	current Sink CURR6 is not connected to charge pump
				1	current sink CURR6 is connected to charge pump

Table 19. Curr low voltage status1 Register

Addr: 2Ah		Curr low voltage status1			
		Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	curr30_low_v	NA	R	0	voltage of current Sink CURR30 >currlv_switch
				1	voltage of current Sink CURR30 <currlv_switch
1	curr31_low_v	NA	R	0	voltage of current Sink CURR31 >currlv_switch
				1	voltage of current Sink CURR31 <currlv_switch
2	curr32_low_v	NA	R	0	voltage of current Sink CURR32 >currlv_switch
				1	voltage of current Sink CURR32 <currlv_switch
3	curr33_low_v	NA	R	0	voltage of current Sink CURR33 >currlv_switch
				1	voltage of current Sink CURR33 <currlv_switch
4	rgb1_low_v	NA	R	0	voltage of current Sink RGB1 >currlv_switch
				1	voltage of current Sink RGB1 <currlv_switch
5	rgb2_low_v	NA	R	0	voltage of current Sink RGB2 >currlv_switch
				1	voltage of current Sink RGB2 <currlv_switch
6	rgb3_low_v	NA	R	0	voltage of current Sink RGB3 >currlv_switch
				1	voltage of current Sink RGB31 <currlv_switch
7	curr6_low_v	NA	R	0	voltage of current Sink CURR6 >currlv_switch
				1	voltage of current Sink CURR6 <currlv_switch

Table 20. Curr low voltage status2 Register

Addr: 2Bh		Curr low voltage status2			
		Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	curr1_low_v	NA	R	0	voltage of current Sink CURR1 >currhv_switch
				1	voltage of current Sink CURR1 <currhv_switch

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Table 20. Curr low voltage status2 Register (Continued)

Addr: 2Bh		Curr low voltage status2			
		Indicates the low voltage status of the current sinks. If the currX_low_v bit is set, the voltage on the current sink is too low, to drive the selected output current			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1	curr2_low_v	NA	R	0	voltage of current Sink CURR2 >currhv_switch
				1	voltage of current Sink CURR2 <currhv_switch
2	curr41_low_v	NA	R	0	voltage of current Sink CURR41 >currlv_switch
				1	voltage of current Sink CURR41 <currlv_switch
3	curr42_low_v	NA	R	0	voltage of current Sink CURR42 >currlv_switch
				1	voltage of current Sink CURR42 <currlv_switch
4	curr43_low_v	NA	R	0	voltage of current Sink CURR43 >currlv_switch
				1	voltage of current Sink CURR43 <currlv_switch

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8.4 Current Sinks

The AS3676 contains general purpose current sinks intended to control RGB LEDs, white LEDs (e.g. backlights) and can also be used for buzzers or vibrators. All current sinks have an integrated over voltage protection.

CURR1, CURR2 and CURR6 are also used as feedback for the Step Up DC/DC Converter (regulated to 0.5V in this configuration) see Feedback Selection on page 12.

- Current sinks CURR1, CURR2 and CURR6 are high-voltage compliant (26V) current sinks, used e.g., for series of white LEDs
- Current sinks CURR3*x* (CURR30, CURR31, CURR32 and CURR33) are parallel 5V current sinks, used for back-lighting, indicator LEDs or RGB LEDs.
- Current sinks RGB1, RGB2, and RGB3 are general purpose current sinks e.g. for a fun LED.
- Current sinks CURR4x (CURR41, CURR42, and CURR43) are general purpose current sinks.

Table 21. Current Sink Function Overview

Current Sink	Max. Voltage (V)	Max. Current (mA)	Resolution		Software Current Control	Hardware On/Off Control	Can be assigned to Audio Controlled LED Channel
			(Bits)	(mA)			
CURR1	26.0	38.25	8	0.15	Separate	LED Pattern; Internal PWM; external PWM at GPIO1/DLS	ch1
CURR2							ch2
CURR6							ch3
CURR30	VBAT (5.5V)	38.25 (75.6mA for strobe if curr3x_strobe_high=1)	8	0.15	Combined in Strobe/ Preview or Separated	Flash LED Strobe (CURR1 or CURR30) & Preview (CURR2); Internal PWM; LED Pattern; external PWM at GPIO1/DLS	Completely individual assignment of the audio channels ch1,ch2 and ch3 to the outputs
CURR31							
CURR32							
CURR33							
RGB1		38.25	8	0.15	Separate	LED Pattern; Internal PWM; external PWM at GPIO1/DLS	ch1
RGB2							ch2
RGB3							ch3
CURR41		38.25	8	0.15	Separate	LED Pattern; Internal PWM; external PWM at GPIO1/DLS	ch1
CURR42							ch2
CURR43							ch3

8.4.1 Unused Current Sinks

Unused current sinks can be left open or used as a ADC input (see Analog-to-Digital Converter on page 65).

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8.4.2 High Voltage Current Sinks CURR1, CURR2, CURR6

The high voltage current sinks have a resolution of 8 bits.

Table 22. HV Current Sinks Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
I_{BIT7}	Current sink if Bit7 = 1	For V(CURRx) > 0.45V			19.2		mA
I_{BIT6}	Current sink if Bit6 = 1				9.6		
I_{BIT5}	Current sink if Bit5 = 1				4.8		
I_{BIT4}	Current sink if Bit4 = 1				2.4		
I_{BIT3}	Current sink if Bit3 = 1				1.2		
I_{BIT2}	Current sink if Bit2 = 1				0.6		
I_{BIT1}	Current sink if Bit1 = 1				0.3		
I_{BIT0}	Current sink if Bit0 = 1				0.15		
Δm^1	matching Accuracy	CURR1,CURR2,CURR6	I_{BIT7} and I_{BIT6}	-5		+5	%
			all other bits	-10		+10	%
Δ^2	absolute Accuracy			-15		+15	%
$V_{CURR1,2,6x}$	Voltage compliance			0.45		26	V

1. Variation between currents within this group
2. Variation between the programmed current and the actual current

High Voltage Current Sinks CURR1, CURR2, CURR6 Registers

Table 23. Curr1 current Register

Addr: 09h		Curr1 current			
		This register controls the High voltage current sink current.			
Bit	Bit Name	Default	Access	Description	
7:0	curr1_current	0	R/W	Defines current into current sink curr1	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

Table 24. Curr2 current Register

Addr: 0Ah		Curr2 current			
		This register controls the High voltage current sink current.			
Bit	Bit Name	Default	Access	Description	
7:0	curr2_current	0	R/W	Defines current into current sink curr2	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

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Table 25. curr6 current Register

Addr: 2Fh		curr6 current			
		This register controls the High voltage current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	curr6_current	0	R/W	Defines current into current sink CURR6	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

Table 26. curr12 control Register

Addr: 01h		curr12 control			
		This register select the mode of the current sinks controls High voltage current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	curr1_mode	0	R/W	Select the mode of the current sink curr1	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled
3:2	curr2_mode	0	R/W	Select the mode of the current sink curr2	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled

Table 27. curr rgb control Register

Addr: 02h		curr rgb control			
		This register select the mode of the current sinks CURR6.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:6	curr6_mode	0	R/W	Select the mode of the current sink CURR6	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled

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8.4.3 Current Sinks CURR30, CURR31, CURR32, CURR33

These current sinks have a resolution of 8 bits and can sink up to 38.25mA. The current values can be controlled individually with curr30_current – curr33_current or common with curr3x_strobe or curr3x_preview.

Table 28. Current Sinks CURR30,31,32,33 Parameters

Symbol	Parameter	Condition		Min	Typ	Max	Unit
I_{BIT7}	Current sink if Bit7 = 1	For V(CURR3x) > 0.2V			19.2		mA
I_{BIT6}	Current sink if Bit6 = 1				9.6		
I_{BIT5}	Current sink if Bit5 = 1				4.8		
I_{BIT4}	Current sink if Bit4 = 1				2.4		
I_{BIT3}	Current sink if Bit3 = 1				1.2		
I_{BIT2}	Current sink if Bit2 = 1				0.6		
I_{BIT1}	Current sink if Bit1 = 1				0.3		
I_{BIT0}	Current sink if Bit0 = 1				0.15		
Δm^1	matching Accuracy	CURR30-33	I_{BIT7} and I_{BIT6}	-5		+5	%
			all other bits	-10		+10	%
Δ^2	absolute Accuracy			-15		+15	%
V_{CURR3X}	Voltage compliance			0.2		CPOUT	V
		curr3x_strobe_high=1 and strobe function		0.4			

1. Variation between currents within this group
2. Variation between the programmed current and the actual current

Current Sinks CURR3x Registers

Table 29. Curr3 control2 Register

Addr: 12h		Curr3 control2			
		This register selects the modes of the current sinks30..33 current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	preview_off_after strobe	0b	R/W	Select the switch off mode after strobe pulse	
				0	normal preview/strobe mode
				1	switch off preview after strobe duration has expired. To reinitiate the torch mode the preview_ctrl has to be set off and on again
2:1	preview_ctrl	00b	R/W	Preview is triggered by	
				00b	off
				01b	software trigger (setting this bit automatically triggers preview)
				10b	CURR2 active high; set gpi_curr2_en=1
				11b	CURR2 active low; set gpi_curr2_en=1
5	curr3x_strobe_high	0b	R/W	Double current on CURR30...CURR33 during strobe function	
				0	normal strobe current (0-37.8mA)
				1	double strobe current (0-75.6mA)

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Table 29. Curr3 control2 Register (Continued)

Addr: 12h		Curr3 control2			
		This register selects the modes of the current sinks30..33 current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7	strobe_pin	0	R/W	Select strobe input pin and current sink outputs (only if strobe_ctrl=10 or 11)	
				0	CURR1 is strobe input; CURR30...CURR33 flash output; set gpi_curr1_en=1
				1	CURR30 is strobe input; CURR1, CURR2, CURR6 flash output; set gpi_curr30_en=1

Table 30. Curr3 strobe control Register

Addr: 11h		Curr3 strobe control			
		This register selects the modes of the current sinks30..33 current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	strobe_ctrl	00b	R/W	Strobe is triggered by	
				00b	off
				01b	software trigger (setting this bit automatically triggers strobe)
				10b	CURR1 (or CURR30 see strobe_pin) active high
				11b	CURR1 (or CURR30 see strobe_pin) active low
3:2	strobe_mode	00b	R/W	Selects strobe mode	
				00b	Mode1 (Tstrobe=Ts; strobe trigger signal ≥ 10µs)
				01b	Mode 2 (Tstrobe=max Ts)
				10b	Mode 3 (Tstrobe = strobe signal)
				11b	not used

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Table 30. Curr3 strobe control Register (Continued)

Addr: 11h		Curr3 strobe control			
		This register selects the modes of the current sinks30..33 current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:4	strobe_timing	0000b	R/W	Selects strobe time (Ts)	
				0000b	100 msec
				0001b	200 msec
				0010b	300 msec
				0011b	400 msec
				0100b	500 msec
				0101b	600 msec
				0110b	700 msec
				0111b	800 msec
				1000b	900 msec
				1001b	1000 msec
				1010b	1100 msec
				1011b	1200 msec
				1100b	1300 msec
				1101b	1400 msec
				1110b	1500 msec
				1111b	1600 msec

Table 31. Curr3x strobe Register

Addr: 0Eh		Curr3x strobe			
		This register selects the strobe current of the current sinks30..33			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5:0	curr3x_strobe	00	R/W	Defines Strobe current of Current sinks curr30-33	
				00h	0 mA
				01h	0.6 mA (1.2mA if curr3x_strobe_high=1)
				....	....
				3Fh	37.8 mA (75.6mA if curr3x_strobe_high=1)

Table 32. Curr3x preview Register

Addr: 0Fh		Curr3x preview			
		This register selects the preview current of the current sinks30..33			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5:0	curr3x_preview	00	R/W	Defines Preview current of Current sinks curr30-33	
				00h	0 mA
				01h	0.6 mA
				....	....
				3Fh	37.8 mA

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Table 33. Curr3x other Register

Addr: 10h		Curr3x other			
		This register selects the current of the current sinks30..33			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5:0	curr3x_other	00	R/W	Selects CURR30...33 current, if CURR30...33 is not programmed for strobe/preview (curr30_mode...curr33_mode=11b)	
				00h	0 mA
				01h	0.6 mA
				....	....
				3Fh	37.8 mA

Table 34. Curr30 current Register

Addr: 40h		Curr30 current			
		This register selects the current of the current sink30			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	curr30_current	00	R/W	Selects curr30 current, if curr30 is not used for strobe/ preview (curr30_mode=11b)	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

Table 35. Curr31 current Register

Addr: 41h		Curr31 current			
		This register selects the current of the current sink31			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	curr31_current	00	R/W	Selects curr31 current, if curr31 is not used for strobe/ preview (curr31_mode=11b)	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

Table 36. Curr32 current Register

Addr: 42h		Curr32 current			
		This register selects the current of the current sink32			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	curr32_current	00	R/W	Selects CURR32 current, if CURR32 is not used for strobe/ preview (curr32_mode=11b)	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

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Table 37. Curr33 current Register

Addr: 43h		Curr33 current			
		This register selects the current of the current sink33			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	curr33_current	00	R/W	Selects curr33 current, if curr33 is not used for strobe/ preview (curr33_mode=11b)	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

Table 38. curr3 control1 Register

Addr: 03h		curr3 control1			
		This register select the mode of the current sinks30 - 33			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	curr30_mode	0	R/W	Select the mode of the current sink curr30	
				00b	off
				01b	strobe/preview
				10b	curr30_current or curr3x_other PWM controlled
				11b	curr30_current or curr3x_other - don't use curr3x_other if softdim_pattern=1, use curr30_current instead
3:2	curr31_mode	0	R/W	Select the mode of the current sink curr31	
				00b	off
				01b	strobe/preview
				10b	curr31_current or curr3x_other PWM controlled
				11b	curr31_current - don't use curr3x_other if softdim_pattern=1, use curr31_current instead
5:4	curr32_mode	0	R/W	Select the mode of the current sink CURR32	
				00b	off
				01b	strobe/preview
				10b	curr32_current or curr3x_other PWM controlled
				11b	curr32_current or curr3x_other - don't use curr3x_other if softdim_pattern=1, use curr32_current instead
7:6	curr33_mode	0	R/W	Select the mode of the current sink curr33	
				00b	off
				01b	strobe/preview
				10b	curr33_current or curr3x_other PWM controlled
				11b	curr33_current or curr3x_other- don't use curr3x_other if softdim_pattern=1, use curr33_current instead

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Table 39. Pattern control Register

Addr: 18h		Pattern control			
		This register controls the LED pattern			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	curr30_pattern	0b	R/W	Additional CURR33 LED pattern control bit	
				0b	CURR30 controlled according curr30_mode register
				1b	CURR30 controlled by LED pattern generator
5	curr31_pattern	0b	R/W	Additional CURR33 LED pattern control bit	
				0b	CURR31 controlled according curr31_mode register
				1b	CURR31 controlled by LED pattern generator
6	curr32_pattern	0b	R/W	Additional CURR33 LED pattern control bit	
				0b	CURR32 controlled according curr33_mode register
				1b	CURR32 controlled by LED pattern generator
7	curr33_pattern	0b	R/W	Additional CURR33 LED pattern control bit	
				0b	CURR33 controlled according curr33_pattern register
				1b	CURR33 controlled by LED pattern generator

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8.4.4 Current Sinks RGB1, RGB2, RGB3

These current sinks have a resolution of 8 bits and can sink up to 38.25mA.

Table 40. Current Sinks RGB1, RGB2, RGB3 Parameters

Symbol	Parameter	Condition		Min	Typ	Max	Unit
I_{BIT7}	Current sink if Bit7 = 1	For V(RGBx) > 0.2V			19.2		mA
I_{BIT6}	Current sink if Bit6 = 1				9.6		
I_{BIT5}	Current sink if Bit5 = 1				4.8		
I_{BIT4}	Current sink if Bit4 = 1				2.4		
I_{BIT3}	Current sink if Bit3 = 1				1.2		
I_{BIT2}	Current sink if Bit2 = 1				0.6		
I_{BIT1}	Current sink if Bit1 = 1				0.3		
I_{BIT0}	Current sink if Bit0 = 1				0.15		
Δm^1	matching Accuracy	RGB1, RGB2, RGB3	I_{BIT7} and I_{BIT6}	-5		+5	%
			all other bits	-10		+10	%
Δ^2	absolute Accuracy			-15		+15	%
V_{RGBX}	Voltage compliance			0.2		CPOUT	V

1. Variation between currents within this group
2. Variation between the programmed current and the actual current

RGB Current Sinks Registers

Table 41. curr rgb control Register

Addr: 02h		curr rgb control			
		This register select the mode of the current sinks RGB1, RGB2, RGB3			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	rgb1_mode	0	R/W	Select the mode of the current sink RGB1	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled
3:2	rgb2_mode	0	R/W	Select the mode of the current sink RGB2	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled
5:4	rgb3_mode	0	R/W	Select the mode of the current sink RGB3	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled

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Table 42. Rgb1 current Register

Addr: 0Bh		Rgb1 current			
		This register controls the RGB current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	rgb1_current	0	R/W	Defines current into Current sink RGB1	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

Table 43. Rgb2 current Register

Addr: 0Ch		Rgb2 current			
		This register controls the RGB current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	rgb2_current	0	R/W	Defines current into Current sink RGB2	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

Table 44. Rgb3 current Register

Addr: 0Dh		Rgb3 current			
		This register controls the RGB current sink current.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	rgb3_current	0	R/W	Defines current into Current sink RGB3	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

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8.4.5 General Purpose Current Sinks CURR4x

These low voltage current sinks have a resolution of 8 bits and can sink up to 38.25mA.

Table 45. CURR4x Sinks Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
I_{BIT7}	Current sink if Bit7 = 1	For V(CURRx) > 0.2V			19.2		mA
I_{BIT6}	Current sink if Bit6 = 1				9.6		
I_{BIT5}	Current sink if Bit5 = 1				4.8		
I_{BIT4}	Current sink if Bit4 = 1				2.4		
I_{BIT3}	Current sink if Bit3 = 1				1.2		
I_{BIT2}	Current sink if Bit2 = 1				0.6		
I_{BIT1}	Current sink if Bit1 = 1				0.3		
I_{BIT0}	Current sink if Bit0 = 1				0.15		
Δm^1	matching Accuracy	CURR4x	I_{BIT7} and I_{BIT6}	-5		+5	%
			all other bits	-10		+10	%
Δ^2	absolute Accuracy			-15		+15	%
$V_{CURR41,42,43x}$	Voltage compliance			0.2		CPOUT	V

1. Variation between currents within this group
2. Variation between the programmed current and the actual current

General Purpose Current Sinks CURR4x Registers

Table 46. curr4 control Register

Addr: 04h		curr4 control			
		This register selects the mode of the current sinks CURR41, CURR42, CURR43			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	curr41_mode	0	R/W	Select the mode of the current sink CURR41	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled
3:2	curr42_mode	0	R/W	Select the mode of the current sink CURR42	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled
5:4	curr43_mode	0	R/W	Select the mode of the current sink CURR43	
				00b	off
				01b	on
				10b	PWM controlled
				11b	LED pattern controlled

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Table 47. Curr41 current Register

Addr: 13h		Curr41 current			
		This register controls the curr41 current sink current.			
Bit	Bit Name	Default	Access	Description	
7:0	curr41_current	0	R/W	Defines current into Current sink CURR41	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

Table 48. Curr42 current Register

Addr: 14h		Curr42 current			
		This register controls the curr42 current sink current.			
Bit	Bit Name	Default	Access	Description	
7:0	curr42_current	0	R/W	Defines current into Current sink CURR42	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

Table 49. Curr43 current Register

Addr: 15h		Curr43 current			
		This register controls the curr43 current sink current.			
Bit	Bit Name	Default	Access	Description	
7:0	curr43_current	0	R/W	Defines current into Current sink CURR43	
				00h	0 mA
				01h	0.15 mA
				....	....
				FFh	38.25 mA

8.4.6 LED Pattern Generator

The LED pattern generator is capable of producing a pattern with 32 bits length and 1 second duration (31.25ms for each bit). The pattern itself can be started every second, every 2^{nd}, 3^{rd} up to 7^{th} second[4].

With this pattern all current sinks can be controlled. The pattern itself switches the configured current sources between 0 and their programmed current.

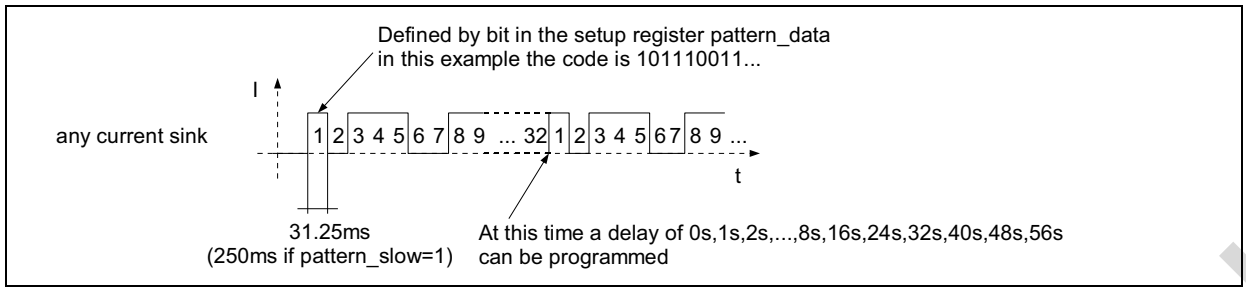
If everything else is switched off, the current consumption in this mode is I_{ACTIVE}. (excluding current through switched on current source) and the charge pump, if required. The charge pump can be automatically switched on/off depending on the pattern (set register cp_auto_on on page 20=1) to reduce the overall current consumption.

LED pattern start/stop depends on writing the pattern registers in correct order - it is recommended to use austriamicrosystems Android driver to ensure this.

4. All times can be extended by a factor of 8 by setting pattern_slow=1 (this result in a delay of up to 56s)

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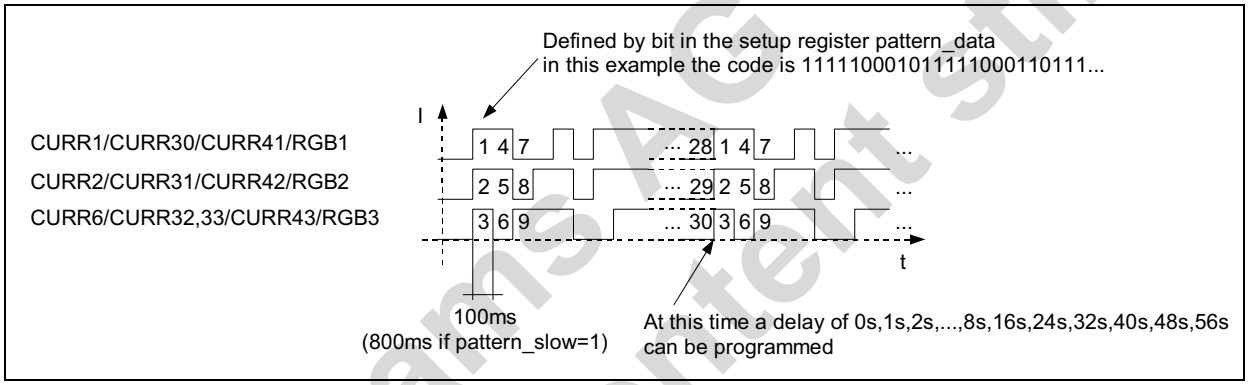
Figure 15. LED Pattern Generator AS3676 *for pattern_color = 0*



To select the different current sinks to be controlled by the LED pattern generator, see the 'xxxx'_mode registers (where 'xxxx' stands for the to be controlled current sink, e.g. curr1_mode for CURR1 current sink). See also the description of the different current sinks.

To allow the generator of a color patterns set the bit pattern_color to '1'. Then the pattern can be connected to CURRx as follows:

Figure 16. LED Pattern Generator AS3676 *for pattern_color = 1*



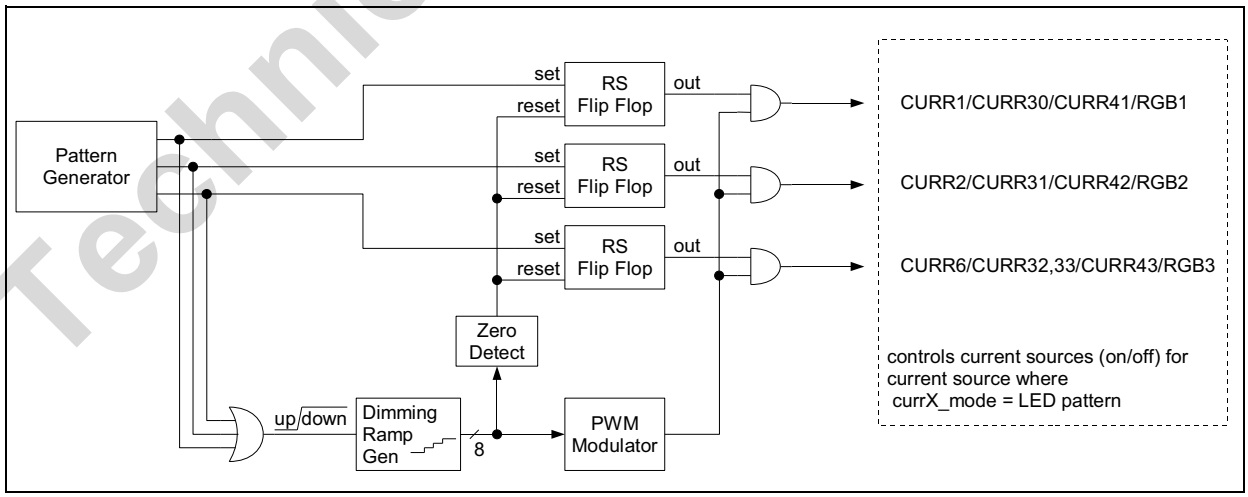
Only those current sinks will be controlled, where the 'xxxx'_mode register is configured for LED pattern.

If the register bit pattern_slow is set, all pattern times are increased by a factor of eight. (bit duration: 250ms if pattern_color=0 / 800ms if pattern_color=1, delays between pattern up to 56s).

Soft Dimming for Pattern

The internal pattern generator can be combined with the internal pwm dimming modulator to obtain as shown in the following figure:

Figure 17. Soft dimming Architecture for the AS3676 *(softdim_pattern=1 and pattern_color = 1)*

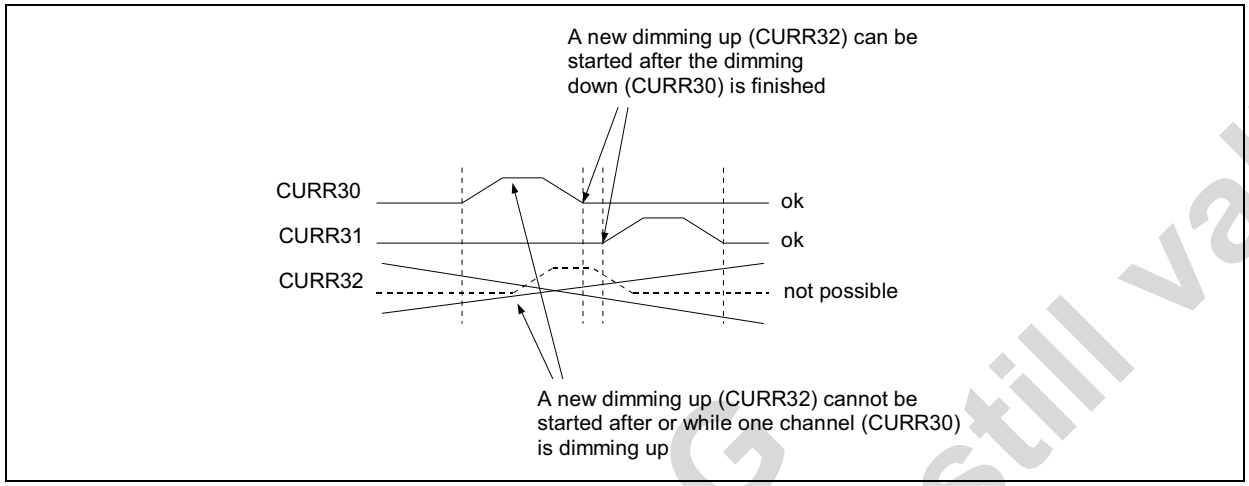


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With the AS3676 smooth fade-in and fade-out effects can be automatically generated.

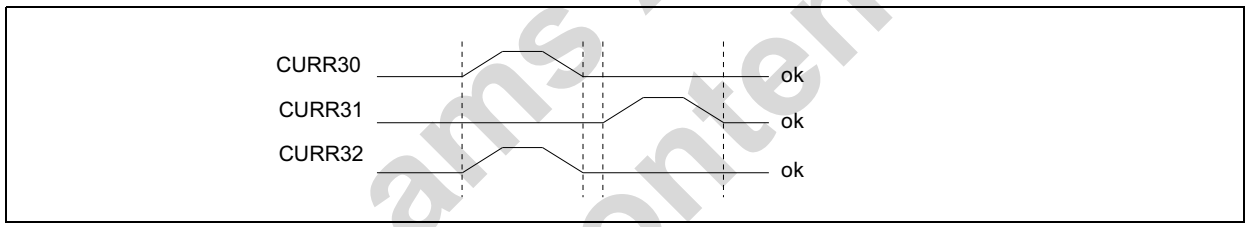
As there is only one dimming ramp generator and one pwm modulator following constraints have to be considered when setting up the pattern (applies only if pattern_color=1):

Figure 18. Soft dimming example Waveform for CURR30-32



However using the identical dimming waveform for two channels is possible as shown in the following figure:

Figure 19. Soft dimming example Waveform for CURR30-32



LED Pattern Registers

Table 50. Pattern data0...Pattern data3 Registers

Addr: 19h,1Ah,1Bh,1Ch		Pattern data0, Pattern data1, Pattern data2, Pattern data3		
		This registers contains the pattern data for the current sinks.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	pattern_data[7:0][1]	0	R/W	Pattern data0
7:0	pattern_data[15:8]	0	R/W	Pattern data1
7:0	pattern_data[23:16]	0	R/W	Pattern data2
7:0	pattern_data[31:24]	0	R/W	Pattern data3

1. Update any of the pattern register only if none of the current sources is connected to the pattern generator ('xxxx'_mode must not be 11b). The pattern generator is automatically started at the same time when any of the current sources is connected to the pattern generator

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Table 51. Pattern control Register

Addr: 18h		Pattern control			
		This register controls the LED pattern			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	pattern_color	0	R/W	Defines the pattern type for the current sinks	
				0b	single 32 bit pattern (also set currX_mode = 11)
				1b	RGB pattern with each 10 bits (set all currX_mode = 11)
2:1	pattern_delay	00b	R/W	Delay between pattern, details (see Table 54); together with pattern_delay2 sets the delay time between patterns	
3	softdim_pattern[1]	0b	R/W	Enable the 'soft' dimming feature for the pattern generator	
				0	Pattern generator directly control current sources
				1	'Soft Dimming' is performed (see page 37)

1. If softdim_pattern=1, don't set curr30_mode, curr31_mode, curr32_mode or curr33_mode to 11b.

Table 52. gpio current Register

Addr: 2Ch		gpio current			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
4	pattern_delay2	0	R/W	Delay between pattern (see Table 54 on page 39); together with pattern_delay sets the delay time between patterns	
6	pattern_slow	0	R/W	Pattern timing control	
				0b	normal mode
				1b	slow mode (all pattern times are increased by a factor of eight)

Table 53. Pattern End Register

Addr: 54h		Pattern End		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	pattern_end	0	R	pattern_end is toggled from 0 to 1 (or from 1 to 0) at each end of the pattern just before restarting of the internal pattern generator at the first bit of the pattern data (can be used to synchronize the baseband software to the pattern generator)[1]

1. pattern_end toggles whenever the AS3676 is in active mode (see Section 8.12 Operating Modes on page 80) even if no pattern data has been setup.

Table 54. LED Pattern timing

pattern_slow	pattern_delay2	pattern_delay[1..0]	bit duration [ms]		delay [s] between patterns	pattern duration [s] (total cycle time: pattern + delay)
	delay between patterns		pattern_color=0	pattern_color=1		
0	0	00	31	100	0[1]	1
0	0	01	31	100	1	2

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Table 54. LED Pattern timing

pattern_slow	pattern_delay2	pattern_delay[1..0]	bit duration [ms]		delay [s] between patterns	pattern duration [s] (total cycle time: pattern + delay)
	delay between patterns		pattern_color=0	pattern_color=1		
0	0	10	31	100	2	3
0	0	11	31	100	3	4
0	1	00	31	100	4	5
0	1	01	31	100	5	6
0	1	10	31	100	6	7
0	1	11	31	100	7	8
1	0	00	250	800	0	8
1	0	01	250	800	8	16
1	0	10	250	800	16	24
1	0	11	250	800	24	32
1	1	00	250	800	32	40
1	1	01	250	800	40	48
1	1	10	250	800	48	56
1	1	11	250	800	56	64

1. Even by setting 000 for pattern delay, there is a small delay before the new patterns starts.

8.4.7 PWM Generator

The PWM generator can be used for any current sink. The setting applies for all current sinks, which are controlled by the pwm generator (e.g. CURR1 is pwm controlled if curr1_mode = 10). The pwm modulated signal can switch on/off the current sinks and therefore depending on its duty cycle change the brightness of an attached LED.

Internal PWM Generator

The internal PWM generator uses the 2MHz internal clock as input frequency and its dimming range is 6 bits digital (2MHz / 2^6 = 31.3kHz pwm frequency) and 2 bits analog. Depending on the actual code in the register pwm_code the following algorithm is used:

If pwm_code bit 7 = 1

Then the upper 6 bits (Bits 7:2) of pwm_code are used for the 6 bits PWM generation, which controls the selected currents sinks directly

If pwm_code bit 7 =0 and bit 6 = 1

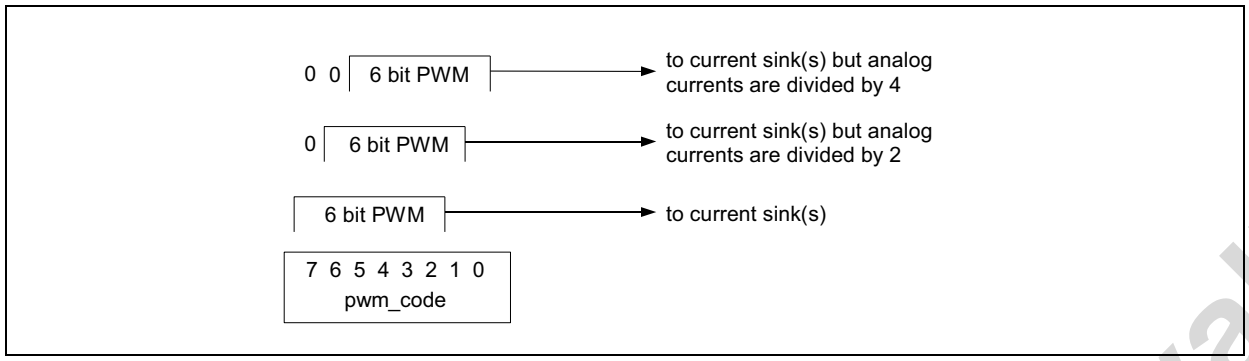
Then bits 6:1 of pwm_code are used for the 6 bits PWM generation. This signal controls the selected current sinks, but the analog current of these sinks is divided by 2

If pwm_code bit 7 and bit 6 = 0

Then bits 5:0 of pwm_code are used for the 6 bits PWM generation. This signal controls the selected current sinks, but the analog current of these sinks is divided by 4

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Figure 20. PWM Control

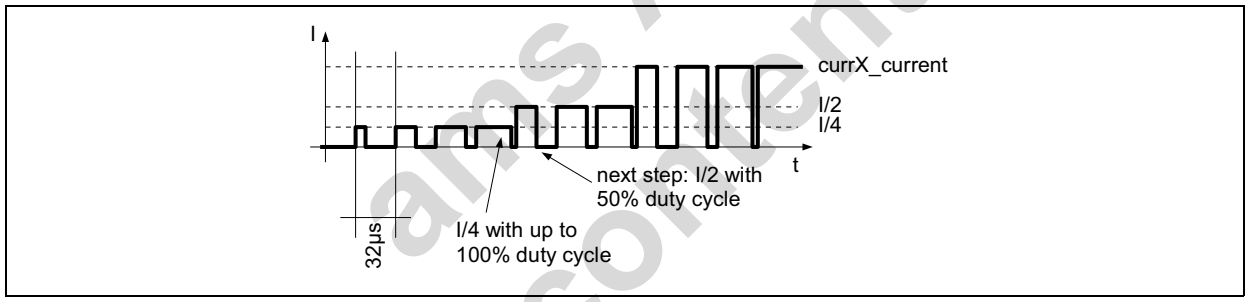


Automatic Up/Down Dimming

If the register pwm_dim_mode is set to 01 (up dimming) or 10 (down dimming) the value within the register pwm_code is increased (up dimming) or decreased (down dimming) every time and amount (either 1/4th or 1/8th) defined by the register pwm_dim_speed. The maximum value of 255 (completely on) and the minimum value of 0 (off) is never exceeded. It is used to smoothly and automatically dim the brightness of the LEDs connected to any of the current sinks. The PWM code is readable all the time (also during up and down dimming).

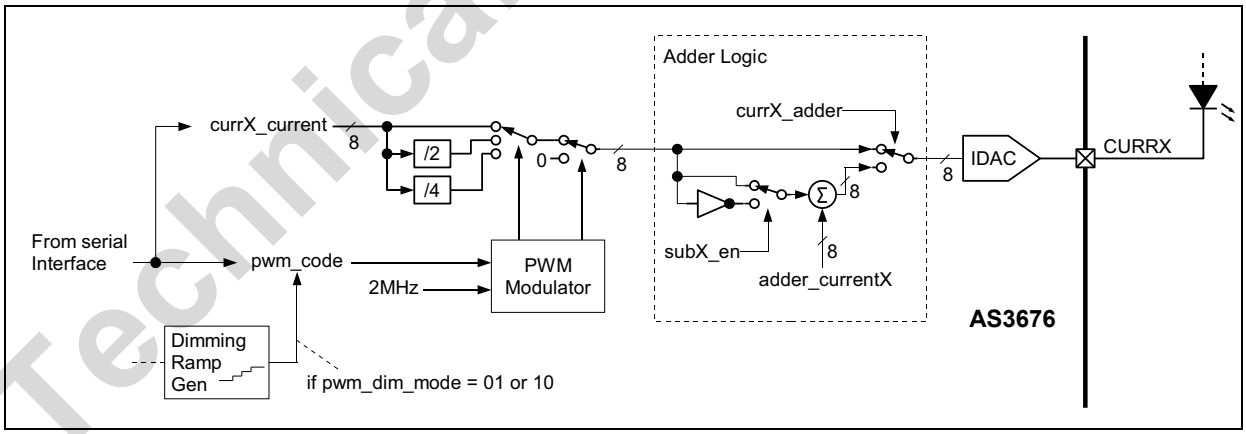
The waveform for up dimming looks as follows (cycles omitted for simplicity):

Figure 21. PWM Dimming Waveform for up dimming (pwm_dim_mode = 01); currX_mode = PWM controlled (not all steps shown)



The internal pwm modulator circuit controls the current sinks as shown in the following figure:

Figure 22. PWM Control Circuit (currX_mode = 10b (PWM controlled)); X = any current sink



The adder logic (available for all current sinks) is intended to allow dimming not only from 0% to 100% (or 100% to 0%) of currX_current, but also e.g. from 10% to 110% (or 110% to 10%) of currX_current. The starting current for up dimming is defined by 0 + currX_adder and the end current is defined by currX_current + currX_adder.

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An overflow of the internal bus (8 Bits wide to the IDAC) has to be avoided by the register settings (currX_current + currX_adder must not exceed 255).

If the register subX_en is set, the result from the pwm modulator is inverted logically. That means for up dimming the starting current is defined by currX_adder - 1 and the end current is defined by currX_adder - currX_current - 1. An overflow of the internal bus (8 Bits wide to the IDAC) has to be avoided by the register settings (currX_adder - currX_current - 1 must not be below zero).

Its purpose is to dim one channel e.g. CURR30 from e.g. 110% to 10% of curr30_current and at the same time dim another channel e.g. CURR31 from 20% to 120% of curr31_current.

Note: The adder logic operates independent of the currX_mode setting, but its main purpose is to work together with the pwm modulator (improved up/down dimming)

If the adder logic is not used anymore, set the bit currX_adder to 0. (Setting adder_currentX to 0 is not sufficient)

At the end of up/down dimming, the pwm_code register keeps its final value (for up-dimming 255 and for down-dimming 0). This can be used to identify the exact time, when up/down dimming is finished.

Table 55. PWM Dimming Table

	Decrease by 1/4th every step		Decrease by 1/8th every step		Seconds	Seconds	Seconds	Seconds
Step	%Dimming	PWM	%Dimming	PWM	50msec/ Step	25msec/ Step	5msec/ Step	2.5msec/ Step
1	100,0	255	100,0	255	0,00s	0,00s	0,000s	0,000s
2	75,3	192	87,8	224	0,05s	0,03s	0,005s	0,003s
3	56,5	144	76,9	196	0,10s	0,05s	0,010s	0,005s
4	42,4	108	67,5	172	0,15s	0,08s	0,015s	0,008s
5	31,8	81	59,2	151	0,20s	0,10s	0,020s	0,010s
6	23,9	61	52,2	133	0,25s	0,13s	0,025s	0,013s
7	18,0	46	45,9	117	0,30s	0,15s	0,030s	0,015s
8	13,7	35	40,4	103	0,35s	0,18s	0,035s	0,018s
9	10,6	27	35,7	91	0,40s	0,20s	0,040s	0,020s
10	8,2	21	31,4	80	0,45s	0,23s	0,045s	0,023s
11	6,3	16	27,5	70	0,50s	0,25s	0,050s	0,025s
12	4,7	12	24,3	62	0,55s	0,28s	0,055s	0,028s
13	3,5	9	21,6	55	0,60s	0,30s	0,060s	0,030s
14	2,7	7	19,2	49	0,65s	0,33s	0,065s	0,033s
15	2,4	6	16,9	43	0,70s	0,35s	0,070s	0,035s
16	2,0	5	14,9	38	0,75s	0,38s	0,075s	0,038s
17	1,6	4	13,3	34	0,80s	0,40s	0,080s	0,040s
18	1,2	3	11,8	30	0,85s	0,43s	0,085s	0,043s
19	0,8	2	10,6	27	0,90s	0,45s	0,090s	0,045s
20	0,4	1	9,4	24	0,95s	0,48s	0,095s	0,048s
21	0,0	0	8,2	21	1,00s	0,50s	0,100s	0,050s
22			7,5	19	1,05s	0,53s	0,105s	0,053s
23			6,7	17	1,10s	0,55s	0,110s	0,055s
24			5,9	15	1,15s	0,58s	0,115s	0,058s

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Table 55. PWM Dimming Table

	Decrease by 1/4th every step		Decrease by 1/8th every step		Seconds	Seconds	Seconds	Seconds
Step	%Dimming	PWM	%Dimming	PWM	50msec/ Step	25msec/ Step	5msec/ Step	2.5msec/ Step
25			5,5	14	1,20s	0,60s	0,120s	0,060s
26			5,1	13	1,25s	0,63s	0,125s	0,063s
27			4,7	12	1,30s	0,65s	0,130s	0,065s
28			4,3	11	1,35s	0,68s	0,135s	0,068s
29			3,9	10	1,40s	0,70s	0,140s	0,070s
30			3,5	9	1,45s	0,73s	0,145s	0,073s
31			3,1	8	1,50s	0,75s	0,150s	0,075s
32			2,7	7	1,55s	0,78s	0,155s	0,078s
33			2,4	6	1,60s	0,80s	0,160s	0,080s
34			2,0	5	1,65s	0,83s	0,165s	0,083s
35			1,6	4	1,70s	0,85s	0,170s	0,085s
36			1,2	3	1,75s	0,88s	0,175s	0,088s
37			0,8	2	1,80s	0,90s	0,180s	0,090s
38			0,4	1	1,85s	0,93s	0,185s	0,093s
39			0,0	0	1,90s	0,95s	0,190s	0,095s

PWM Generator Registers

Table 56. Pwm control Register

Addr: 16h		Pwm control			
		This register controls PWM generator			
Bit	Bit Name	Default	Access	Description	
2:1	pwm_dim_mode	00b	R/W	Selects the dimming mode	
				00b	no dimming; actual content of register pwm_code is used for pwm generator
				01b	logarithmic up dimming (codes are increased). Start value is actual pwm_code
				10b	logarithmic down dimming (codes are decreased). Start value is actual pwm_code; switch off the dimmed current source after dimming is finished to avoid unnecessary quiescent current
				11b	NA

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Table 56. Pwm control Register (Continued)

Addr: 16h		Pwm control			
		This register controls PWM generator			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5:3	pwm_dim_speed	000b	R/W	Defines dimming speed by increase/decrease pwm_code	
				000b	by 1/4th every 50 msec (total dim time 1.0s)
				001b	by 1/8th every 50 msec (total dim time 1.9s)
				010b	by 1/4th every 25 msec (total dim time 0.5s)
				011b	by 1/8th every 25 msec (total dim time 0.95s)
				100b	by 1/4th every 5 msec (total dim time 100ms)
				101b	by 1/8th every 5 msec (total dim time 190ms)
				110b	by 1/4th every 2.5 msec (total dim time 50ms)
				111b	by 1/8th every 2.5 msec (total dim time 95ms)

Table 57. pwm code Register

Addr: 17h		pwm code			
		This register controls the Pwm code.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	pwm_code	00b	R/W	Selects the PWM code	
				00h	0% duty cycle
				....	....
				FFh	100% duty cycle

Table 58. Adder Current 1 Register

Addr: 30h		Adder Current 1			
		This register defines the current which can be added to CURR1, CURR30, CURR41, RGB1			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	adder_current1	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text)	
				00h	0 (represents 0mA)
				....	....
				FFh	255 (represents 38.25mA)

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Table 59. Adder Current 2 Register

Addr: 31h		Adder Current 2			
		This register defines the current which can be added to CURR2, CURR31, CURR42, RGB2			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	adder_current2	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text)	
				00h	0 (represents 0mA)
				....	....
				FFh	255 (represents 38.25mA)

Table 60. Adder Current 3 Register

Addr: 32h		Adder Current 3			
		This register defines the current which can be added to CURR6, CURR32, CURR43, RGB3			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	adder_current3	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text)	
				00h	0 (represents 0mA)
				....	....
				FFh	255 (represents 38.25mA)

Table 61. Adder Current 4 Register

Addr: 52h		Adder Current 4			
		This register defines the current which can be added to CURR33			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:0	adder_current4	00b	R/W	Selects the added current value – do not exceed together with currX_current the internal 8 Bit range (see text)	
				00h	0 (represents 0mA)
				....	....
				FFh	255 (represents 38.25mA)

Table 62. Adder Enable 1 Register

Addr: 33h		Adder Enable 1			
		Enables the adder circuit for the selected current sources			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	rgb1_adder	0	R/W	Enables adder circuit for current source RGB1	
				0	Normal Operation of the current source
				1	adder_current1 gets added to the current source current
1	rgb2_adder	0	R/W	Enables adder circuit for current source RGB2	
				0	Normal Operation of the current source
				1	adder_current2 gets added to the current source current

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Table 62. Adder Enable 1 Register (Continued)

Addr: 33h		Adder Enable 1			
		Enables the adder circuit for the selected current sources			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2	rgb3_adder	0	R/W	Enables adder circuit for current source RGB3	
				0	Normal Operation of the current source
				1	adder_current3 gets added to the current source current
3	curr41_adder	0	R/W	Enables adder circuit for current source CURR41	
				0	Normal Operation of the current source
				1	adder_current1 gets added to the current source current
4	curr42_adder	0	R/W	Enables adder circuit for current source CURR42	
				0	Normal Operation of the current source
				1	adder_current2 gets added to the current source current
5	curr43_adder	0	R/W	Enables adder circuit for current source CURR43	
					Normal Operation of the current source
					adder_current3 gets added to the current source current

Table 63. Adder Enable 2 Register

Addr: 34h		Adder Enable 2			
		Enables the adder circuit for the selected current sources			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	curr1_adder	0	R/W	Enables adder circuit for current source CURR1	
				0	Normal Operation of the current source
				1	adder_current1 gets added to the current source current
1	curr2_adder	0	R/W	Enables adder circuit for current source CURR2	
				0	Normal Operation of the current source
				1	adder_current2 gets added to the current source current
2	curr6_adder	0	R/W	Enables adder circuit for current source CURR6	
				0	Normal Operation of the current source
				1	adder_current3 gets added to the current source current
3	curr30_adder	0	R/W	Enables adder circuit for current source CURR30	
				0	Normal Operation of the current source
				1	adder_current1 gets added to the current source current
4	curr31_adder	0	R/W	Enables adder circuit for current source CURR31	
				0	Normal Operation of the current source
				1	adder_current2 gets added to the current source current

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Table 63. Adder Enable 2 Register (Continued)

Addr: 34h		Adder Enable 2			
		Enables the adder circuit for the selected current sources			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5	curr32_adder	0	R/W	Enables adder circuit for current source CURR32	
				0	Normal Operation of the current source
				1	adder_current3 gets added to the current source current
6	curr33_adder	0	R/W	Enables adder circuit for current source CURR33	
				0	Normal Operation of the current source
				1	adder_current4 gets added to the current source current

Table 64. Subtract Enable Register

Addr: 35h		Subtract Enable			
		Enable the inversion from the signal from the pwm generator			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	sub_en1	0	R/W	Inverts the signal from the pwm generator	
				0	Direct Operation (no inversion)
				1	The signal from the pwm generator for which the adder is enabled (curr1_adder = 1, curr30_adder = 1, rgb1_adder = 1, curr41_adder = 1) is inverted
1	sub_en2	0	R/W	Inverts the signal from the pwm generator	
				0	Direct Operation (no inversion)
				1	The signal from the pwm generator for which the adder is enabled (curr2_adder = 1, curr31_adder = 1, rgb2_adder = 1, curr42_adder = 1) is inverted
2	sub_en3	0	R/W	Inverts the signal from the pwm generator	
				0	Direct Operation (no inversion)
				1	The signal from the pwm generator for which the adder is enabled (curr6_adder = 1, curr32_adder = 1, rgb3_adder = 1, curr43_adder = 1) is inverted
3	sub_en4	0	R/W	Inverts the signal from the pwm generator	
				0	Direct Operation (no inversion)
				1	The signal from the pwm generator for which the adder is enabled (curr33_adder = 1) is inverted

8.4.8 ALS - Ambient Light Sensing

The ADC converts every 1ms the ambient light sensor signal from pin GPIO2/LIGHT[5]. This signal is pre-processed with a offset defined by amb_offset and a gain defined by amb_gain (1/4, 1/2, 1, 2). Then it is low-pass filtered with a programmable cut-off frequency going from 0.25Hz to 32Hz. Increasing signals and decreasing signal can have individual cut-off frequencies adjustable from 0.25Hz to 32Hz (amb_filter_up and amb_filter_down). When setting amb_on=1, this filter is pre-loaded with the initial value from the ADC to startup the filter at a defined condition.

5. adc_select=0 (select GPIO2/LIGHT input)

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This filtered signal can be readout from the register amb_result<7:0>.

Each of the available three channels (N=1, 2 or 3) has six 8-bit registers:

- groupN_y0: define current multiplier for values below groupN_X1
- groupN_y3: define current multiplier for high values (actual starting point defined by groupN_x1,groupN_k1 and groupN_x2,groupN_k2)
- groupN_x1, groupN_k1: If ADC reading is > groupN_x1 then groupN_k1 divided by 32 defines the slope of the first ramp
- groupN_x2, groupN_k2: If ADC reading is > groupN_x2 then groupN_k2 divided by 32 defines the slope of the second ramp

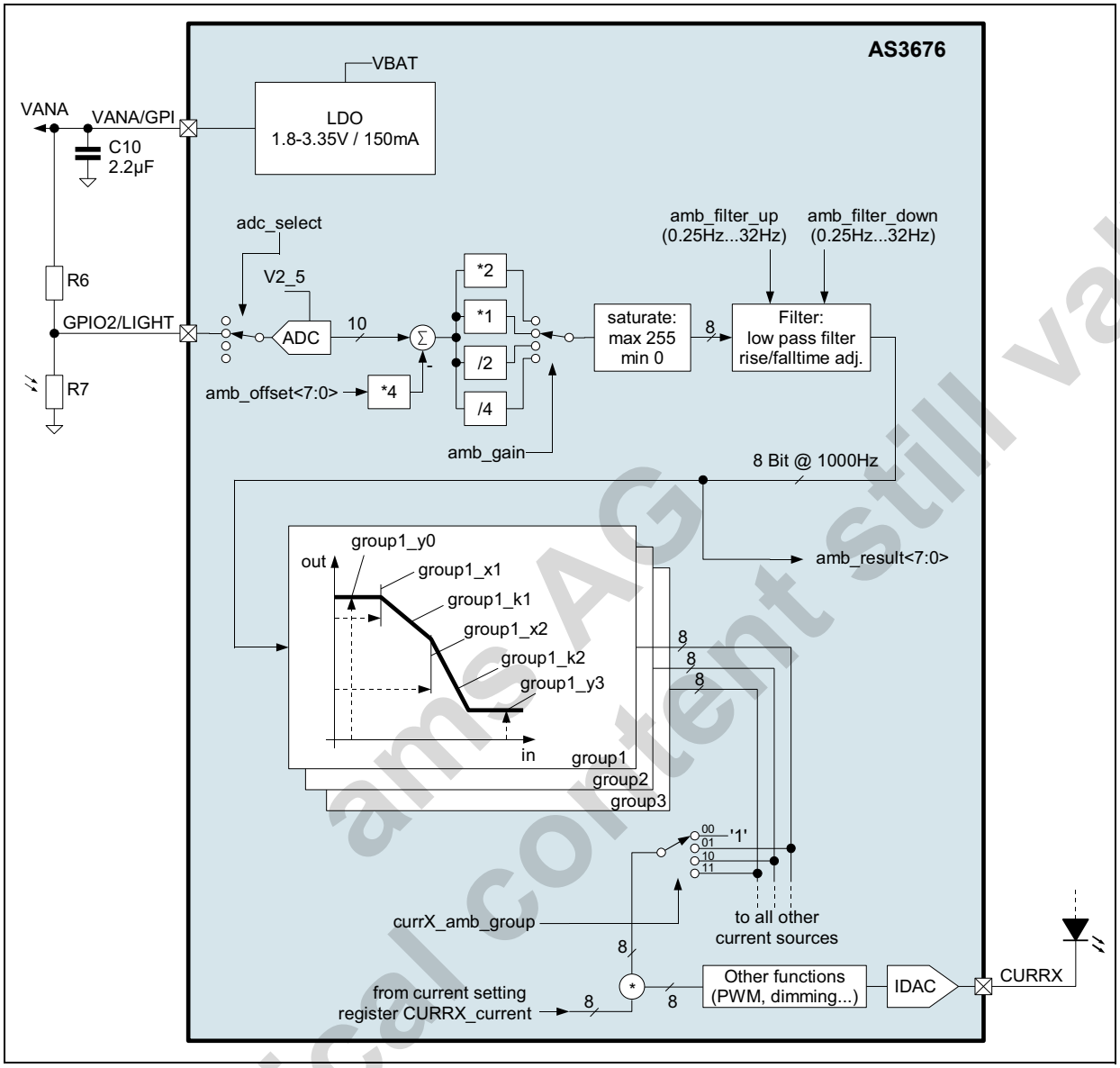
Each current sources has a 2 bit register (currX_amb_group) to select None, Group1, Group2 or Group3 of ambient light sensing.

The calculations are done every 1ms resulting in a flicker-free 1000Hz update rate of the current sources.

Note: A current source should not use adder or subtractor current at the same time together with ALS (e.g. curr1_adder=1 and curr1_amb_group=01, 10 or 11). For details see austriamicrosystems application note AN3676_ALS_with_adder_current.

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Figure 23. Ambient Light Sensor internal circuit



Ambient Light Sensor Registers

Table 65. ALS control Register

Addr: 90h		ALS control			
		control ambient light sensing			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	amb_on	0	R/W	Enables the ambient light sensing feature	
				0	ambient light sensor disabled
				1	ambient light sensor enabled

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Table 65. ALS control Register (Continued)

Addr: 90h		ALS control			
		control ambient light sensing			
Bit	Bit Name	Default	Access	Description	
2:1	amb_gain	0	R/W	Control Ambient Light Sensor preprocessing gain	
				00	gain = 1/4
				01	gain = 1/2
				10	gain = 1
				11	gain = 2

Table 66. ALS filter Register

Addr: 91h		ALS filter			
		control for ambient light sensor filtering			
Bit	Bit Name	Default	Access	Description	
2:0	amb_filter_up	000	R/W	Controls the filter cut off (-3dB) frequency (increasing)	
				000	0.25Hz
				001	0.5Hz
				010	1Hz
				011	2Hz
				100	4Hz
				101	8Hz
				110	16Hz
				111	32Hz
6:4	amb_filter_down	000	R/W	Controls the filter cut off (-3dB) frequency (decreasing)	
				000	0.25Hz
				001	0.5Hz
				010	1Hz
				011	2Hz
				100	4Hz
				101	8Hz
				110	16Hz
				111	32Hz

Table 67. ALS offset Register

Addr: 92h		ALS offset		
Bit	Bit Name	Default	Access	Description
7:0	amb_offset	00h	R/W	Controls the offset of the ambient light sensor

Table 68. ALS result Register

Addr: 93h		ALS result		
Bit	Bit Name	Default	Access	Description
7:0	amb_result	00h	R/W	Filtered result of the ambient light sensor value

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Table 69. ALS curr12 group Register

Addr: 94h		ALS curr12 group			
		controls the group mapping for CURR1 and CURR2			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	curr1_amb_group	00	R/W	CURR1 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
3:2	curr2_amb_group	00	R/W	CURR2 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3

Table 70. ALS rgb group Register

Addr: 95h		ALS rgb group			
		controls the group mapping for RGB1, RGB2, RGB3 and CURR6			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	rgb1_amb_group	00	R/W	RGB1 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
3:2	rgb2_amb_group	00	R/W	RGB2 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
5:4	rgb3_amb_group	00	R/W	RGB3 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
7:6	curr6_amb_group	00	R/W	CURR6 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3

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Table 71. ALS curr3x group Register

Addr: 96h		ALS curr3x group			
		controls the group mapping for CURR30, CURR31, CURR32 and CURR33			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	curr30_amb_group	00	R/W	CURR30 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
3:2	curr31_amb_group	00	R/W	CURR31 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
5:4	curr32_amb_group	00	R/W	CURR32 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
7:6	curr33_amb_group	00	R/W	CURR33 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3

Table 72. ALS curr4x group Register

Addr: 97h		ALS curr4x group			
		controls the group mapping for CURR41, CURR42 and CURR43			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	curr41_amb_group	00	R/W	CURR41 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3
3:2	curr42_amb_group	00	R/W	CURR42 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3

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Table 72. ALS curr4x group Register (Continued)

Addr: 97h		ALS curr4x group			
		controls the group mapping for CURR41, CURR42 and CURR43			
Bit	Bit Name	Default	Access	Description	
5:4	curr43_amb_group	00	R/W	CURR43 is mapped to ambient light sensor group	
				00	None - no ambient light sensor control
				01	Group 1
				10	Group 2
				11	Group 3

Group1

Table 73. ALS group 1 Y0 Register

Addr: 98h		ALS group 1 Y0		
Bit	Bit Name	Default	Access	Description
7:0	group1_y0	00h	R/W	Group 1 y0 value - divided by 256

Table 74. ALS group 1 Y3 Register

Addr: 99h		ALS group 1 Y3		
Bit	Bit Name	Default	Access	Description
7:0	group1_y3	00h	R/W	Group 1 y3 value - divided by 256

Table 75. ALS group 1 X1 Register

Addr: 9Ah		ALS group 1 X1		
Bit	Bit Name	Default	Access	Description
7:0	group1_x1	00h	R/W	Group 1 x1 value

Table 76. ALS group 1 K1 Register

Addr: 9Bh		ALS group 1 K1		
Bit	Bit Name	Default	Access	Description
7:0	group1_k1	00h	R/W	Group 1 k1 value - divided by 32 defines first slope

Table 77. ALS group 1 X2 Register

Addr: 9Ch		ALS group 1 X2		
Bit	Bit Name	Default	Access	Description
7:0	group1_x2	00h	R/W	Group 1 x2 value

Table 78. ALS group 1 K2 Register

Addr: 9Dh		ALS group 1 K2		
Bit	Bit Name	Default	Access	Description
7:0	group1_k2	00h	R/W	Group 1 k2 value- value divided by 32 defines second slope

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Group2

Table 79. ALS group 2 Y0 Register

Addr: 9Eh		ALS group 2 Y0		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_y0	00h	R/W	Group 2 y0 value - divided by 256

Table 80. ALS group 2 Y3 Register

Addr: 9Fh		ALS group 2 Y3		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_y3	00h	R/W	Group 2 y3 value - divided by 256

Table 81. ALS group 2 X1 Register

Addr: A0h		ALS group 2 X1		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_x1	00h	R/W	Group 2 x1 value

Table 82. ALS group 2 K1 Register

Addr: A1h		ALS group 2 K1		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_k1	00h	R/W	Group 2 k1 value - divided by 32 defines first slope

Table 83. ALS group 2 X2 Register

Addr: A2h		ALS group 2 X2		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_x2	00h	R/W	Group 2 x2 value

Table 84. ALS group 2 K2 Register

Addr: A3h		ALS group 2 K2		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group2_k2	00h	R/W	Group 2 k2 value- value divided by 32 defines second slope

Group3

Table 85. ALS group 3 Y0 Register

Addr: A4h		ALS group 3 Y0		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_y0	00h	R/W	Group 3 y0 value - divided by 256

Table 86. ALS group 3 Y3 Register

Addr: A5h		ALS group 3 Y3		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_y3	00h	R/W	Group 3 y3 value - divided by 256

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Table 87. ALS group 3 X1 Register

Addr: A6h		ALS group 3 X1		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_x1	00h	R/W	Group 3 x1 value

Table 88. ALS group 3 K1 Register

Addr: A7h		ALS group 3 K1		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_k1	00h	R/W	Group 3 k1 value - divided by 32 defines first slope

Table 89. ALS group 3 X2 Register

Addr: A8h		ALS group 3 X2		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_x2	00h	R/W	Group 3 x2 value

Table 90. ALS group 3 K2 Register

Addr: A9h		ALS group 3 K2		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	group3_k2	00h	R/W	Group 3 k2 value- value divided by 32 defines second slope

8.4.9 DLS - Dynamic Luminance Scaling Input

The pin GPIO1/DLS can be used for dynamic backlight scaling input. Dynamic backlight scaling is used to reduce the power of the backlight especially when showing dark picture contents on the display. The control unit to operate DLS is the display processor sending a PWM signal to the AS3676 and in parallel changing the display content to compensate for a reduced brightness backlight.

Table 91. DLS Input Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{DLS}	DLS input frequency range	pin GPIO1/DLS if used for DLS (any bit set in register DLS mode control1 or DLS mode control2)	25		1000	kHz

Note: If the input signal from the PWM (e.g. for DLS) is '0', the voltage on the current sink is captured with a S/H. Do not enable DLS operation using the DCDC step up converter if the input GPIO1/DLS is continuously at 0.

When this feature is enabled, the current sink current is disabled when the pin GPIO1/DLS is at 0. If GPIO1/DLS=1, the current sink operates at its programmed current as shown in Figure 24:

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Figure 24. DLS (Dynamic Luminance Scaling) internal circuit shown for a single current sink

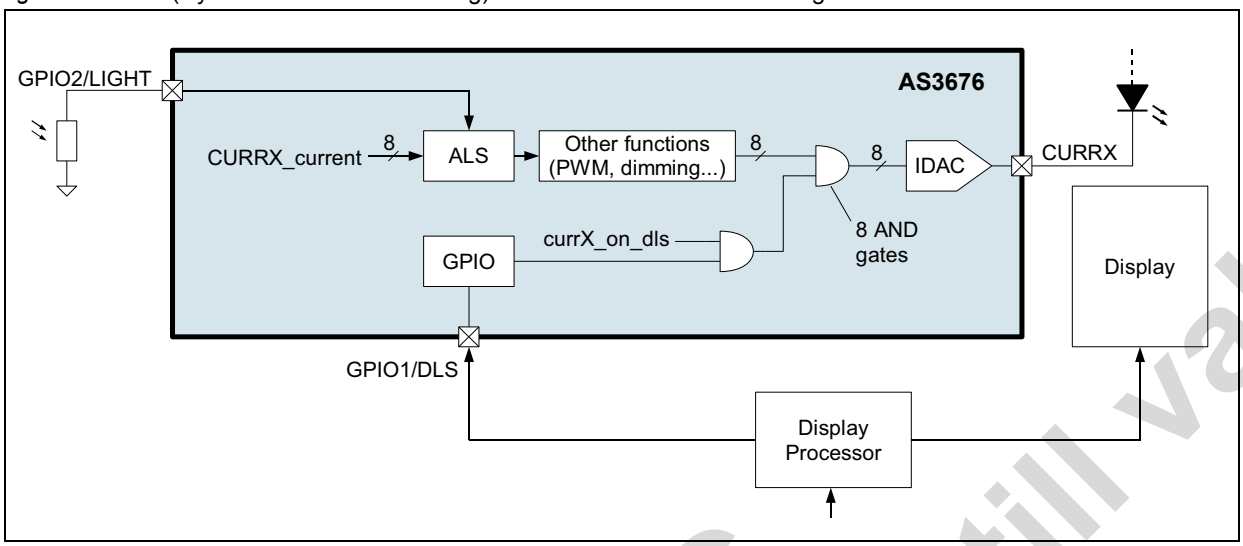


Table 92. DLS mode control1 Register

Addr: 56h		DLS mode control1			
		Setup which current sinks are connected to the DLS; if set to '1' the correspond current source (sink) is combined with the DLS input			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	curr30_on_dls	0	R/W	0	CURR30 current sink is not combined with DLS
				1	CURR30 current sink is combined with DLS
1	curr31_on_dls	0	R/W	0	CURR31 current sink is not combined with DLS
				1	CURR31 current sink is combined with DLS
2	curr32_on_dls	0	R/W	0	CURR32 current sink is not combined with DLS
				1	CURR32 current sink is combined with DLS
3	curr33_on_dls	0	R/W	0	CURR33 current sink is not combined with DLS
				1	CURR33 current sink is combined with DLS
4	rgb1_on_dls	0	R/W	0	RGB1 current sink is not combined with DLS
				1	RGB1 current sink is combined with DLS
5	rgb2_on_dls	0	R/W	0	RGB2 current sink is not combined with DLS
				1	RGB2 current sink is combined with DLS
6	rgb3_on_dls	0	R/W	0	RGB3 current sink is not combined with DLS
				1	RGB3 current sink is combined with DLS

Table 93. DLS mode control2 Register

Addr: 57h		DLS mode control2			
		Setup which current sinks are connected to the DLS; if set to '1' the correspond current source (sink) is combined with the DLS input			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	curr1_on_dls	0	R/W	0	CURR1 current sink is not combined with DLS
				1	CURR1 current sink is combined with DLS

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Table 93. DLS mode control2 Register (Continued)

Addr: 57h		DLS mode control2			
		Setup which current sinks are connected to the DLS; if set to '1' the correspond current source (sink) is combined with the DLS input			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1	curr2_on_dls	0	R/W	0	CURR2 current sink is not combined with DLS
				1	CURR2 current sink is combined with DLS
2	curr41_on_dls	0	R/W	0	CURR41 current sink is not combined with DLS
				1	CURR41 current sink is combined with DLS
3	curr42_on_dls	0	R/W	0	CURR42 current sink is not combined with DLS
				1	CURR42 current sink is combined with DLS
4	curr43_on_dls	0	R/W	0	CURR43 current sink is not combined with DLS
				1	CURR43 current sink is combined with DLS
7	curr6_on_dls	0	R/W	0	CURR6 current sink is not combined with DLS
				1	CURR6 current sink is combined with DLS

8.5 General Purpose Input / Output

The GPIOs are a highly-configurable general purpose input/output pins which can be used for the following functionality:

- Digital Schmitt Trigger Input
- Digital Output with 4mA Driving Capability at 2.8V Supply (VANA)
- Tristate Output
- Analog Input to the ADC
- Default Mode for GPIO1/DLS, GPIO2/LIGHT and VANA/GPI is Input (Pull-Down)

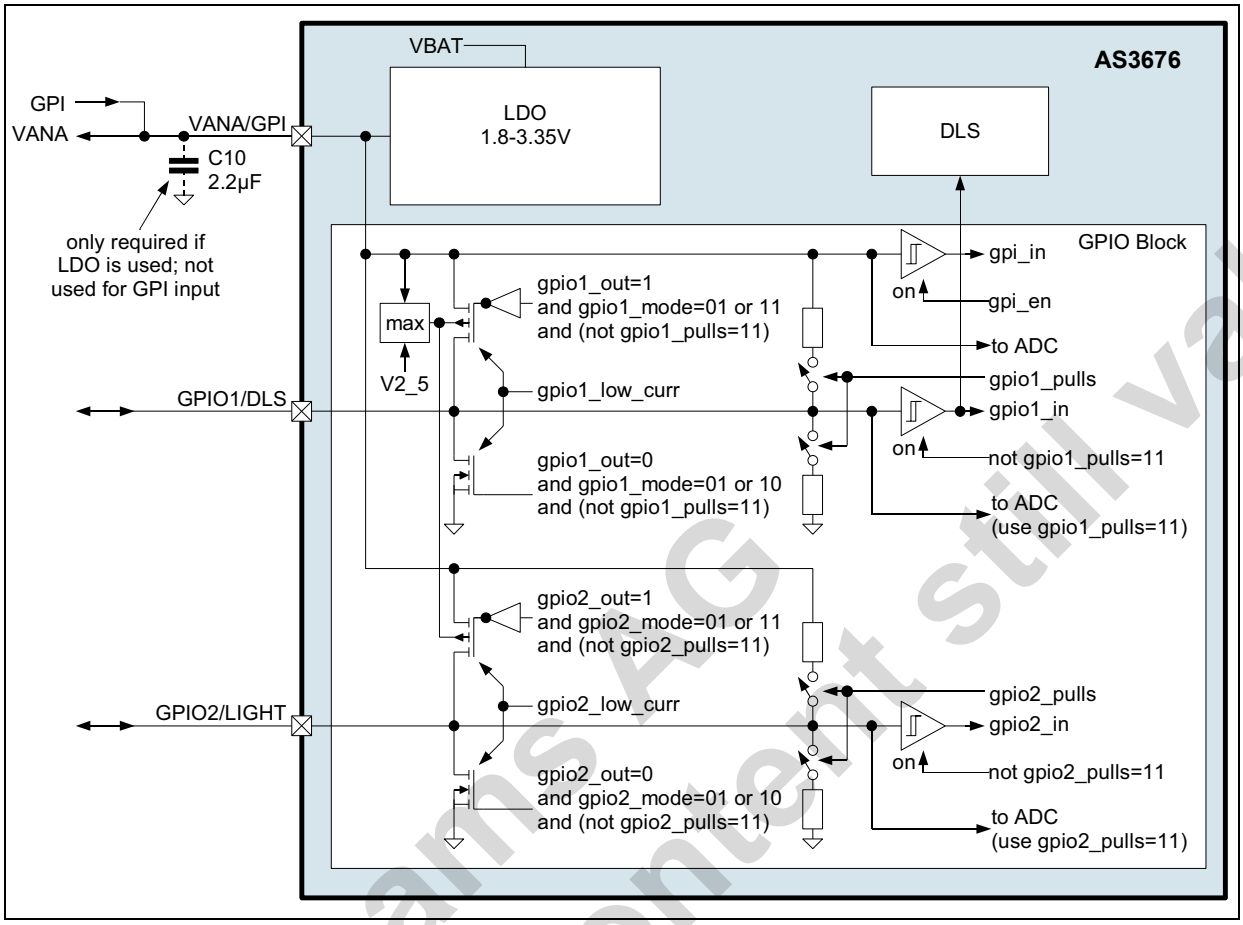
Table 94. GPIO Pin Function Summary

GPIO Pin	Configuration	Additional Function
GPIO1/DLS	Digital Input, Totem-Pole Output (Push/Pull), Open Drain (PMOS or NMOS), High-Z, Pull-Down or Pull-Up Resistor	ADC Input, PWM Input, DLS input (see page 55)
GPIO2/LIGHT	Digital Input, Totem-Pole Output (Push/Pull), Open Drain (PMOS or NMOS), High-Z, Pull-Down or Pull-Up Resistor	ADC Input, ALS - light sensor input (see page 47)
VANA/GPI	Digital Input[1]	ADC Input, LDO output

1. As VANA/GPI is used as a power supply for GPIO1/DLS, GPIO2/LIGHT, it is not recommended to use it as a digital input.

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Figure 25. GPIOs and VANA/GPI Blockdiagram



8.5.1 Unused GPIO Pins

If the pins GPIO1/DLS or GPIO2/LIGHT are not used, they can be left open (an internal pulldown, which is enabled by default, will pull them to GND).

8.5.2 GPIO Characteristics

Table 95. GPIO DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Rpull	Pull up/Pull down Resistance	enabled by gpio1_pulls and gpio2_pulls	30		75	kΩ
VGPIO	Supply Voltage	=VANA/GPI	1.8		3.35	V
V_{IH}	High Level Input Voltage	pins GPIO1/DLS and GPIO2/ LIGHT	55% of VANA/ GPI			V
V_{IL}	Low Level Input Voltage				28% of VANA/ GPI	V
V_{HYS}	Hysteresis			5% of VANA/ GPI		V
I_{LEAK}	Input Leakage Current	To V2_5 or VANA/GPI and VSS	-5		5	µA
V_{OH}	High Level Output Voltage	at Iout	0.8·VANA /GPI			V

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Table 95. GPIO DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VOL	Low Level Output Voltage	at Iout			0.2· VANA/ GPI	V
IOUT	Driving Capability	VANA/GPI = 2.8V, gpio1_low_curr or gpio2_low_curr= 1	4			mA
		VANA/GPI = 2.8V, gpio1_low_curr or gpio2_low_curr = 0	16			
CLOAD	Capacitive Load				50	pF

8.5.3 GPIO Registers

Table 96. GPIO output 1 Register

Addr: 05h		GPIO output 1			
		This register controls GPIO outputs.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	gpi_curr1_en	0	R/W	Enables the CURR1 input	
				0	input disabled
				1	input enabled
1	gpi_curr2_en	0	R/W	Enables the CURR2 input	
				0	input disabled
				1	input enabled
2	gpi_curr6_en	0	R/W	Enables the CURR6 input	
				0	input disabled
				1	input enabled
3	gpi_en	0	R/W	Enables the VANA/GPI input	
				0	input disabled
				1	input enabled
4	gpi_curr30_en	0	R/W	Enables the CURR30 input	
				0	input disabled
				1	input enabled
5	gpi_curr31_en	0	R/W	Enables the CURR31 input	
				0	input disabled
				1	input enabled
6	gpi_curr32_en	0	R/W	Enables the CURR32 input	
				0	input disabled
				1	input enabled
7	gpi_curr33_en	0	R/W	Enables the CURR33 input	
				0	input disabled
				1	input enabled

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Table 97. GPIO signal 1 Register

Addr: 06h		GPIO signal 1		
		This register controls GPIO outputs.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpi_curr1_in	N/A	R	Reads a logic signal from pin CURR1; if gpi_curr1_en=1
1	gpi_curr2_in	N/A	R	Reads a logic signal from pin CURR2; if gpi_curr2_en=1
2	gpi_curr6_in	N/A	R	Reads a logic signal from pin CURR6; if gpi_curr6_en=1
3	gpi_in	N/A	R	Reads a logic signal from pin CURR6; if gpi_en=1
4	gpi_curr30_in	N/A	R	Reads a logic signal from pin CURR30; if gpi_curr30_en=1
5	gpi_curr31_in	N/A	R	Reads a logic signal from pin CURR31; if gpi_curr31_en=1
6	gpi_curr32_in	N/A	R	Reads a logic signal from pin CURR32; if gpi_curr32_en=1
7	gpi_curr33_in	N/A	R	Reads a logic signal from pin CURR33; if gpi_curr33_en=1

Table 98. GPIO output 2 Register

Addr: 50h		GPIO output 2			
		This register controls GPIO outputs.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	gpio1_out	0	R/W	Writes a logic signal to pin GPIO1/DLS; this is independent of any other bit setting e.g., gpio1_mode Table 100.	
1	gpio2_out	0	R/W	Writes a logic signal to pin GPIO1/DLS; this is independent of any other bit setting e.g., gpio2_mode Table 100	
2	gpi_rgb1_en	0	R/W	Enables the RGB1 input	
				0	input disabled
				1	input enabled
3	gpi_rgb2_en	0	R/W	Enables the RGB2 input	
				0	input disabled
				1	input enabled
4	gpi_rgb3_en	0	R/W	Enables the RGB3 input	
				0	input disabled
				1	input enabled
5	gpi_curr41_en	0	R/W	Enables the CURR41 input	
				0	input disabled
				1	input enabled
6	gpi_curr42_en	0	R/W	Enables the CURR42 input	
				0	input disabled
				1	input enabled
7	gpi_curr43_en	0	R/W	Enables the CURR43 input	
				0	input disabled
				1	input enabled

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Table 99. GPIO signal 2 Register

Addr: 51h		GPIO signal 2		
		This register controls GPIO outputs.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0	gpio1_in	N/A	R	Reads a logic signal from pin GPIO1/DLS; this is independent of any other setting e.g.,Table 100 except gpio1_pulls=11
1	gpio2_ in	N/A	R	Reads a logic signal from pin GPIO2/LIGHT; this is independent of any other setting e.g.,Table 100 except gpio2_pulls=11
2	gpi_rgb1_in	N/A	R	Reads a logic signal from pin RGB1; if gpi_rgb1_en=1
3	gpi_rgb2_in	N/A	R	Reads a logic signal from pin RGB2; if gpi_rgb2_en=1
4	gpi_rgb3_in	N/A	R	Reads a logic signal from pin RGB3; if gpi_rgb3_en=1
5	gpi_curr41_in	N/A	R	Reads a logic signal from pin CURR41; if gpi_curr41_en=1
6	gpi_curr42_in	N/A	R	Reads a logic signal from pin CURR42; if gpi_curr42_en=1
7	gpi_curr43_in	N/A	R	Reads a logic signal from pin CURR43; if gpi_curr43_en=1

Table 100. GPIO control Register

Addr: 1Eh		GPIO control			
		This register controls GPIO and GPIO1 pin functions.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	gpio1_mode	00	R/W	Defines the direction for pin GPIO1/DLS	
				00	Input only
				01	Output (push and pull)
				10	Output (open drain, only push; only NMOS is active)
				11	Output (open drain, only pull; only PMOS is active)
3:2	gpio1_pulls	01	R/W	Adds the following pullup/pulldown to pin GPIO1/DLS; this is independent of setting of bits gpio1_mode	
				00	None
				01	Pulldown
				10	Pullup
				11	ADC input (gpio1_mode = XX); recommended for analog signals
5:4	gpio2_mode	00	R/W	Defines the direction for pin GPIO2/LIGHT	
				00	Input only
				01	Output (push and pull)
				10	Output (open drain, only push; only NMOS is active)
				11	Output (open drain, only pull; only PMOS is active)

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Table 100. GPIO control Register (Continued)

Addr: 1Eh		GPIO control			
		This register controls GPIO and GPIO1 pin functions.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:6	gpio2_pulls	01	R/W	Adds the following pullup/pulldown to pin GPIO2/LIGHT; this is independent of setting of bits gpio2_mode	
				00	None
				01	Pulldown
				10	Pullup
				11	ADC input (gpio2_mode = XX); recommended for analog signals

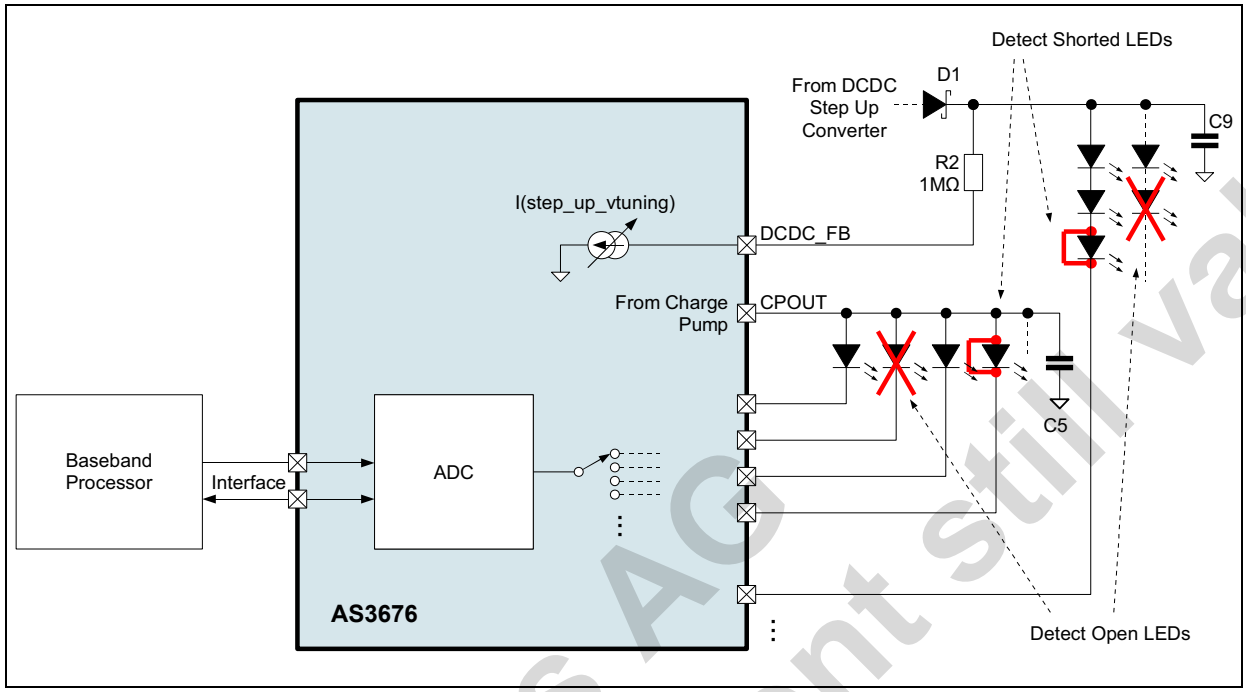
Table 101. GPIO driving cap Register

Addr: 20h		GPIO driving cap			
		This register enables low current mode for GPIOs.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	gpio1_low_curr	0	R/W	Defines the driving capability of pin GPIO1/DLS	
				0	Iout
				1	Iout /4
1	gpio2_low_curr	0	R/W	Defines the driving capability of pin GPIO2/LIGHT	
				0	Iout
				1	Iout /4

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8.6 LED Test

Figure 26. LED Function Testing



The AS3676 supports the verification of the functionality of all the connected LEDs (open and shorted LEDs can be detected). This feature is especially useful in production test to verify the correct assembly of the LEDs, all its connectors and cables. It can also be used in the field to verify if any of the LEDs is damaged. A damaged LED can then be disabled (to avoid unnecessary currents).

The current sources, charge pump, dcdc converter and the internal ADC are used to verify the forward voltage of the LEDs. If this forward voltage is within the specified limits of the LEDs, the external circuitry is assumed to operate.

8.6.1 Function Testing for single LEDs connected to the Charge Pump

For any current source connected to the charge pump (CURR30-33) where only one LED is connected between the charge pump and the current sink (see Figure 1) use:

Table 102. Function Testing for LEDs connected to the Charge Pump

Step	Action	Example Code
1	Switch on the charge pump and set it into manual 1:2 mode (to avoid automatic mode switching during measurements)	Reg 23h ≤ 14h (cp_mode = 1:2, manual) Reg 00h ≤ 04h (cp_on = 1)
2	Switch on the current sink for the LED to be tested	e.g. for register CURR31set to 9mA use Reg 10h ≤ 0Fh (curr3x_other = 9mA) Reg 03h ≤ 0ch (curr31_mode = curr31_other)
3	Measure with the ADC the voltage on CPOUT	Reg 26h ≤ 95h (adc_select=CPOUT,start ADC) Fetch the ADC result from Reg 27h and 28h
4	Measure with the ADC the voltage on the switched on current sink	Reg 26h ≤ 8bh (adc_select=CURR31,start ADC) Fetch the ADC result from Reg 27h and 28h
5	Switch off the current sink for the LED to be tested	Reg 03h ≤ 00h (curr31_mode = off)
6	Compare the difference between the ADC measurements (which is the actual voltage across the tested LED) against the specification limits of the tested LED	Calculation performed in baseband uProcessor

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Table 102. Function Testing for LEDs connected to the Charge Pump

Step	Action	Example Code
7	Do the same procedure for the next LED starting from point 2	Jump to 2. If not all the LEDs have been tested
8	Switch off the charge pump set charge pump automatic mode	Reg 00h ≤ 00h (cp_on = 0) Reg 23h ≤ 00h

8.6.2 Function Testing for LEDs connected to the Step Up DCDC Converter

For LEDs connected to the DCDC converter (usually current sinks CURR1,CURR2 and CURR6) use the following procedure:

Table 103. Function Testing for LEDs connected to the DCDC converter

Step	Action	Example Code
1	Switch on the current sink for the LED string to be tested (CURR1,2 or 6)	e.g. Test LEDs on CURR1: Reg 01h ≤ 01h (curr1_mode=on) Reg 09h ≤ 3ch (curr1_current = 9mA)
2	Select the feedback path for the LED string to be tested (e.g. step_up_fb = 01 for LED string on CURR1)	Reg 21h ≤ 02h (step_up_fb=curr1)
3	Set the current for step_up_vtuning exactly above the maximum forward voltage of the tested LED string + 0.6V (for the current sink) + 0.25V; add 6% margin (accuracy of step_up_vtuning); this sets the maximum output voltage limit for the DCDC converter	e.g. 4 LEDs with UfMAX = 4.1V gives 17.25V +6% = 18.29V; if R2=1MΩ and R3 = open, then select step_up_vtuning = 18 (Reg 21h ≤ 92h; results in 19.25V over voltage protection voltage – Table 9 on page 14)
4	Set step_up_prot = 1	Reg 22h ≤ 04h
5	Switch on the DCDC converter	Reg 00h ≤ 08h
6	Wait 80ms (DCDC_FB settling time)	
7	Measure the voltage on DCDC_FB (ADC)	Reg 26h ≤ 96h (adc_select=DCDC_FB, start ADC; Fetch the ADC result from Reg 27h and 28h)
8	If the voltage on DCDC_FB is above 1.0V, the tested LED string is broken – then skip the following steps	(Code >199h)
9	Switch off the over voltage protection (step_up_prot=0)	Reg 22h ≤ 00h
10	Reduce step_up_vtuning step by step until the measured voltage on DCDC_FB (ADC) is above 1.0V. After changing step_up_vtuning always wait 80ms, before AD-conversion	e.g.: Reg 21h ≤ 62h (step_up_vtuning=12): ADC result=1,602V
11	Measure voltage on DCDC_FB	e.g. DCDC_FB=1.602V
12	Switch off the DCDC converter	Reg 00h ≤ 00h
13	The voltage on the LED string can be calculated now as follows (R4 = open): $V_{LEDSTRING}$ = V(DCDC_FB) + I(step_up_vtuning) * R2 – 0.5V (current sinks feedback voltage: V_{FB2}). V(DCDC_FB) = ADC Measurement from point 11 I(step_up_vtuning) = last setting used for point 10	e.g.: V_{LED} = (1.602V + 12V – 0.5V) / 4 = 3.276V
14	Compare the calculated value against the specification limits of the tested LEDs	

Note: With the above described procedures electrically open and shorted LEDs can be automatically detected

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8.7 Analog-to-Digital Converter

The AS3676 has a built-in 10-bit successive approximation analog-to-digital converter (ADC). It is internally supplied by V2_5, which is also the full-scale input range (0V defines the ADC zero-code). For input signals exceeding V2_5 (typ. 2.5V) a resistor divider with a gain of 0.4 (Ratioprescaler) is used to scale the input of the ADC converter. Consequently the resolution is:

Table 104. ADC Input Ranges, Compliances and Resolution

Channels (Pins)	Input Range	V_{LSB}	Note
DCDC_FB, GPIO1/DLS, GPIO2/ LIGHT, VANA/GPI, audio controlled LED buffer output	0V-2.5V	2.44mV	V_{LSB}=2.5/1024
ADC_{TEMP_CODE}	-30°C to 125°C	1 / ADC_{TC}	junction temperature
CURR3x, CURR4x, RGBx VBAT, CPOUT	0V-5.5V	6.1mV	V_{LSB}=(2.5/1024)/0.4; internal resistor divider used
CURR1, CURR2, CURR6	0V-1.0V	2.44mV	V_{LSB}=2.5/1024

Table 105. ADC Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Resolution		10			Bit
V_{IN}	Input Voltage Range	V_{SUPPLY} = V2_5	VSS		see Table 104	V
DNL	Differential Non-Linearity			± 0.25		LSB
INL	Integral Non-Linearity			± 0.5		LSB
Vos	Input Offset Voltage			± 0.25		LSB
Rin	Input Impedance		100			MΩ
Cin	Input Capacitance				9	pF
V_{SUPPLY} (V2_5)	Power Supply Range	± 2%, internally trimmed.		2.5		V
Idd	Power Supply Current	During conversion only.		300		µ A
Idd	Power Down Current			100		nA
T_{TOL}	Temperature Sensor Accuracy	@ 25 °C	-10		+10	°C
$ADC_{TOFFSET}$	ADC temperature measurement offset value			375		°C
ADC_{TC}	Code temperature coefficient	Temperature change per ADC LSB		1.2939		°C/ Code
$Ratio_{PRESCALER}$	Ratio of Prescaler	For all low voltage current sinks, CPOUT and VBAT		0.4		
Transient Parameters (2.5V, 25 ºC)						
Tc	Conversion Time	All signals are internally generated and triggered by start_conversion		27		µs
fc	Clock Frequency			1.0		MHz
ts	Settling Time of S&H			16		µs

The junction temperature ($T_{JUNCTION}$) can be calculated with the following formula (ADC_{TEMP_CODE} is the adc conversion result for channel 17h selected by register adc_select = 010111b):

$$T_{JUNCTION}\,[°C] = ADC_{TOFFSET} - ADC_{TC} \cdot ADC_{TEMP_CODE} \qquad \text{(EQ 5)}$$

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ADC Registers

Table 106. ADC_MSB result Register

Addr: 27h		ADC_MSB result			
		Together with Register 27h, this register contains the results (MSB) of an ADC cycle.			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
6:0	D9:D3	N/A	R	ADC results register.	
7	result_not_ready	N/A	R	Indicates end of ADC conversion cycle	
				0	Result is ready
				1	Conversion is running

Table 107. ADC_LSB result Register

Addr: 28h		ADC_LSB result		
		Together with Register 28h, this register contains the results (LSB) of an ADC cycle		
Bit	**Bit Name**	**Default**	**Access**	**Description**
2:0	D2:D0	N/A	R	ADC result register

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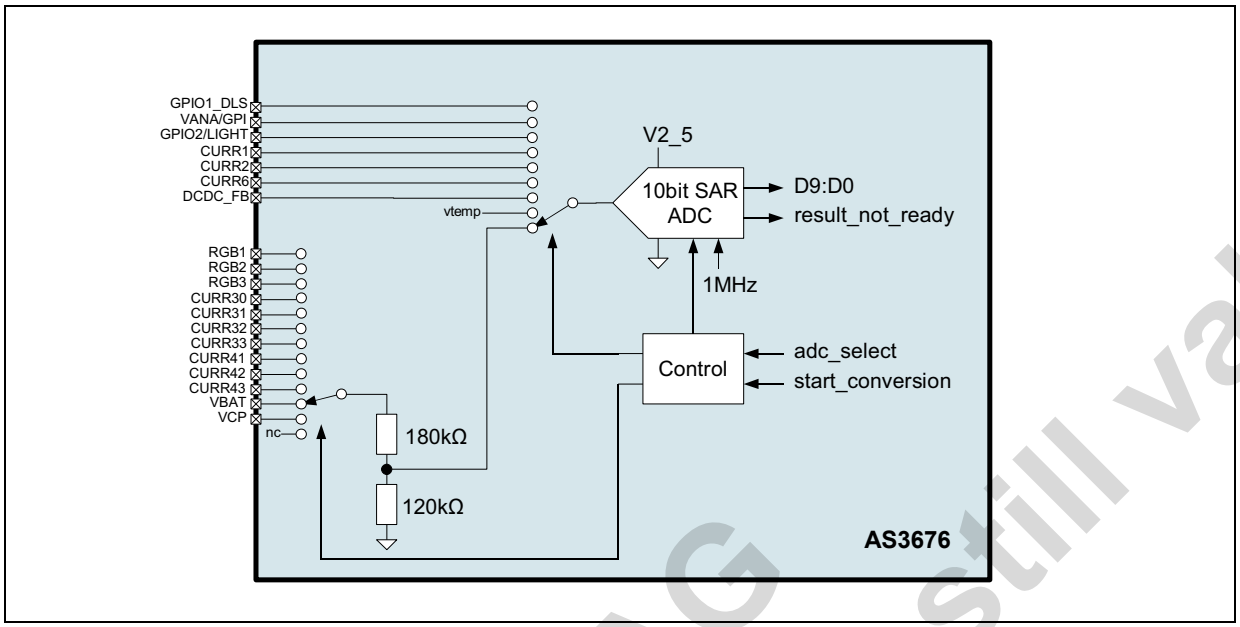
Table 108. ADC_control Register

Addr: 26h		ADC_control			
		This register input source selection and initialization of ADC			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5:0	adc_select[1]	03h	R/W	Selects input source as ADC input	
				000000 (00h)	GPIO2/LIGHT
				000001 (01h)	VANA/GPI
				000010 (02h)	GPIO1/DLS
				000011 (03h)	audio controlled LED buffer output
				000100 (04h)	reserved
				000101 (05h)	RGB1
				000110 (06h)	RGB2
				000111 (07h)	RGB3
				001000 (08h)	CURR1
				001001 (09h)	CURR2
				001010 (0Ah)	CURR30
				001011 (0Bh)	CURR31
				001100 (0Ch)	CURR32
				001101 (0Dh)	CURR33
				001110 (0Eh)	CURR41
				001111 (0Fh)	CURR42
				010000 (10h)	CURR43
				010001 (11h)	reserved
				010010 (12h)	reserved
				010011 (13h)	CURR6
				010100 (14h)	VBAT
				010101 (15h)	CPOUT
				010110 (16h)	DCDC_FB
				010111 (17h)	ADCTEMP_CODE (junction temperature)
				011xxx, 1xxxxx	reserved
6					NA
7	start_conversion	N/A	W	Writing a 1 into this bit starts one ADC conversion cycle.	

1. See Table Table 104 for ADC ranges and resolution.

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Figure 27. ADC Circuit

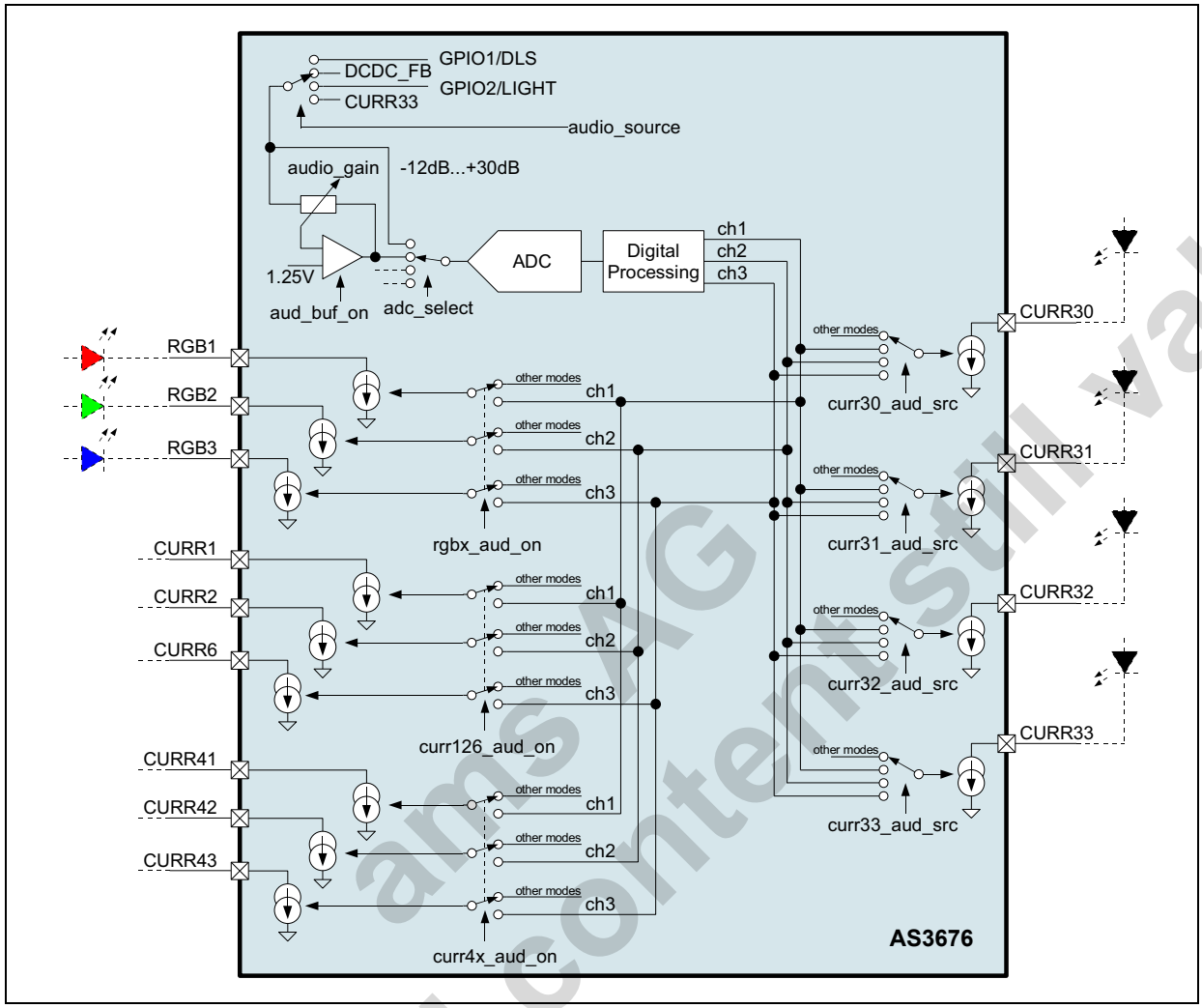


8.8 Audio controlled LEDs

Up to four RGB LEDs and/or up to 13 LEDs (number of LEDs is fully configurable) can be controlled by an audio source (connected to the pin CURR33, DCDC_FB or GPIO2/LIGHT). The color of the RGB LED(s) or the brightness of the single color LED(s) is depending on the input amplitude. For the RGB LEDs it starts from black transitions to blue, green, cyan, yellow, red and for high amplitudes white is used (internal lookup table if audio_color=000b).

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Figure 28. Audio controlled LED internal circuit



The audio controlled LED block is enabled if any of the registers curr30_aud_src[1:0]...curr33_aud_src[1:0], curr126_aud_on, rgbx_aud_on or curr4x_aud_on not equal zero.

The audio input amplifier (enabled by aud_buf_on=1) is used to allow the attenuation (or amplification of the input signal) and has the following parameters:

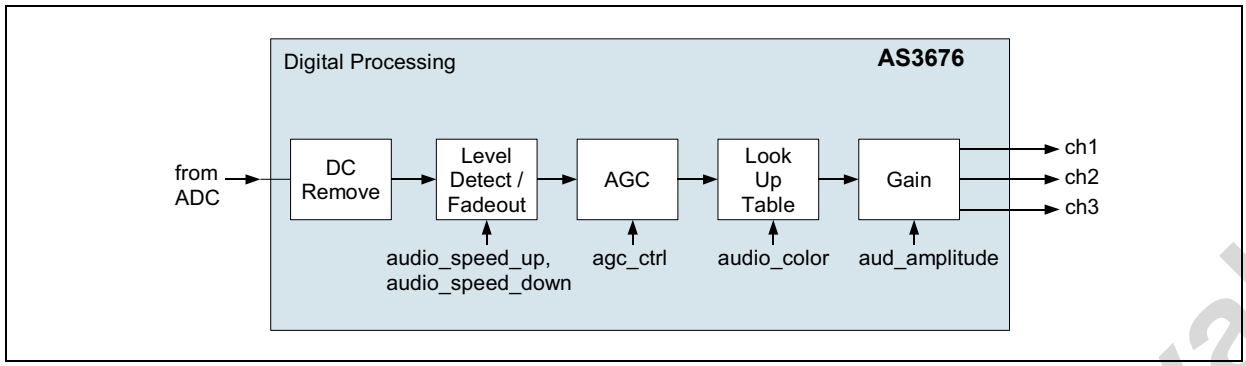
Table 109. Audio input Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIN	Input Voltage Range		0		2.5	V
Rin_min	min. Input Impedance	at max. input gain (30dB)		20		kΩ

The signal is converted with the ADC (If the audio controlled LED is active, the internal ADC is continuously running. In this case the ADC cannot be used for any other purpose). The digital processing converts this signal into 3 channels (ch1, ch2, ch3):

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Figure 29. Audio controlled LED digital processing internal circuit



These three output channels (ch1, ch2, ch3) can be routed to any of the current sources according to Figure 28.

The input amplitude is mapped into different colors (Look Up Table in Figure 29) for RGB LED(s) or brightness for single color LED(s). The mapping is controlled by the register audio_color. If audio_color = 000, then the mapping is done as follows:

Very low amplitudes are mapped to black, for higher amplitudes, the color smoothly transitions from blue, green, cyan, yellow, red and eventually to white (for high input amplitudes).

8.8.1 AGC

The AGC is used to 'compress' the input signal and to attenuate very low input amplitude signals (this is performed to ensure no light output for low signals especially for noisy input signals).

The AGC monitors the input signal amplitude and filters this amplitude with a filter with a short attack time, but a long decay time (decay time depends on the register agc_ctrl). This amplitude measurement (represented by an integer value from 0 to 15) is then used to amplify or attenuate the input signal with one of the following amplification ratios (output to input ratio) – the curve A, B, or C is selected depending on the register agc_ctrl:

Figure 30. AGC curve A (x-axis: input amplitude, y-axis: output amplitude; actual value: gain between output to input)

15													1,3	1,2	1,1	1,0
14									1,8	1,6	1,4	1,3				
13					3,3	2,6	2,2	1,9								
12				4,0												
11				4,0												
10				4,0												
9				4,0												
8			4,0													
7			4,0													
6			4,0													
5			4,0													
4		4,0														
3		4,0														
2		4,0														
1		4,0														
0	0,0															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

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Figure 31. AGC curve B (x-axis: input amplitude, y-axis: output amplitude; actual value: gain between output to input)

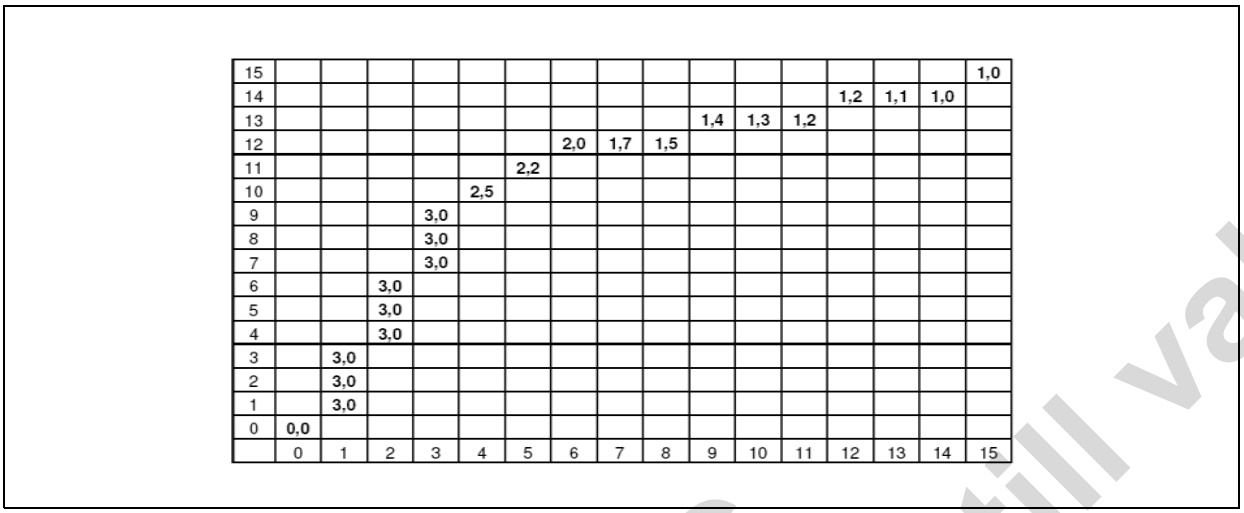
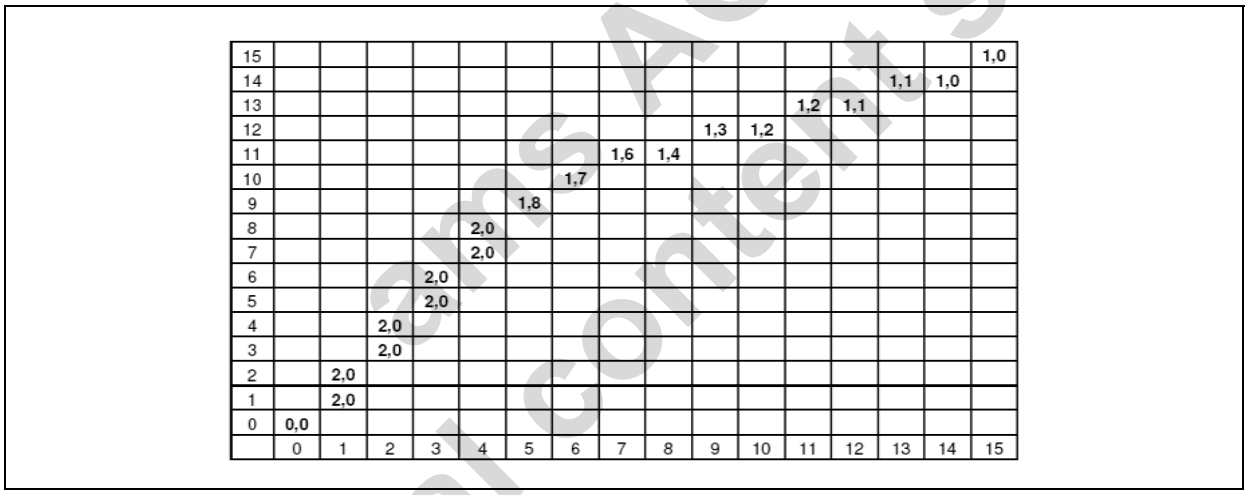


Figure 32. AGC curve C (x-axis: input amplitude, y-axis: output amplitude; actual value: gain between output to input)



8.8.2 Audio Controlled LED Registers

Table 110. Audio Control Register

Addr: 46h		Audio Control			
		Audio Sync Mode control			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
0	aud_buf_on	0b	R/W	Audio input buffer enable	
				0	off; for audio direct input to ADC use adc_select = 00h (AUDIO_IN)
				1	on; set adc_select = 03h (buffer output)
4:2	audio_color	000b	R/W	audio controlled LED color selection (amplitude mode)	
				000	color scheme defined by lookup table
				001-111	single color scheme (b2=R, b1=G, b0=B)

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Table 110. Audio Control Register (Continued)

Addr: 46h		Audio Control			
		Audio Sync Mode control			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
7:6	audio_speed_down	00b	R/W	Audio controlled LED persistence time (ramping down)	
				00	none
				01	200ms
				10	400ms
				11	800ms

Table 111. Audio input Register

Addr: 47h		Audio input			
		Audio Sync input control			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2:0	audio_gain	000b	R/W	Audio input buffer gain control	
				000	-12dB
				001	-6dB
				010	0dB
				011	+6dB
				100	+12dB
				101	+18dB
				110	+24dB
				111	+30dB
5:3	agc_ctrl	000b	R/W	Audio input buffer AGC function controls AGC switching threshold	
				000	AGC off
				001	Attenuate low amplitude signals otherwise linear response (to remove e.g. noise)
				010	AGC curve A; slow decay of amplitude detection
				011	AGC curve A; fast decay of amplitude detection
				100	AGC curve B; slow decay of amplitude detection
				101	AGC curve B; fast decay of amplitude detection
				110	AGC curve C; slow decay of amplitude detection
				111	AGC curve C; fast decay of amplitude detection
6	audio_man_start[1]	0b	R/W	Startup Control of audio input buffer (used to charge optional external dc blocking capacitor)	
				0	automatic precharging 300us (if audio_dis_start = 0)
				1	continuously precharging (if aud_buf_on = 1)
7	audio_dis_start[2]	0b	R/W	Disable Startup Control of audio input buffer (used to charge optional external dc blocking capacitor)	
				0	precharging enabled
				1	precharging disabled

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1. Its safe to keep default value
2. Its safe to keep default value

Table 112. Audio output Register

Addr: 48h		Audio output			
		Audio Sync input control			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
2:0	aud_amplitude	000b	R/W	LED(s) output amplitude control (in percent of selected output current)	
				000	6.25%
				001	12.5%
				010	25%
				011	50%
				100	75%
				101	87.5%
				110	93.75%
				111	100%
4	curr126_aud_on	0b	R/W	Audio controlled LED enable for CURR1, CURR2, CURR6	
				0	off
				1	on, audio controlled LED is enabled
5	rgbx_aud_on	0b	R/W	Audio controlled LED enable for RGB1-RGB3	
				0	off
				1	on, audio controlled LED is enabled
6	curr4x_aud_on	0b	R/W	Audio controlled LED enable for CURR41-CURR43	
				0	off
				1	on, audio controlled LED is enabled

Table 113. CURR3x audio source Register

Addr: 53h		CURR3x audio source			
		Controls CURR30,31,32,33 audio outputs and enables audio controlled LED			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
1:0	curr30_aud_src[1:0]	00b	R/W	Audio controlled LED source for CURR30	
				00	All other modes
				01	ch1 connected to CURR30, audio controlled LED on
				10	ch2 connected to CURR30, audio controlled LED on
				11	ch3 connected to CURR30, audio controlled LED on

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Table 113. CURR3x audio source Register (Continued)

Addr: 53h		CURR3x audio source		
		Controls CURR30,31,32,33 audio outputs and enables audio controlled LED		
Bit	**Bit Name**	**Default**	**Access**	**Description**
3:2	curr31_aud_src[1:0]	00b	R/W	Audio controlled LED source for CURR31
				00 All other modes
				01 ch1 connected to CURR31, audio controlled LED on
				10 ch2 connected to CURR31, audio controlled LED on
				11 ch3 connected to CURR32, audio controlled LED on
5:4	curr32_aud_src[1:0]	00b	R/W	Audio controlled LED source for CURR32
				00 All other modes
				01 ch1 connected to CURR32, audio controlled LED on
				10 ch2 connected to CURR32, audio controlled LED on
				11 ch3 connected to CURR32, audio controlled LED on
7:6	curr33_aud_src[1:0]	00b	R/W	Audio controlled LED source for CURR33
				00 All other modes
				01 ch1 connected to CURR33, audio controlled LED on
				10 ch2 connected to CURR33, audio controlled LED on
				11 ch3 connected to CURR33, audio controlled LED on

Table 114. Audio Control 2 Register

Addr: 55h		Audio Control 2		
		Audio Mode Control Register		
Bit	**Bit Name**	**Default**	**Access**	**Description**
0		NA	not used	
3:1	audio_speed_up	000b	R/W	Audio controlled LED filtering time (ramping up)
				000 none
				001 50ms
				010 100ms
				011 150ms
				100 200ms
				101 250ms
				110 400ms
				111 800ms

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Table 114. Audio Control 2 Register (Continued)

Addr: 55h		Audio Control 2			
		Audio Mode Control Register			
Bit	**Bit Name**	**Default**	**Access**	**Description**	
5:4	audio_source	00b	R/W	Audio Buffer input source	
				00	CURR33
				01	DCDC_FB
				10	GPIO1/DLS
				11	GPIO2/LIGHT

8.9 Power-On Reset

The internal reset is controlled by two sources:

- VBAT Supply
- Serial interface state (CLK, DATA)

The internal reset is forced if VBAT is low or if both interface pins (CLK, DATA) are low for more than t_{POR_DEB} (typ. 100ms)[6]. Then device enters shutdown mode. For details see section Operating Modes on page 80.

The reset levels control the state of all registers. As long as VBAT and CLK/DATA are below their reset thresholds, the register contents are set to default. Access by serial interface is possible once the reset thresholds are exceeded.

Figure 33. Zero Power Device Wakeup block diagram

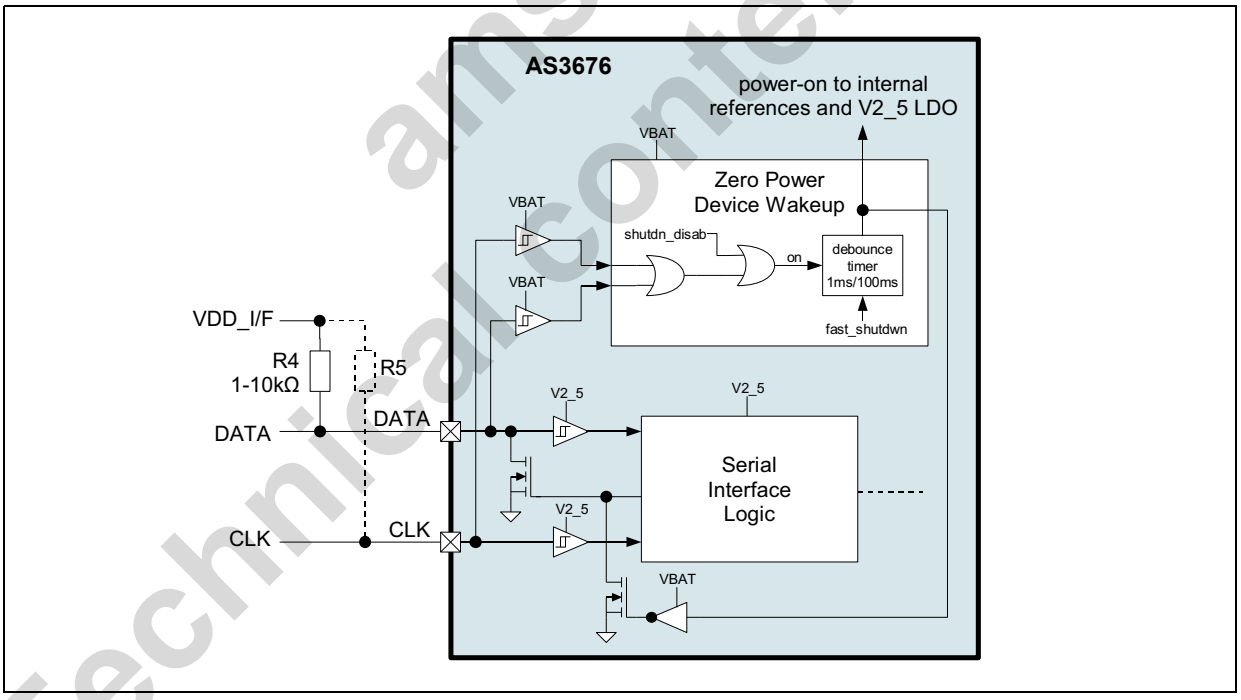


Table 115. Power On Reset Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{POR_VBAT}	Overall Power-On Reset	Monitor voltage on V2_5; power-on reset for all internal functions.	1.8	2.15	2.4[1]	V

6. Only if shutdwn_enab=1

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Table 115. Power On Reset Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VPOR_PERI	Reset Level for pins CLK, DATA	Monitor voltage on pins CLK, DATA	0.29	1.0	1.38	V
tPOR_DEB	Reset debounce time for pins CLK, DATA		80	100	120	ms
tstart	Interface Startup Time		4	6	8	ms

1. Guaranteed by design - min./max. limits not production tested

8.9.1 Reset control register

Table 116. Reset and Overtemp control Register

Addr: 29h		Reset and Overtemp control			
		This register reads and resets the overtemperature flag.			
Bit	Bit Name	Default	Access	Description	
4	shutdwn_enab	0	R/W	Enable Shutdown mode and serial interface reset.	
				0	Serial Interface reset disabled. Device does not enter Shutdown mode
				1	Serial Interface reset enabled, device enters shutdown when SCL and SDA remain low for tPOR_DEB

8.10 Temperature Supervision

An integrated temperature sensor provides over-temperature protection for the AS3676. This sensor generates a flag if the device temperature reaches the overtemperature threshold of 140º. The threshold has a hysteresis to prevent oscillation effects.

If the device temperature exceeds the T140 threshold all current sources, the charge pump and the dcdc converter is disabled and the ov_temp flag is set. After decreasing the temperature by THYST operation is resumed.

The ov_temp flag can only be reset by first writing a 1 and then a 0 to the register bit rst_ov_temp.

Bit ov_temp_on = 1 activates temperature supervision (Table 118). It is recommend to leave this bit set (default state).

Table 117. Overtemperature Detection

Symbol	Parameter	Condition		Min	Typ	Max	Unit
T140	ov_temp Rising Threshold				140		ºC
THYST	ov_temp Hysteresis				5		ºC

Table 118. Reset and Overtemp control Register

Addr: 29h		Reset and Overtemp control			
		This register reads and resets the overtemperature flag.			
Bit	Bit Name	Default	Access	Description	
0	ov_temp_on	1	W	Activates/deactivates device temperature supervision. Default: Off - all other bits are only valid if this bit is set to 1	
				0	Temperature supervision is disabled. No reset will be generated if the device temperature exceeds 140ºC
				1	Temperature supervision is enabled

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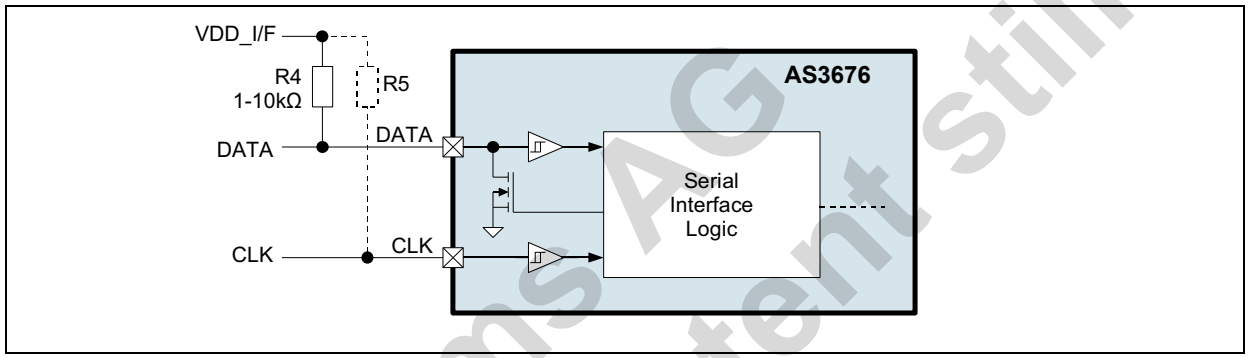
Table 118. Reset and Overtemp control Register (Continued)

Addr: 29h		Reset and Overtemp control			
		This register reads and resets the overtemperature flag.			
Bit	**Bit Name**	**Default**	**Access**	Description	
1	ov_temp	N/A	R	1	Indicates that the overtemperature threshold has been reached; this flag is not cleared by an overtemperature reset. It has to be cleared using rst_ov_temp
2	rst_ov_temp	0	R/W	The ov_temp flag is cleared by first setting this bit to 1, and then setting this bit to 0.	

8.11 Serial Interface

The AS3676 is controlled using serial interface pins CLK and DATA:

Figure 34. Serial interface block diagram



The clock line CLK is never held low by the AS3676 (as the AS3676 does not use clock stretching of the bus).

Table 119. Serial Interface Voltages and Timings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IHI/F}$	High Level Input Voltage	Pins DATA and CLK	1.38		VBAT	V
$V_{ILI/F}$	Low Level Input Voltage		0.0		0.52	V
$V_{HYSTI/F}$	Hysteresis			0.1		V
t_{RISE}	Rise Time		0		1000	ns
t_{FALL}	Fall Time		0		300	ns
t_{CLK_FILTER}	Spike Filter on CLK			100		ns
t_{DATA_FILTER}	Spike Filter on DATA			300		ns

The AS3676 is compatible to the NXP two wire specification http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf, Version 2.1, January 2000 for standard and fast mode (no high speed mode).

8.11.1 Serial Interface Features

- Fast Mode Capability (Maximum Clock Frequency is 400 kHz)
- 7-bit Addressing Mode
- Write Formats
  - Single-Byte Write
  - Page-Write

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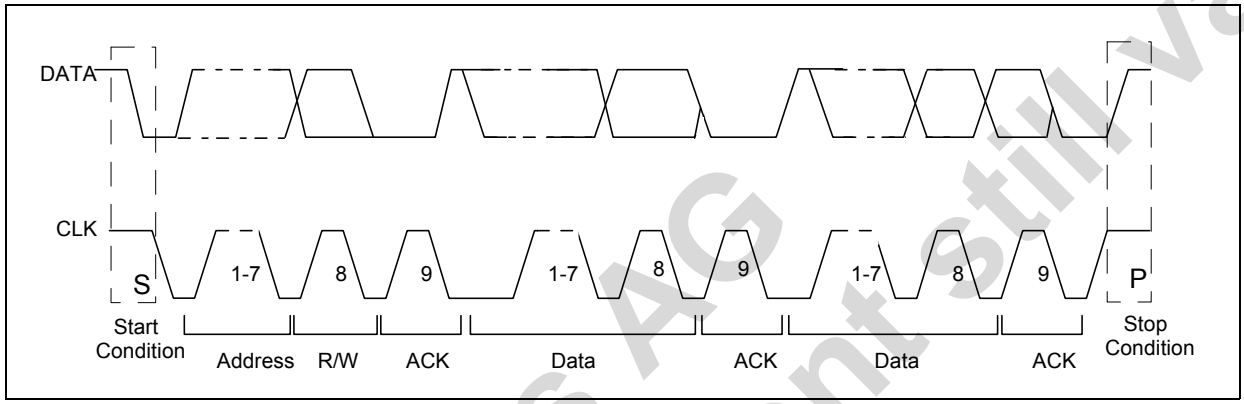
- Read Formats
  - Current-Address Read
  - Random-Read
  - Sequential-Read
- DATA Input Delay and CLK spike filtering by integrated RC components

8.11.2 Device Address Selection

The serial interface address of the AS3676 has the following address:

- 80h – Write Commands
- 81h – Read Commands

Figure 35. Complete Serial Data Transfer



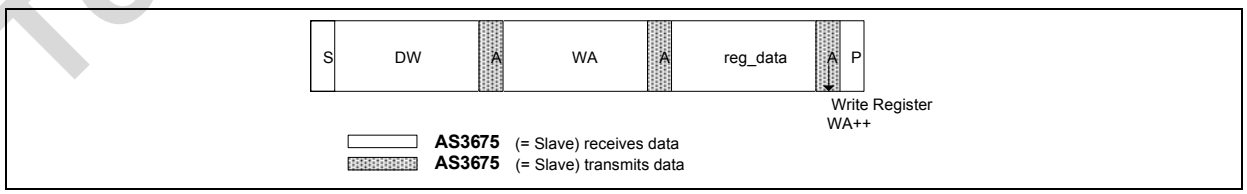
Serial Data Transfer Formats

Definitions used in the serial data transfer format diagrams are listed in the following table:

Table 120. Serial Data Transfer Byte Definitions

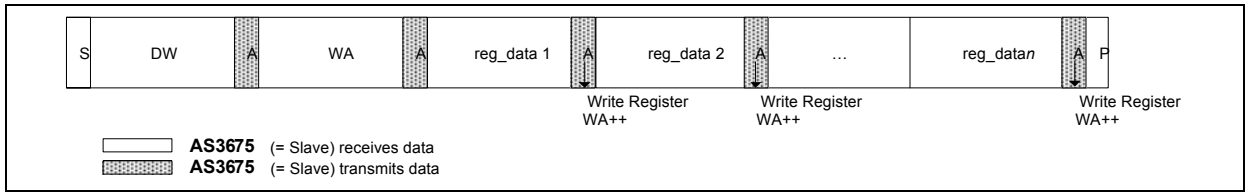
Symbol	Definition	R/W (AS3676 Slave)	Note
S	Start Condition after Stop	R	1 bit
Sr	Repeated Start	R	1 bit
DW	Device Address for Write	R	10000000b (80h).
DR	Device Address for Read	R	10000001b (81h)
WA	Word Address	R	8 bits
A	Acknowledge	W	1 bit
N	Not Acknowledge	R	1 bit
reg_data	Register Data/Write	R	8 bits
data (n)	Register Data/read	R	1 bit
P	Stop Condition	R	8 bits
WA++	Increment Word Address Internally	R	During Acknowledge

Figure 36. Serial Interface Byte Write



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Figure 37. Serial Interface Page Write



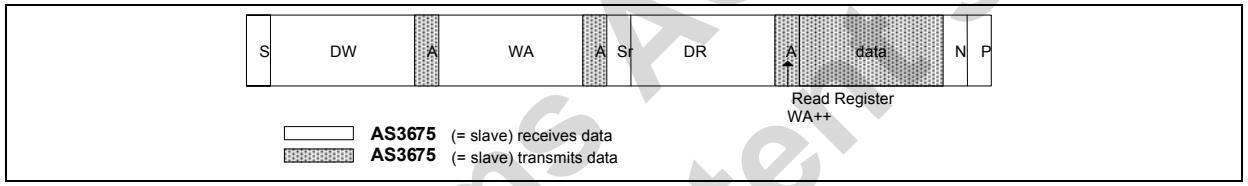
Byte Write and Page Write formats are used to write data to the slave.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

The following diagrams show the serial read formats supported by the AS3676.

Figure 38. Serial Interface Random Read

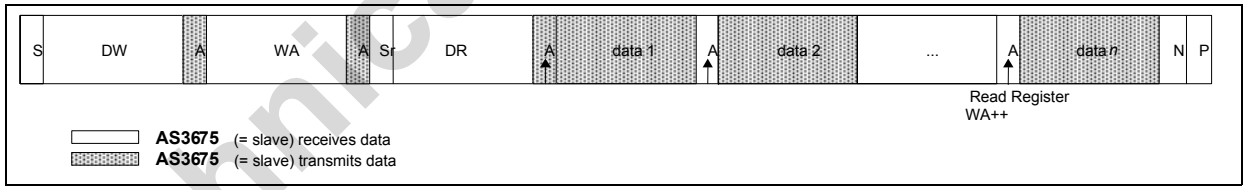


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st CLKpulse after the ACKNOWLEDGE bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a NOT ACKNOWLEDGE, and issues a STOP condition on the bus.

Figure 39. Serial Interface Sequential Read

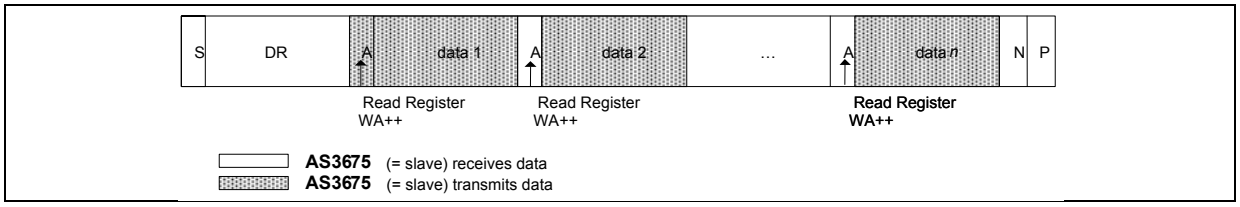


Sequential Read is the extended form of Random Read, as multiple register-data bytes are subsequently transferred.

In contrast to the Random Read, in a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a NOT ACKNOWLEDGE following the last data byte and subsequently generate the STOP condition.

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Figure 40. Serial Interface Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address.

Analogous to Random Read, a single byte transfer is terminated with a NOT ACKNOWLEDGE after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes must be responded to with an ACKNOWLEDGE from the master.

For termination of the transmission the master sends a NOT ACKNOWLEDGE following the last data byte and a subsequent STOP condition.

8.12 Operating Modes

If the voltages on CLK and DATA is less than V_{POR_PERI} for > t_{POR_DEB} (see Table 115 on page 75), the AS3676 is in shutdown mode and its current consumption is minimized (I_{BAT} = $I_{SHUTDOWN}$) and all internal registers are reset to their default values.

If the voltage at CLK or DATA rises above V_{POR_PERI}, the AS3676 serial interface is enabled and the AS3676 and the standby mode is selected. The AS3676 is switched automatically from standby mode (I_{BAT} = I_{STANBY}) into normal mode (I_{BAT} = I_{ACTIVE}) and back, if one of the following blocks are activated:

- Charge pump
- Step up regulator
- Any current sink
- ADC conversion started
- PWM active
- Pattern mode active.

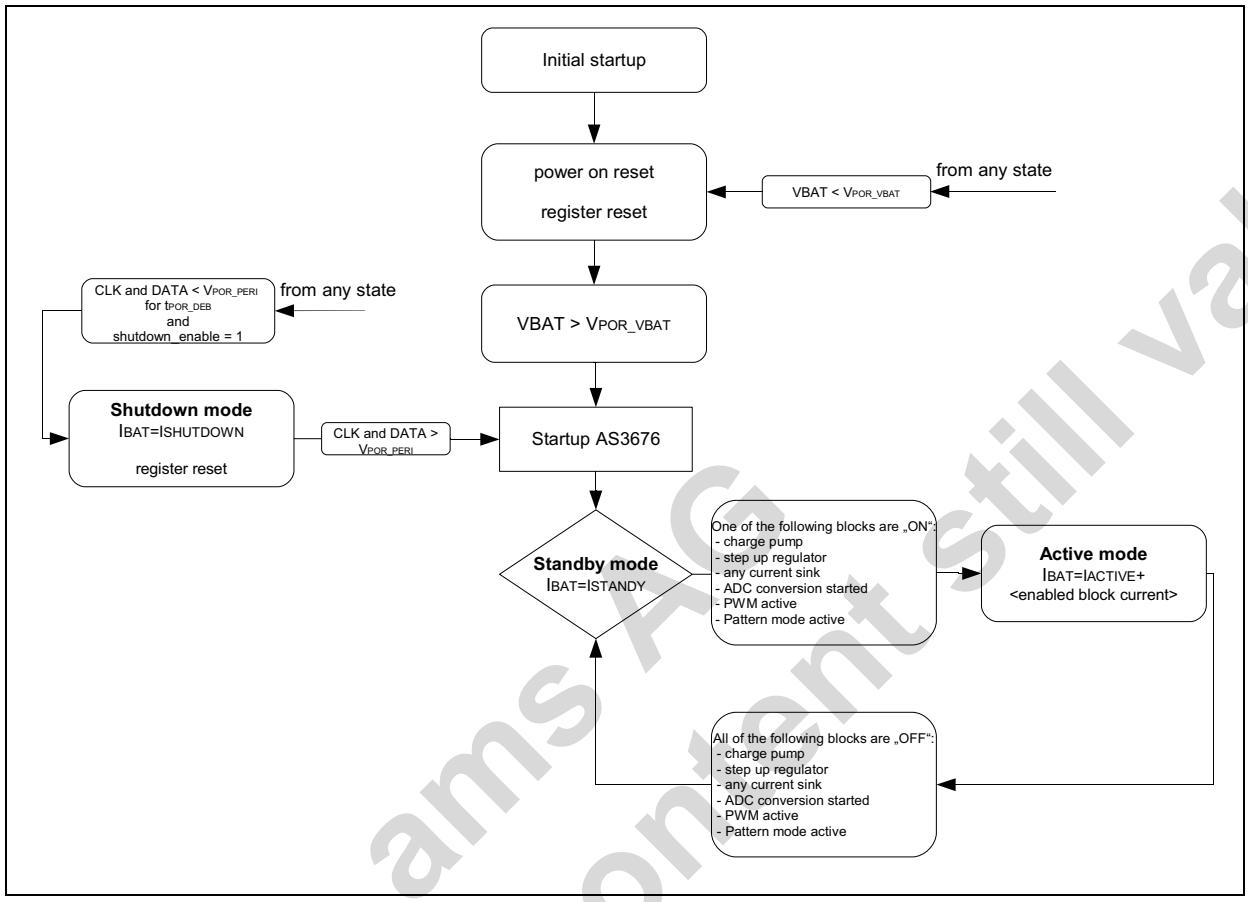
If any of these blocks are already switched on the internal oscillator is running and a write instruction to the registers is directly evaluated within 1 internal CLK cycle (typ. 1µs)

If all these blocks are disabled, a write instruction to enable these blocks is delayed by 64 CLK cycles (oscillator will startup, within max 200µs).

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The mode switching is shown in Figure 41:

Figure 41. Startup and Operating Mode Selection



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9 Register Map

Table 121. Registermap

Register Definition	Addr	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Reg. control	00h	00					step_up_on	cp_on		ldo_on
curr12 control	01h	00h					curr2_mode		curr1_mode	
curr rgb control	02h	00h	curr6_mode		rgb3_mode		rgb2_mode		rgb1_mode	
curr3 control1	03h	00h	curr33_mode		curr32_mode		curr31_mode		curr30_mode	
curr4 control	04h	00h			curr43_mode		curr42_mode		curr41_mode	
GPIO output 1	05h	00h	gpi_curr33_en	gpi_curr32_en	gpi_curr31_en	gpi_curr30_en	gpi_en	gpi_curr6_en	gpi_curr2_en	gpi_curr1_en
GPIO signal 1	06h	00h	gpi_curr33_in	gpi_curr32_in	gpi_curr31_in	gpi_curr30_in	gpi_in	gpi_curr6_in	gpi_curr2_in	gpi_curr1_in
LDO Voltage	07h	00h				ldo_voltage				
Curr1 current	09h	00h	curr1_current							
Curr2 current	0Ah	00h	curr2_current							
Rgb1 current	0Bh	00h	rgb1_current							
Rgb2 current	0Ch	00h	rgb2_current							
Rgb3 current	0Dh	00h	rgb3_current							
Curr3x strobe	0Eh	00h			curr3x_strobe					
Curr3x preview	0Fh	00h			curr3x_preview					
Curr3x other	10h	00h			curr3x_other					
Curr3 strobe control	11h	00h	strobe_timing				strobe_mode		strobe_ctrl	
Curr3 control2	12h	00h	strobe_pin		curr3x_strobe_high			preview_ctrl		preview_off_after strobe
Curr41 current	13h	00h	curr41_current							
Curr42 current	14h	00h	curr42_current							
Curr43 current	15h	00h	curr43_current							
Pwm control	16h	00h			pwm_dim_speed			pwm_dim_mode		
pwm code	17h	00h	pwm_code							
Pattern control	18h	00h	curr33_pattern	curr32_pattern	curr31_pattern	curr30_pattern	softdim_pattern	pattern_delay		pattern_color
Pattern data0	19h	00h	pattern_data[7:0]							
Pattern data1	1Ah	00h	pattern_data[15:8]							
Pattern data2	1Bh	00h	pattern_data[23:16]							
Pattern data3	1Ch	00h	pattern_data[31:24]							
GPIO control	1Eh	44h	gpio2_pulls		gpio2_mode		gpio1_pulls		gpio1_mode	
GPIO driving cap	20h	00h							gpio2_low_curr	gpio1_low_curr

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Table 121. Registermap

Register Definition	Addr	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
DCDC control1	21h	00h	step_up_vtuning					step_up_fb		step_up_frequ
DCDC control2	22h	04h	step_up_fb_auto				step_up_lowcur	step_up_prot	skip_fast	step_up_res
CP control	23h	00h		cp_auto_on	cp_start_debounce	cp_mode_switching		cp_mode		cp_clk
CP mode Switch1	24h	00h		rgb3_on_cp	rgb2_on_cp	rgb1_on_cp	curr33_on_cp	curr32_on_cp	curr31_on_cp	curr30_on_cp
CP mode Switch2	25h	00h	curr6_on_cp			curr43_on_cp	curr42_on_cp	curr41_on_cp	curr2_on_cp	curr1_on_cp
ADC_control	26h	03h	start_conversion		adc_select					
ADC_MSB result	27h	NA	result_not_ready	D9:D3						
ADC_LSB result	28h	NA						D2:D0		
Reset and Overtemp control	29h	01h				shutdwn_enab		rst_ov_temp	ov_temp	ov_temp_on
Curr low voltage status1	2Ah	NA	curr6_low_v	rgb3_low_v	rgb2_low_v	rgb1_low_v	curr33_low_v	curr32_low_v	curr31_low_v	curr30_low_v
Curr low voltage status2	2Bh	NA				curr43_low_v	curr42_low_v	curr41_low_v	curr2_low_v	curr1_low_v
gpio current	2Ch	00h		pattern_slow		pattern_delay2				
curr6 current	2Fh	00h	curr6_current							
Adder Current 1	30h	00h	adder_current1 (can be enabled for CURR30, CURR1, RGB1, CURR41)							
Adder Current 2	31h	00h	adder_current2 (can be enabled for CURR31, CURR2, RGB2, CURR42)							
Adder Current 3	32h	00h	adder_current3 (can be enabled for CURR32, CURR6, RGB3, CURR43)							
Adder Enable 1	33h	00h			curr43_adder	curr42_adder	curr41_adder	rgb3_adder	rgb2_adder	rgb1_adder
Adder Enable 2	34h	00h		curr33_adder	curr32_adder	curr31_adder	curr30_adder	curr6_adder	curr2_adder	curr1_adder
Subtract Enable	35h	00h					sub_en4	sub_en3	sub_en2	sub_en1
ASIC ID1	3Eh	AEh	1	0	1	0	1	1	1	0
ASIC ID2	3Fh	5Xh	0	1	0	1	revision			
Curr30 current	40h	00h	curr30_current							
Curr31 current	41h	00h	curr31_current							
Curr32 current	42h	00h	curr32_current							
Curr33 current	43h	00h	curr33_current							
Audio Control	46h	00h	audio_speed_down			audio_color				aud_buf_on
Audio input	47h	00h	audio_dis_start	audio_man_start	agc_ctrl			audio_gain		

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Table 121. Registermap

Register Definition	Addr	Default	Content							
Name			b7	b6	b5	b4	b3	b2	b1	b0
Audio output	48h	00h		curr4x_aud_on	rgbx_aud_on	curr126_aud_on		aud_amplitude		
GPIO output 2	50h	00h	gpi_curr43_en	gpi_curr42_en	gpi_curr41_en	gpi_rgb3_en	gpi_rgb2_en	gpi_rgb1_en	gpio2_out	gpio1_out
GPIO signal 2	51h	00h	gpi_curr43_in	gpi_curr42_in	gpi_curr41_in	gpi_rgb3_in	gpi_rgb2_in	gpi_rgb1_in	gpio2_ in	gpio1_in
Adder Current 4	52h	00h	adder_current4 (can be enabled for CURR33)							
CURR3x audio source	53h	00h	curr33_aud_src[1:0]		curr32_aud_src[1:0]		curr31_aud_src[1:0]		curr30_aud_src[1:0]	
Pattern End	54h	00h								pattern_end
Audio Control 2	55h	00h			audio_source		audio_speed_up			
DLS mode control1	56h	00h		rgb3_on_dls	rgb2_on_dls	rgb1_on_dls	curr33_on_dls	curr32_on_dls	curr31_on_dls	curr30_on_dls
DLS mode control2	57h	00h	curr6_on_dls			curr43_on_dls	curr42_on_dls	curr41_on_dls	curr2_on_dls	curr1_on_dls
ALS control	90h	00h						amb_gain		amb_on
ALS filter	91h	00h		amb_filter_down				amb_filter_up		
ALS offset	92h	00h	amb_offset							
ALS result	93h	00h	amb_result							
ALS curr12 group	94h	00h					curr2_amb_group		curr1_amb_group	
ALS rgb group	95h	00h	curr6_amb_group		rgb3_amb_group		rgb2_amb_group		rgb1_amb_group	
ALS curr3x group	96h	00h	curr33_amb_group		curr32_amb_group		curr31_amb_group		curr30_amb_group	
ALS curr4x group	97h	00h			curr43_amb_group		curr42_amb_group		curr41_amb_group	
ALS group 1 Y0	98h	00h	group1_y0							
ALS group 1 Y3	99h	00h	group1_y3							
ALS group 1 X1	9Ah	00h	group1_x1							
ALS group 1 K1	9Bh	00h	group1_k1							
ALS group 1 X2	9Ch	00h	group1_x2							
ALS group 1 K2	9Dh	00h	group1_k2							
ALS group 2 Y0	9Eh	00h	group2_y0							
ALS group 2 Y3	9Fh	00h	group2_y3							
ALS group 2 X1	A0h	00h	group2_x1							
ALS group 2 K1	A1h	00h	group2_k1							
ALS group 2 X2	A2h	00h	group2_x2							
ALS group 2 K2	A3h	00h	group2_k2							
ALS group 3 Y0	A4h	00h	group3_y0							
ALS group 3 Y3	A5h	00h	group3_y3							
ALS group 3 X1	A6h	00h	group3_x1							

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Table 121. Registermap

Register Definition	Addr	Default	Content							
Name			**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
ALS group 3 K1	A7h	00h	group3_k1							
ALS group 3 X2	A8h	00h	group3_x2							
ALS group 3 K2	A9h	00h	group3_k2							

Note: If writing to register, write 0 to unused bits

Write to read only bits will be ignored

yellow color = read only

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10 External Components

Table 122. External Components List

Part Number	Min	Value Typ	Max	tol. (min.)	Rating (max)	Notes	Package (min.)[1]
C1		1µF		±20%	6.3V	Ceramic, X5R (V2_5 output) (e.g. Taiyo Yuden JMK105BJ105KV-F)	0402
C2		1µF		±20%	6.3V	Ceramic, X5R (VBAT) (e.g. Taiyo Yuden JMK105BJ105KV-F)	0402
C3		1µF		±20%	6.3V	Ceramic, X5R (Charge Pump) (e.g. Taiyo Yuden JMK105BJ105KV-F)	0402
C4		1µF		±20%	6.3V	Ceramic, X5R (Charge Pump) (e.g. Taiyo Yuden JMK105BJ105KV-F)	0402
C5		2.2µF		±20%	6.3V	Ceramic, X5R (Charge Pump Output) (e.g. Taiyo Yuden JMK107BJ225MA-T)	0403
C6		1µF		±20%	6.3V	Ceramic, X5R (Step Up DCDC input) (e.g. Taiyo Yuden JMK105BJ105KV-F)	0402
C7 - optional	only required in voltage feedback mode of DCDC	1.5nF		±20%	25V	Ceramic, X5R (Step Up DCDC Feedback, 150pF for over voltage protection)	0402
C8 - optional		15nF		±20%	6.3V	Ceramic, X5R (Step Up DCDC Feedback, 1.5nF for over voltage protection)	0402
C9		10µF		±20%	25V	Ceramic, X5R, X7R (Step Up DCDC output) e.g. Murata GRM188R61E106MA73[2]	0603
		4.7µF				e.g. Taiyo Yuden TMK316BJ475KD	3.2x1.6x 0.85mm
C10		2.2µF		±20%	6.3V	Ceramic, X5R (VANA/GPI output) (e.g. Taiyo Yuden JMK107BJ225MA-T)	0402
R1		100mΩ		±5%		Shunt Resistor	0603
R2		1MΩ		±1%		Step Up DC/DC Converter Voltage Feedback	0201
R3		100kΩ		±1%		Step Up DC/DC Converter Voltage Feedback - not required for over voltage protection	0201
R4, R5		1-10kΩ		±1%		DATA, CLK Pullup resistor – usually already inside master	0201
L1		10µH (15µH[3])		±20%		Recommended Type: Coilcraft LPS3010-123[4] or Murata LQH3NPN100NJ0, LQH3NPN150NJ0 or Panasonic ELLSFG100MA or TDK VLF3012Aor Taiyo Yuden NRH3012T100MN	3x3x1mm

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Table 122. External Components List

Part Number	Min	Value Typ	Max	tol. (min.)	Rating (max)	Notes	Package (min.)[1]
Q1 (+ D1)	Fairchild FDFMA3N109					Integrated NMOS and Schottky diode	MicroFET 2x2mm
	Fairchild FDFME3N311ZT or OnSemi NTLUF4189NZ					Integrated NMOS and Schottky diode; recommended for configurations up to 12 LEDs	MicroFET 1.6x1.6mm
D2:D20	LED					As required by application	

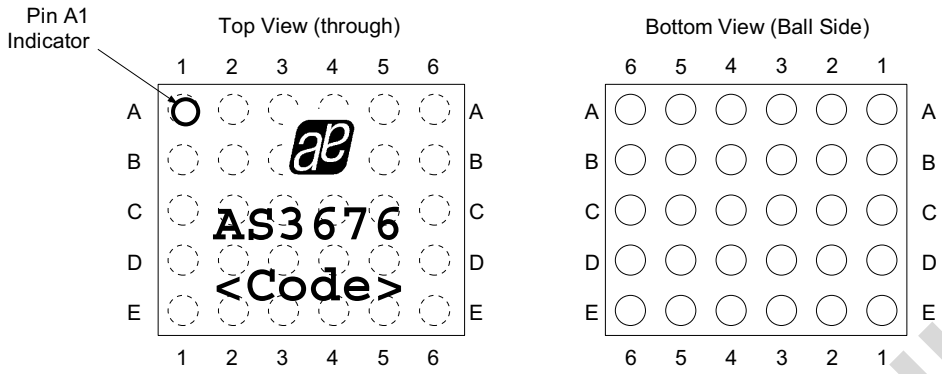
1. in 1/100 inch (unless otherwise specified)
2. Specified >1µF at 20V; use up to 20V DCDC output voltage
3. Results in improved efficiency compared to 10µH
4. For highest efficiency

As system efficiency is depending on LED configurations, external components and operating conditions, see austriamicrosystems application note 'Mobile Backlight Selection Guide 1vx.pdf' for optimizing efficiency and components size (coil L1, transistor Q1, diode D1).

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11 Package Drawings and Markings

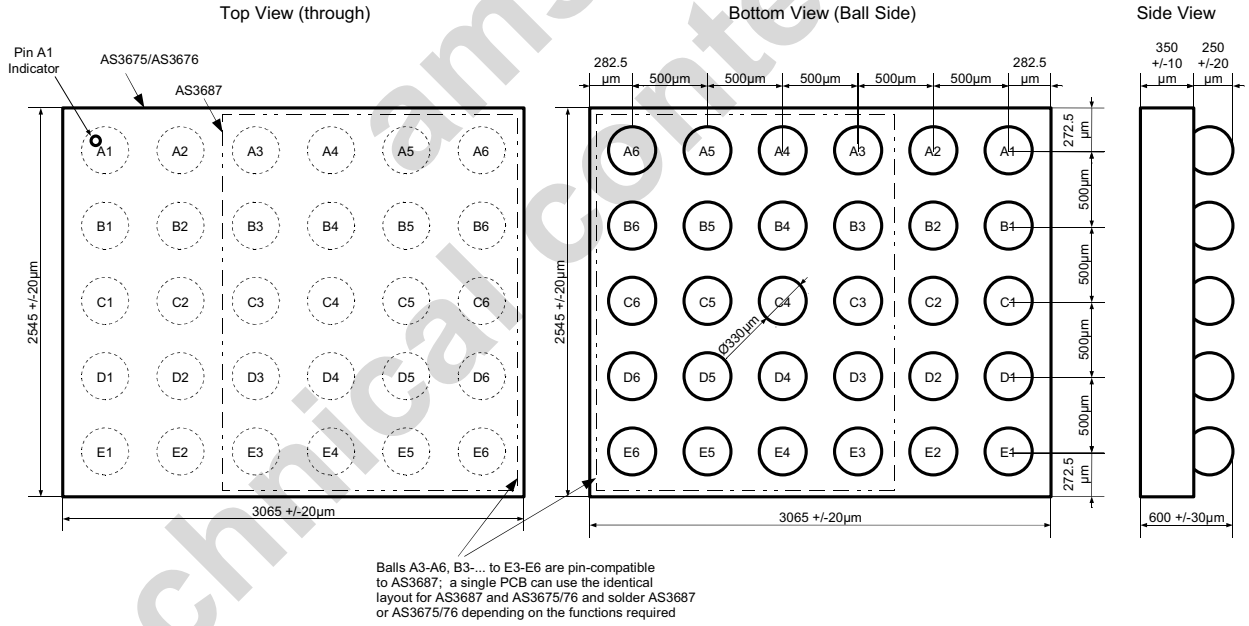
Figure 42. WL-CSP30 3x2.5mm 6x5 Balls Package Drawing



Note:

Line 1: austriamicrosystems logo
Line 2: AS3676
Line 3: <Code>
Encode datecode 4 characters

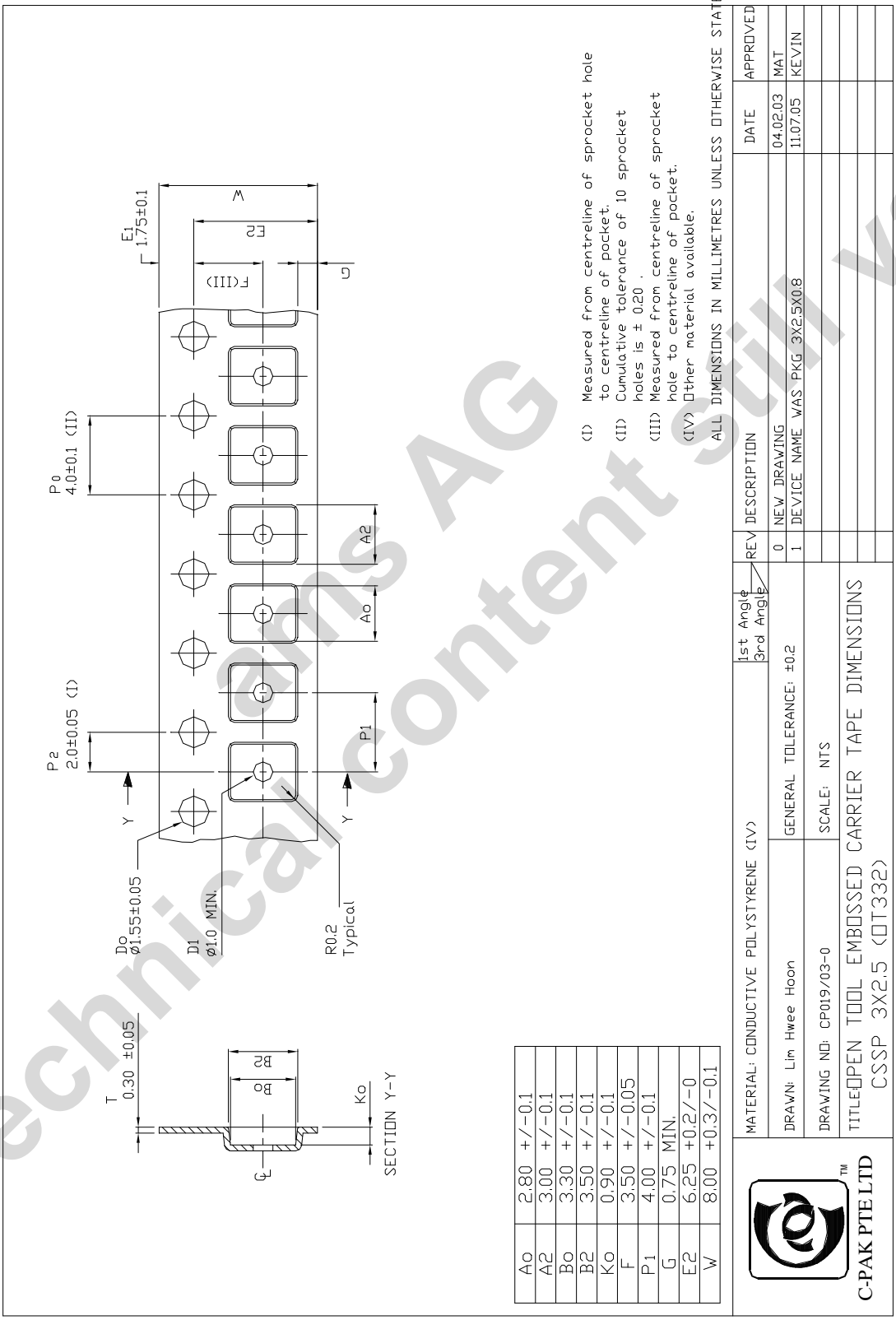
Figure 43. WL-CSP30 3x2.5mm 6x5 Balls Detail Dimensions



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11.1 Tape & Reel Information

Figure 44. Tape & Reel Dimensions



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12 Ordering Information

The devices are available as the standard products shown in Table 123.

Table 123. Ordering Information

Model	Description	Delivery Form	Package
AS3676-ZWLT	AS3676 Wafer Level Chip Scale Package, size 3x2.5mm, 6x5 balls, 0.5mm pitch, Pb-Free	Tape & Reel	30pin WL-CSP (3x2.5mm) RoHS compliant / Pb-Free

Note: All products are RoHS compliant and austriamicrosystems green.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

Technical support is found at http://www.austriamicrosystems.com/Technical-Support
For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

Note: AS3676-ZWLT

AS3676-
- Z Temperature Range: -30ºC - 85ºC
- WL Package: Wafer Level Chip Scale Package (WL-CSP) 3x2.5mm
- T Delivery Form: Tape & Reel

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