# ATP Industrial Grade mSATA Embedded Module Specification

Version 1.2

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## Revision History

| Date | Version | Changes compared to previous issue |
|---|---|---|
| Dec. 15th, 2011 | 1.0 | - First release |
| Jan. 12th, 2012 | 1.1 | - Updated SSD endurance data |
| Aug. 6th, 2012 | 1.2 | - Added Static Data Refresh feature |

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# 1 Introduction

## 1.1 Product Overview

The ATP industrial grade mSATA Embedded Module is a high performance and high capacity mass storage solution. It provides outstanding performance and proven reliability for products operating.

ATP industrial grade mSATA Embedded Module is perfect for thin devices, especially networking, thin clients and embedded appliance and also suit for enterprise storage systems with outstanding sequential read and write performance to relieve performance bottlenecks associated with traditional rotating media HDD storage.

## 1.2 Main Features

- Capacities: 4GB to 64GB
- SLC (Single Level Cell) NAND flash memory
- Operating temperature: -40℃ to 85℃
- Maximum performance: Sequential read up to 258MB/s, sequential write up to 220MB/s
- JEDEC standard: MO-300A (mSATA)
- Slim form factor for design in thin devices, especially networking, thin clients and embedded appliance.
- Secure erase drive protection.
- Extensive application for storage
- Compliant with Serial ATA Revision 2.6.
- Support PIO mode 0~4, MDMA mode 0~2,UDMA mode 0~6
- Compatible with SATA 1.5Gbps and SATA 3.0Gbps interface rates
- SMART function support by ATA CMD
- ATP SMART tool for Windows 2000/XP/Vista/7 and Linux.
- Support TRIM command (Windows 7 and up, latest Linux Kernel), Off-line TRIM utility available for Windows XP/2000/2003/Vista
- Enhanced endurance by Global wear-leveling
- Static data refresh feature
- PowerProtector, data integrity under power-cycling
- RoHS compliant
- CE , FCC certification

# 2 Product Specification

## 2.1 Product Image


## 2.2 Product Capacities

Table 2-1

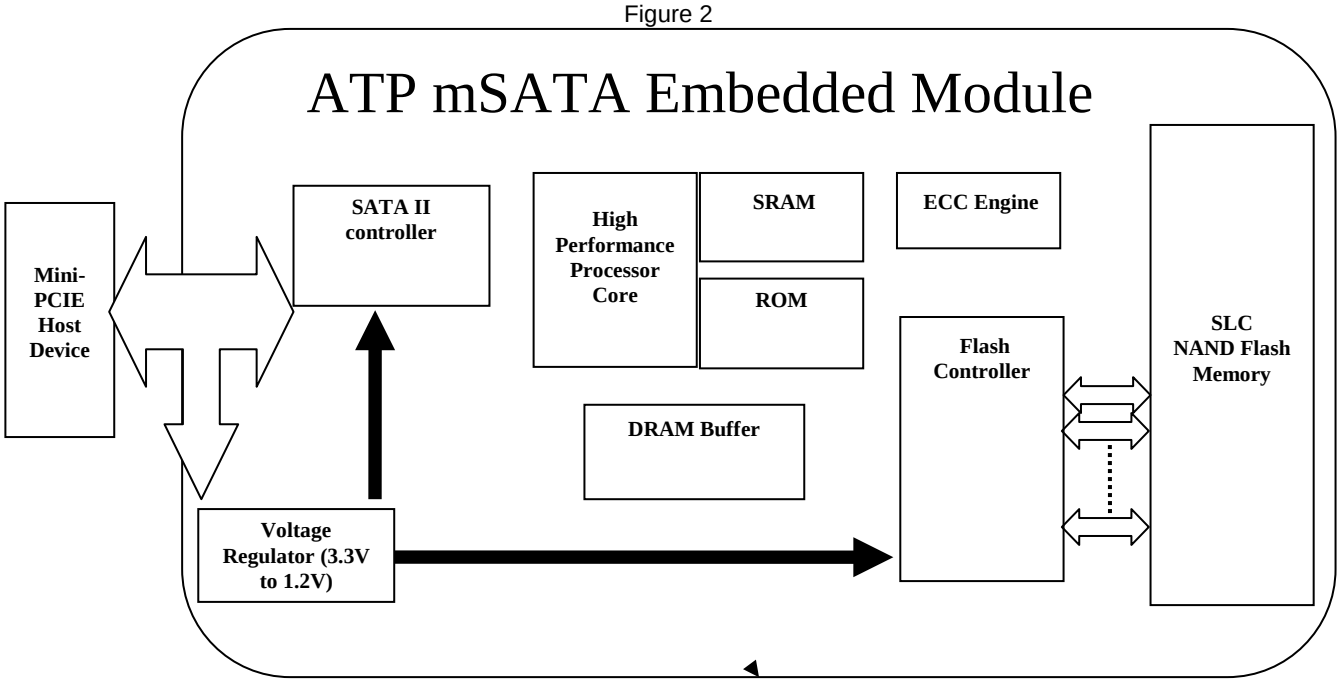
| ATP P/N | CAPACITY |
|---|---|
| AF4GSSHI-OAAXP | 4GB |
| AF8GSSHI-OAAXP | 8GB |
| AF16GSSHI-OAAXP | 16GB |
| AF32GSSHI-OAAXP | 32GB |
| AF64GSSHI-OAAXP | 64GB |

Notes:
1GB = 1,000,000,000 Byte

## 2.3 Block Diagram

ATP industrial grade mSATA Embedded Module consists of below functional blocks. The advanced architecture is optimized to provide highest data reliability and transfer performance.

Figure 2



## 2.4 Performance

### 2.4.1 IOPS

Table 2-2

| Type | Value |
|---|---|
| 4K Random Read IOPS | 4,700 IOPS |

Notes: IOPS: Input/Output Operations per Second

### 2.4.2 Read/Write Performance

Table 2-3

| Type | Value |
|---|---|
| Host Interface Speed | SATA 1.5Gb/s and SATA 3.0 Gb/s |
| Data Transfer Rate[1] | Sequential Read: up to 258MB/s |
| | Sequential Write: up to 220MB/s |

Notes:

The performance may vary according to different product capacity.

## 2.5 Electrical Characteristics

### 2.5.1 Supply Voltage

Table 2-4

| Parameter | Symbol | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 3.15 | 3.3 | 3.45 | V | |

### 2.5.2 System Power Requirement

Table 2-5

| Parameter | Symbol | Min | Typ | Max | Unit | Remark |
|---|---|---|---|---|---|---|
| Sustained write power | $P_W$ | - | 1.40 | - | W | RMS value |
| Sustained read power | $P_R$ | - | 1.00 | - | W | RMS value |
| Idle power | $P_S$ | - | 0.45 | - | W | RMS value |

## 2.6 Environment Specifications

### 2.6.1 Temperature and Humidity

Table 2-6

| Type | | Value |
|---|---|---|
| Temperature | Operating | -40°C to 85°C |
| | Non-Operating | -45°C to 85°C |
| Humidity | Operating | 25°C， 8% to 95%, noncondensing |
| | Non-Operating | 40°C， 8% to 93%, noncondensing |

### 2.6.2 Vibration and Shock

Table 2-7

| Type | | Value |
|---|---|---|
| Vibration | Operating | sine 16.4G, 10~2000Hz |
| Shock | Operating | Half sine 1500G/0.5ms |

### 2.6.3 Altitude

Table 2-8

| Type | | Value |
|---|---|---|
| Altitude | Operating | 80,000 feet Max. |
| | Non-Operating | 80,000 feet Max. |

## 2.7 MTBF

Table 2-9

| Type | Value |
|---|---|
| MTBF (@ 25°C) [1] | 4GB: 1,080,000 hours<br>8GB: 1,060,000 hours<br>16GB: 1,030,000 hours<br>32GB: 1,000,000 hours<br>64GB: 1,000,000 hours |

Notes:

The Mean Time between Failures (MTBF) is calculated using a prediction methodology, Telcordia SR-332, which based on reliability data of the individual components in the mSATA. It assumes nominal voltage, with all other parameters within specified range.

## 2.8 Write/Erase Endurance

Table 2-10

| Type | Value |
|---|---|
| Endurance Technology | Enhanced global dynamic and static wear-leveling algorithm<br>SLC flash block: 100,000 program/erase cycles |
| SSD Endurance | 4GB: 40 terabyte random write<br>80 terabyte sequential write<br>8GB: 80 terabyte random write<br>160 terabyte sequential write<br>16GB: 160 terabyte random write<br>320 terabyte sequential write<br>32GB: 320 terabyte random write<br>640 terabyte sequential write<br>64GB: 640 terabyte random write<br>1,280 terabyte sequential write |

Note:

Endurance for the mSATA module can be predicted based on the usage conditions applied to the device, the internal NAND component cycles, the write amplification factor, and the wear leveling efficiency of the drive.

## 2.9 Certification

Table 2-11

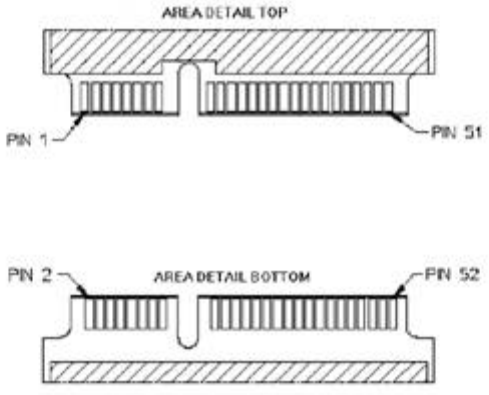
| Mark/Approval | Documentation | Compliant |
|---|---|---|
|  | The CE marking (also known as CE mark) is a mandatory conformance mark on many products placed on the single market in the European Economic Area (EEA). The CE marking certifies that a product has met EU consumer safety, health or environmental requirements. CE stands for Conformité Européenne, "European conformity" in French. | Yes |
|  | FCC Part 15 Class B was used for Evolution of United States (US) Emission Standards for Commercial Electronic Products, The United States (US) covers all types of unintentional radiators under Subparts A and B (Sections 15.1 through 15.199) of FCC 47 CFR Part 15, usually called just FCC Part 15 | Yes |
|   | RoHS is the acronym for Restriction of Hazardous Substances. RoHS, also known as Directive 2002/95/EC, originated in the European Union and restricts the use of specific hazardous materials found in electrical and electronic products. All applicable products in the EU market after July 1, 2006 must pass RoHS compliance. For the complete directive, see Directive 2002/95/EC of the European Parliament. | Yes |

# 3 SATA Embedded Module Pin Assignment

## 3.1 Pin Location

The following figure shows the pin location of the mSATA embedded module, the connector is with both signal and power segments

Figure 3



## 3.2 Pin Assignments

There are total of 52 pins, the pin definitions are shown in Table 3-1

Table 3-1

| Pin No. | Function | Description |
|---|---|---|
| P1 | Reserved | No Connect |
| P2 | +3.3V | 3.3V Source |
| P3 | Reserved | No Connect |
| P4 | GND | Return Current Path |
| P5 | Reserved | No Connect |
| P6 | +1.5V | Not used in ATP design |
| P7 | Reserved | No Connect |
| P8 | Reserved | No Connect |
| P9 | GND | Return Current Path |
| P10 | Reserved | No Connect |
| P11 | Reserved | No Connect |
| P12 | Reserved | No Connect |
| P13 | Reserved | No Connect |
| P14 | Reserved | No Connect |
| P15 | GND | Return Current Path |
| P16 | Reserved | No Connect |
| P17 | Reserved | No Connect |
| P18 | GND | Return Current Path |
| P19 | Reserved | No Connect |
| P20 | Reserved | No Connect |
| P21 | GND | Return Current Path |
| P22 | Reserved | No Connect |
| P23 | +B | Host Receiver Differential Signal Pair |
| P24 | +3.3V | 3.3V Source |
| P25 | -B | Host Receiver Differential Signal Pair |
| P26 | GND | Return Current Path |
| P27 | GND | Return Current Path |
| P28 | +1.5V | Not used in ATP design |
| P29 | GND | Return Current Path |
| P30 | Two Wire Interface | Two Wire interface Clock[3] |
| P31 | +A | Host Transmitter Differential Signal Pair |
| P32 | Two Wire Interface | Two Wire interface Data[3] |
| P33 | -A | Host Transmitter Differential Signal Pair |
| P34 | GND | Return Current Path |
| P35 | GND | Return Current Path |
| P36 | Reserved | No Connect |
| P37 | GND | Return Current Path |
| P38 | Reserved | No Connect |

| Pin No. | Function | Description |
|---|---|---|
| P39 | +3.3V | 3.3V Source |
| P40 | GND | Return Current Path |
| P41 | +3.3V | 3.3V Source |
| P42 | Reserved | No Connect |
| P43 | GND | Return Current Path |
| P44 | Reserved | No Connect |
| P45 | Vender | Not used in ATP design [2] |
| P46 | Reserved | No Connect |
| P47 | Vender | Not used in ATP design [2] |
| P48 | +1.5V | Not used in ATP design |
| P49 | DA/DSS | Device Activity Signal / Disable Staggered Spin-up |
| P50 | GND | Return Current Path |
| P51 | Presence Detection | Shall be pulled to GND by device[1] |
| P52 | +3.3V | 3.3V Source |

Notes:
1. Presence detection pin provided for tamper proof functionality
2. No connect on the host side.
3. Pins 30 and 32 are intended for use as a two wire interface to read a memory device to determine device information (an example of this would be for use as SMB bus pins). These pins are not designed to be active in conjunction with the SATA signal differential pairs. Not used in ATP design.

# 4 Command Sets

## 4.1 ATA Command Set

ATP industrial grade mSATA Embedded module support the commands show in the following table

Table 4-1

| Command | Code | Protocol |
|---|---|---|
| General Feature Set | | |
| Execute Drive Diagnostic | 90h | Device diagnostic |
| Flush Cache | E7h | Non-data |
| Identify Device | ECh | PIO data-in |
| Read DMA | C8h | DMA |
| Read Multiple | C4h | PIO data-in |
| Read Sector(s) | 20h | PIO data-in |
| Read Verify Sector(s) | 40h or 41h | Non-data |
| Set Feature | EFh | Non-data |
| Set Multiple Mode | C6h | Non-data |
| Write DMA | CAh | DMA |
| Write Multiple | C5h | PIO data-out |
| Write Sector(s) | 30h | PIO data-out |
| NOP | 00h | Non-data |
| Read Buffer | E4h | PIO data-in |
| Write Buffer | E8h | PIO data-out |
| Power Management Feature Set | | |
| Check Power Mode | E5h or 98h | Non-data |
| Idle | E3h or 97h | Non-data |
| Idle Immediate | E1h or 95h | Non-data |
| Sleep | E6h or 99h | Non-data |
| Standby | E2h or 96h | Non-data |
| Standby Immediate | E0h or 94h | Non-data |
| Security Mode Feature Set | | |
| Security Set Password | F1h | PIO data-out |
| Security Unlock | F2h | PIO data-out |
| Security Erase Prepare | F3h | Non-data |
| Security Erase Unit | F4h | PIO data-out |
| Security Freeze Lock | F5h | Non-data |
| Security Disable Password | F6h | PIO data-out |
| SMART Feature Set | | |
| SMART Disable Operation | B0h | Non-data |
| SMART Enable/Disable Autosave | B0h | Non-data |
| SMART Enable Operations | B0h | Non-data |
| SMART Return Status | B0h | Non-data |
| SMART Execute Off-Line Immediate | B0h | Non-data |

| Command | Code | Protocol |
|---|---|---|
| SMART Read Data | B0h | PIO data-in |
| Host Protected Area Feature Set | | |
| Read Native Max Address | F8h | Non-data |
| Set Max Address | F9h | Non-data |
| Set Max Set Password | F9h | PIO data-out |
| Set Max Lock | F9h | Non-data |
| Set Max Freeze Lock | F9h | Non-data |
| Set Max Unlock | F9h | PIO data-out |

## 4.2 Identify Device Data

Table 4-2

| Word Address | Default Value | Total Bytes | Data Field Type Information |
|---|---|---|---|
| 0 | 044Ah | 2 | General Configuration |
| 1 | XXXXh | 2 | Default number of cylinders |
| 2 | 0000h | 2 | Reserved |
| 3 | 00XXh | 2 | Default number of heads |
| 4 | 0000h | 2 | Obsolete |
| 5 | 0240h | 2 | Obsolete |
| 6 | XXXXh | 2 | Default number of sectors per track |
| 7-8 | XXXXh | 4 | Number of sectors per card (Word 7 = MSW, Word 8 = LSW) |
| 9 | 0000h | 2 | Obsolete |
| 10-19 | XXXXh | 20 | Serial number in ASCII (Right justified) |
| 20 | 0002h | 2 | Obsolete |
| 21 | 0002h | 2 | Obsolete |
| 22 | 0000h | 2 | Obsolete |
| 23-26 | XXXXh | 8 | Firmware revision in ASCII. Big Endian Byte Order in Word |
| 27-46 | XXXXh | 40 | Model number in ASCII (Left justified) Big Endian Byte Order in Word |
| 47 | 8001h | 2 | Maximum number of sectors on Read/Write Multiple command |
| 48 | 0000h | 2 | Reserved |
| 49 | 0F00h | 2 | Capabilities |
| 50 | 4000h | 2 | Capabilities |
| 51 | 0200h | 2 | PIO data transfer cycle timing mode |
| 52 | 0000h | 2 | Obsolete |
| 53 | 0007h | 2 | Field validity |
| 54 | XXXXh | 2 | Current numbers of cylinders |
| 55 | XXXXh | 2 | Current numbers of heads |
| 56 | XXXXh | 2 | Current sectors per track |
| 57-58 | XXXXh | 4 | Current capacity in sectors (LBAs) (Word57=LSW, Word58=MSW) |
| 59 | 0100h | 2 | Multiple sector setting |

| Word Address | Default Value | Total Bytes | Data Field Type Information |
|---|---|---|---|
| 60-61 | XXXXh | 4 | Total number of sectors addressable in LBA Mode (Word60=LSW, Word61=MSW) |
| 62 | 0000h | 2 | Reserved |
| 63 | 0007h | 2 | Multiword DMA transfer |
| 64 | 0003h | 2 | Advanced PIO modes supported |
| 65 | 0078h | 2 | Minimum Multiword DMA transfer cycle time per word |
| 66 | 0078h | 2 | Recommended Multiword DMA transfer cycle time |
| 67 | 0078h | 2 | Minimum PIO transfer cycle time without flow control |
| 68 | 0078h | 2 | Minimum PIO transfer cycle time with lORDY flow control |
| 69~75 | 0000h | 20 | Reserved |
| 76 | 0060h | 2 | Serial ATA capabilities<br>Support Serial ATA Gen1<br>Support Serial ATA Gen2 |
| 77~79 | 0000h | 6 | Reserved |
| 80 | 0080h | 2 | Major version number (ATAPI-7) |
| 81 | 0000h | 2 | Minor version number |
| 82 | 742Bh | 2 | Command sets supported 0 |
| 83 | 5500h | 2 | Command sets supported 1 |
| 84 | 4002h | 2 | Command sets supported 2 |
| 85~87 | XXXXh | 6 | Command set/feature enabled |
| 88 | 007Fh | 2 | Ultra DMA supported and selected |
| 89 | 0003h | 2 | Time required for Security erase unit completion |
| 90 | 0000h | 2 | Time required for Enhanced security erase unit completion |
| 91 | 0000h | 2 | Current Advanced power management value |
| 92 | FFFEh | 2 | Master Pasword Revision Code |
| 93~127 | 0000h | 70 | Reserved |
| 128 | 0001h | 2 | Security status |
| 129~159 | 0000h | 62 | Vendor unique bytes |
| 160 | 0000h | 2 | Power requirement description |
| 161 | 0000h | 2 | Reserved |
| 162 | 0000h | 2 | Key management schemes supported |
| 163 | 0000h | 2 | CFA True lDE Timing Mode Capability and Setting |
| 164 | 0000h | 2 | Reserved |
| 165~175 | 0000h | 22 | Reserved |
| 176~216 | 0000h | 82 | Reserved |
| 217 | 0100h | 2 | Non-rotating media(SSD) |
| 218~255 | 0000h | 76 | Reserved |

## 4.3 SMART Information

ATP industrial grade mSATA Embedded Module Support S.M.A.R.T. ATA feature set in IDE mode, not support in RAID mode and AHCI mode

### 4.3.1 SMART subcommand sets

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Function Set command. The subcommands are listed below.

Table 4-3

| Command | Command Code |
|---|---|
| SMART READ DATA | D0h |
| SMART SAVE ATTRIBUTE THRESHOLD | D1h |
| SMART ENABLE/DISABLE AUTOSAVE | D2h |
| SMART SAVE ATTRIBUTE VALUES | D3h |
| SMART EXECUTE OFF-LINE IMMIDIATE | D4h |
| RESERVED | D5h |
| RESERVED | D6h |
| SMART ENABLE OPERATIONS | D8h |
| SMART DISABLE OPERATIONS | D9h |
| SMART RETURN STATUS | DAh |

Note:
If the reserved size is below a threshold, status can be read from the Cylinder Register using the Return Status command (DAh)

### 4.3.2 SMART Read Data (subcommand D0h)

The following 512 bytes make up the device SMART data structure. Users can obtain the data using the “Read Data” command (D0h).

Table 4-4

| Byte | F/V | Description |
|---|---|---|
| 0~1 | X | Revision code |
| 2~361 | X | Vendor Specific |
| 362 | V | Off-line data collection status |

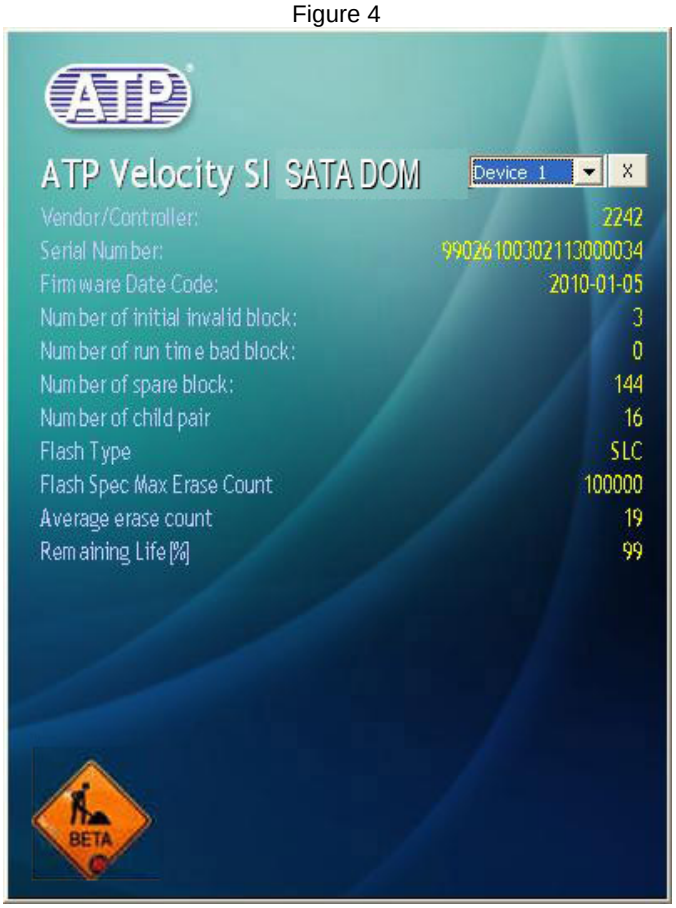
| Byte | F/V | Description |
|---|---|---|
| 363 | X | Self-test execution status byte |
| 364~365 | V | Total time in seconds to complete off-line data collection activity |
| 366 | X | Vendor Specific |
| 367 | F | Off-line data collection capability |
| 368~369 | F | SMART capability |
| 370 | F | Error logging capability：7-1 Reserved<br>0 -1 = Device error logging supported |
| 371 | X | Vendor Specific |
| 372 | F | Short self-test routine recommended polling time(in minutes) |
| 373 | F | Extended self-test routine recommended polling time(in minutes) |
| 374 | F | Conveyance self-test routine recommended polling time(in minutes) |
| 375~385 | R | Reserved |
| 386~395 | F | Firmware Version/Date Code |
| 396~397 | F | Number of initial invalid block (396=MSB, 397=LSB) |
| 398~399 | V | Number of run time bad block (398=MSB, 399=LSB) |
| 400~406 | F | SMI2242 |
| 407~415 | X | Vendor specific |
| 416 | F | Reserved |
| 417 | F | Program/write the strong page only |
| 418~419 | V | Number of spare block |
| 420 | F | Reserved |
| 421~423 | V | Average erase count |
| 424~425 | V | Number of child pair |
| 426~428 | V | Maximum erase count |
| 429~431 | V | Minimum erase count |
| 432~445 | F | Reserved |
| 446~510 | X | Vendor specific |
| 511 | V | Data structure checksum |

Notes:
F=content (byte) is fixed and does not change
V=content (byte) is variable and maybe change depending on the state of the device or the command executed by the device
X= content (byte) is vendor specific and maybe fixed or variable
R=content (byte) is reserved and shall be zero

### 4.3.3 ATP SMART Tool

ATP provides SMART Tool for Windows 2000/XP/Vista/7 and Linux, it can monitor the state of mSATA Embedded module, the following picture shows SMART tool operation. This tool supports that users read spare and bad block information. Users can thus evaluate drive health at run time and receive an early warning before the drive life ends.

Figure 4



# 5 Mechanical Information

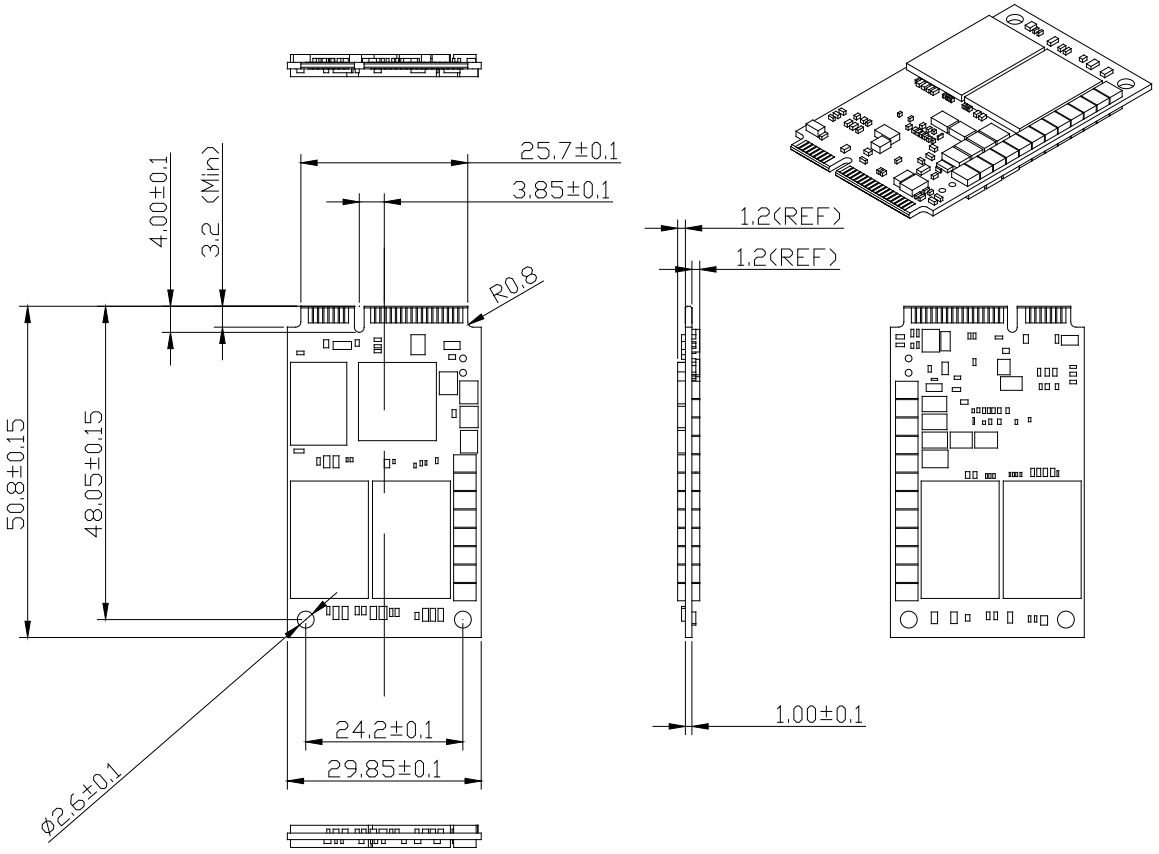
## 5.1 Physical Dimension Specifications

Table 5-1

| Type | | Value |
|---|---|---|
| mSATA Embedded module | Length | 50.80 mm +/- 0.15mm |
| | Width | 29.85mm +/- 0.1mm |
| | Thickness | 3.40mm +/- 0.1mm |

## 5.2 Mechanical Form Factor (Units in mm)

Figure 5




# 6 Appendix