## Product List

**MSU2031L16**, low working voltage 16 MHz ROM less MCU
**MSU2031S16**, small sink current 16 MHz ROM less MCU
**MSU2031C16**, 16 MHz ROM less MCU
**MSU2031C25**, 25 MHz ROM less MCU
**MSU2031C40**, 40 MHz ROM less MCU

**MSU2051L16**, low working voltage 16 MHz 4 KB internal ROM MCU
**MSU2051S16**, small sink current 16 MHz 4 KB internal ROM MCU
**MSU2051C16**, 16 MHz 4 KB internal ROM MCU
**MSU2051C25**, 25 MHz 4 KB internal ROM MCU
**MSU2051C40**, 40 MHz 4 KB internal ROM MCU

## Description

The MVI MSU2051 series product is an 8 - bit single chip microcontroller. It provides hardware features and a powerful instruction set, necessary to make it a versatile and cost effective controller for those applications demand up to 32 I/O pins or need up to 64 K byte external memory either for program or for data or mixed.
A serial input / output port is provided for I/O expansion, Inter - processor communications, and full duplex UART.

## Ordering Information

MSU2031ihhk
MSU2051ihh - yyyk

i: process identifier {S, L, C}.
hh: working clock in MHz {16, 25, 40}.
yyy: production code {001, ..., 999}
k: package type postfix {as below table}.

| Postfix | Package | Pin/Pad Configuration | Dimension | Logo Size at Top Marking |
|---|---|---|---|---|
| blank | dice | page 18 | page 18 | - |
| P | 40L PDIP | page 2 | page 14 | 5.0 x 4.2 mm |
| J | 44L PLCC | page 2 | page 15 | 4.5 x 3.8 mm |
| Q | 44L PQFP | page 2 | page 16 | 2.8 x 2.4 mm |
| U | 44L LQFP | page 2 | page 17 | 2.8 x 2.4 mm |

## Features

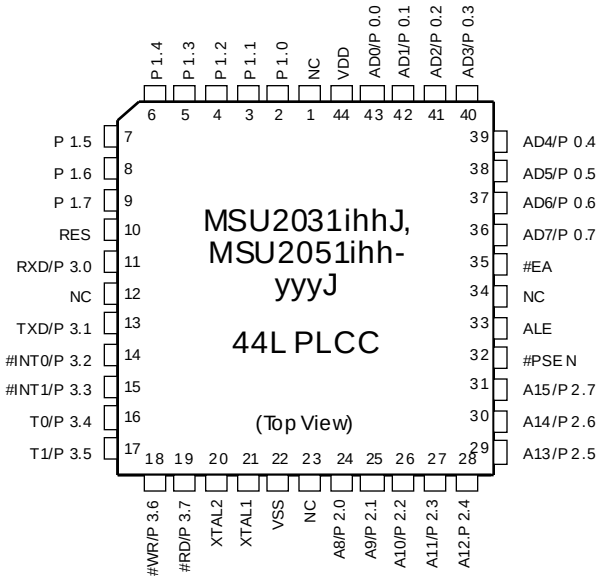
- Working voltage : L series at 2.7V through 4.5V while S & C series at 4.5 V through 5.5 V
- General 80C51 family compatible
- 64 K byte External Memory Space
- 4 K byte ROM
- 128 byte data RAM
- Two 16 bit Timers/Counters
- Four 8-bit I/O ports
- Full duplex serial channel
- Bit operation instructions
- Page free jumps
- 8 - bit Unsigned Division
- 8 - bit Unsigned Multiply
- BCD arithmatic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes: Idle mode and Power down mode
- Working at 16/25/40 MHz Clock

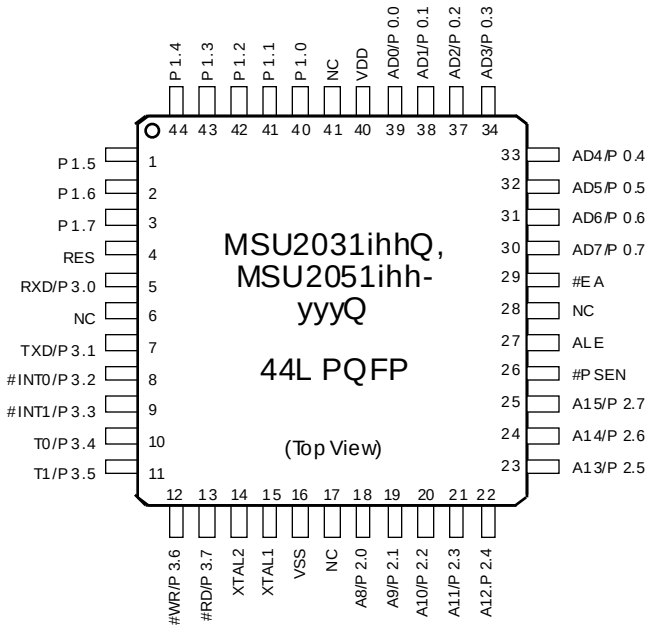
## Cross Reference

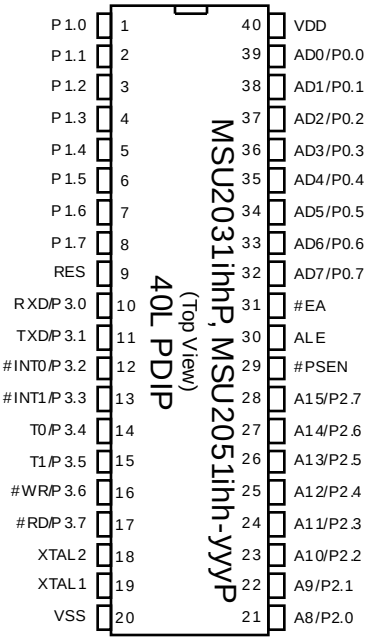
| M.V.I. | MSU2051 | MSU2031 |
|---|---|---|
| W.B. | W78C51 | W78C31 |
| Philips | 80C51 | 80C31 |
| L.G. | GMS80C501 | GMS80C301 |
| Intel | 80C51 | 80C31 |
| CCL. itri | CIC80510 | - - - - - |
| Atmel | AT80C51 | AT80C31 |

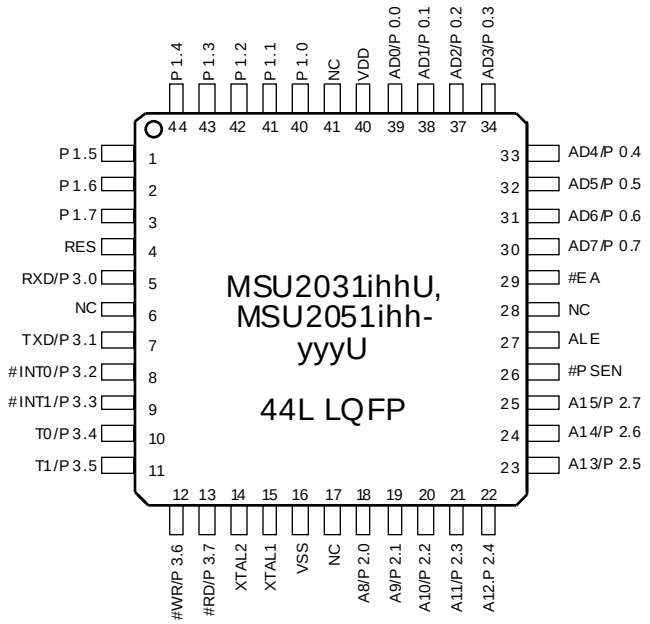
Specifications subject to change without notice, contact your sales representatives for the most recent information.

## Pin Configurations

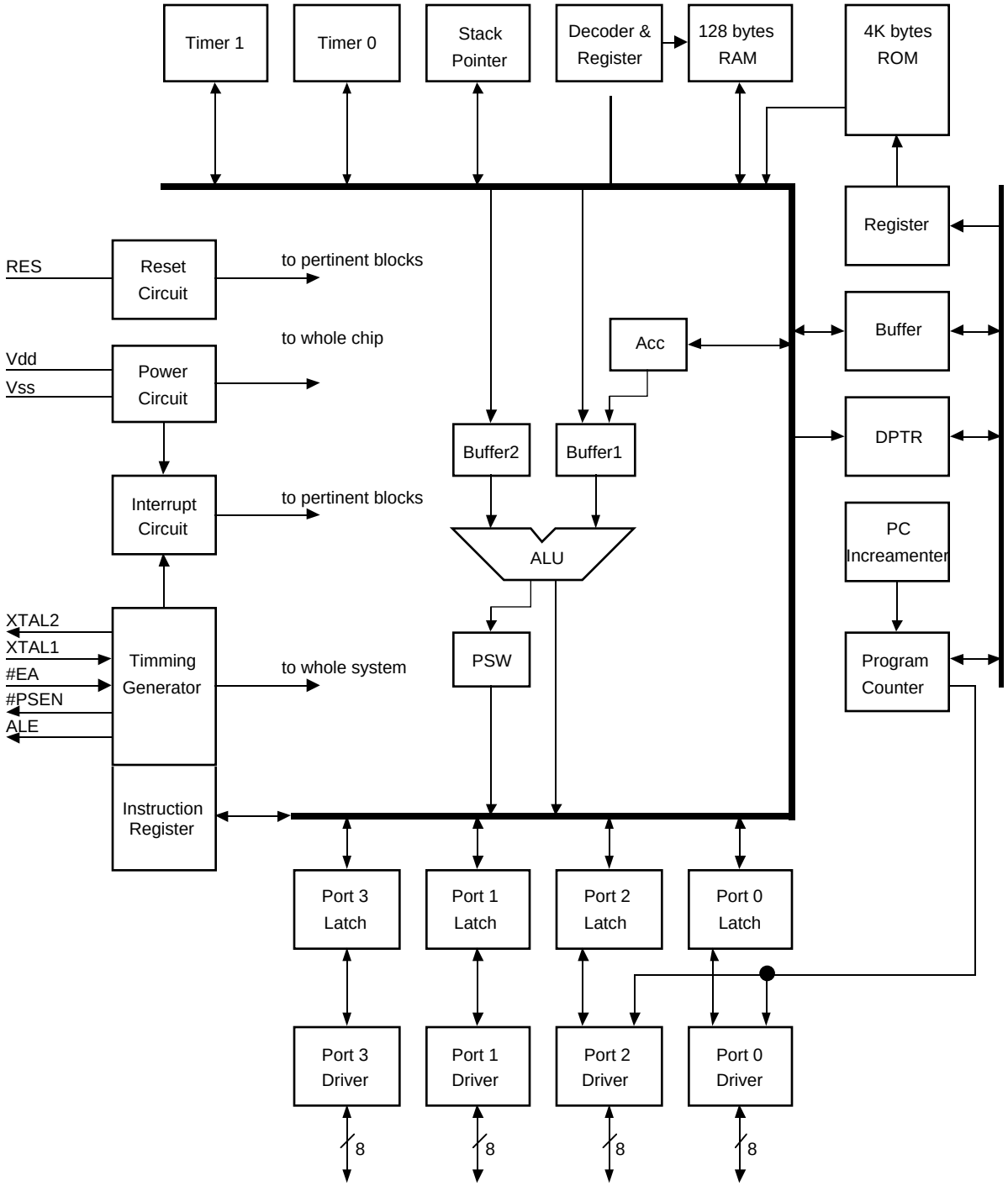


## Block Diagram



## Pin Descriptions

| 40 PDIP Pin# | Dice Pad# | 44 LQFP Pin# | 44 PQFP Pin# | 44 PLCC Pin# | Symbol | Active | I/O | Names |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 40 | 40 | 2 | P1.0 | | i/o | bit 0 of Port 1 |
| 2 | 2 | 41 | 41 | 3 | P1.1 | | i/o | bit 1 of Port 1 |
| 3 | 3 | 42 | 42 | 4 | P1.2 | | i/o | bit 2 of Port 1 |
| 4 | 4 | 43 | 43 | 5 | P1.3 | | i/o | bit 3 of Port 1 |
| 5 | 5 | 44 | 44 | 6 | P1.4 | | i/o | bit 4 of Port 1 |
| 6 | 6 | 1 | 1 | 7 | P1.5 | | i/o | bit 5 of Port 1 |
| 7 | 7 | 2 | 2 | 8 | P1.6 | | i/o | bit 6 of Port 1 |
| 8 | 8 | 3 | 3 | 9 | P1.7 | | i/o | bit 7 of Port 1 |
| 9 | 9 | 4 | 4 | 10 | RES | | i | Reset |
| 10 | 10 | 5 | 5 | 11 | RXD/P3.0 | | i/o | bit 0 of Port 3 & Receive data |
| 11 | 11 | 7 | 7 | 13 | TXD/P3.1 | | i/o | bit 1 of Port 3 & Transmit data |
| 12 | 12 | 8 | 8 | 14 | #INT0/P3.2 | L/- | i/o | bit 2 of Port 3 & low true Interrupt 0 |
| 13 | 13 | 9 | 9 | 15 | #INT1/P3.3 | L/- | i/o | bit 3 of Port 3 & low true Interrupt 1 |
| 14 | 14 | 10 | 10 | 16 | T0/P3.4 | | i/o | bit 4 of Port 3 & Timer 0 |
| 15 | 15 | 11 | 11 | 17 | T1/P3.5 | | i/o | bit 5 of Port 3 & Timer 1 |
| 16 | 16 | 12 | 12 | 18 | #WR/P3.6 | L/- | i/o | bit 6 of Port 3 & Write (low enable) |
| 17 | 17 | 13 | 13 | 19 | #RD/P3.7 | L/- | i/o | bit 7 of Port 3 & Read (low enable) |
| 18 | 18 | 14 | 14 | 20 | XTAL2 | | o | Crystal out |
| 19 | 19 | 15 | 15 | 21 | XTAL1 | | i | Crystal in |
| 20 | 20-22 | 16 | 16 | 22 | VSS | | | Sink Voltage, Ground |
| 21 | 23 | 18 | 18 | 24 | A8/P2.0 | | i/o | bit 0 of Port 2 & Address 8 |
| 22 | 24 | 19 | 19 | 25 | A9/P2.1 | | i/o | bit 1 of Port 2 & Address 9 |
| 23 | 25 | 20 | 20 | 26 | A10/P2.2 | | i/o | bit 2 of Port 2 & Address 10 |
| 24 | 26 | 21 | 21 | 27 | A11/P2.3 | | i/o | bit 3 of Port 2 & Address 11 |
| 25 | 27 | 22 | 22 | 28 | A12/P2.4 | | i/o | bit 4 of Port 2 & Address 12 |
| 26 | 28 | 23 | 23 | 29 | A13/P2.5 | | i/o | bit 5 of Port 2 & Address 13 |
| 27 | 29 | 24 | 24 | 30 | A14/P2.6 | | i/o | bit 6 of Port 2 & Address 14 |
| 28 | 30 | 25 | 25 | 31 | A15/P2.7 | | i/o | bit 7 of Port 2 & Address 15 |
| 29 | 31 | 26 | 26 | 32 | #PSEN | L | o | Program store enable (low enable) |
| 30 | 32 | 27 | 27 | 33 | ALE | H | o | Address latch enable |
| 31 | 33 | 29 | 29 | 35 | #EA | L | i | External access first 4K memory |
| 32 | 34 | 30 | 30 | 36 | AD7/P0.7 | | i/o | bit 7 of Port 0 & Address or Data 7 |
| 33 | 35 | 31 | 31 | 37 | AD6/P0.6 | | i/o | bit 6 of Port 0 & Address or Data 6 |
| 34 | 36 | 32 | 32 | 38 | AD5/P0.5 | | i/o | bit 5 of Port 0 & Address or Data 5 |
| 35 | 37 | 33 | 33 | 39 | AD4/P0.4 | | i/o | bit 4 of Port 0 & Address or Data 4 |
| 36 | 38 | 34 | 34 | 40 | AD3/P0.3 | | i/o | bit 3 of Port 0 & Address or Data 3 |
| 37 | 39 | 35 | 35 | 41 | AD2/P0.2 | | i/o | bit 2 of Port 0 & Address or Data 2 |
| 38 | 40 | 36 | 36 | 42 | AD1/P0.1 | | i/o | bit 1 of Port 0 & Address or Data 1 |
| 39 | 41 | 37 | 37 | 43 | AD0/P0.0 | | i/o | bit 0 of Port 0 & Address or Data 0 |
| 40 | 42,43 | 38 | 38 | 44 | VDD | | | Drive Voltage, +3 Vcc (or +5 Vcc) |

## Pin Descriptions

**Vss**
Circuit ground potential.

**VDD**
+3V (or +5 V) power supply during operation.

**PORT 0**
Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory.

**PORT 1**
Port 1 is an 8-bit quasi-bidirectional I/O port with internal pull-up resistance.

**PORT 2**
Port 2 is an 8-bit quasi-bidirectional I/O port with internal pull-up resistance. It also emit the high-order address byte when accessing external memory.

**PORT 3**
Port 3 is an 8-bit quasi-bidirectinal I/O port with internal pull-up resistance. It also contains the interrupt, timer, serial port and #RD as well as #WR pins that are used by various options. The output latch corresponding to a secondary function must be programmed to one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:
- RXD/data (P3.0). Serial port's transmitter data output (asynchronous) or data input/output (asynchronous).
- TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or data output (asynchronous).
- #INT0 (P3.2). Interrupt 0 input or gate control input for counter 0.
- #INT1 (P3.3). Interrupt 1 input or gate control input for counter 1.
- T0 (P3.4). Input to counter 0.
- T1 (P3.4). Input to counter 1.
- #WR (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory.
- #RD (P3.7). The read control signal enables External Data Memory to Port 0.

**RES**
A high on this pin for two machine cycles (24 clocks) while the oscillator is running, resets the device. The data in RAM is preserved when reset signals - reset does not clear the data in RAM.

**ALE**
Provides Address Latch Enable output used for latching the address into external memory during normal operation.

**#PSEN**
The Program Store Enable output is a control signal that enables the external Program Memory to the bus during normal fetch operations.

**#EA**
When held at a TTL high level, the MSU2051 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the MSU2051 fetches all instuctions from external Program Memory.

**XTAL 1**
Input to the oscillator's high gain amplifier. A crystal or external source can be used.

**XTAL 2**
Output from the oscillator's amplifier. Required when a crystal is used.

## Terms

**Idle Mode**
During idle mode, the CPU is stopped but below blocks are kept functioning: clock generator, RAM, timer/ counters, serial port and interrupt block. To save power consumption, user's software program can invoke this mode. The on-chip data RAM retains the values during this mode, but the processor stops executing instructions. In Idle mode (IDL=1), the oscillator continues to run and the interrput, and timer blocks continue to be clocked but the clock signal is gated off to the CPU. The activities of the CPU no longer exist unless waiting for an interrupt request.
-An instruction that sets flag (PCON.0) causes that to be the last instruction executed before going into the Idle Mode.
-In the Idle Mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer function.
-The CPU status is entirely preserved in its:
the Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data during Idle mode.
-There are three ways to terminate the Idle Mode.
1) By interrupt
Activation of any enabled interrupt will cause flag (PCON.0) to be cleared by hardware, termination the Idle Mode. After the program wakes up, the PC value will point as interrupt vector (if enable IE register) and execute interrupt service routine then return to PC+1 address after the program wakes up.
2) By hardware reset
Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset. All SFR and PC value will be cleared to reset value.
3) By one of CLK, DATA, PORT 2.0-2.7 transition to low (falling edge trigger)
After the program wakes up, the PC value will be 0023h (if enable IE register) and execute interrupt service routine and then returns to PC+1 address after the program wakes up.

**Power Down Mode**

It saves the RAM content, stops the clock generator and disables every other blocks' function until the coming hardware reset. To save even more power consumption, user's software program can invoke this mode. The SFRs and the on-chip data RAM retain their values during this mode, but the porcessor stops executing instructions. In Power-Down mode (PD=1) the oscillator is frozen.

-An instruction that sets flag (PCON.1) causes that to be the last instruction executed before going into the Power Down Mode.

-In the Power Down Mode, the on-chip oscillator is stopped.
With the clock frozen, all functions are stopped, but the on-chip RAM and Special Function Registers are held.

-Reset redefines all the SFRs, but does not change the on-chip RAM.

-There are two ways to terminate the Power Down Mode.
1) By hardware reset
All SFR and PC value will be cleared to reset value.
2) One of CLK, DATA, PORT 2.0-2.7 transition to low (falling edge trigger)
After the program wakes up, the PC value will be 0023h (if enable IE register) and execute interrupt service routine and then returns to PC+1 address after the program wakes up.

-Care must be taken, however, to ensure that VCC is not reduced before the Power Down Mode is invoked, and that VCC is restored to its normal operating level before the Power Down Mode is terminated.

-The hardware reset must be held active long enough to allow the oscillator to restart and stabilize.

**General of above**

User should fix the attention on using wake up from port 2:

-The user should write the power down or idle mode flag value to one RAM address before write PCON to distinguish waking up from power down mode or idle mode.

-After idle mode or power down mode wakes up, the interrupt service routine will be executed first and then executes PC+1 address if the IE register is enabled before entering power down mode or idle mode. The interrupt service routine will not be executed but CPU executes PC+1 address program if disable IE register.

-After wake up power down or idle mode the IDF flag will be set by hardware. The IDF flag be cleared at the ISR execution time. If IE register is disable, the IDF flag will not be cleared when power down or idle mode wakes up.

The state of pins during Idle and Power-Down Mode

| Mode | Program memory | ALE | #PSEN | Port 0 | Port 1 | Port 2 | Port 3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power Down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power Down | External | 0 | 0 | Float | Data | Data | Data |

## Absolute Maximal Rating

| Symbol | Name | Rating | Unit | Remark |
|---|---|---|---|---|
| $V_{dd}$ - $V_{ss}$ | DC supply Voltage | -0.5 ~ +5.0 | V | U20x1L |
| | | -0.5 ~ +7.0 | V | U20x1S,U20x1C |
| $V_{IN}$ | Input voltage | $V_{ss}$-0.3 ~ $V_{dd}$+0.3 | V | |
| $V_{OUT}$ | output voltage | $V_{ss}$ ~ $V_{dd}$ | | |
| T (Operating) | Operating Temperature | 0 ~ +70 | °C | |
| T (Storage) | Storage Temperature | -55 ~ +125 | °C | |

* Note:
Operation beyond Absolute Maximal Rating can adversely affect device reliability.

## Operating Conditions

| Symbol | Description | Min. | Typ. | Max. | Unit | Remarks |
|---|---|---|---|---|---|---|
| t A | Ambient temperature under bias | 0 | 25 | 70 | °C | |
| V CC3 | Supply voltage | 2.7 | 3.0 | 4.5 | V | U20x1L |
| V CC5 | | 4.5 | 5.0 | 5.5 | V | U20x1S, U20x1C |
| f osc 16 | Oscillator Frequency | 3.0 | 16 | 16 | MHz | U20x1i16 |
| f osc 25 | | 16 | 25 | 25 | MHz | U20x1i25 |
| f osc 40 | | 25 | 40 | 40 | MHz | U20x1i40 |

## AC Characteristics

(16/25/40 MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=150pF; CL for all OtherOutputs=80pF)

| Symbol | Parameter | Valid Cycle | f osc 16 | | | Variable f osc | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max | Min. | Typ. | Max. | | |
| T LHLL | ALE pulse width | RD/WRT | 115 | | | 2xT - 10 | | | nS | |
| T AVLL | Address Valid to ALE low | RD/WRT | 43 | | | T - 20 | | | nS | |
| T LLAX | Address Hold after ALE low | RD/WRT | 53 | | | T - 10 | | | nS | |
| T LLIV | ALE low to Valid Instruction In | RD | | | 240 | | | 4xT - 10 | nS | |
| T LLPL | ALE low to #PSEN low | RD | 53 | | | T - 10 | | | nS | |
| T PLPH | #PSEN pulse width | RD | 173 | | | 3xT - 15 | | | nS | |
| T PLIV | #PSEN low to Valid Instruction In | RD | | | 177 | | | 3xT - 10 | nS | |
| T PXIX | Instruction Hold after #PSEN | RD | 0 | | | 0 | | | nS | |
| T PXIZ | Instruction Float after #PSEN | RD | | | 87 | | | T + 25 | nS | |
| T AVIV | Address to Valid Instruction In | RD | | | 292 | | | 5xT - 20 | nS | |
| T PLAZ | #PSEN low to Address Float | RD | | | 10 | | | 10 | nS | |
| T RLRH | #RD pulse width | RD | 365 | | | 6xT - 10 | | | nS | |
| T WLWH | #WR pulse width | WRT | 365 | | | 6xT - 10 | | | nS | |
| T RLDV | #RD low to Valid Data in | RD | | | 302 | | | 5xT - 10 | nS | |
| T RHDX | Data Hold after #RD | RD | 0 | | | 0 | | | nS | |
| T RHDZ | Data Float after #RD | RD | | | 145 | | | 2xT + 20 | nS | |
| T LLDV | ALE low to Valid Data In | RD | | | 490 | | | 8xT - 10 | nS | |
| T AVDV | Address to Valid Data In | RD | | | 542 | | | 9xT - 20 | nS | |
| T LLYL | ALE low to #WR or #RD low | RD/WRT | 178 | | 197 | 3xT - 10 | | 3xT + 10 | nS | |
| T AVYL | Address Valid to #WR or #RD low | RD/WRT | 230 | | | 4xT - 20 | | | nS | |
| T QVWH | Data Valid to #WR High | WRT | 403 | | | 7xT - 35 | | | nS | |
| T QVWX | Data Valid to #WR transition | WRT | 38 | | | T - 25 | | | nS | |
| T WHQX | Data hold after #WR | WRT | 73 | | | T + 10 | | | nS | |
| T RLAZ | #RD low to Address Float | RD | | | | | | 5 | nS | |
| T YHLH | #WR or #RD high to ALE high | RD/WRT | 53 | | 72 | T - 10 | | T + 10 | nS | |
| T CHCL | Clock fall time | | | | | | | | nS | |
| T CLCX | Clock low time | | | | | | | | nS | |
| T CLCH | Clock rise time | | | | | | | | nS | |
| T CHCX | Clock high time | | | | | | | | nS | |
| T, T CLCL | Clock period | | | 63 | | | 1/ fosc | | nS | |

## DC Characteristics

(16/25/40 MHz, typical operating conditons, valid for U20x1C series)

| Symbol | Parameter | Valid | Min. | Typ. | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| V ILX | Input Low Voltage | XTAL1 | -0.5 | | 20%Vcc-0.1 | V | |
| V ILE | " | #EA | 0 | | 20%Vcc-0.3 | V | |
| V ILR | " | RES | -0.5 | | 20%Vcc-0.1 | V | |
| V IHX | Input High Voltage | XTAL1 | 70%Vcc | | Vcc+0.5 | V | |
| V IHE | " | #EA | 20%Vcc+0.9 | | Vcc+0.5 | V | |
| V IHR | " | RES | 70%Vcc | | Vcc+0.5 | V | |
| V OLA | Output Low Voltage | ALE, #PSEN | | | 450 | mV | I OL = 3.2 mA |
| V OL0 | " | ports 0,3 | | | 450 | mV | I OL = 3.2 mA |
| V OL1 | " | ports 1,2 | | | 450 | mV | I OL = 1.6 mA |
| V OHA | Output High Voltage | ALE, #PSEN | 2.4 | | | V | I OH = -60 uA |
| | " | | 90%Vcc | | | V | I OH = -10 uA |
| V OH0 | " | port 0 | 2.4 | | | V | I OH = -800 uA |
| | " | | 90%Vcc | | | V | I OH = -80 uA |
| V OH1 | " | ports 1,3 | 2.4 | | | V | I OH = -60 uA |
| | " | | 90%Vcc | | | V | I OH = -10 uA |
| V OH2 | " | port 2 | 2.4 | | | V | I OH = -60 uA |
| | " | | 90%Vcc | | | V | I OH = -10 uA |
| I OL0 | Output Low Current | ports 0,3 | | 18 | | mA | V OL = 0.45V, note 1 |
| I IL | Logical 0 Input Current | ports 1,2,3 | | | -50 | uA | V in = 0.45 V |
| I IH | Logical 1 Input Current | port 0 | | | 1.5 | uA | V in = 5.0 V |
| | | | | | | | |
| I TL | Logic Transition Current | ports 1,2,3 | | | -650 | uA | V in = 2.0 V |
| I LI | Input Leakage Current | port 0 | | | 10 | uA | 0.45V < Vin < Vcc |
| R RES | Reset Pulldown Resistance | RES | 50 | | 150 | Kohm | |
| R X | Crystal feedback Resistance | XTAL1,2 | 90 | | 330 | Kohm | |
| C IO | Pin Capacitance | | | | 10 | pF | Freq=1MHz, Ta=25 ¢J |
| I CC | Power Supply Current | Vdd | | 5 | 8 | mA | Active mode, 16 MHz |
| | | Vdd | | 3 | 5 | mA | Idle mode, 16MHz |
| | | Vdd | | 10 | 45 | uA | Power down mode |

**note 1 : no more than 80 mA I OLs for all 16-bit ports 0 & 3 output pins.**

## DC Characteristics

(16 MHz, typical operating conditons, valid for U20x1S series)

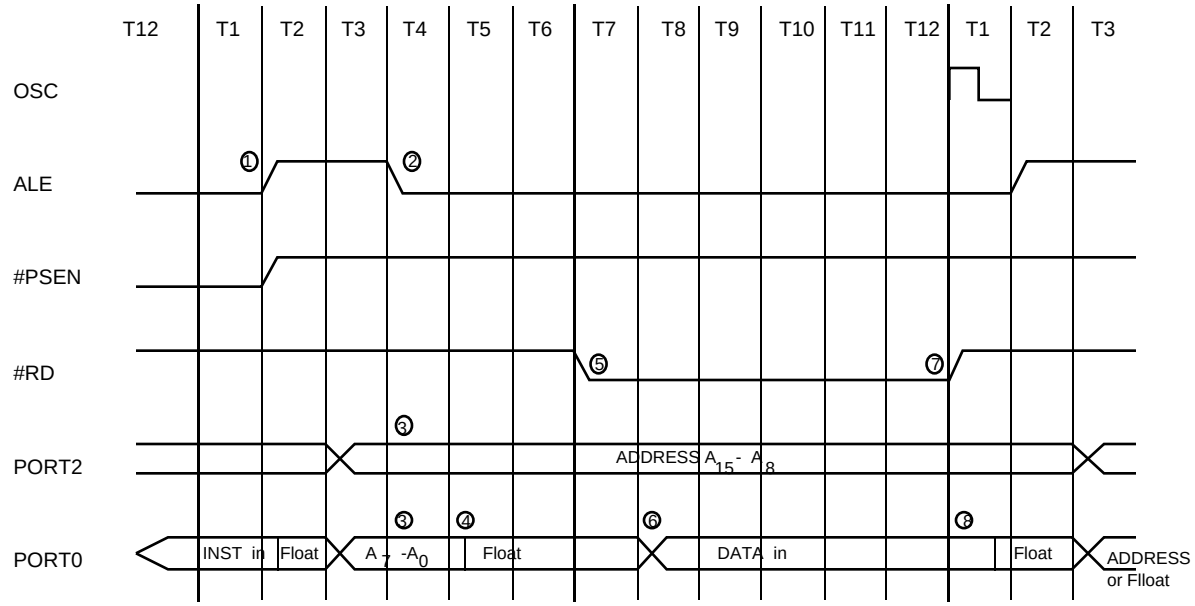
| Symbol | Parameter | Valid | Min. | Typ. | Max. | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| I OL0 | Output Low Current | ports 0 & 3 | | 3 | | mA | V OL = 0.45V |
| others | | | **identical to U20x1C series'** | | | | |

## DC Characteristics

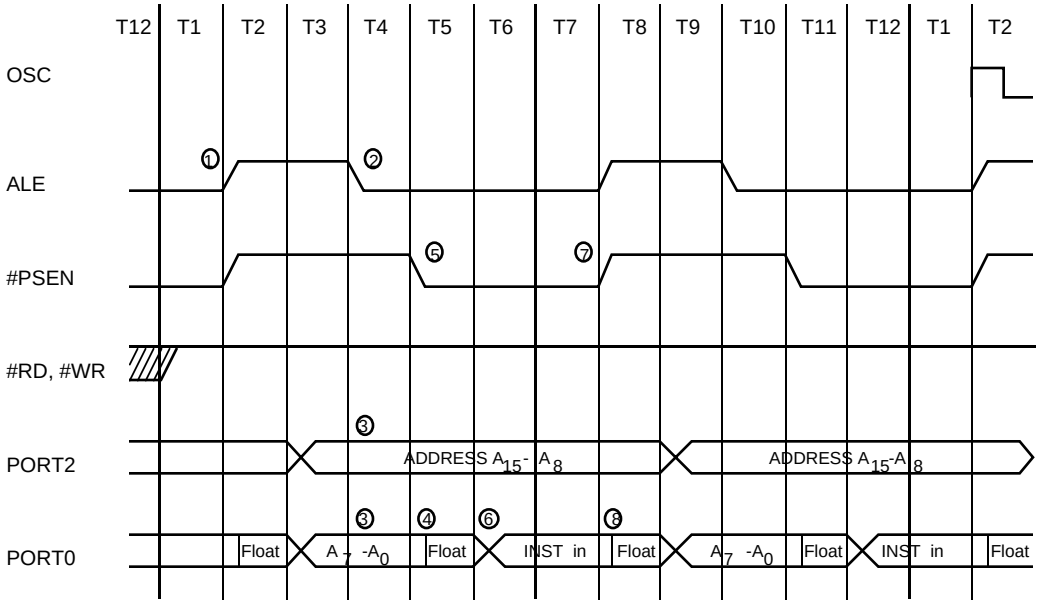
(16 MHz, typical operating conditons, valid for U20x1L series)

| Symbol | Parameter | Valid | Min. | Typ. | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| V ILX | Input Low Voltage | XTAL1 | | | | mV | |
| V ILE | " | #EA | | | | mV | |
| V ILR | " | RES | | | | mV | |
| V IHX | Input High Voltage | XTAL1 | | | Vcc+0.3 | V | |
| V IHE | " | #EA | | | Vcc+0.3 | V | |
| V IHR | " | RES | | | Vcc+0.3 | V | |
| V OLA | Output Low Voltage | ALE, #PSEN | | | 400 | mV | I OL = 3.2 mA |
| V OL0 | " | ports 0,3 | | | 400 | mV | I OL = 3.2 mA |
| V OL1 | " | ports 1,2 | | | 400 | mV | I OL = 1.6 mA |
| V OHA | Output High Voltage | ALE, #PSEN | 1.8 | | | V | I OH = -60 uA |
| | " | | 2.4 | | | V | I OH = -10 uA |
| V OH0 | " | port 0 | 2.2 | | | V | I OH = -800 uA |
| | " | | 2.4 | | | V | I OH = -80 uA |
| V OH1 | " | ports 1,3 | 1.8 | | | V | I OH = -60 uA |
| | " | | 2.4 | | | V | I OH = -10 uA |
| V OH2 | " | port 2 | 1.8 | | | V | I OH = -60 uA |
| | " | | 2.4 | | | V | I OH = -10 uA |
| | | | | | | | |
| I IL | Logical 0 Input Current | ports 1,2,3 | | | 45 | uA | V in = 0.45 V |
| I IH | Logical 1 Input Current | port 0 | | | 1 | uA | V in = 3.0 V |
| | | | | | | | |
| I TL | Logic Transition Current | ports 1,2,3 | | | 250 | uA | V in = 1.4 V |
| I LI | Input Leakage Current | port 0 | | | 8 | uA | 0.45V < Vin < Vcc |
| R RES | Reset Pulldown Resistance | RES | 50 | | 150 | Kohm | |
| R X | Crystal feedback Resistance | XTAL1,2 | 90 | | 330 | Kohm | |
| C IO | Pin Capacitance | | | | 10 | pF | Freq=1MHz, Ta=25 ¢J |
| I CC | Power Supply Current | Vdd | | 2 | 7 | mA | Active mode, 16 MHz |
| | | Vdd | | 1 | 4.5 | mA | Idle mode, 16MHz |
| | | Vdd | | 10 | 45 | uA | Power down mode |

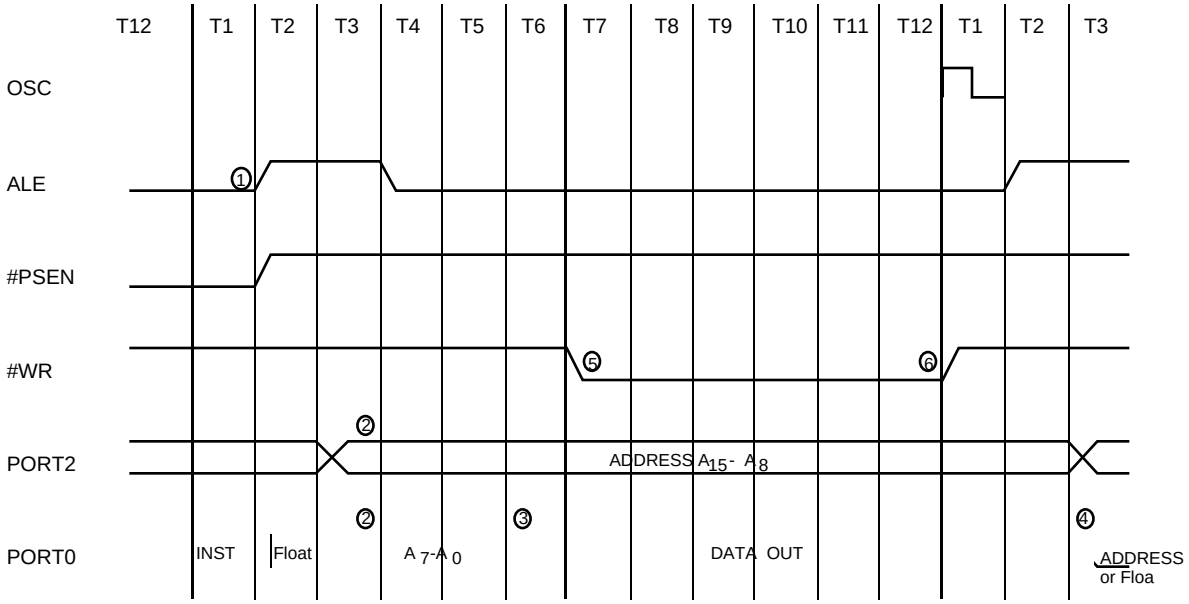
## Data Memory Read Cycle Timing



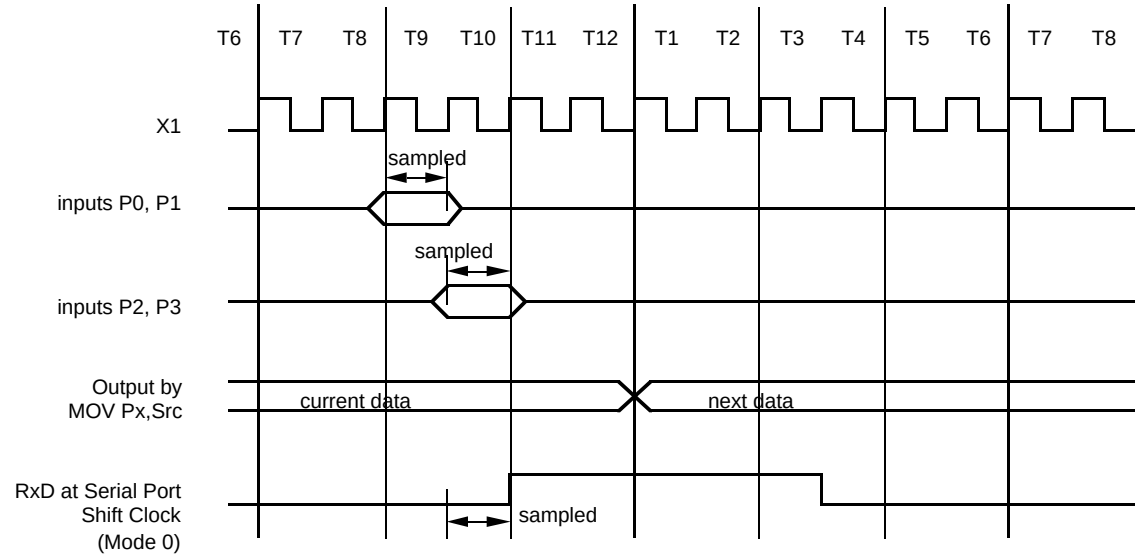

## Program Memory Read Cycle Timing



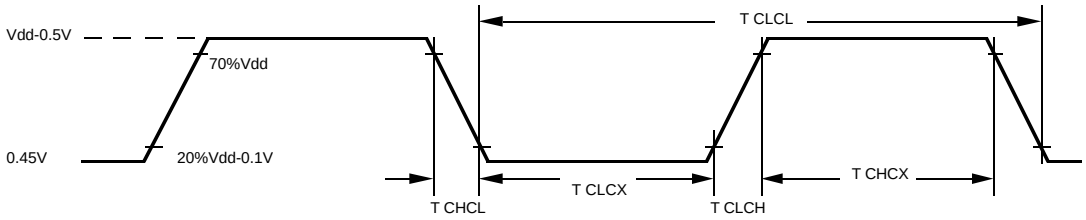
## Data Memory Write Cycle Timing



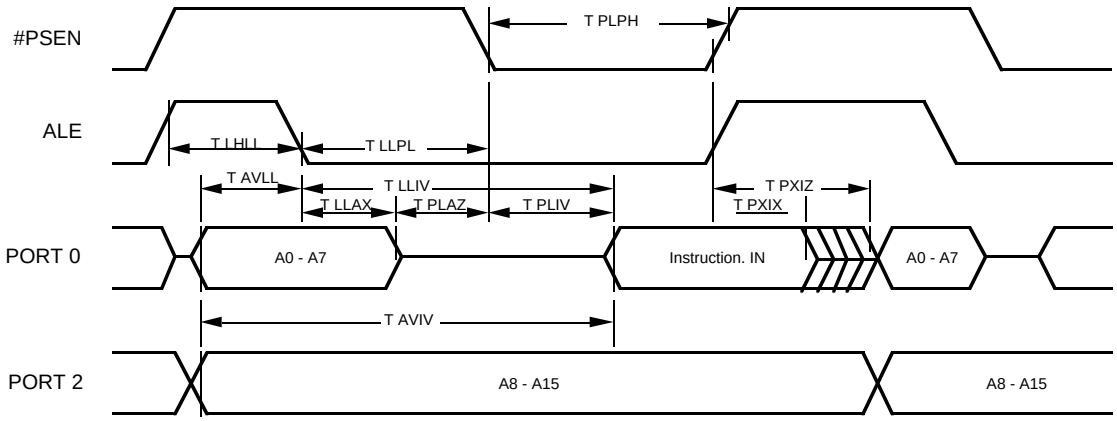

## I/O Ports Timing



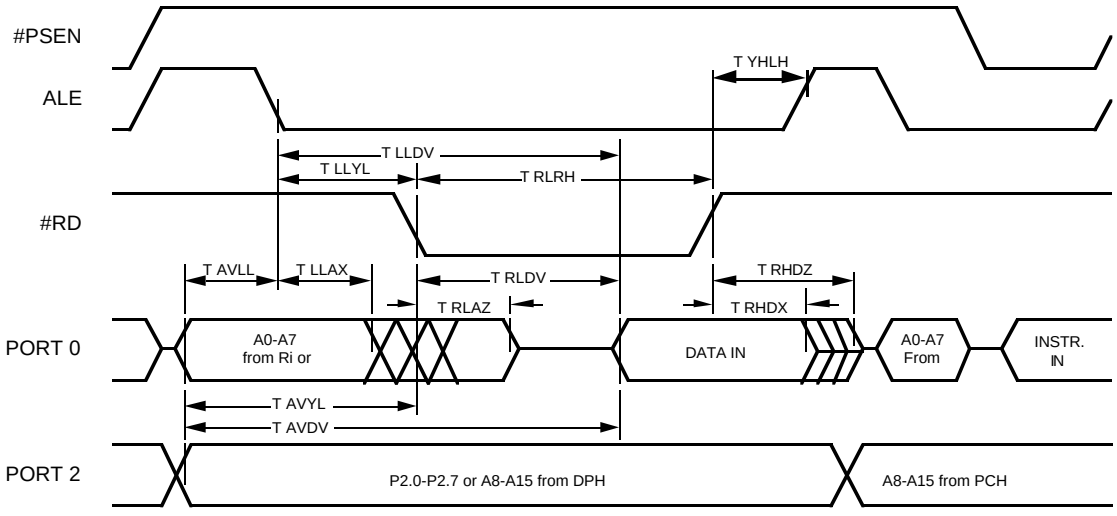
## Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



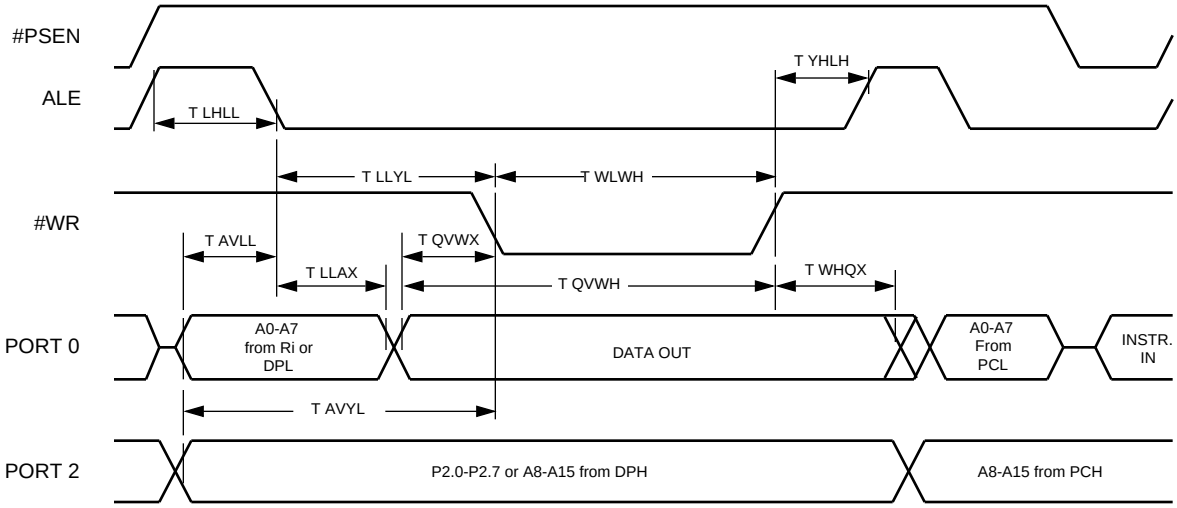

## Tm.I External Program Memory Read Cycle




## Tm.II External Data Memory Read Cycle

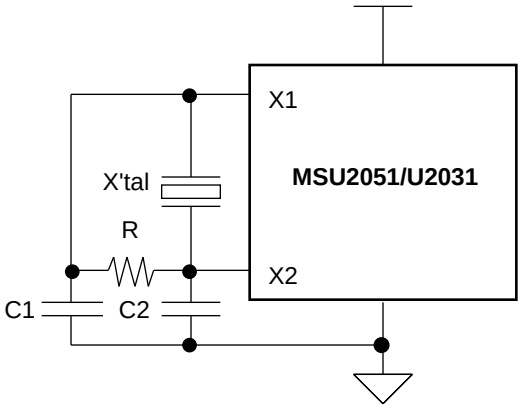


## Tm.III External Data Memory Write Cycle

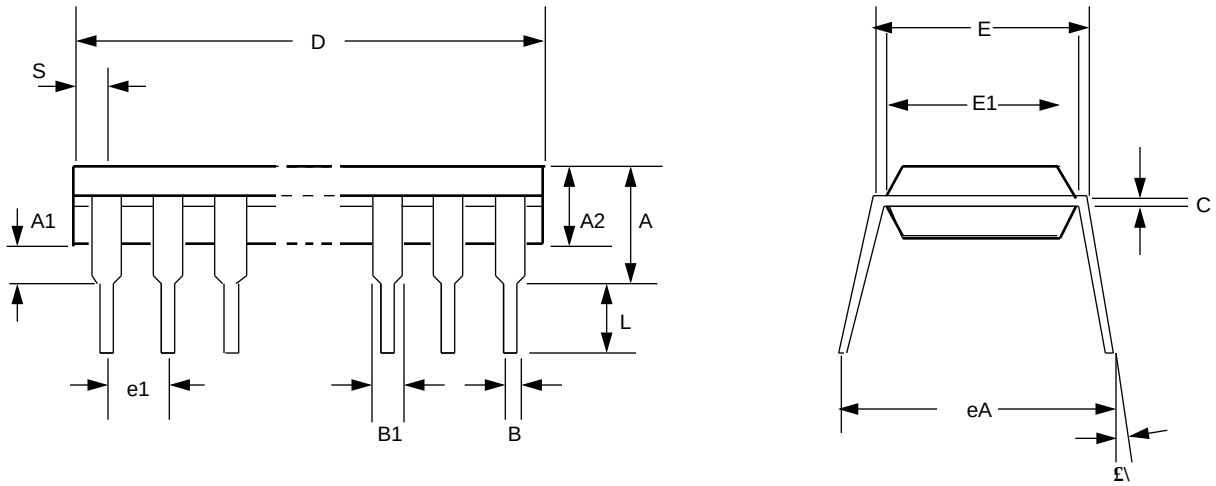



## Application Reference

| Valid for U2051L16/ U2031L16/ U2051S16/ U2031S16 | | | | |
|---|---|---|---|---|
| X'tal | 3 MHz | 6 MHz | 12 MHz | 16 MHz |
| C1 | 15 pF | 15 pF | 30 pF | 30 pF |
| C2 | 15 pF | 15 pF | 30 pF | 30 pF |
| R | open | open | open | open |
| **Valid for U2051C16/ U2031C16/ U2051C25/ U2031C25/ U2051C40/ U2031C40** | | | | |
| X'tal | 12 MHz | 16 MHz | 25 MHz | 40 MHz |
| C1 | 30 pF | 30 pF | 15 pF | 5 pF |
| C2 | 30 pF | 30 pF | 15 pF | 5 pF |
| R | open | open | 62 Kohm | 4.7 Kohm |



## 40L 600mil PDIP Information

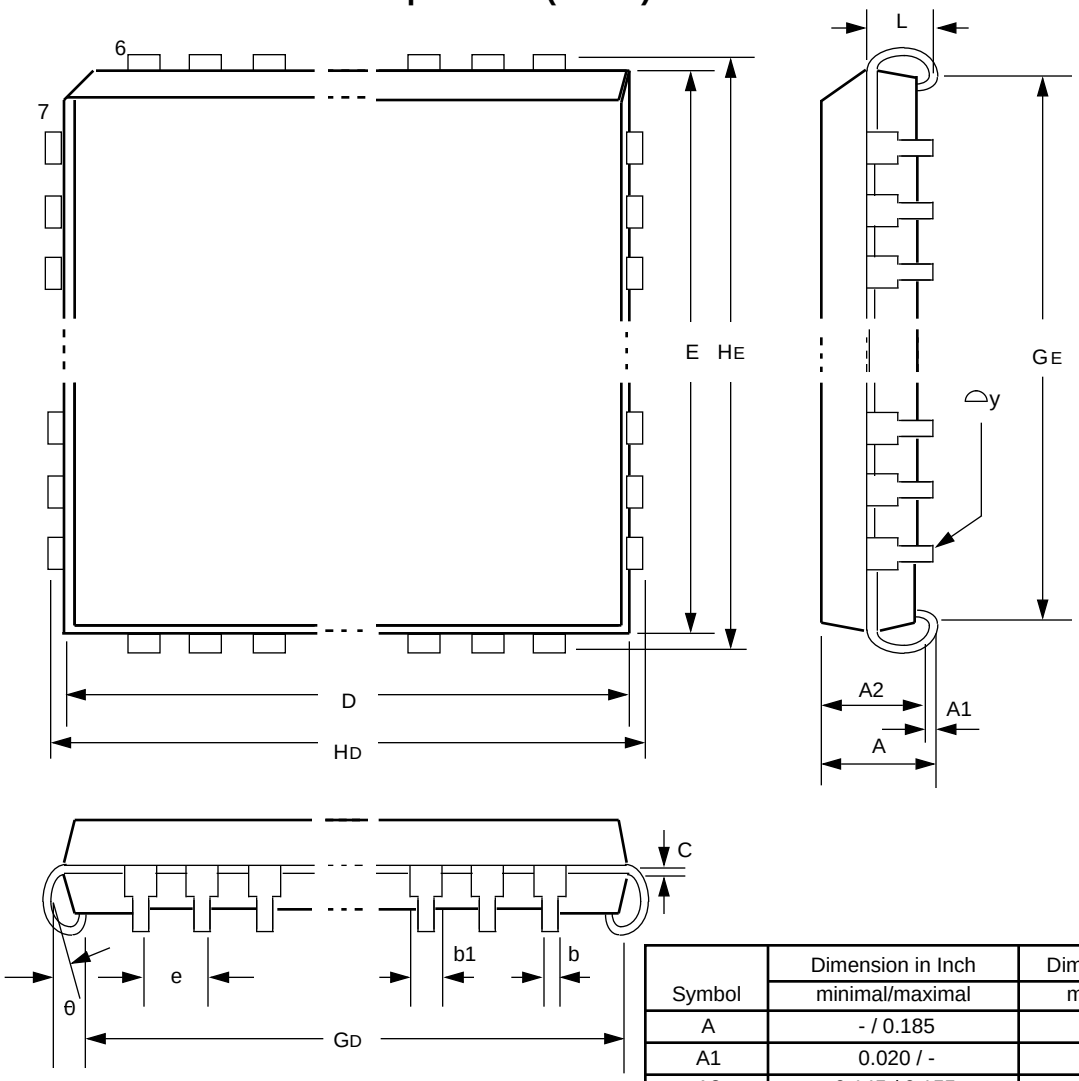



Note:

1. Dimension D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimenseion D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/ infrusion.
5. Controlling dimension is inch.
6. General appearance spec. should base on final visualinspection spec.

| Symbol | Dimension in Inch minimal/maximal | Dimension in mm minimal/maximal |
|---|---|---|
| A | - / 0.210 | - / 5.33 |
| A1 | 0.010 / - | 0.25 / - |
| A2 | 0.150 / 0.160 | 3.81 / 4.06 |
| B | 0.016 / 0.022 | 0.41 / 0.56 |
| B1 | 0.048 / 0.054 | 1.22 / 1.37 |
| C | 0.008 / 0.014 | 0.20 / 0.36 |
| D | - / 2.070 | - / 52.58 |
| E | 0.590 / 0.610 | 14.99 / 15.49 |
| E1 | 0.540 / 0.552 | 13.72 / 14.02 |
| e1 | 0.090 / 0.110 | 2.29 / 2.79 |
| L | 0.120 / 0.140 | 3.05 / 3.56 |
| £\ | 0° / 15° | 0° / 15° |
| eA | 0.630 / 0.670 | 16.00 / 17.02 |
| S | / 0.090 | - / 2.29 |

## 44L Plastic Leaded Chip Carrier (PLCC)

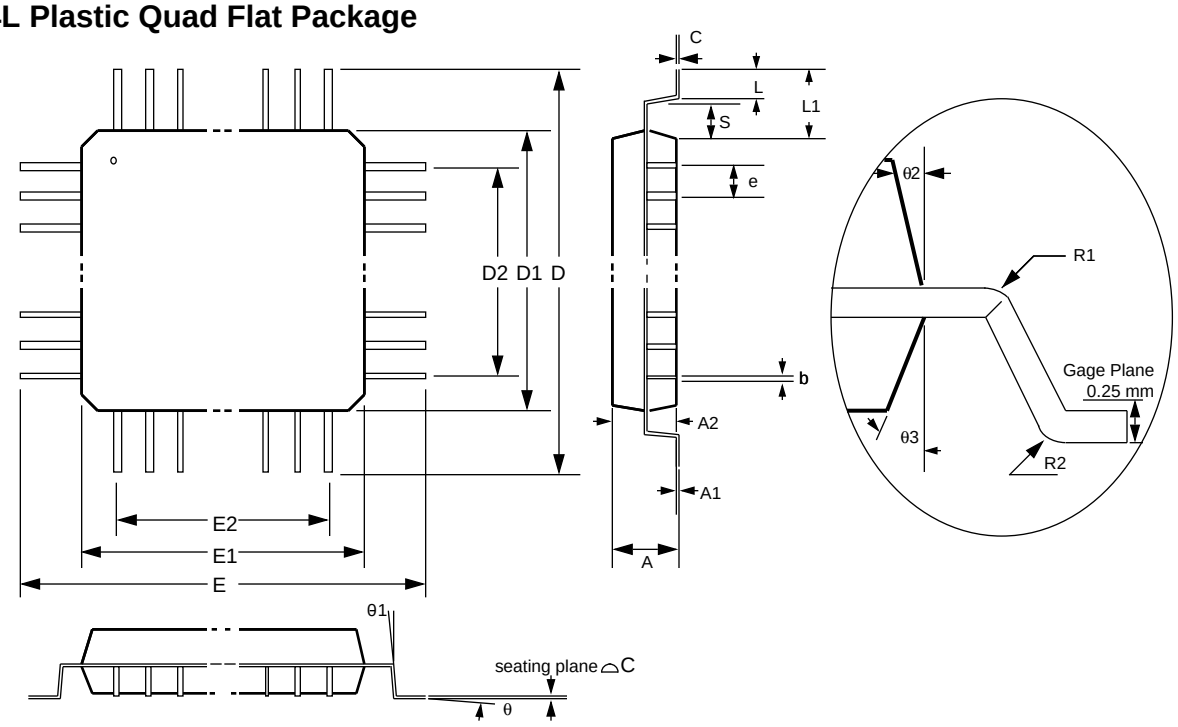



| Symbol | Dimension in Inch minimal/maximal | Dimension in mm minimal/maximal |
|---|---|---|
| A | - / 0.185 | - / 4.70 |
| A1 | 0.020 / - | 0.51 / - |
| A2 | 0.145 / 0.155 | 3.68 / 3.94 |
| b1 | 0.026 / 0.032 | 0.66 / 0.81 |
| b | 0.016 / 0.022 | 0.41 / 0.56 |
| C | 0.008 / 0.014 | 0.20 / 0.36 |
| D | 0.648 / 0.658 | 16.46 / 16.71 |
| E | 0.648 / 0.658 | 16.46 / 16.71 |
| e | 0.050 BSC | 1.27BSC |
| GD | 0.590 / 0.630 | 14.99 / 16.00 |
| GE | 0.590 / 0.630 | 14.99 / 16.00 |
| HD | 0.680 / 0.700 | 17.27 / 17.78 |
| HE | 0.680 / 0.700 | 17.27 / 17.78 |
| L | 0.090 / 0.110 | 2.29 / 2.79 |
| y | - / 0.004 | - / 0.10 |
| θ | / | / |

Note:

1.Dimension D & E does not include interlead flash.
2.Dimension b1 does not include dambar protrusion/ intrusion.
3.Controlling dimension:Inch
4.General appreance spec. should base on final visual inspection spec.

## 44L Plastic Quad Flat Package

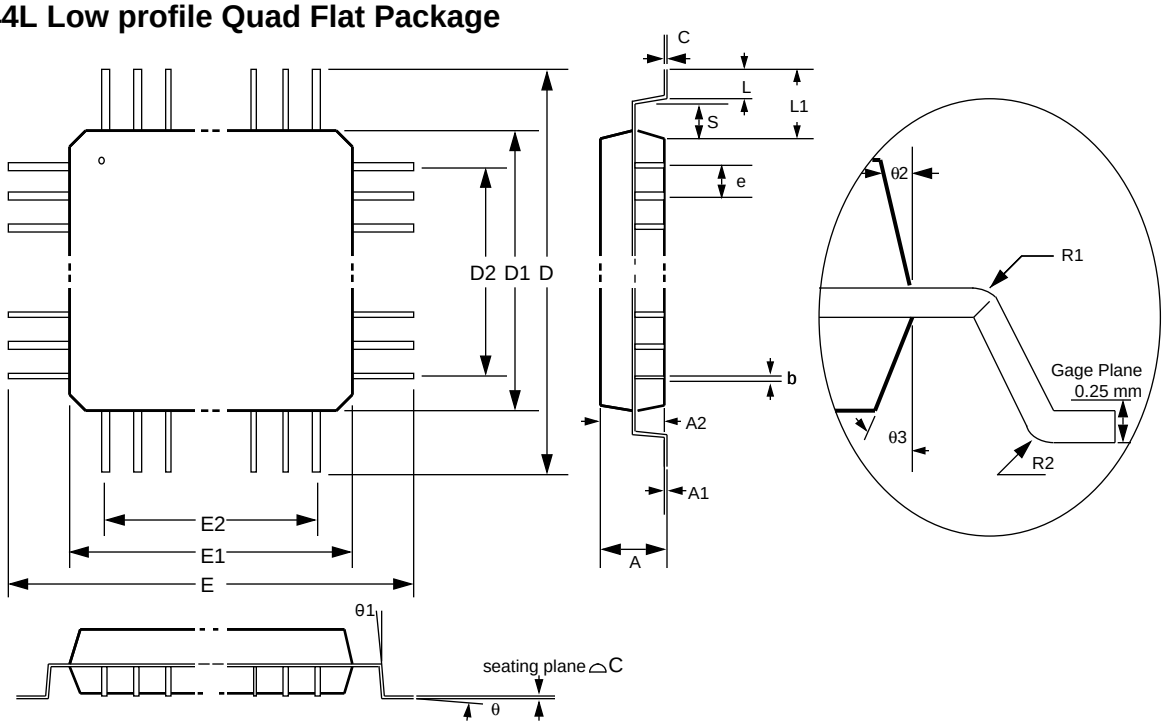



Note:

1. Dimension D1 and E1 do not include mold protrustion. Allowance protrusion is 0.25mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane.
2. Dimension b does not include dambar protrusion. Allowance dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.

| Symbol | Dimension in Inch<br>minimal/maximal | Dimension in mm<br>minimal/maximal |
|---|---|---|
| A | - / 0.100 | - / 2.55 |
| A1 | 0.006 / 0.014 | 0.15 / 0.35 |
| A2 | 0.071 / 0.087 | 1.80 / 2.20 |
| b | 0.012 / 0.018 | 0.30 / 0.45 |
| c | 0.004 / 0.009 | 0.09 / 0.20 |
| D | 0.520 BSC | 13.20 BSC |
| D1 | 0.394 BSC | 10.00 BSC |
| D2 | 0.315 | 8.00 |
| E | 0.520 BSC | 13.20 BSC |
| E1 | 0.394 BSC | 10.00 BSC |
| E2 | 0.315 | 8.00 |
| e | 0.031 BSC | 0.80 BSC |
| L | 0.029 / 0.041 | 0.73 / 1.03 |
| L1 | 0.063 | 1.60 |
| R1 | 0.005 / - | 0.13 / - |
| R2 | 0.005 / 0.012 | 0.13 / 0.30 |
| S | 0.008 / - | 0.20 / - |
| θ | 0° / 7° | as left |
| θ1 | 0° / - | as left |
| θ2 | 10° REF | as left |
| θ3 | 7° REF | as left |
| C | 0.004 | 0.10 |

## 44L Low profile Quad Flat Package




Note:

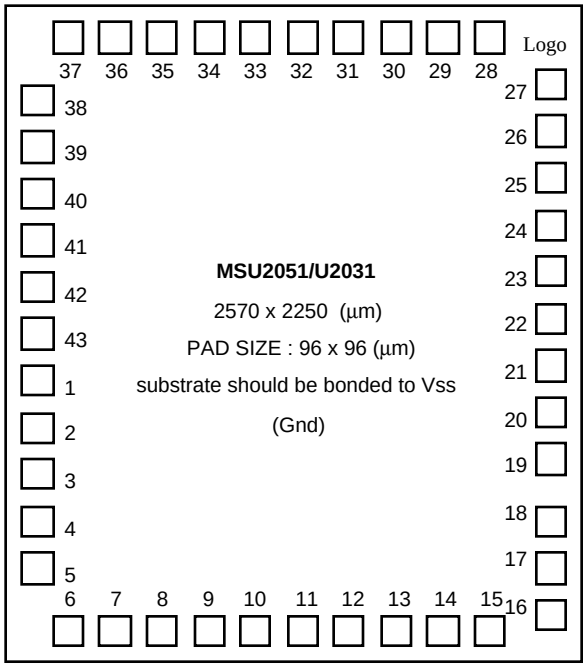
1. Dimension D1 and E1 do not include mold protrustion. Allowance protrusion is 0.25mm per side. D1 and E1 are maximal plastic body size dimensions including mold mismatch.
2. Dimension b does not include dambar protrusion. Allowance dambar protrusion shall not cause the lead width to exceed the maximal b dimension by more than 0.08 mm.
3. Dambar can not be located on the lower radius or the foot. Minimal space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

| Symbol | Dimension in Inch<br>minimal/maximal | Dimension in mm<br>minimal/maximal |
|---|---|---|
| A | - / 0.063 | - / 1.60 |
| A1 | 0.002 / 0.006 | 0.05 / 0.15 |
| A2 | 0.053 / 0.057 | 1.35 / 1.45 |
| b | 0.012 / 0.018 | 0.30 / 0.45 |
| c | 0.004 / 0.008 | 0.09 / 0.20 |
| D | 0.472 BSC | 12.00 BSC |
| D1 | 0.393 BSC | 10.00 BSC |
| D2 | 0.315 | 8.00 |
| E | 0.472 BSC | 12.00 BSC |
| E1 | 0.393 BSC | 10.00 BSC |
| E2 | 0.315 | 8.00 |
| e | 0.031 BSC | 0.80 BSC |
| L | 0.018 / 0.030 | 0.45 / 0.75 |
| L1 | 0.039 REF | 1.00 REF |
| R1 | 0.003 / - | 0.08 / - |
| R2 | 0.003 / 0.008 | 0.08 / 0.20 |
| S | 0.008 / - | 0.20 / - |
| θ | 0° / 7° | as left |
| θ1 | 0° / - | as left |
| θ2 | 11°/13° | as left |
| θ3 | 11°/13° | as left |
| C | 0.004 | 0.10 |

## Bonding Information

| ORDER | PAD-NAME | X-COORD | Y-COORD |
|---|---|---|---|
| 1 | P1_0 | 186 | 1080 |
| 2 | P1_1 | 186 | 921 |
| 3 | P1_2 | 186 | 758 |
| 4 | P1_3 | 186 | 599 |
| 5 | P1_4 | 186 | 436 |
| 6 | P1_5 | 270 | 186 |
| 7 | P1_6 | 432 | 186 |
| 8 | P1_7 | 592 | 186 |
| 9 | RES | 754 | 186 |
| 10 | P3_0 | 914 | 186 |
| 11 | P3_1 | 1077 | 186 |
| 12 | P3_2 | 1236 | 186 |
| 13 | P3_3 | 1399 | 186 |
| 14 | P3_4 | 1558 | 186 |
| 15 | P3_5 | 1721 | 186 |
| 16 | P3_6 | 1964 | 255 |
| 17 | P3_7 | 1964 | 418 |
| 18 | XTAL2 | 1964 | 577 |
| 19 | XTAL1 | 1964 | 839 |
| 20 | GND | 1964 | 1000 |
| 21 | GND | 1964 | 1151 |
| 22 | GND | 1964 | 1302 |

| ORDER | PAD-NAME | X-COORD | Y-COORD |
|---|---|---|---|
| 23 | P2_0 | 1964 | 1463 |
| 24 | P2_1 | 1964 | 1623 |
| 25 | P2_2 | 1964 | 1786 |
| 26 | P2_3 | 1964 | 1945 |
| 27 | P2_4 | 1964 | 2108 |
| 28 | P2_5 | 1721 | 2281 |
| 29 | P2_6 | 1558 | 2281 |
| 30 | P2_7 | 1399 | 2281 |
| 31 | #PSEN | 1236 | 2281 |
| 32 | ALE | 1077 | 2281 |
| 33 | #EA | 914 | 2281 |
| 34 | P0_7 | 754 | 2281 |
| 35 | P0_6 | 592 | 2281 |
| 36 | P0_5 | 432 | 2281 |
| 37 | P0_4 | 270 | 2281 |
| 38 | P0_3 | 186 | 2038 |
| 39 | P0_2 | 186 | 1876 |
| 40 | P0_1 | 186 | 1716 |
| 41 | P0_0 | 186 | 1554 |
| 42 | VDD | 186 | 1393 |
| 43 | VDD | 186 | 1241 |




pid 251* 11/95
pid 251** 01/96
pid 251*** 03/96
pid 251**** 08/96
pid 251***** 10/96
pid 251A 11/96
pid 263* 11/97
pid 251B 01/98

To: Mosel Vitelic Inc.
886-3-578-4732 (fax #)
Attn: Sales & Marketing Department

# Product Request Form

We hereby request MVI to start producing MSU2051 which is specified below.
Please send us the product code and a hardcopy of data code as well as data code file duplicated on floppy diskette. No further confirmation is necessary.
Production will start automatically once you receive our data code and verify that the checksum is match.
Mass Production of the captioned device shall be done in accordance with the purchase order(s) issued by us or a company specified by us. All terms and conditions are based on the development agreement and/or contract signed between MVI and us.

| **Data Code Descriptions** | | **IC descriptions** | |
|---|---|---|---|
| Code Length | | ☐ Dice form<br>☐ P type = 40L-PDIP<br>☐ J type = 44L-PLCC<br>☐ Q type = 44L-PQFP<br>☐ L type = 44L-LQFP | ☐ U2051S16, 16 MHz small current<br>☐ U2051L16, 16 MHz low working voltage<br>☐ U2051C16, 16 MHz<br>☐ U2051C25, 25 MHz<br>☐ U2051C40, 40 MHz |
| File Length | | | |
| File Name | | | |
| Checksum | h | | |
| Unused Data Byte | ☐ 00h filled<br>☐ FFh filled | **Top Marking (fill only for packaged)** | |
| Format | ☐ HEX format<br>☐ Binary code format | ☐ Use MVI logo, date code and part number<br>☐ Use my specifications as described below | |
| Media | ☐ EPROM<br>☐ 8751 chip<br>☐ File on Floppy<br>☐ E-mail file | **Specify below fields only for customer top marking** | |
| | | Date code location descriptions | |
| | | ☐ Use regular date code as MVI's<br>☐ Leave it as blank<br>☐ use right side five letters ☐☐☐☐☐ | |
| | | Logo Specifications | |
| | | ☐ Leave it blank<br>☐ Use my specifications as attachment | |
| | | Part number specified, less than 15 digits | |
| | | ☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐ | |

Phone # : _____ Fax # : _____

Company Name : _____

Signature : _____

Name (Typed) : _____

Position Title : _____

Department, Section : _____

Signature Date : _____

To: Mosel Vitelic Inc.
886-3-578-4732 (fax#)
Attn: Sales & Marketing Department

# Logo Top Marking Request & spec.

We hereby request MVI to have our logo printed on top of the device package. Below is the specification of our logo in 20:1 scale base. This logo diagram is clear enough and is able to be shrunk directly to fit into available top marking area described on page.

Phone # : _____ Fax # : _____

Company Name : _____

Signature : _____

Name (Typed) : _____

Position Title : _____

Department, Section : _____

Signature Date : _____

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FAX: 852-2664-7535

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MIN-CHUAN E. ROAD, SEC. 3
TAIPEI
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FAX: 886-2-2545-1209

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