Quad I²C 16-/12-Bit Rail-to-Rail DACs with 10ppm/°C Max Reference

FEATURES

- **Integrated Reference 10ppm/°C Max**
- **Maximum INL Error: ±4LSB at 16 Bits**
- **Guaranteed Monotonic Over Temperature**
- **Selectable Internal or External Reference**
- 2.7V to 5.5V Supply Range (LTC2655-L)
- Integrated Reference Buffers
- Ultralow Crosstalk Between DACs (<1nV•s)
- Power-On-Reset to Zero-Scale/Mid-Scale
- Asynchronous DAC Update Pin
- Tiny 20-Lead 4mm × 4mm QFN and 16-Lead Narrow SSOP packages

APPLICATIONS

- Mobile Communications
- Process Control and Industrial Automation
- Instrumentation
- Automatic Test Equipment
- Automotive

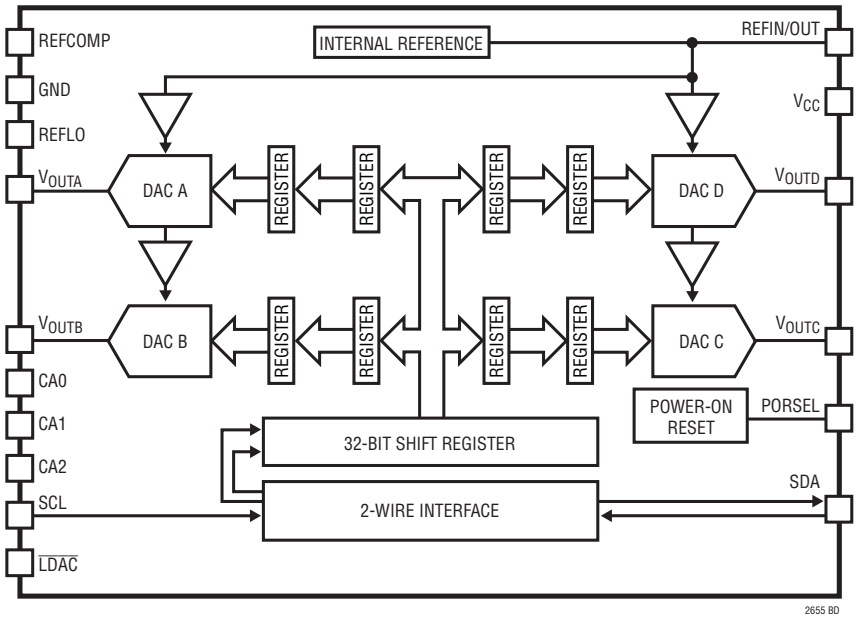
DESCRIPTION

The LTC®2655 is a family of Quad I²C 16-/12-Bit Rail-to-Rail DACs with integrated 10ppm/°C max reference. The DACs have built-in high performance, rail-to-rail, output buffers and are guaranteed monotonic. The LTC2655-L has a full-scale output of 2.5V with the integrated reference and operates from a single 2.7V to 5.5V supply. The LTC2655-H has a full-scale output of 4.096V with the integrated reference and operates from a 4.5V to 5.5V supply. Each DAC can also operate with an external reference, which sets the full-scale output to 2 times the external reference voltage.

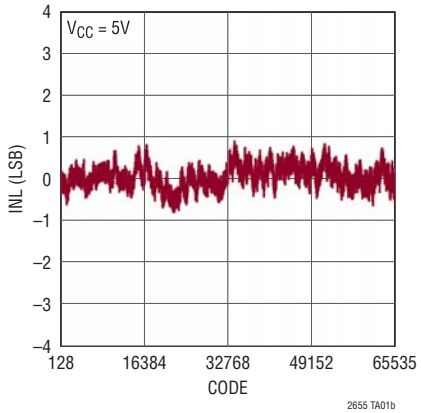
The parts use the 2-wire I²C compatible serial interface. The LTC2655 operates in both the standard mode (maximum clock rate of 100kHz) and the fast mode (maximum clock rate of 400kHz). The LTC2655 incorporates a power-on reset circuit that is controlled by the PORSEL pin. If PORSEL is tied to GND the DACs power-on reset to zero-scale. If PORSEL is tied to V_{CC}, the DACs power-on reset to mid-scale.

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BLOCK DIAGRAM



INL Curve



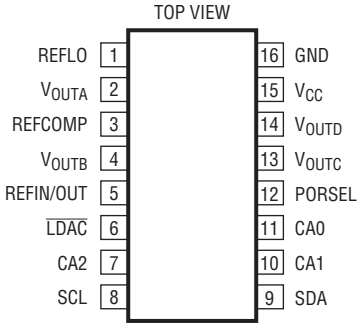
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 6V
SCL, SDA, $\overline{LDAC}$, REFLO ..... –0.3V to 6V
V_{OUTA} to V_{OUTD} ..... –0.3V to Min (V_{CC} + 0.3V, 6V)
REFIN/OUT, REFCOMP ..... –0.3V to Min (V_{CC} + 0.3V, 6V)
PORSEL, CA0, CA1, CA2 .. –0.3V to Min (V_{CC} + 0.3V, 6V)

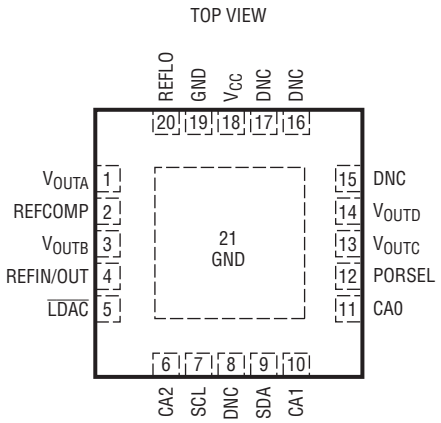
Operating Temperature Range
LTC2655C ..... 0°C to 70°C
LTC2655I ..... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65 to 150°C
Lead Temperature, GN Only (Soldering, 10 sec).... 300°C

PIN CONFIGURATION



GN PACKAGE
16-LEAD PLASTIC SSOP

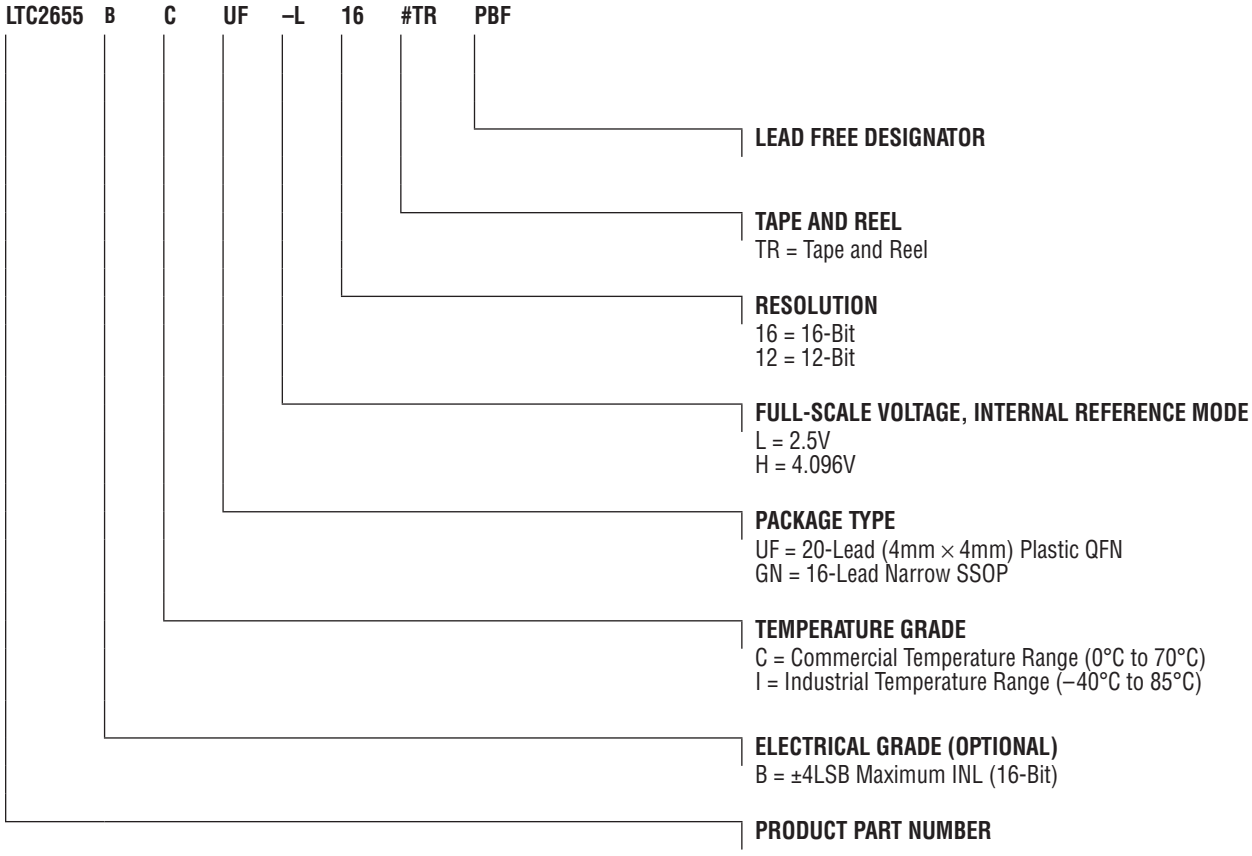
T_{JMAX} = 150°C, θ_{JA} = 110°C/W



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION



Consult LTC Marketing for information on non-standard lead based finish parts. Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

PRODUCT SELECTION GUIDE

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE	MAXIMUM INL
LTC2655BCGN-L16#PBF	LTC2655BCGN-L16#TRPBF	655L16	16-Lead Narrow SSOP	0°C to 70°C	±4
LTC2655BIGN-L16#PBF	LTC2655BIGN-L16#TRPBF	655L16	16-Lead Narrow SSOP	–40°C to 85°C	±4
LTC2655BCUF-L16#PBF	LTC2655BCUF-L16#TRPBF	55L16	20-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C	±4
LTC2655BIUF-L16#PBF	LTC2655BIUF-L16#TRPBF	55L16	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C	±4
LTC2655BCGN-H16#PBF	LTC2655BCGN-H16#TRPBF	655H16	16-Lead Narrow SSOP	0°C to 70°C	±4
LTC2655BIGN-H16#PBF	LTC2655BIGN-H16#TRPBF	655H16	16-Lead Narrow SSOP	–40°C to 85°C	±4
LTC2655BCUF-H16#PBF	LTC2655BCUF-H16#TRPBF	55H16	20-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C	±4
LTC2655BIUF-H16#PBF	LTC2655BIUF-H16#TRPBF	55H16	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C	±4
LTC2655CGN-L12#PBF	LTC2655CGN-L12#TRPBF	655L12	16-Lead Narrow SSOP	0°C to 70°C	±1
LTC2655IGN-L12#PBF	LTC2655IGN-L12#TRPBF	655L12	16-Lead Narrow SSOP	–40°C to 85°C	±1
LTC2655CUF-L12#PBF	LTC2655CUF-L12#TRPBF	55L12	20-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C	±1
LTC2655IUF-L12#PBF	LTC2655IUF-L12#TRPBF	55L12	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C	±1
LTC2655CGN-H12#PBF	LTC2655CGN-H12#TRPBF	655H12	16-Lead Narrow SSOP	0°C to 70°C	±1
LTC2655IGN-H12#PBF	LTC2655IGN-H12#TRPBF	655H12	16-Lead Narrow SSOP	–40°C to 85°C	±1
LTC2655CUF-H12#PBF	LTC2655CUF-H12#TRPBF	55H12	20-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C	±1
LTC2655IUF-H12#PBF	LTC2655IUF-H12#TRPBF	55H12	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C	±1

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2655B-L16/ LTC2655-L12 (Internal Reference=1.25V)

SYMBOL	PARAMETER	CONDITIONS		LTC2655-12 MIN	LTC2655-12 TYP	LTC2655-12 MAX	LTC2655B-16 MIN	LTC2655B-16 TYP	LTC2655B-16 MAX	UNITS
DC Performance										
	Resolution		●	12			16			Bits
	Monotonicity	(Note 3)	●	12			16			Bits
DNL	Differential Nonlinearity	(Note 3)	●		±0.1	±0.5		±0.3	±1	LSB
INL	Integral Nonlinearity (Note 3)	V_{CC} = 5.5V, V_{REF} = 2.5V	●		±0.5	±1		±2	±4	LSB
	Load Regulation	V_{CC} = 5V ±10%, Internal Reference, Mid-Scale, –15mA ≤ I_{OUT} ≤ 15mA	●		0.04	0.125		0.6	2	LSB/mA
		V_{CC} = 3V ±10%, Internal Reference, Mid-Scale, –7.5mA ≤ I_{OUT} ≤ 5mA	●		0.06	0.25		1	4	LSB/mA
ZSE	Zero-Scale Error		●		1	3		1	3	mV
V_{OS}	Offset Error	V_{REF} = 1.25V (Note 4)	●		±1	±2		±1	±2	mV
	V_{OS} Temperature Coefficient				5			5		µV/°C
GE	Gain Error		●		±0.02	±0.1		±0.02	±0.1	%FSR
	Gain Temperature Coefficient				1			1		ppm/°C

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	Internal Reference External Reference = V_{EXTREF}			0 to 2.5 0 to 2•V_{EXTREF}		V V
PSR	Power Supply Rejection	V_{CC} ±10%			–80		dB
R_{OUT}	DC Output Impedance	V_{CC} = 5V ±10%, Internal Reference, Mid-Scale, –15mA ≤ I_{OUT} ≤ 15mA V_{CC} = 3V ±10%, Internal Reference, Mid-Scale, –7.5mA ≤ I_{OUT} ≤ 7.5mA	● ●		0.04 0.04	0.15 0.15	Ω Ω
	DC Crosstalk (Note 5)	Due to Full-Scale Output Change Due to Load Current Change Due to Powering Down (per Channel)			±1.5 ±2 ±1		µV µV/mA µV
I_{SC}	Short-Circuit Output Current (Note 6)	V_{CC} = 5.5V V_{EXTREF} = 2.8V Code: Zero-Scale; Forcing Output to V_{CC} Code: Full-Scale; Forcing Output to GND	 ● ●	 20 20		 65 65	 mA mA
		V_{CC} = 2.7V V_{EXTREF} = 1.4V Code: Zero-Scale; Forcing Output to V_{CC} Code: Full-Scale; Forcing Output to GND	 ● ●	 10 10		 45 45	 mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2655B-L16/LTC2655-L12 (Internal Reference = 1.25V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference							
	Reference Output Voltage			1.248	1.25	1.252	V
	Reference Temperature Coefficient	(Note 7)			±2	±10	ppm/°C
	Reference Line Regulation	V_{CC} ±10%			–80		dB
	Reference Short-Circuit Current	V_{CC} = 5.5V, Forcing REFIN/OUT to GND	●		3	5	mA
	REFCOMP Pin Short-Circuit Current	V_{CC} = 5.5V, Forcing REFCOMP to GND	●		65	200	µA
	Reference Load Regulation	V_{CC} = 3V±10% or 5V±10%, I_{OUT} = 100µA Sourcing			40		mV/mA
	Reference Output Voltage Noise Density	$C_{REFCOMP}$ = $C_{REFIN/OUT}$ = 0.1µF, at f = 1kHz			30		nV/√Hz
	Reference Input Range	External Reference Mode (Note 14)	●	0.5		V_{CC}/2	V
	Reference Input Current		●		0.001	1	µA
	Reference Input Capacitance	(Note 9)			20		pF
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	2.7		5.5	V
I_{CC}	Supply Current (Note 8)	V_{CC} = 5V, Internal Reference On V_{CC} = 5V, Internal Reference Off V_{CC} = 3V, Internal Reference On V_{CC} = 3V, Internal Reference Off	● ● ● ●		1.7 1.3 1.6 1.2	2.5 2 2.2 1.7	mA mA mA mA
I_{SD}	Supply Current in Shutdown Mode (Note 8)	V_{CC} = 5V	●			3	µA
Digital I/O							
V_{IL}	Low Level Input Voltage (SDA and SCL)		●			0.3V_{CC}	V
V_{IH}	High Level Input Voltage (SDA and SCL)		●	0.7V_{CC}			V
$V_{IL(\overline{LDAC})}$	Low Level Input Voltage (LDAC)	V_{CC} = 4.5V to 5.5V	●			0.8	V
		V_{CC} = 2.7V to 4.5V	●			0.6	V
$V_{IH(\overline{LDAC})}$	High Level Input Voltage (LDAC)	V_{CC} = 3.6V to 5.5V	●	2.4			V
		V_{CC} = 2.7V to 3.6V	●	2			V
$V_{IL(CA)}$	Low Level Input Voltage (CA0 to CA2)	See Test Circuit 1	●			0.15V_{CC}	V
$V_{IH(CA)}$	High Level Input Voltage (CA0 to CA2)	See Test Circuit 1	●	0.85V_{CC}			V
R_{INH}	Resistance from CA*n* (*n* = 0,1,2) to V_{CC} to Set CA*n* = V_{CC}	See Test Circuit 2	●			10	kΩ
R_{INL}	Resistance from CAn (*n* = 0,1,2) to GND to Set CA*n* = GND	See Test Circuit 2	●			10	kΩ
R_{INF}	Resistance from CA*n* (*n* = 0,1,2) to V_{CC} or GND to Set Ca*n* = FLOAT	See Test Circuit 2	●	2			MΩ
V_{OL}	Low Level Output Voltage	Sink Current =3mA	●	0		0.4	V
t_{OF}	Output Fall Time	V_O = $V_{IH(MIN)}$ to V_O = $V_{IL(MAX)}$, C_B = 10pF to 400pF (Note 13)		20+0.1C_B		250	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns
I_{IN}	Input Leakage	0.1V_{CC} ≤ V_{IN} ≤ 0.9V_{CC}	●			1	µA
C_{IN}	I/O Pin Capacitance	(Note 9)	●			10	pF
C_B	Capacitance Load for Each Bus Line		●			400	pF
C_{CAn}	External Capacitive Load on Address Pins CA0, CA1 and CA2		●			10	pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2655B-H16/LTC2655-H12 (Internal Reference = 2.048V)

SYMBOL	PARAMETER	CONDITIONS		LTC2655-12 MIN	LTC2655-12 TYP	LTC2655-12 MAX	LTC2655B-16 MIN	LTC2655B-16 TYP	LTC2655B-16 MAX	UNITS
DC Performance										
	Resolution		●	12			16			Bits
	Monotonicity	(Note 3)	●	12			16			Bits
DNL	Differential Nonlinearity	(Note 3)	●		±0.1	±0.5		±0.3	±1	LSB
INL	Integral Nonlinearity (Note 3)	V_{CC} = 5.5V, V_{REF} = 2.5V	●		±0.5	±1		±2	±4	LSB
	Load Regulation	V_{CC} = 5V ±10%, Internal Reference, Mid-Scale, –15mA ≤ I_{OUT} ≤ 15mA	●		0.04	0.125		0.6	2	LSB/mA
ZSE	Zero-Scale Error		●		1	3		1	3	mV
V_{OS}	Offset Error	V_{REF} = 2.048V (Note 4)	●		±1	±2		±1	±2	mV
	V_{OS} Temperature Coefficient				5			5		µV/°C
GE	Gain Error		●		±0.02	±0.1		±0.02	±0.1	%FSR
	Gain Temperature Coefficient				1			1		ppm/°C

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	DAC Output Span	Internal Reference External Reference = V_{EXTREF}			0 to 4.096 0 to 2•V_{EXTREF}		V V
PSR	Power Supply Rejection	V_{CC} ±10%			–80		dB
R_{OUT}	DC Output Impedance	V_{CC} = 5V ±10%, Internal Reference, Mid-Scale, –15mA ≤ I_{OUT} ≤ 15mA	●		0.04	0.15	Ω
	DC Crosstalk	Due to Full Scale Output Change Due to Load Current Change Due to Powering Down (per Channel)			±1.5 ±2 ±1		µV µV/mA µV
I_{SC}	Short-Circuit Output Current (Note 4)	V_{CC} = 5.5V V_{EXTREF} = 2.8V Code: Zero-Scale; Forcing Output to V_{CC} Code: Full-Scale; Forcing Output to GND	 ● ●	 20 20		 65 65	 mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 4.5V to 5.5V, V_{OUT} unloaded unless otherwise specified.

LTC2655B-H16/LTC2655-H12 (Internal Reference = 2.048V)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference							
	Reference Output Voltage			2.044	2.048	2.052	V
	Reference Temperature Coefficient	(Note 7)			±2	±10	ppm/°C
	Reference Line Regulation	V_{CC} ±10%			–80		dB
	Reference Short-Circuit Current	V_{CC} = 5.5V, Forcing REFIN/OUT to GND	●		3	5	mA
	REFCOMP Pin Short-Circuit Current	V_{CC} = 5.5V, Forcing REFCOMP to GND	●		65	200	µA
	Reference Load Regulation	V_{CC} = 5V±10%, I_{OUT} = 100µA Sourcing			40		mV/mA
	Reference Output Voltage Noise Density	$C_{REFCOMP}$ = $C_{REFIN/OUT}$ = 0.1µF, at f = 1kHz			35		nV/√Hz
	Reference Input Range	External Reference Mode (Note 14)	●	0.5		V_{CC}/2	V
	Reference Input Current		●		0.001	1	µA
	Reference Input Capacitance	(Note 9)	●		20		pF
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance	●	4.5		5.5	V
I_{CC}	Supply Current (Note 8)	V_{CC} = 5V, Internal Reference On V_{CC} = 5V, Internal Reference Off	● ●		1.9 1.5	2.5 2	mA mA
I_{SD}	Supply Current in Shutdown Mode (Note 8)	V_{CC} = 5V	●			3	µA
Digital I/O							
V_{IL}	Low Level Input Voltage (SDA and SCL)		●			0.3V_{CC}	V
V_{IH}	High Level Input Voltage (SDA and SCL)		●	0.7V_{CC}			V
$V_{IL(\overline{LDAC})}$	Low Level Input Voltage ($\overline{LDAC}$)	V_{CC} = 4.5V to 5.5V	●			0.8	V
$V_{IH(\overline{LDAC})}$	High Level Input Voltage ($\overline{LDAC}$)	V_{CC} = 4.5V to 5.5V	●	2.4			V
$V_{IL(CA)}$	Low Level Input Voltage (CA0 to CA2)	See Test Circuit 1	●			0.15V_{CC}	V
$V_{IH(CA)}$	High Level Input Voltage (CA0 to CA2)	See Test Circuit 1	●	0.85V_{CC}			V
R_{INH}	Resistance from CAn (*n* = 0,1,2) to V_{CC} to Set CA*n* = V_{CC}	See Test Circuit 2	●			10	kΩ
R_{INL}	Resistance from CA*n* (*n* = 0,1,2) to GND to Set CA*n* = GND	See Test Circuit 2	●			10	kΩ
R_{INF}	Resistance from CA*n* (*n* = 0,1,2) to V_{CC} or GND to Set CA*n* = FLOAT	See Test Circuit 2	●	2			MΩ
V_{OL}	Low Level Output Voltage	Sink Current = 3mA	●	0		0.4	V
t_{OF}	Output Fall Time	V_O = $V_{IH(MIN)}$ to V_O = $V_{IL(MAX)}$, C_B = 10pF to 400pF (Note 13)	●	20+0.1C_B		250	ns
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		●	0		50	ns
I_{IN}	Input Leakage	0.1V_{CC} ≤ V_{IN} ≤ 0.9V_{CC}	●			1	µA
C_{IN}	I/O Pin Capacitance	(Note 9)	●			10	pF
C_B	Capacitance Load for Each Bus Line		●			400	pF
C_{CAn}	External Capacitive Load on Address Pins CA0, CA1 and CA2		●			10	pF

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V (LTC2655B-L16/LTC2655-L12), V_{CC} = 4.5V to 5.5V (LTC2655B-H16, LTC2655-H12), V_{OUT} unloaded unless otherwise specified.

LTC2655B-L16/LTC2655-L12/LTC2655B-H16/LTC2655-H12

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Performance							
t_S	Settling Time (Note 10)	±0.024%(±1LSB at 12 Bits) ±0.0015%(±1LSB at 16 Bits)			3.9 9.1		µs µs
	Settling Time for 1LSB Step	±0.024%(±1LSB at 12 Bits) ±0.0015%(±1LSB at 16 Bits)			2.4 4.5		µs µs
	Voltage Output Slew Rate				1.8		V/µs
	Capacitive Load Driving				1000		pF
	Glitch Impulse (Note 11)	At Mid-Scale Transition, -L Option			4		nV•s
		At Mid-Scale Transition, -H Option			7		nV•s
	DAC to DAC Crosstalk (Note 12)	$C_{REFCOMP}$ = $C_{REFIN/OUT}$ = 0.22µF			0.5		nV•s
	Multiplying Bandwidth				150		kHz
e_n	Output Voltage Noise Density	At f = 1kHz At f = 10kHz			85 80		nV/√Hz nV/√Hz
	Output Voltage Noise	0.1Hz to 10Hz, Internal Reference (-L Options) 0.1Hz to 10Hz, Internal Reference (-H Options) 0.1Hz to 200KHz, Internal Reference (-L Options) 0.1Hz to 200KHz, Internal Reference (-H Options)			8 12 400 450		μV_{P-P} μV_{P-P} μV_{P-P} μV_{P-P}

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V (LTC2655B-L16/LTC2655-L12), V_{CC} = 4.5V to 5.5V (LTC2655B-H16, LTC2655-H12), V_{OUT} unloaded unless otherwise specified.

LTC2655B-L16/LTC2655-L12/LTC2655B-H16/LTC2655-H12 (see Figure 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(STA)}$	Hold Time (Repeated) Start Condition		●	0.6			µs
t_{LOW}	Low Period of the SCL Clock Pin		●	1.3			µs
t_{HIGH}	High Period of the SCL Clock Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated Start Program		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
tr	Rise Time of Both SDA and SCL Signals	(Note 13)	●	20+0.1C_B		300	ns
tf	Fall Time of Both SDA and SCL Signals	(Note 13)	●	20+0.1C_B		300	ns
$t_{SU(STO)}$	Set-Up Time for Stop Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition		●	1.3			µs
t1	Falling edge of the 9th Clock of the 3rd Input Byte to $\overline{LDAC}$ High or Low Transition		●	400			ns
t2	$\overline{LDAC}$ Low Pulse Width		●	20			ns

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to GND.

Note 3: Linearity and monotonicity are defined from code k_L to code 2^N–1, where N is the resolution and k_L is the lower end code for which no output limiting occurs. For V_{REF} = 2.5V and N = 16, k_L = 128 and linearity is defined from code 128 to code 65535. For V_{REF} = 2.5V and N = 12, k_L =8 and linearity is defined from code 8 to code 4095.

Note 4: Inferred from measurement at code 128 (LTC2655-16), or code 8 (LTC2655-12).

Note 5: DC Crosstalk is measured with V_{CC} = 5V and using internal reference, with the measured DAC at mid-scale.

Note 6: This IC includes current limiting that is intended to protect the device during momentary overload conditions. Junction temperature can exceed the rated maximum during current limiting. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range. Maximum temperature coefficient is guaranteed for C-grade only.

Note 8: Digital inputs at 0V or V_{CC}.

Note 9: Guaranteed by design and not production tested.

Note 10: Internal Reference mode. DAC is stepped 1/4 scale to 3/4 scale and 3/4 scale to 1/4 scale. Load is 2kΩ in parallel with 200pF to GND.

Note 11: V_{CC} = 5V (-H Options) or V_{CC} = 3V (-L Options), internal reference mode. DAC is stepped ±1 LSB between half-scale and half-scale – 1. Load is 2kΩ n parallel with 200pF to GND.

Note 12: DAC to DAC Crosstalk is the glitch that appears at the output of one DAC due to a full scale change at the output of another DAC. It is measured with V_{CC} = 5V and using internal reference, with the measured DAC at mid-scale.

Note 13: C_B = Capacitance of one bus line in pF.

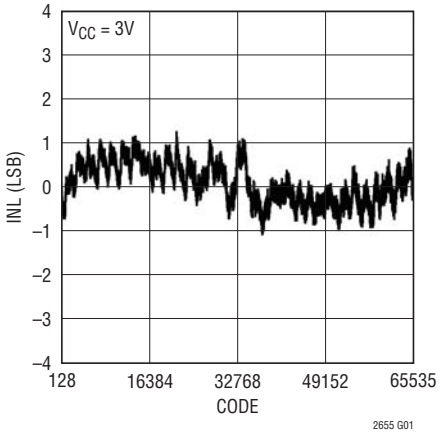
Note 14: Gain error specification may be degraded for reference input voltages less than 1V. See Gain Error vs Reference Input Curve in the Typical Performance Characteristics section.

TYPICAL PERFORMANCE CHARACTERISTICS

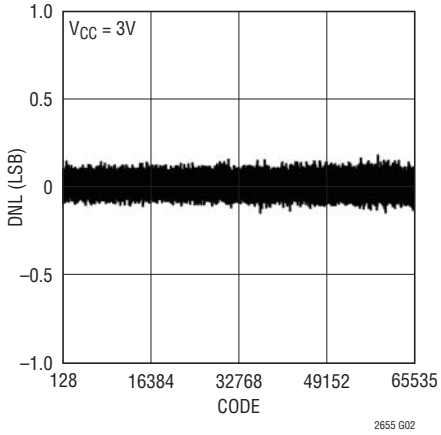
T_A = 25°C unless otherwise noted.

LTC2655-L16

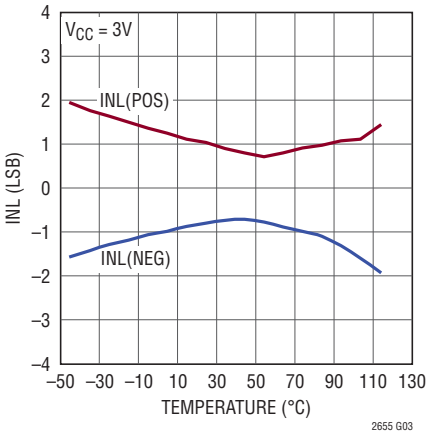
Integral Nonlinearity (INL)



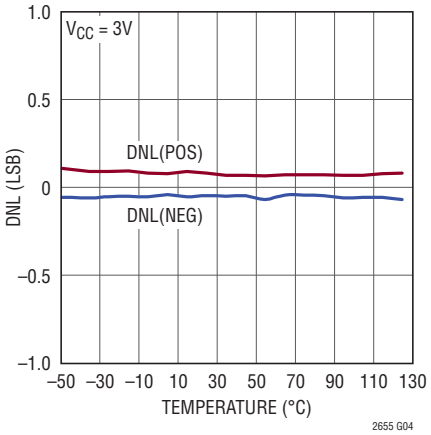
Differential Nonlinearity (DNL)



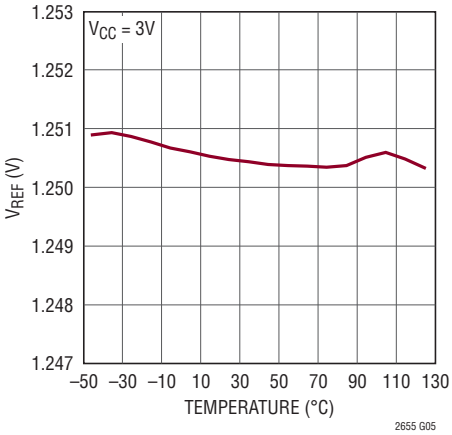
INL vs Temperature



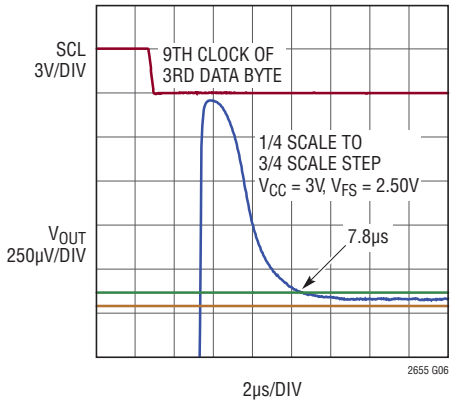
DNL vs Temperature



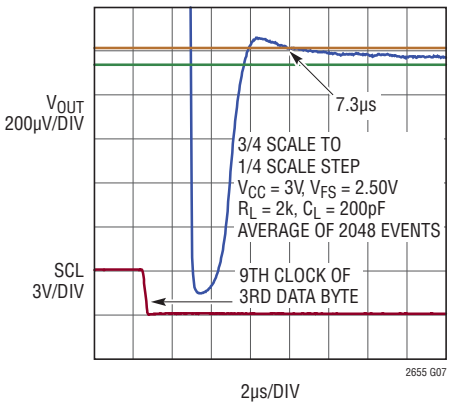
REFIN/OUT Output Voltage vs Temperature



Settling to ±1LSB Rising



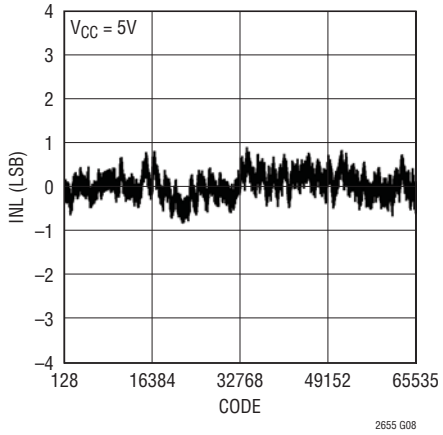
Settling to ±1LSB Falling



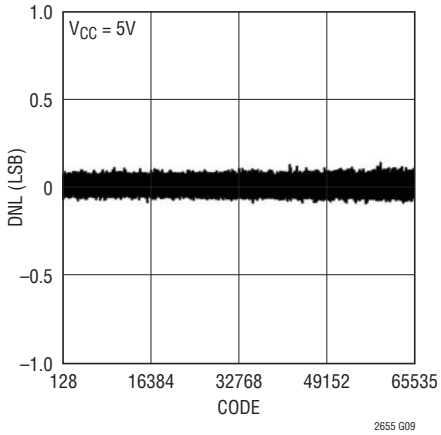
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

LTC2655-H16

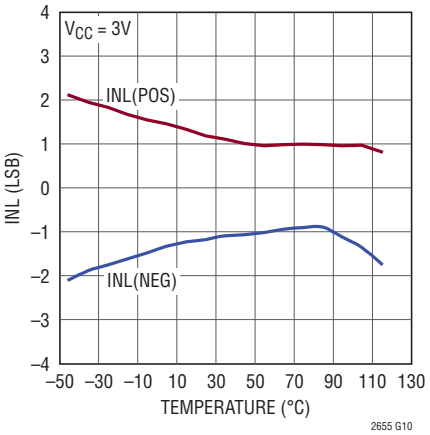
Integral Nonlinearity (INL)



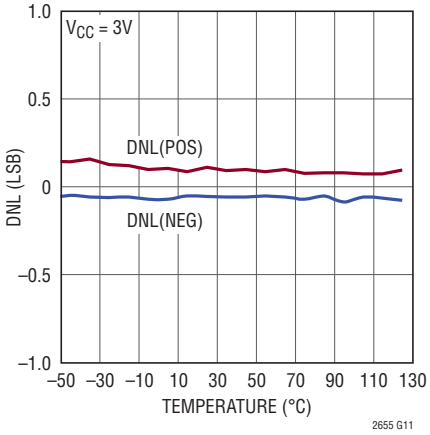
Differential Nonlinearity (DNL)



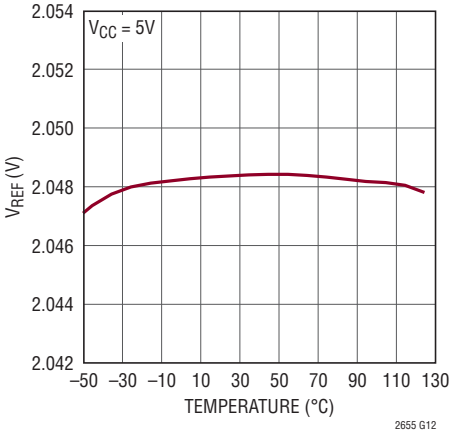
INL vs Temperature



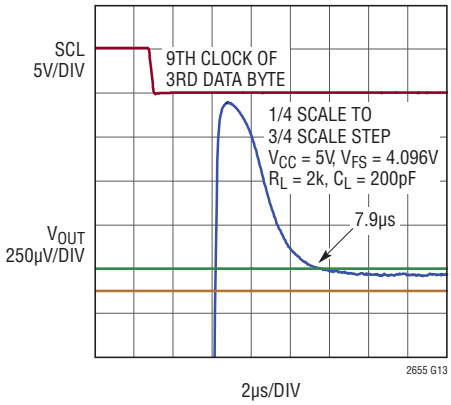
DNL vs Temperature



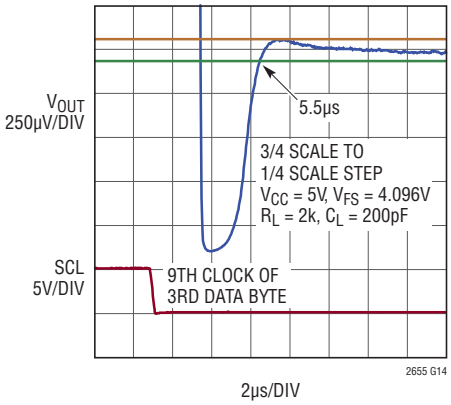
Reference Output Voltage vs Temperature



Settling to ±1LSB Rising



Settling to ±1LSB Falling

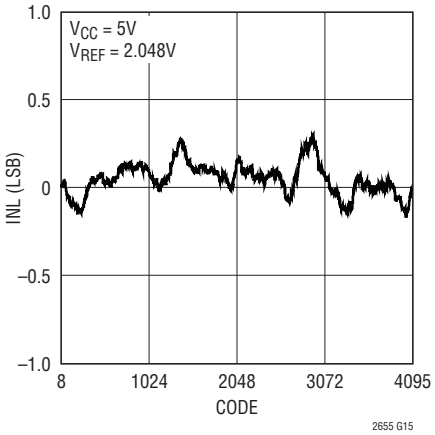


TYPICAL PERFORMANCE CHARACTERISTICS

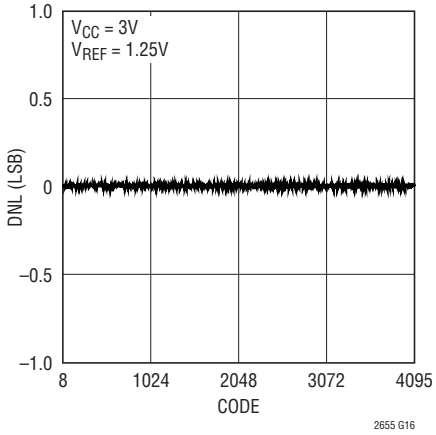
T_A = 25°C unless otherwise noted.

LTC2655-12

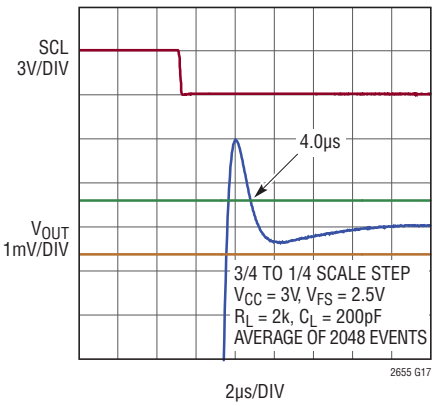
Integral Nonlinearity (INL)



Differential Nonlinearity (INL)

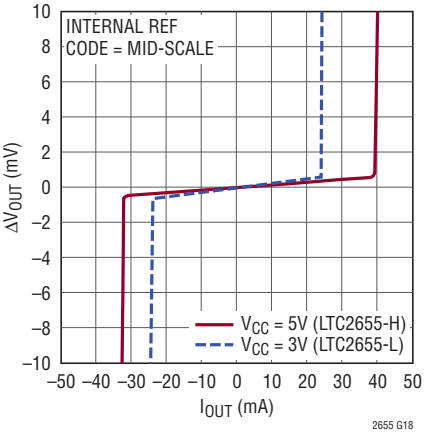


Settling to ±1LSB Falling

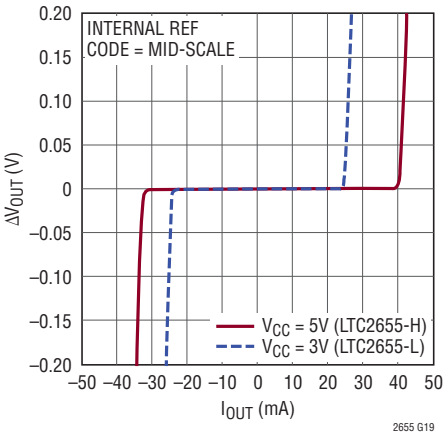


LTC2655

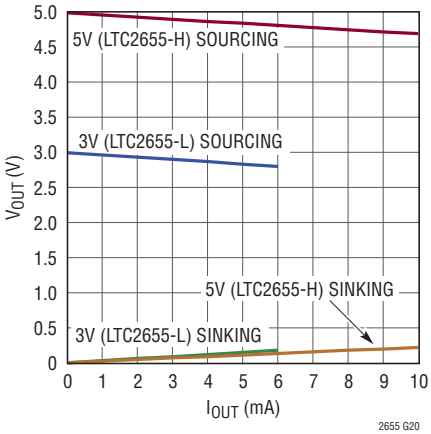
Load Regulation



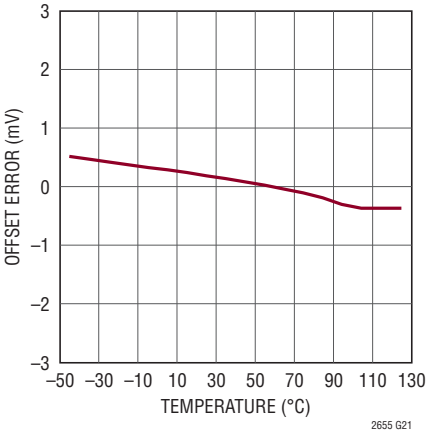
Current Limiting



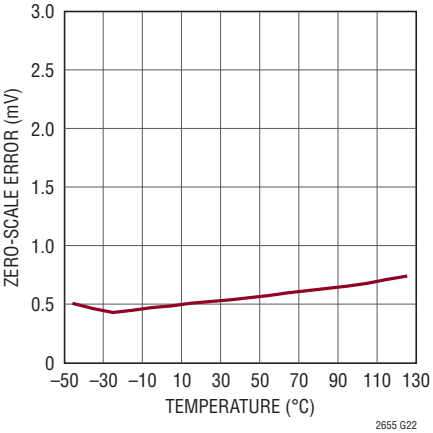
Headroom at Rails vs Output Current



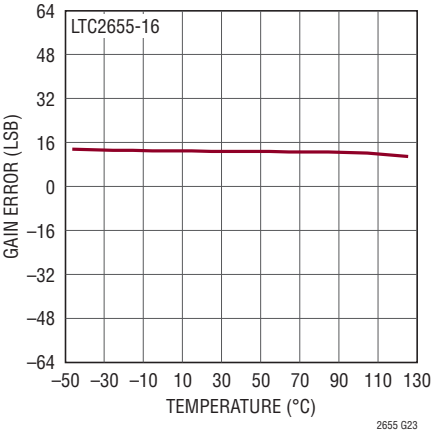
Offset Error vs Temperature



Zero-Scale Error vs Temperature



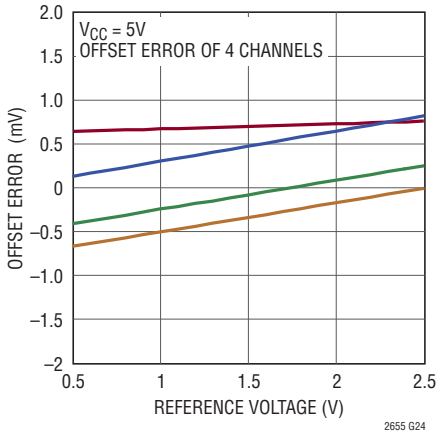
Gain Error vs Temperature



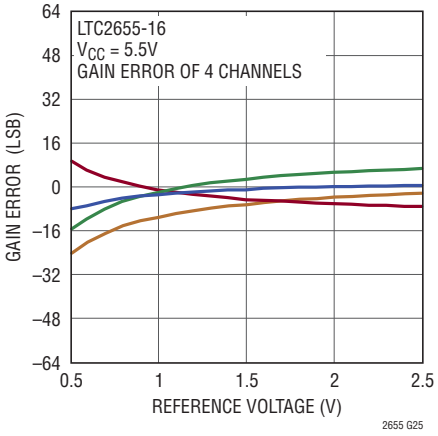
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

LTC2655

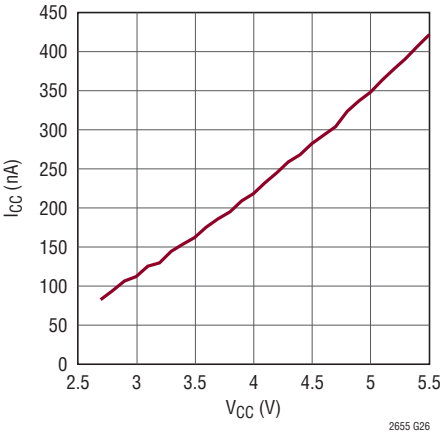
Offset Error vs Reference Input



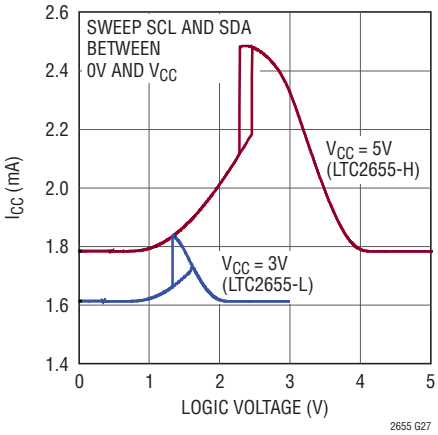
Gain Error vs Reference Input



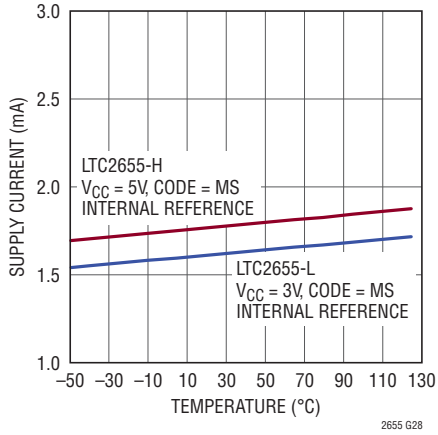
I_{CC} Shutdown vs V_{CC}



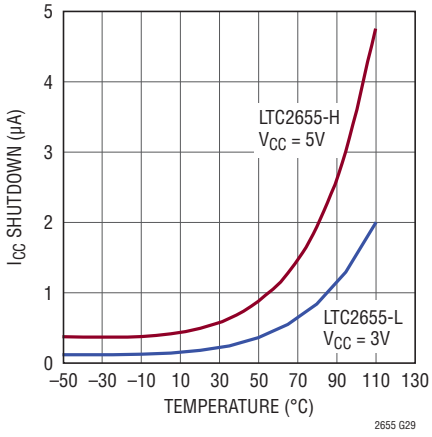
Supply Current vs Logic Voltage



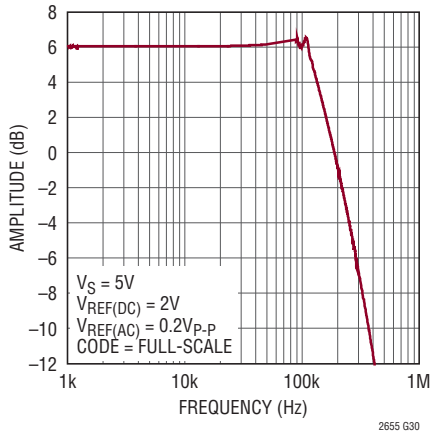
Supply Current vs Temperature



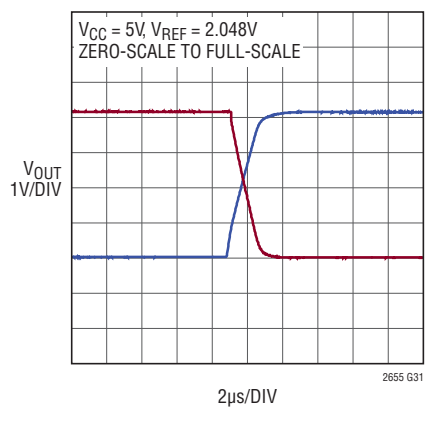
I_{CC} Shutdown vs Temperature



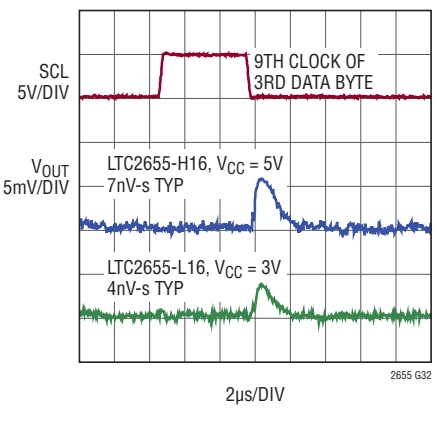
Multiplying Bandwidth



Large-Signal Response



Mid-Scale Glitch Impulse

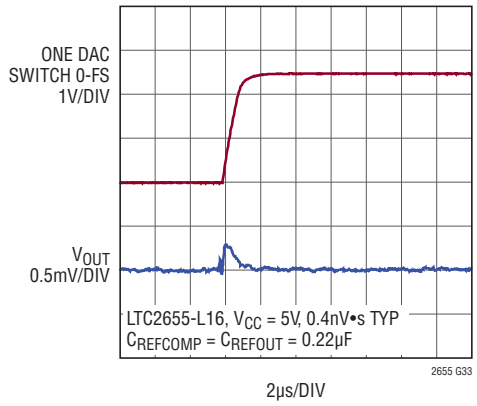


TYPICAL PERFORMANCE CHARACTERISTICS

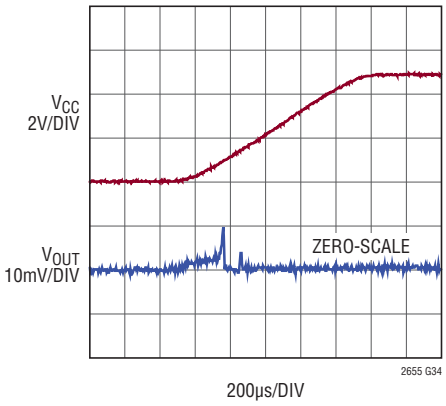
T_A = 25°C unless otherwise noted.

LTC2655

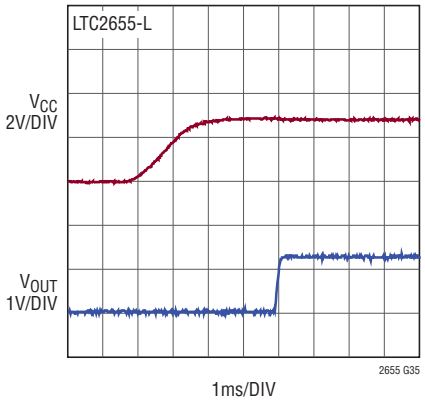
DAC to DAC Crosstalk (Dynamic)



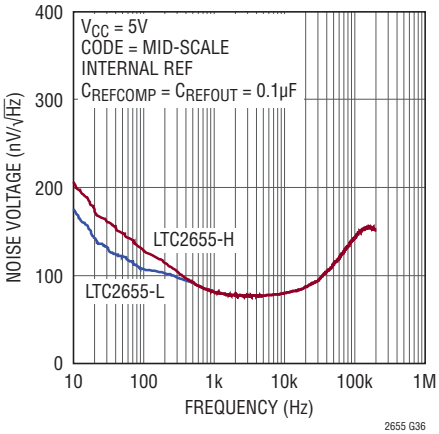
Power-On Reset Glitch



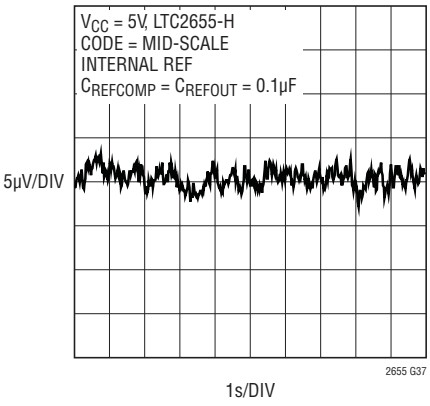
Power-On Reset to Mid-Scale



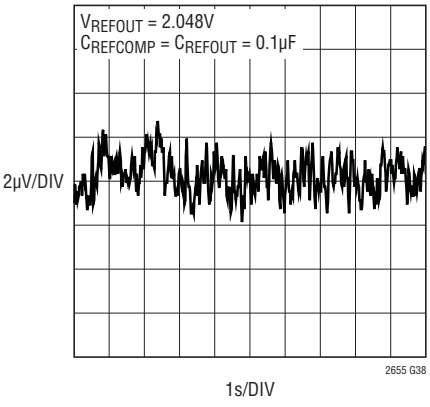
Noise Voltage vs Frequency



DAC Output 0.1Hz to 10Hz Voltage Noise



Reference 0.1Hz to 10Hz Voltage Noise



PIN FUNCTIONS (GN/UF)

REFLO (Pin 1/Pin 20): Reference Low. The voltage at this pin sets the zero-scale voltage of all DACs. This pin should be tied to GND.

V_{OUTA} to V_{OUTD} (Pins 2,4,13,14/Pins 1, 3, 13, 14): DAC Analog Voltage Outputs. The output range is 0V to 2 times the voltage at the REFIN/OUT pin.

REFCOMP (Pin 3/Pin 2): Internal Reference Compensation. For low noise and reference stability, tie 0.1µF capacitor to GND. Connect to GND to use an external reference at start-up. Command 0111b must still be issued to turn off internal reference.

REFIN/OUT (Pin 5/Pin 4): This pin acts as the internal reference output in internal reference mode and acts as the reference input pin in external reference mode. When acting as an output the nominal voltage at this pin is 1.25V for -L options and 2.048V for -H options. For low noise and reference stability tie a capacitor from this pin to GND. Capacitor value must be ≤ $C_{REFCOMP}$. In external reference mode, the allowable reference input voltage range is 0.5V to $V_{CC}/2$.

$\overline{LDAC}$ (Pin 6/Pin 5): Asynchronous DAC Update. A falling edge on this input after four bytes have been written into the part, immediately updates the DAC register with the contents of the input register. A low on this input without a complete 32-bit (four bytes including the slave address) data write transfer to the part does not update the DAC output. Software power-down is disabled when $\overline{LDAC}$ is low.

CA2 (Pin 7/Pin 6): Chip Address Bit 2. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 2).

SCL (Pin 8/Pin 7): Serial Clock Input. Data is shifted into the SDA pin at the rising edges of the clock. This high impedance pin requires a pull-up resistor or current source to V_{CC}.

SDA (Pin 9/Pin 9): Serial Data Bidirectional. Data is shifted into the SDA pin and acknowledged by the SDA pin. This is a high impedance pin while data is shifted in. It is an open-drain N-channel output during acknowledgement. This pin requires a pull-up resistor or current source to V_{CC}.

CA1 (Pin 10/Pin 10): Chip Address Bit 1. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 2).

CA0 (Pin 11/Pin 11): Chip Address Bit 0. Tie this pin to V_{CC}, GND or leave it floating to select an I^2C slave address for the part (Table 2).

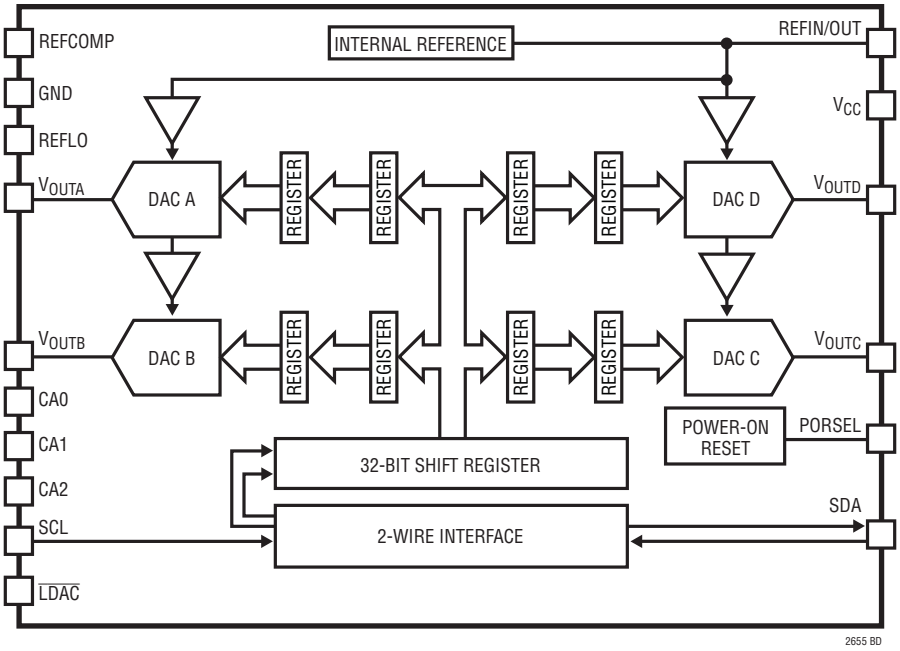
PORSEL (Pin 12/Pin 12): Power-On-Reset Select. If tied to GND, the part resets to zero-scale at power-up, if tied to V_{CC}, the part resets to mid-scale.

V_{CC} (Pin 15/Pin 18): Supply Voltage Input. For -L options, 2.7V ≤ V_{CC} ≤ 5.5V, and for -H options, 4.5V ≤ V_{CC} ≤ 5.5V. Bypass to ground with a 0.1µF capacitor placed as close to pin as possible.

GND (Pin 16/Pin 19, Exposed Pad Pin 21): Ground. Must be soldered to PCB Ground.

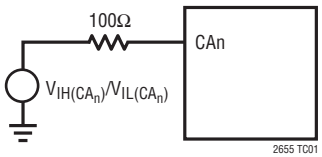
DNC (NA/Pins 8, 15, 16, 17): Do not connect these pins.

BLOCK DIAGRAM

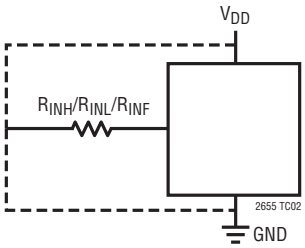


TEST CIRCUITS

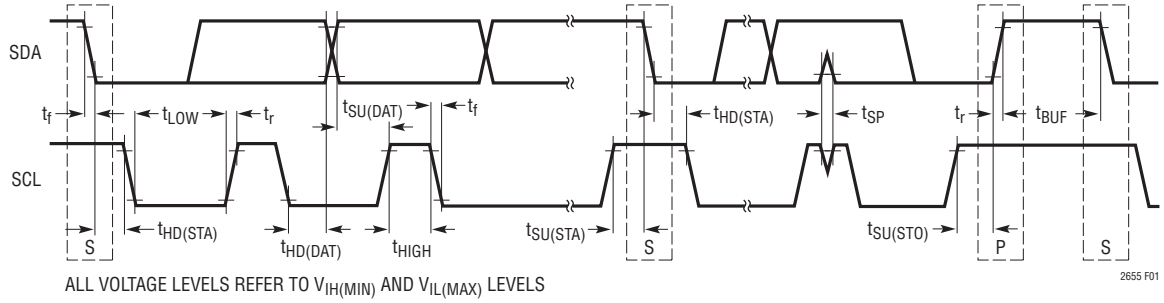
Test Circuit 1



Test Circuit 2



TIMING DIAGRAM



ALL VOLTAGE LEVELS REFER TO $V_{IH(MIN)}$ AND $V_{IL(MAX)}$ LEVELS

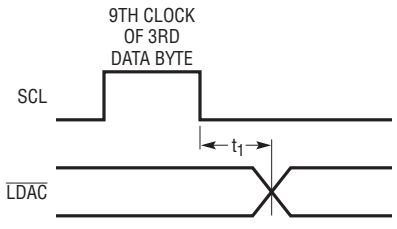


Figure 1

OPERATION

The LTC2655 is a family of quad voltage output DACs in 20-lead 4mm × 4mm QFN and in 16-lead narrow SSOP packages. Each DAC can operate rail-to-rail in external reference mode, or with its full-scale voltage set by an integrated reference. Four combinations of accuracy (16-bit and 12-bit), and full-scale voltage (2.5V or 4.096V) are available. The LTC2655 is controlled using a 2-wire I^2C compatible interface.

Power-On Reset

The LTC2655-L/LTC2655-H clear the output to zero-scale if PORSEL pin is tied to GND, when power is first applied, making system initialization consistent and repeatable. For some applications, downstream circuits are active during DAC power-up, and may be sensitive to nonzero outputs from the DAC during this time. The LTC2655 contains circuitry to reduce the power-on glitch. The analog outputs typically rise less than 10mV above zero-scale during power on if the power supply is ramped to 5V in 1ms or more. In general, the glitch amplitude decreases as the power supply ramp time is increased. See Power-On Reset Glitch in the Typical Performance Characteristics section.

Alternatively, if PORSEL pin is tied to V_{CC}, The LTC2655-L/LTC2655-H set the output to mid-scale when power is first applied.

Power Supply Sequencing and Start-Up

For the LTC2655 family of parts, the internal reference is powered up at start-up by default. If an external reference is to be used, REFCOMP (Pin 3/Pin 2, GN/UF) must be hardwired to GND. This configuration allows the use of an external reference at start-up and converts the REFIN/OUT pin to an input. However, the internal reference will still be ON and draw supply current. In order to use an external reference, command 0111b should be used to turn the internal reference off (see Table 1).

The voltage at REFIN/OUT (Pin 5/Pin 4, GN/UF) should be kept within the range – 0.3V ≤ REFIN/OUT ≤ V_{CC} + 0.3V (see the Absolute Maximum Ratings section). Particular care should be taken to observe these limits during power supply turn-on and turn-off sequences, when the voltage at V_{CC} (Pin 15/Pin 18, GN/UF) is in transition.

Transfer Function

The digital-to-analog transfer function is

$$V_{OUT(IDEAL)} = 2 \bullet k/2^N [V_{REF} – REFLO] + REFLO$$

where k is the decimal equivalent of the binary DAC input code, N is the resolution, and V_{REF} is the voltage at the REFIN/OUT Pin. The resulting DAC output span is 0V to $2 \bullet V_{REF}$, as it is necessary to tie REFLO to GND. V_{REF} is nominally 1.25V for LTC2655-L and 2.048V for LTC2655-H, in internal reference mode.

Table 1

COMMAND*				
C3	**C2**	**C1**	**C0**	
0	0	0	0	Write to Input Register *n*
0	0	0	1	Update (Power-Up) DAC Register *n*
0	0	1	0	Write to Input Register *n*, Update (Power-Up) All
0	0	1	1	Write to and Update (Power-Up) *n*
0	1	0	0	Power-Down *n*
0	1	0	1	Power-Down Chip (All DAC's and Reference)
0	1	1	0	Select Internal Reference (Power-Up Reference)
0	1	1	1	Select External Reference (Power-Down Reference)
1	1	1	1	No Operation
ADDRESS (*n*)*				
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
1	1	1	1	All DACs

* Command and address codes not shown are reserved and should not be used.

Serial Interface

The LTC2655 communicates with a host using the standard 2-wire I^2C interface. The Timing Diagram (Figure 1) shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The value of these pull-up resistors is dependent on the power supply and can be obtained from the I^2C specifications. For an I^2C bus operating in the fast mode, an active pull-up will be

OPERATION

necessary if the bus capacitance is greater than 200pF. The LTC2655 is a receive-only (slave) device. The master can write to the LTC2655. The LTC2655 does not respond to a read command from the master.

The START (S) and STOP (P) Conditions

When the bus is not in use, both SCL and SDA must be high. A bus master signals the beginning of a communication to a slave device by transmitting a START condition (see Figure 1). A START condition is generated by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition. A STOP condition is generated by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I^2C device.

Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active LOW) generated by the slave lets the master know that the latest byte of information was received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the Acknowledge clock pulse. The slave-receiver must pull down the SDA bus line during the Acknowledge clock pulse so that it remains a stable LOW during the HIGH period of this clock pulse. The LTC2655 responds to a write by a master in this manner. The LTC2655 does not acknowledge a read (retains SDA HIGH during the period of the Acknowledge clock pulse).

Chip Address

The state of CA0, CA1 and CA2 decides the slave address of the part. The pins CA0, CA1 and CA2 can be each set to any one of three states: V_{CC}, GND or float. This results in 27 selectable addresses for the part. The slave address assignments are shown in Table 2.

In addition to the address selected by the address pins, the parts also respond to a global address. This address allows a common write to all LTC2655 parts to be accomplished with one 3-byte write transaction on the I^2C bus.

The global address is a 7-bit on-chip hardwired address and is not selectable by CA0, CA1 and CA2. The addresses corresponding to the states of CA0, CA1 and CA2 and the global address are shown in Table 2. The maximum capacitive load allowed on the address pins (CA0, CA1 and CA2) is 10pF, as these pins are driven during address detection to determine if they are floating.

Table 2. Slave Address Map

CA2	CA1	CA0	A6	A5	A4	A3	A2	A1	A0
GND	GND	GND	0	0	1	0	0	0	0
GND	GND	FLOAT	0	0	1	0	0	0	1
GND	GND	V_{CC}	0	0	1	0	0	1	0
GND	FLOAT	GND	0	0	1	0	0	1	1
GND	FLOAT	FLOAT	0	1	0	0	0	0	0
GND	FLOAT	V_{CC}	0	1	0	0	0	0	1
GND	V_{CC}	GND	0	1	0	0	0	1	0
GND	V_{CC}	FLOAT	0	1	0	0	0	1	1
GND	V_{CC}	V_{CC}	0	1	1	0	0	0	0
FLOAT	GND	GND	0	1	1	0	0	0	1
FLOAT	GND	FLOAT	0	1	1	0	0	1	0
FLOAT	GND	V_{CC}	0	1	1	0	0	1	1
FLOAT	FLOAT	GND	1	0	0	0	0	0	0
FLOAT	FLOAT	FLOAT	1	0	0	0	0	0	1
FLOAT	FLOAT	V_{CC}	1	0	0	0	0	1	0
FLOAT	V_{CC}	GND	1	0	0	0	0	1	1
FLOAT	V_{CC}	FLOAT	1	0	1	0	0	0	0
FLOAT	V_{CC}	V_{CC}	1	0	1	0	0	0	1
V_{CC}	GND	GND	1	0	1	0	0	1	0
V_{CC}	GND	FLOAT	1	0	1	0	0	1	1
V_{CC}	GND	V_{CC}	1	1	0	0	0	0	0
V_{CC}	FLOAT	GND	1	1	0	0	0	0	1
V_{CC}	FLOAT	FLOAT	1	1	0	0	0	1	0
V_{CC}	FLOAT	V_{CC}	1	1	0	0	0	1	1
V_{CC}	V_{CC}	GND	1	1	1	0	0	0	0
V_{CC}	V_{CC}	FLOAT	1	1	1	0	0	0	1
V_{CC}	V_{CC}	V_{CC}	1	1	1	0	0	1	0
GLOBAL ADDRESS			1	1	1	0	0	1	1

OPERATION

Write Word Protocol

The master initiates communication with the LTC2655 with a START condition and a 7-bit slave address followed by the Write bit (W) = 0. The LTC2655 acknowledges by pulling the SDA pin low at the 9th clock if the 7-bit slave address matches the address of the part (set by CA0, CA1 and CA2) or the global address. The master then transmits three bytes of write data. The LTC2655 acknowledges each byte of data by pulling the SDA line low at the 9th clock of each data byte transmission. After receiving three complete bytes of data, the LTC2655 executes the command specified in the 24-bit input word. If more than three data bytes are transmitted after a valid 7-bit slave address, the LTC2655 does not acknowledge the extra bytes of data (SDA is high during the 9th clock). The first byte of the input word consists of the 4-bit command followed by the 4-bit address. The next two bytes consist of the 16-bit data word. The 16-bit data word consists of the 16-bit, or 12-bit input code, MSB to LSB, followed by 0 or 4 don't care bits (LTC2655-16 and LTC2655-12 respectively). A typical LTC2655 write transaction is shown in Figure 2. The command (C3-C0) and address (A3-A0) assignments are shown in Table 1. The first four commands in the table consist of write and update operations. A write operation loads a 16-bit data word from the 32-bit shift register into the input register. In an update operation, the data word is copied from the input register to the DAC register and converted to an analog voltage at the DAC output. The update operation also powers up the DAC if it had been in power-down mode. The data path and registers are shown in the Block Diagram.

Power-Down Mode

For power-constrained applications, power-down mode can be used to reduce the supply current whenever less than four outputs are needed. When in power-down, the buffer amplifiers, bias circuits and integrated reference circuits are disabled, and draw essentially zero current. The DAC outputs are put into a high-impedance state, and the output pins are passively pulled to ground through individual 80k resistors. Input- and DAC-register contents are not disturbed during power-down.

Any channel or combination of channels can be put into power-down mode by using command 0100b in combination with the appropriate DAC address, (*n*). The integrated reference is automatically powered down when external reference mode is selected using command 0111b. In addition, all the DAC channels and the integrated reference together can be put into power-down mode using the Power-Down Chip command 0101b. For all power-down commands the 16-bit data word is ignored, but still required in order to complete a full communication cycle.

Normal operation resumes by executing any command which includes a DAC update, in software as shown in Table 1 or using the asynchronous LDAC pin. The selected DAC is powered up as its voltage output is updated. When a DAC which is in a powered-down state is powered up and updated, normal settling is delayed. If less than four DACs are in a powered-down state prior to the update command, the power-up delay time is approximately 12µs. If on the other hand, all four DACs and the integrated reference are powered down, then the main bias generation circuit block has been automatically shut down in addition to the individual DAC amplifiers and the integrated reference.

OPERATION

In this case, the power-up delay time is approximately 14µs. The power-up of the integrated reference depends on the command that powered it down. If the reference is powered down using the Select External Reference command (0111b), then it can only be powered back up by sending the Select Internal Reference command (0110b). However if the reference was powered down by sending the Power-Down Chip command (0101b), then in addition to the Select Internal Reference command (0110b), any command that powers up the DACs will also power-up the integrated reference.

Reference Modes

For applications where an accurate external reference is not available, the LTC2655 has a user-selectable, integrated reference. The LTC2655-L has a 1.25V reference that provides a full-scale output of 2.5V. The LTC2655-H has a 2.048V reference that provides a full-scale output of 4.096V. Both references exhibit a typical temperature drift of 2ppm/°C. Internal reference mode can be selected by using command 0110b, and is the power-on default. A buffer is needed if the internal reference is required to drive external circuitry. For reference stability and low noise, it is recommended that a 0.1µF capacitor be tied between REFCOMP and GND. In this configuration, the internal reference can drive up to 0.1µF capacitive load without any stability problems. In order to ensure stable operation, the capacitive load on the REFIN/OUT pin should not exceed the capacitive load on the REFCOMP pin.

The DAC can also operate in external reference mode using command 0111b. In this mode, the REFIN/OUT pin acts as an input that sets the DAC's reference voltage. This input is high impedance and does not load the external reference source. The acceptable voltage range at this pin is 0.5V ≤ REFIN/OUT ≤ V_{CC}/2. The resulting full-scale output voltage is 2•$V_{REFIN/OUT}$. For using external reference at start-up, see the Power Supply Sequencing and Start-Up Sections.

Integrated Reference Buffers

Each of the four DACs in LTC2655 has its own integrated high performance reference buffer. The buffers have very high input impedance and do not load the reference voltage source. These buffers shield the reference voltage from glitches caused by DAC switching and thus minimize DAC-to-DAC dynamic crosstalk. By tying 0.22µF capacitors between REFCOMP and GND, and also between REFIN/OUT and GND, the crosstalk can be reduced to less than 1nV•s. See the curve DAC-to-DAC Crosstalk (Dynamic) in the Typical Performance Characteristics section.

Voltage Outputs

Each of the four rail-to-rail amplifiers contained in LTC2655 has guaranteed load regulation when sourcing or sinking up to 15mA at 5V (7.5mA at 3V).

Load regulation is a measure of the amplifier's ability to maintain the rated voltage accuracy over a wide range of load conditions. The measured change in output voltage per milliampere of forced load current change is expressed in LSB/mA.

DC output impedance is equivalent to load regulation, and may be derived from it by simply calculating a change in units from LSB/mA to ohms. The amplifiers' DC output impedance is 0.040Ω when driving a load well away from the rails.

When drawing a load current from either rail, the output voltage headroom with respect to that rail is limited by the 30Ω typical channel resistance of the output devices; e.g., when sinking 1mA, the minimum output voltage = 30Ω • 1mA = 30mV. See the graph Headroom at Rails vs Output Current in the Typical Performance Characteristics section.

The amplifiers are stable driving capacitive loads of up to 1000pF.

OPERATION

Board Layout

The excellent load regulation and DC crosstalk performance of these devices is achieved in part by keeping signal and power grounds separate.

The PC board should have separate areas for the analog and digital sections of the circuit. This keeps digital signals away from sensitive analog signals and facilitates the use of separate digital and analog ground planes which have minimal capacitive and resistive interaction with each other.

Digital and analog ground planes should be joined at only one point, establishing a system star ground as close to the device's ground pin as possible. Ideally, the analog ground plane should be located on the component side of the board, and should be allowed to run under the part to shield it from noise. Analog ground should be a continuous and uninterrupted plane, except for necessary lead pads and vias, with signal traces on another layer.

The GND pin functions as a return path for power supply currents in the device and should be connected to analog ground. The REFLO pin should be connected to system star ground. Resistance from the REFLO pin to system star ground should be as low as possible.

Rail-to-Rail Output Considerations

In any rail-to-rail voltage output device, the output is limited to voltages within the supply range.

Since the analog outputs of the device cannot go below ground, they may limit for the lowest codes as shown in Figure 3b. Similarly, limiting can occur in external reference mode near full scale when the REFIN/OUT pin is at $V_{CC}/2$. If $V_{REFIN/OUT} = V_{CC}/2$ and the DAC full-scale error (FSE) is positive, the output for the highest codes limits at V_{CC} as shown in Figure 3c. No full-scale limiting can occur if $V_{REFIN/OUT} \leq (V_{CC} – F_{SE})/2$.

Offset and linearity are defined and tested over the region of the DAC transfer function where no output limiting can occur.

OPERATION

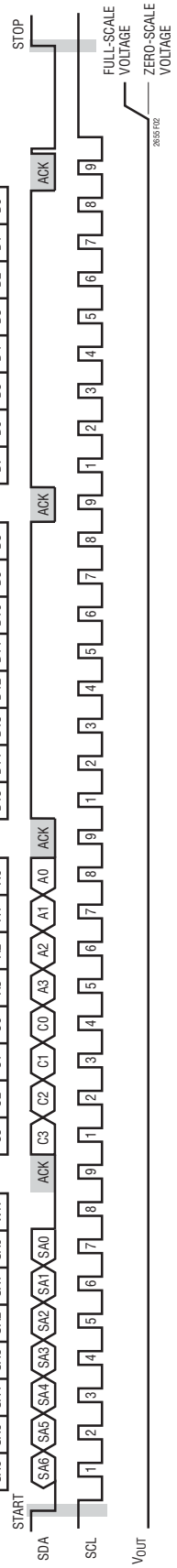


Figure 2. Typical LTC2655 Input Waveform—Programming DAC Output for Full-Scale

OPERATION

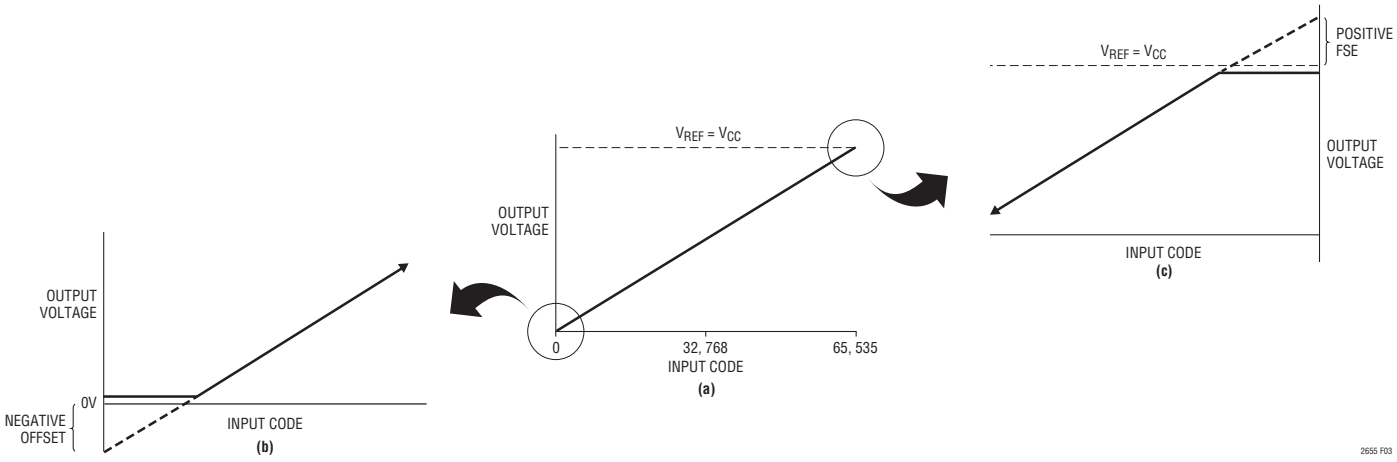
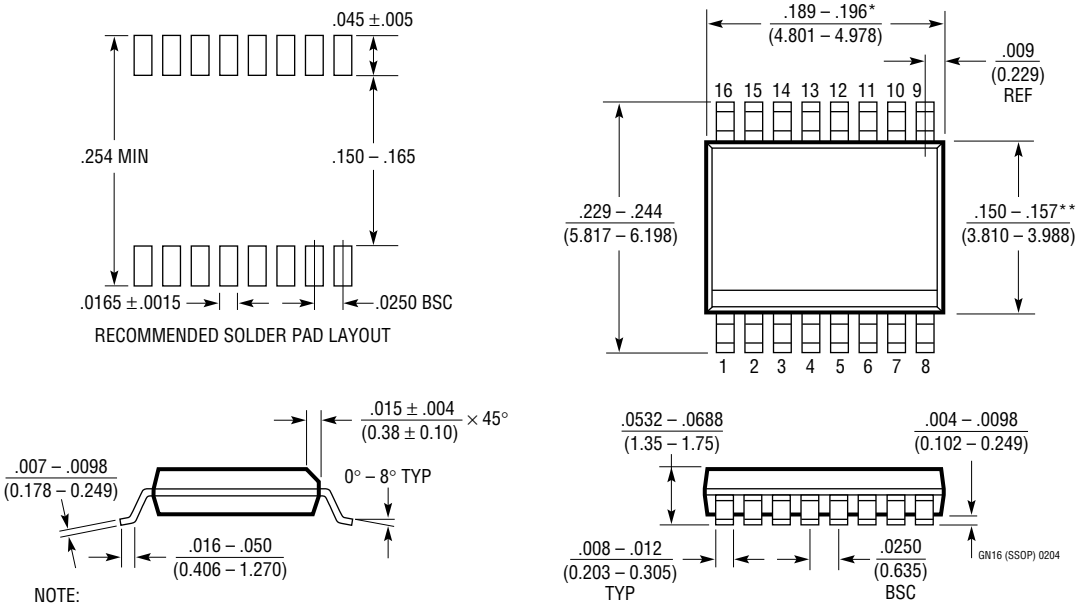


Figure 3. Effects of Rail-to-Rail Operation On a DAC Transfer Curve. (a) Overall Transfer Function, (b) Effect of Negative Offset for Codes Near Zero-Scale, (c) Effect of Positive Full-Scale Error for Codes Near Full-Scale

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP
(Reference LTC DWG # 05-08-1641)



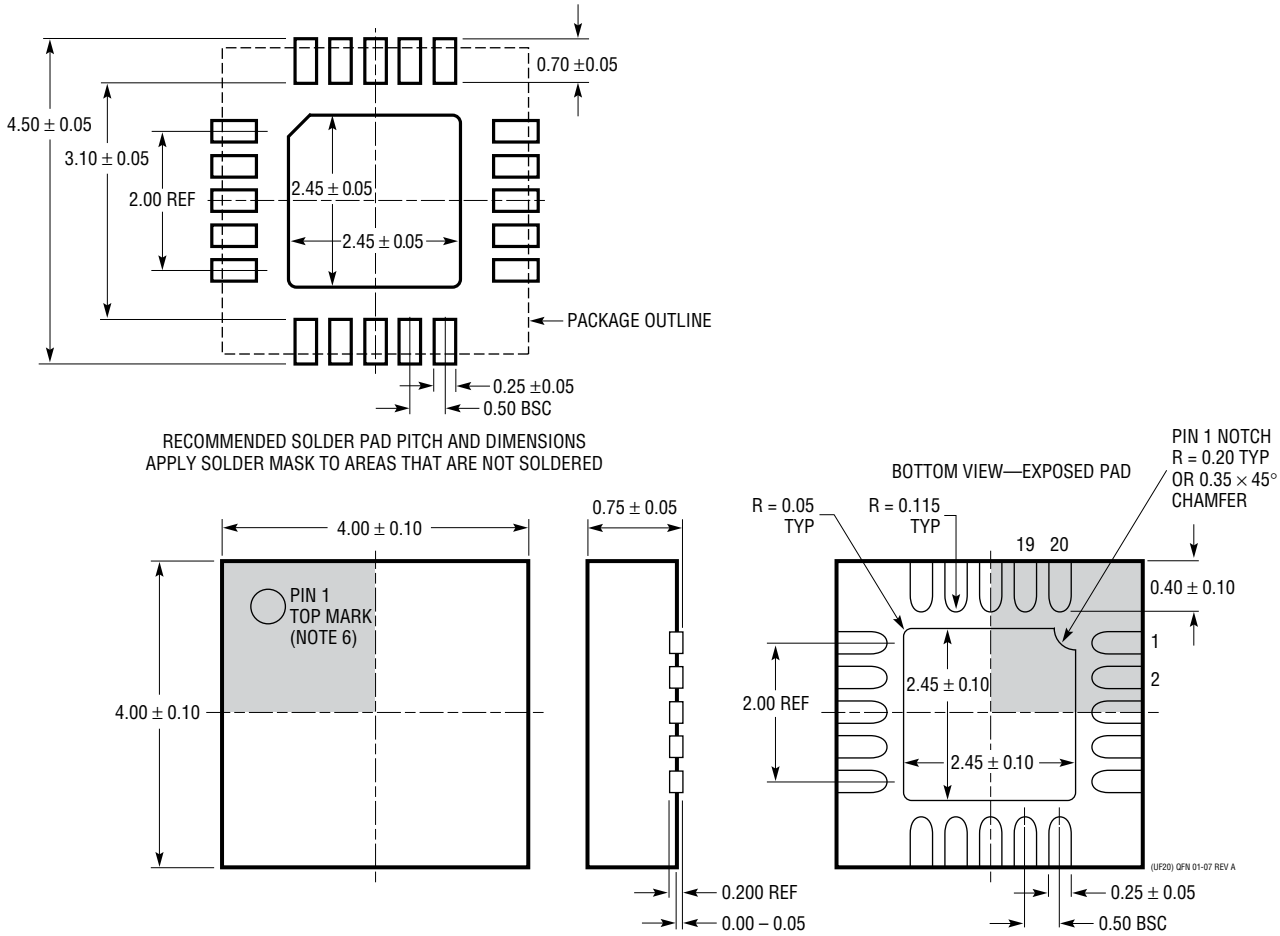
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

UF Package
20-Lead (4mm × 4mm) Plastic QFN
(Reference LTC DWG # 05-08-1710 Rev A)

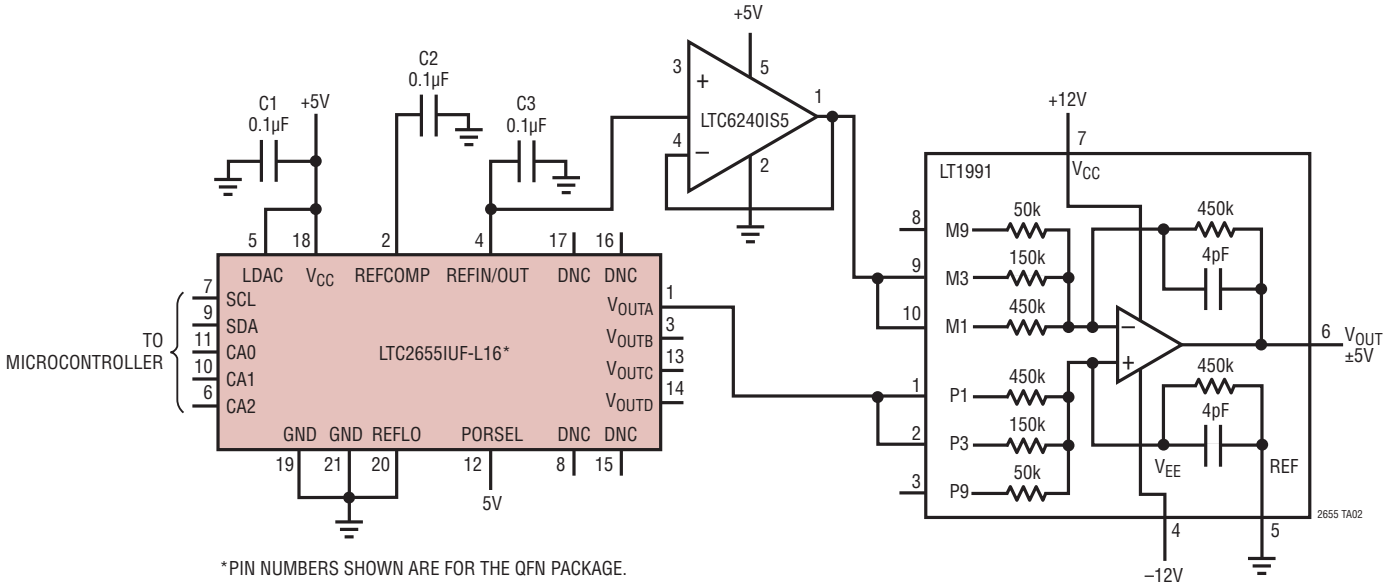


NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

±5V Bipolar Output DAC



*PIN NUMBERS SHOWN ARE FOR THE QFN PACKAGE.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2609/LTC2619/ LTC2629	Quad 16-/14-/12-Bit I²C V_{OUT} DACs	250µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output with Separate V_{REF} Pins for Each DAC, SSOP-16 Package
LTC2605/LTC2615/ LTC2625	Octal 16-/14-/12-Bit I²C V_{OUT} DACs	250µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, SSOP-16 Package
LTC2607/LTC2617/ LTC2627	Dual 16-/14-/12-Bit I²C V_{OUT} DACs	260µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, 3mm × 4mm DFN-12 Package
LTC2606/LTC2616/ LTC2626	Single 16-/14-/12-Bit I²C V_{OUT} DACs	270µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, 3mm × 3mm DFN-10 Package
LTC2654	Quad 16-/12-Bit SPI V_{OUT} DACs with 10ppm/°C (Max) Reference	±4LSB INL, ±1LSB DNL, 4mm × 4mm QFN-20, Narrow SSOP-16 Packages
LTC2656/LTC2657	Octal 16-/12-Bit SPI/I²C V_{OUT} DACs with 10ppm/°C (Max) Reference	±4LSB INL, ±1LSB DNL, 4mm × 5mm QFN-20, TSSOP-20 Packages
LTC2634/LTC2635	Quad 12-/10-/8-Bit SPI/I²C V_{OUT} DACs with 10ppm/°C (Typ) Reference	125µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, 3mm × 3mm QFN-16 and MSOP-10 Packages
LTC2636/LTC2637	Octal 12-/10-/8-Bit SPI/I²C V_{OUT} DACs with 10ppm/°C (Typ) Reference	125µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, 4mm × 3mm DFN-14 and MSOP-16 Packages
LTC2630/LTC2631	Single 12-/10-/8-Bit SPI/I²C V_{OUT} DACs with Bidirectional 10ppm/°C (Typ) Reference	180µA per DAC, 2.7V to 5.5V Supply Range, Rail-to-Rail Output, 6-Lead SC70 Package (LTC2630), 8-Lead TSOT-23 (LTC2631)
LTC2641/LTC2642	Single 16-/14-/12-Bit SPI V_{OUT} DACs with ±1LSB INL, DNL	±1LSB (Max) INL, DNL, 120µA, 3mm × 3mm DFN and MSOP Packages
LTC1669	10-Bit I²C Interface V_{OUT} Micropower DAC	60µA, ±0.75 LSB DNL, Rail-to-Rail, 5-Lead SOT-23 and MSOP-8 Packages
LTC6240	Single 18MHz, CMOS Op Amp	Low Noise, Rail-to-Rail
LT1991	Precision Gain Selectable Difference Amplifier	100µA Micropower, Pin Selectable Gain = –13 to 14

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