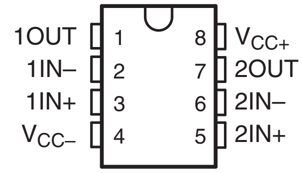
FEATURES

- **Qualified for Automotive Applications**
- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Low Total Harmonic Distortion: 0.003% Typ**
- **High Input Impedance: JFET-Input Stage**
- **Latchup-Free Operation**
- **High Slew Rate: 13 V/μs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

D PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TL082 JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The device features high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient.

The I-suffix device is characterized for operation from –40°C to 85°C. The Q-suffix device is characterized for operation from –40°C to 125°C.

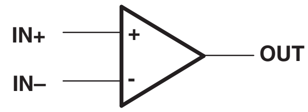
ORDERING INFORMATION(1)

T_J	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Reel of 2500	TL082IDRQ1	TL082I
–40°C to 125°C	SOIC – D	Reel of 2500	TL082QDRQ1	TL082Q

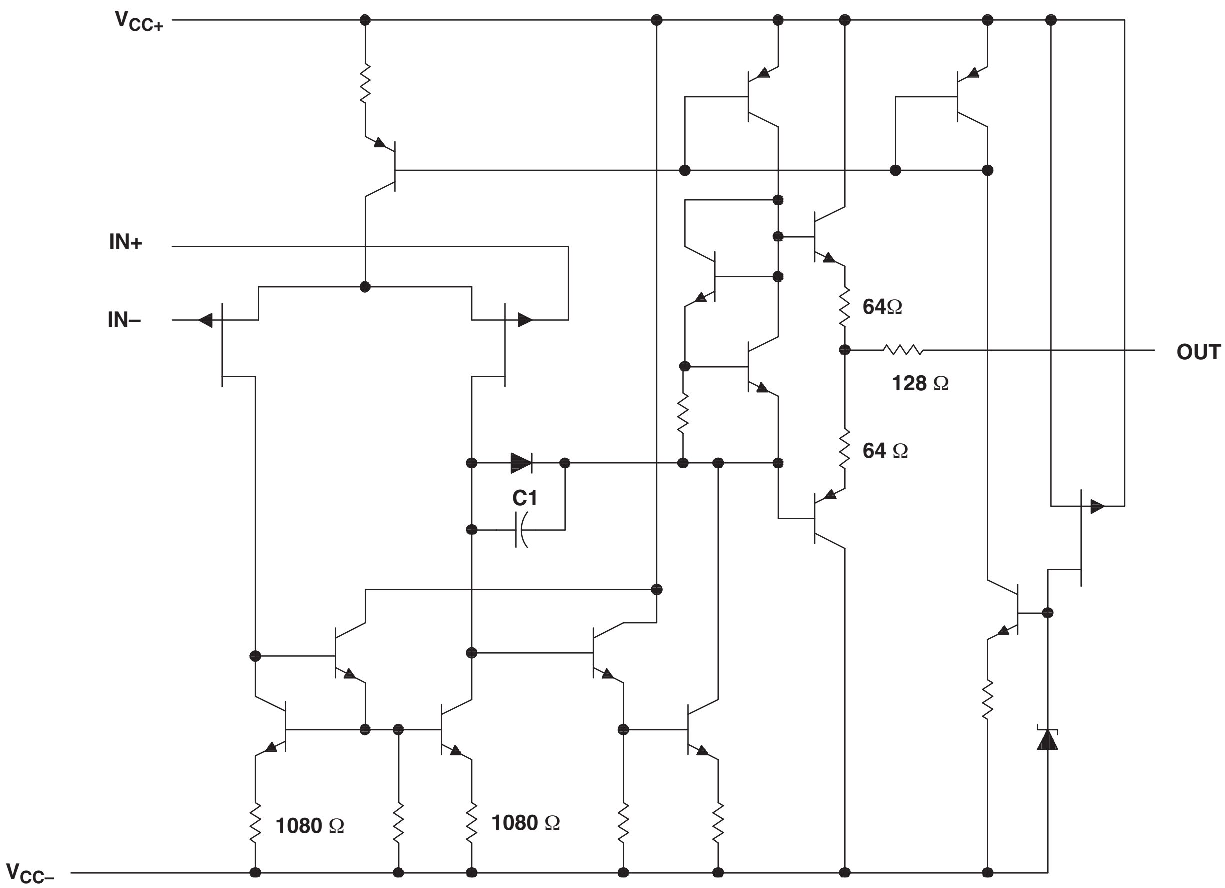
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SYMBOL (EACH AMPLIFIER)



SCHEMATIC (EACH AMPLIFIER)



A. Component values shown are nominal.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			VALUE
V_{CC+}	Supply voltage, positive[2]		18 V
V_{CC-}	Supply voltage, negative[2]		–18 V
V_{ID}	Differential input voltage[3]		±30 V
V_I	Input voltage[2][4]		±15 V
	Duration of output short circuit[5]		Unlimited
	Continuous total power dissipation		[6]
T_A	Operating free-air temperature range	TL082I	–40°C to 85°C
		TL082Q	–40°C to 125°C
θ_{JA}	Package thermal impedance, junction to free air[7]		97°C/W
	ESD rating[8]	Human-Body Model	1.5 kV (H1C)
		Charged-Device Model	1.5 kV (C5)
		Machine Model	200 V (M3)
	Operating virtual junction temperature		150°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+ with respect to IN–.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
(6) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is PD = (T_J(max) – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.
(8) ESD protection level per JEDEC classifications JESD22-A114 (HBM), JESD22-A115 (MM), and JESD22-C101 (CDM).

ELECTRICAL CHARACTERISTICS[1]

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A[2]	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6	mV
			Full range			9	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18		μV/°C
I_{IO}	Input offset current[3]	V_O = 0	25°C		5	100	pA
			Full range			20	nA
I_{IB}	Input bias current[3]	V_O = 0	25°C		30	200	pA
			Full range			50	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			
		R_L ≥ 2 kΩ		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	50	200		V/mV
			Full range	15			
B1	Unity-gain bandwidth		25°C		3		MHz
r_i	Input resistance		25°C		10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}(min), V_O = 0, R_S = 50 Ω	25°C	75	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω	25°C	80	86		dB
I_{CC}	Supply current (per amplifier)	V_O = 0, No load	25°C		1.4	2.8	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range for T_A is –40°C to 85°C for I-suffix devices and –40°C to 125°C for Q-suffix devices.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 14. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

OPERATING CHARACTERISTICS

$V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		8	13		V/μs
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1			0.05		μs
	Overshoot factor	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1			20		%
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	R_S = 20 Ω, f = 1 kHz			0.01		pA/√Hz
THD	Total harmonic distortion	V_{Irms} = 6 V, f = 1 kHz, AVD = 1, R_S ≤ 1 kΩ, R_L ≥ 2 kΩ			0.003		%

PARAMETER MEASUREMENT INFORMATION

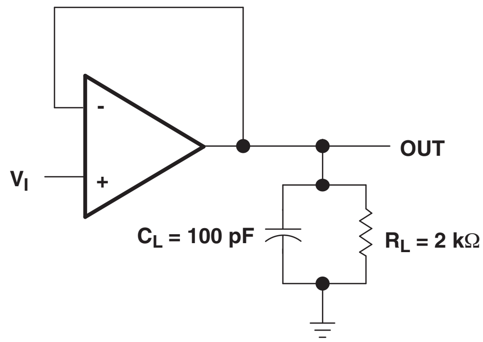


Figure 1.

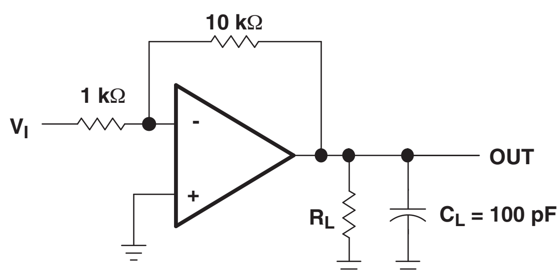


Figure 2.

TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the devices.

Table of Graphs

			FIGURE
V_{OM}	Maximum peak output voltage	vs Frequency	3, 4, 5
		vs Free-air temperature	6
		vs Load resistance	7
		vs Supply voltage	8
A_{VD}	Large-signal differential voltage amplification	vs Free-air temperature	9
		vs Frequency	10
P_D	Total power dissipation	vs Free-air temperature	11
I_{CC}	Supply current	vs Free-air temperature	12
		vs Supply voltage	13
I_{IB}	Input bias current	vs Free-air temperature	14
	Large-signal pulse response	vs Time	15
V_O	Output voltage	vs Elapsed time	16
CMRR	Common-mode rejection ratio	vs Free-air temperature	17
V_n	Equivalent input noise voltage	vs Frequency	18
THD	Total harmonic distortion	vs Frequency	19

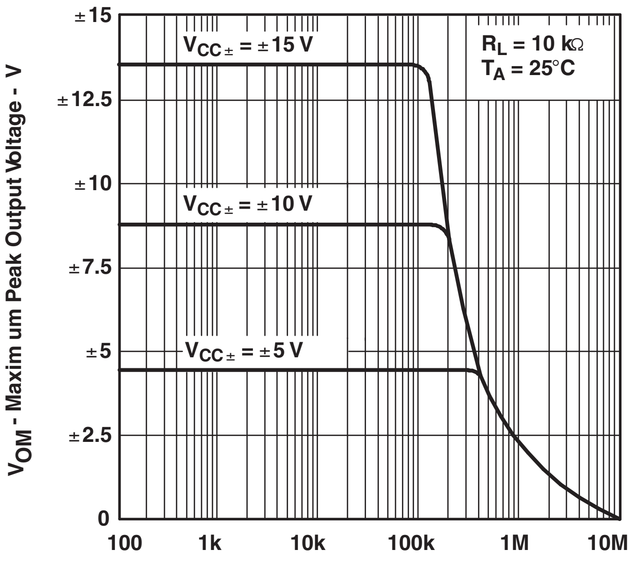


Figure 3.

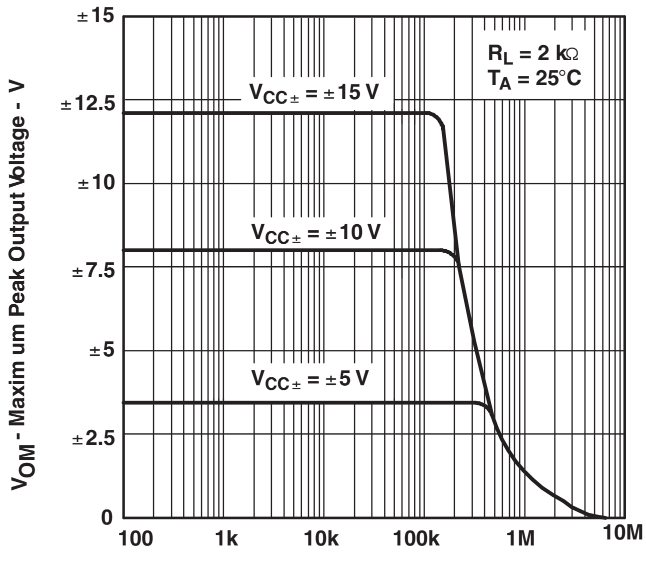


Figure 4.

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY
(See Figure 2)

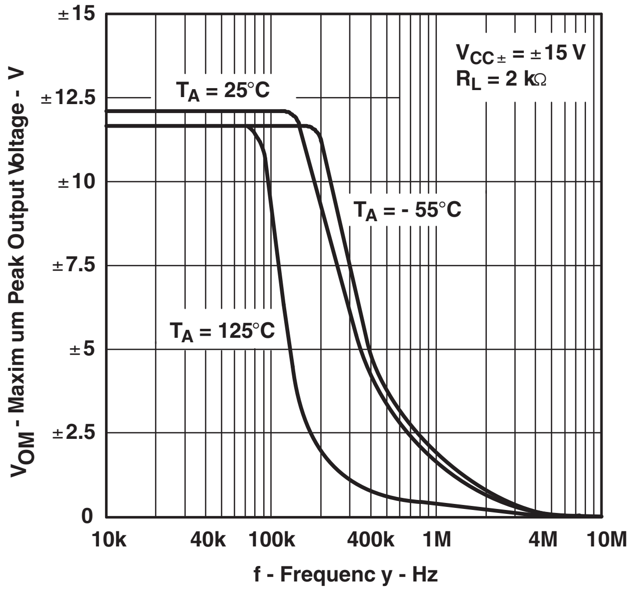


Figure 5.

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE
(See Figure 2)

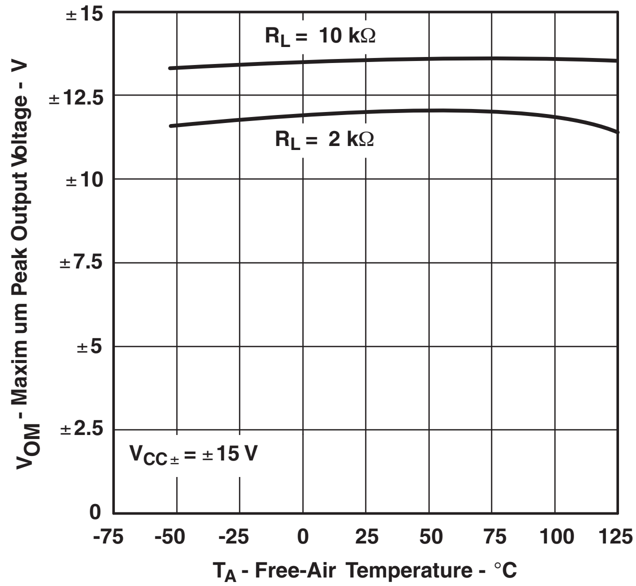


Figure 6.

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE
(See Figure 2)

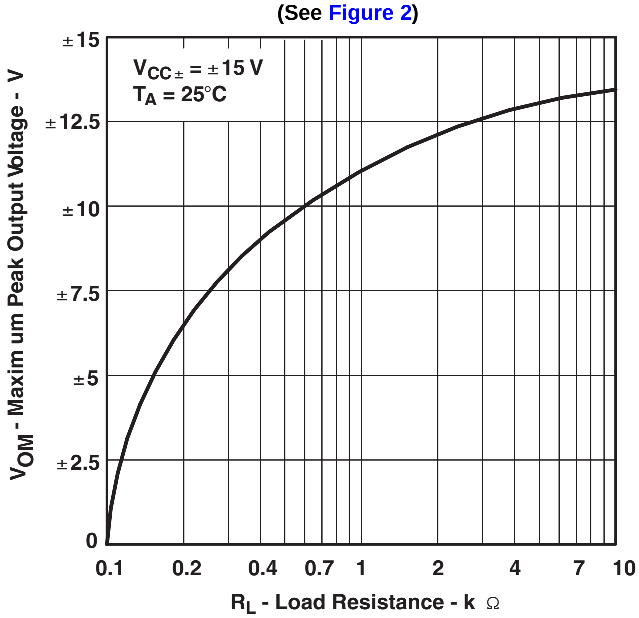


Figure 7.

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

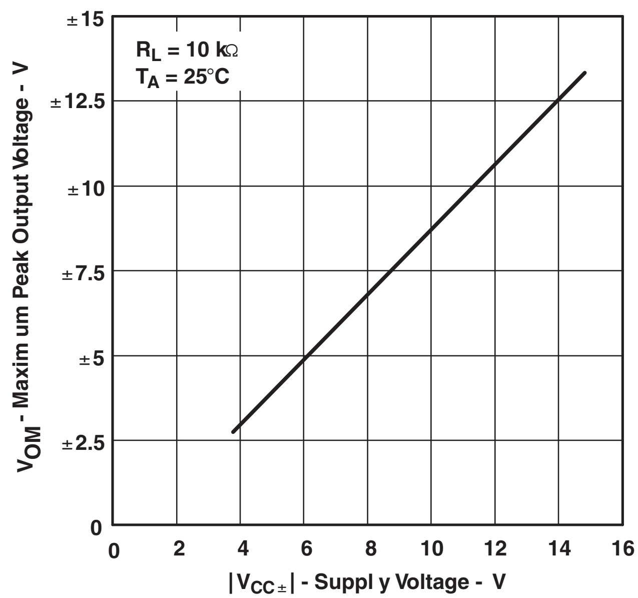


Figure 8.

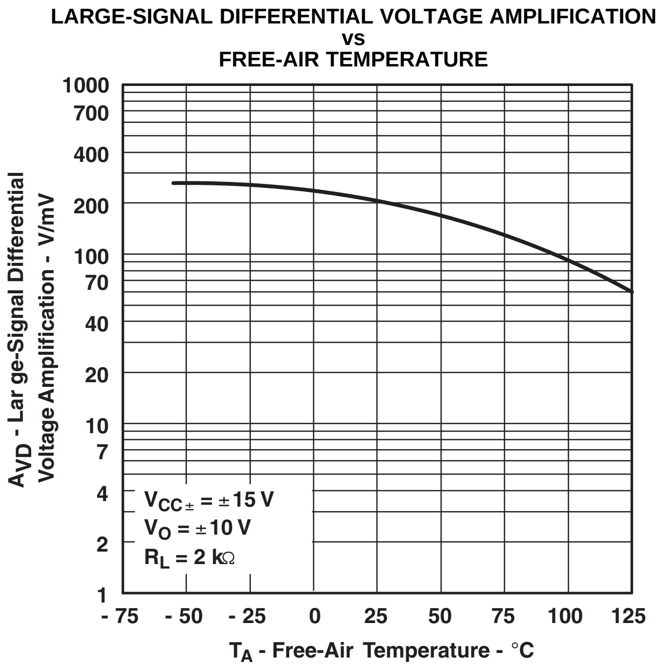


Figure 9.

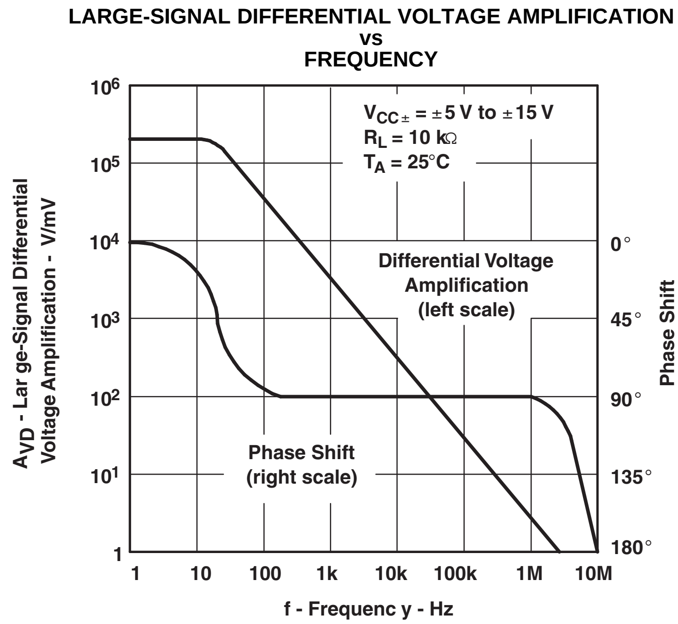


Figure 10.

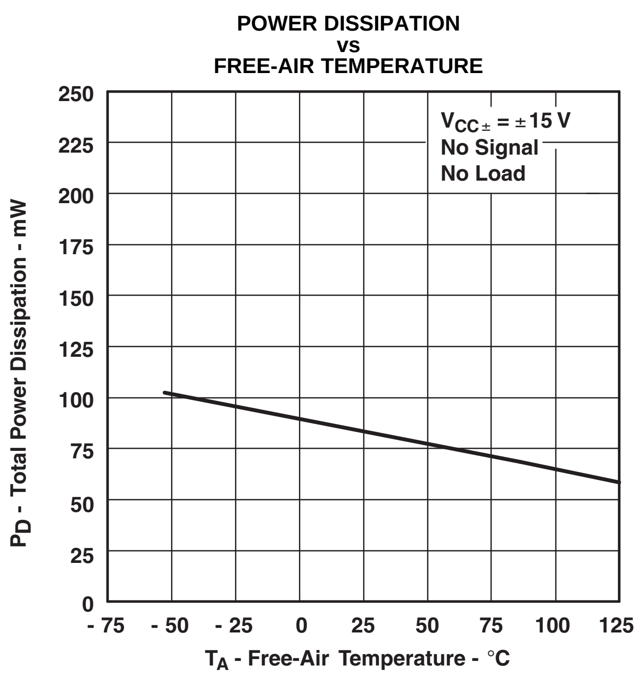


Figure 11.

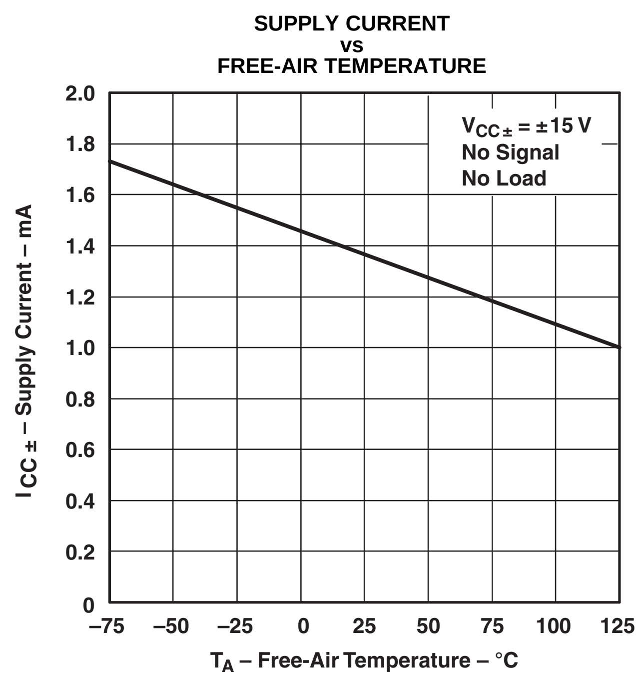


Figure 12.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

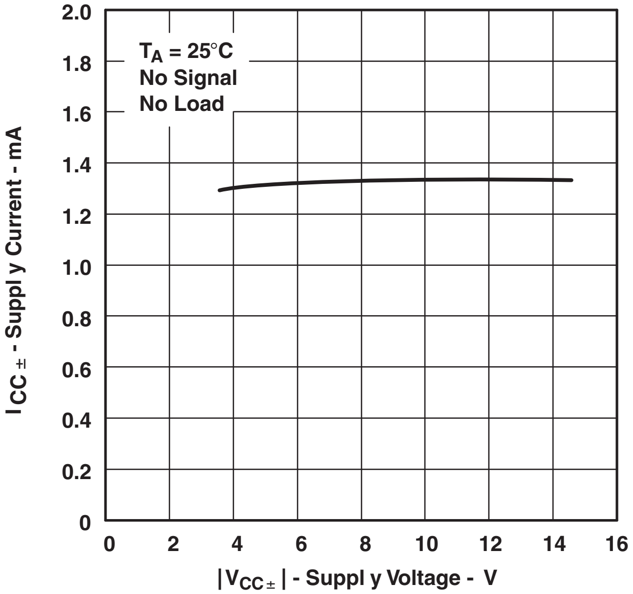


Figure 13.

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

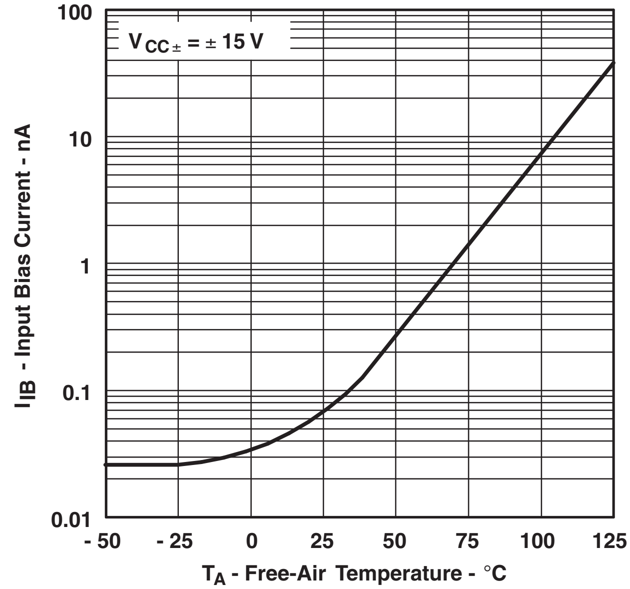


Figure 14.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

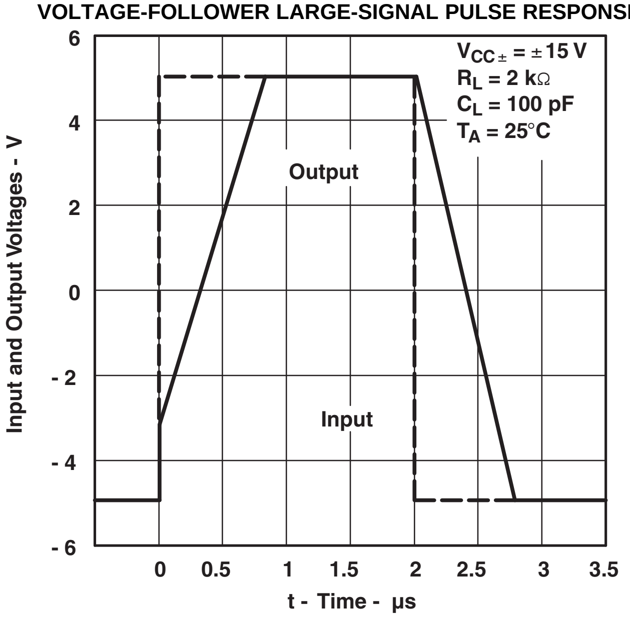


Figure 15.

OUTPUT VOLTAGE
vs
ELAPSED TIME
(See Figure 1)

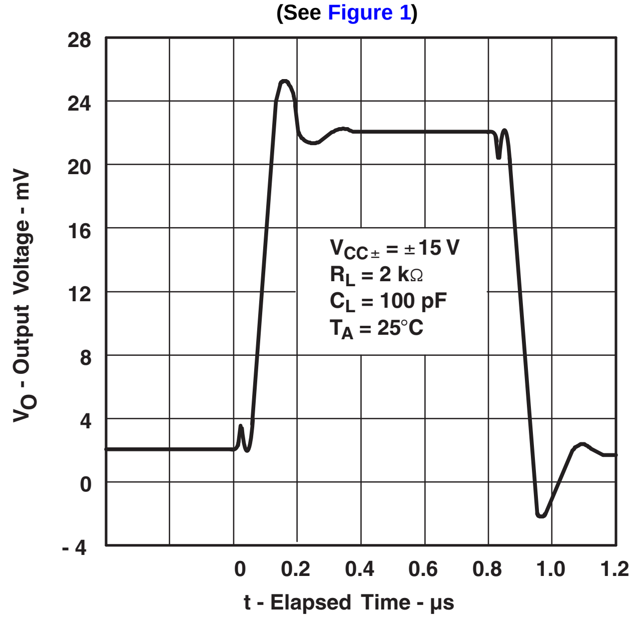


Figure 16.

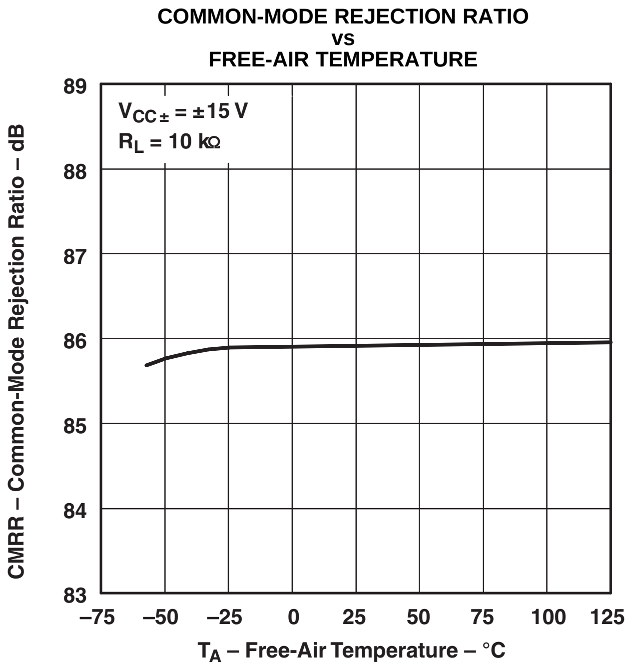


Figure 17.

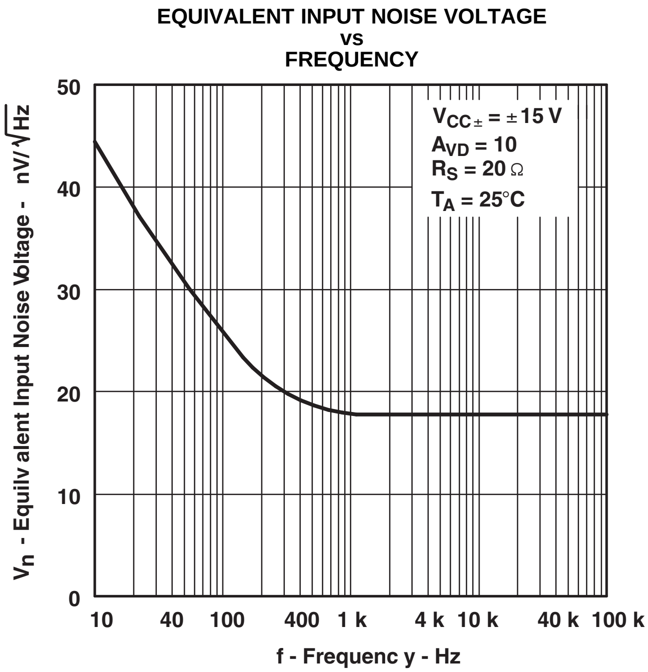


Figure 18.

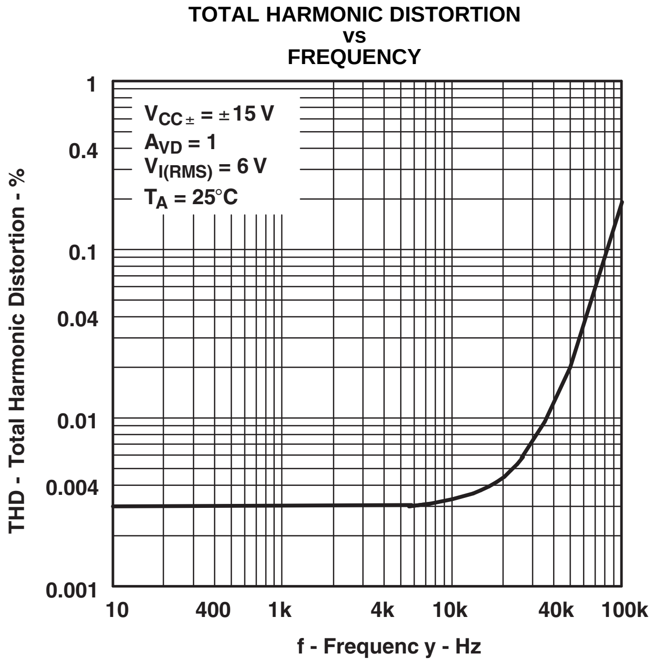


Figure 19.

APPLICATION INFORMATION

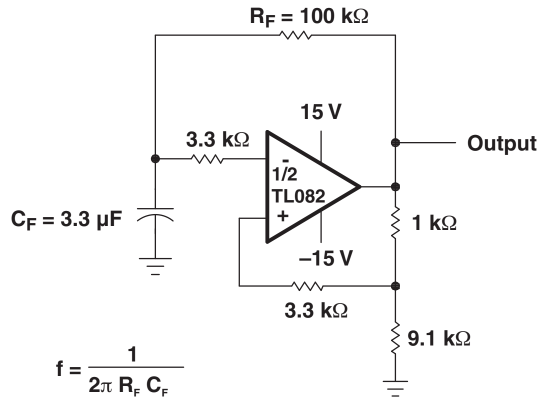


Figure 20.

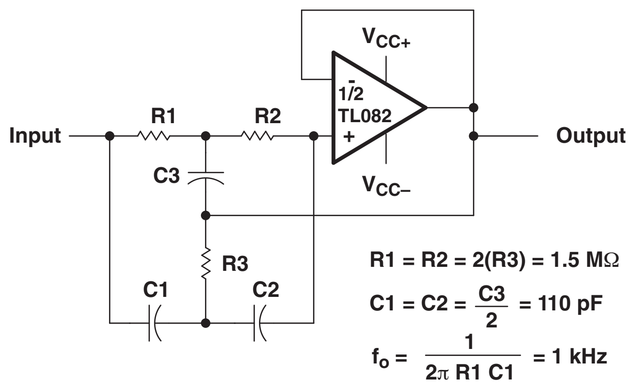


Figure 21.

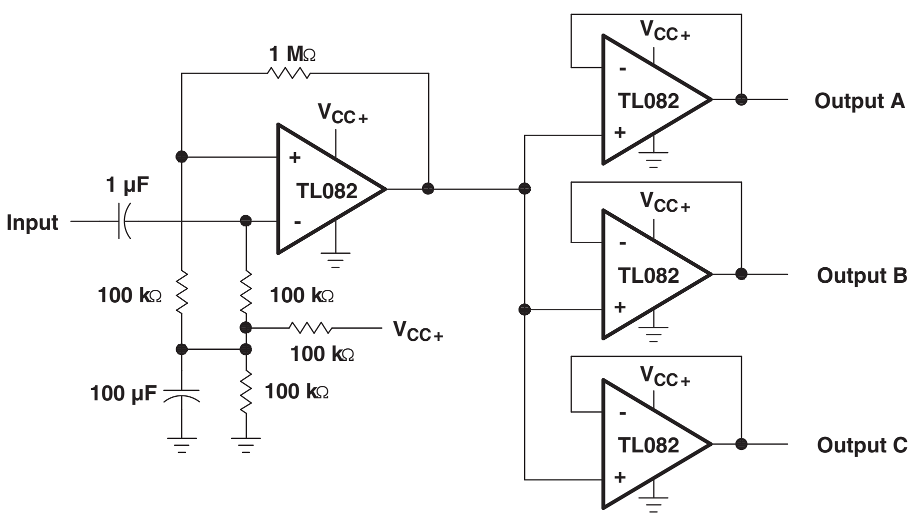
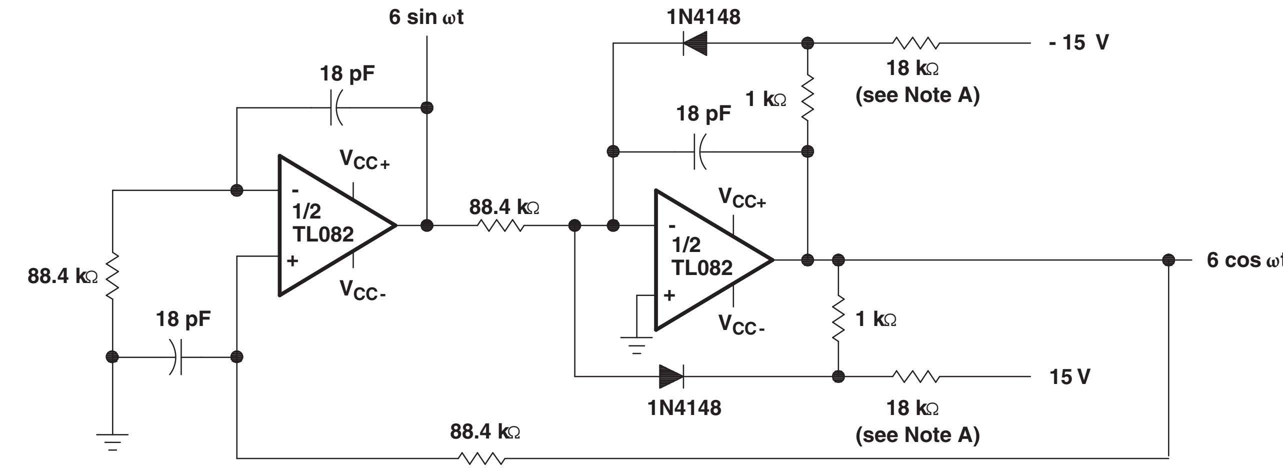
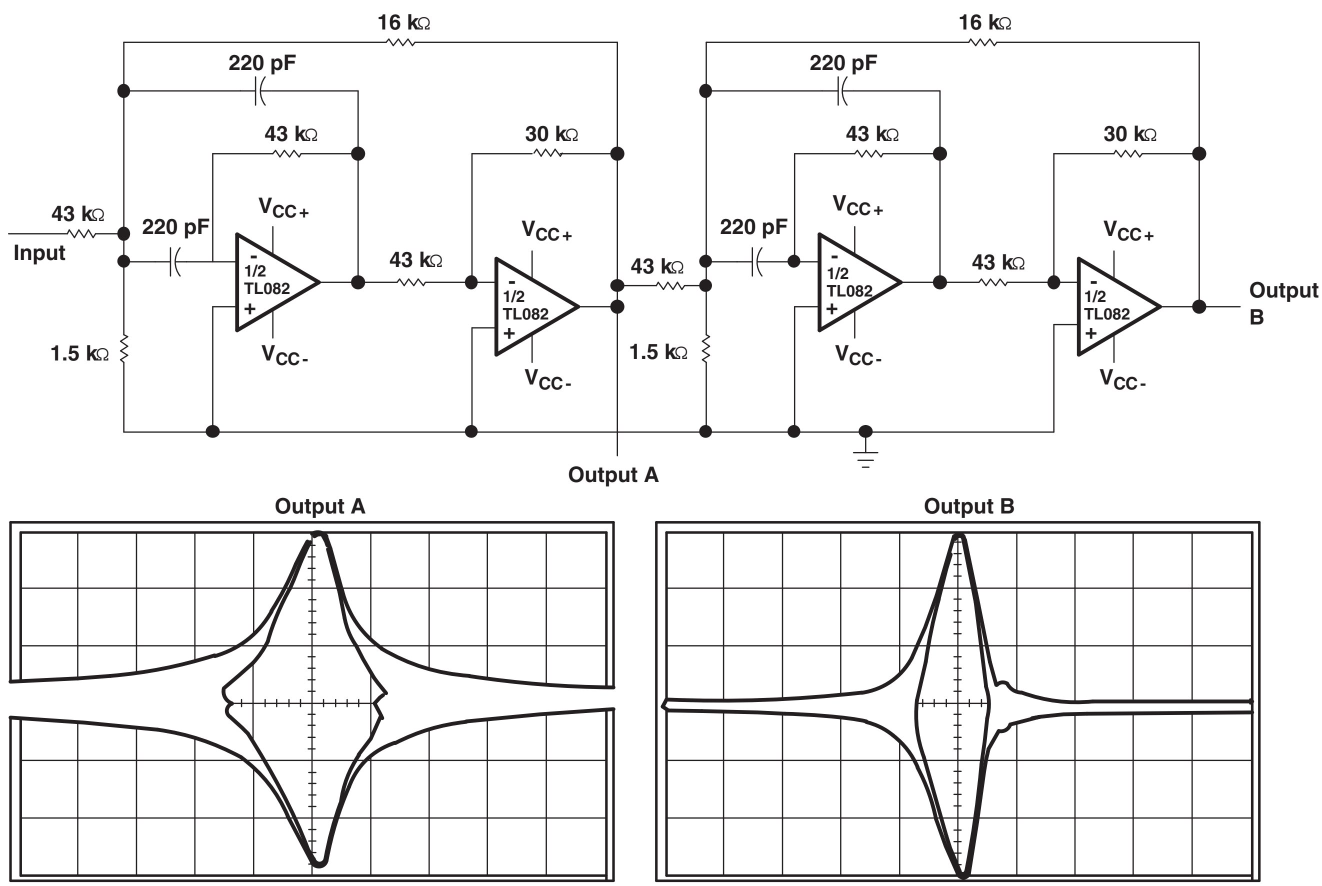


Figure 22. Audio-Distribution Amplifier



A. These resistor values may be adjusted for a symmetrical output.

Figure 23. 100-kHz Quadrature Oscillator



2 kHz/div
Second-Order Bandpass Filter
f_o = 100 kHz, Q = 30, GAIN = 4

2 kHz/div
Cascaded Bandpass Filter
f_o = 100 kHz, Q = 69, GAIN = 16

Figure 24. Positive-Feedback Bandpass Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL082IDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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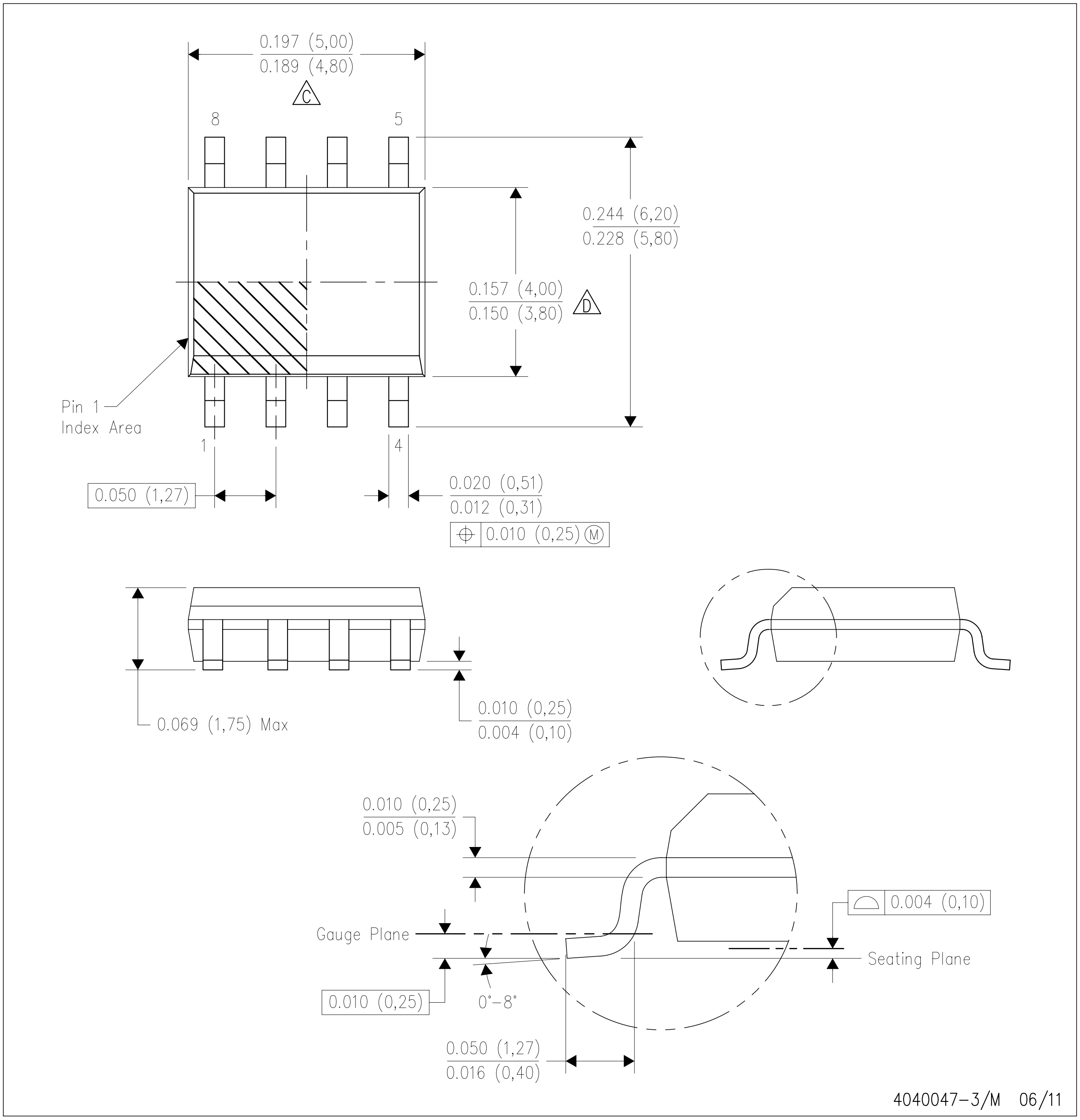
OTHER QUALIFIED VERSIONS OF TL082-Q1 :
- Catalog: TL082
- Military: TL082M

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
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DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
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		TI E2E Community Home Page	e2e.ti.com

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