# CMOS Static RAM 64K (16K x 4-Bit)

**IDT7188S**
**IDT7188L**

## Features

- **High-speed (equal access and cycle times)**
  - *Military: 25/35/45/55/70/85ns (max.)*
- **Low power consumption**
- **Battery backup operation — 2V data retention (L version only)**
- **Available in high-density industry standard 22-pin, 300 mil ceramic DIP**
- **Produced with advanced CMOS technology**
- **Inputs/outputs TTL-compatible**
- **Military product compliant to MIL-STD-883, Class B**

## Description

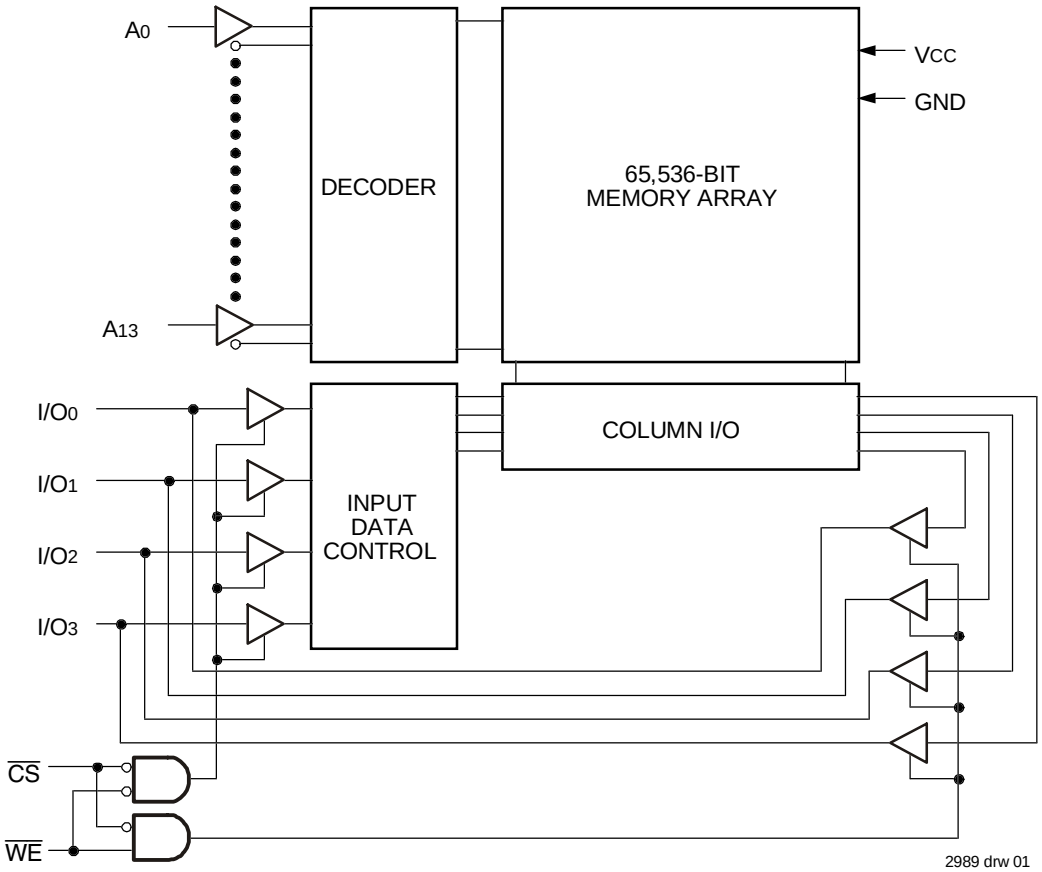
The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology — CMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 25ns are available. The IDT7188 offers a reduced power standby mode, $I_{SB1}$, which is activated when $\overline{CS}$ goes HIGH. This capability significantly decreases power while enhancing system reliability. The low-power version (L) version also offers a battery backup data retention capability where the circuit typically consumes only 30µW operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply. The IDT7188 is packaged in a 22-pin, 300 mil ceramic DIP providing excellent board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## Functional Block Diagram

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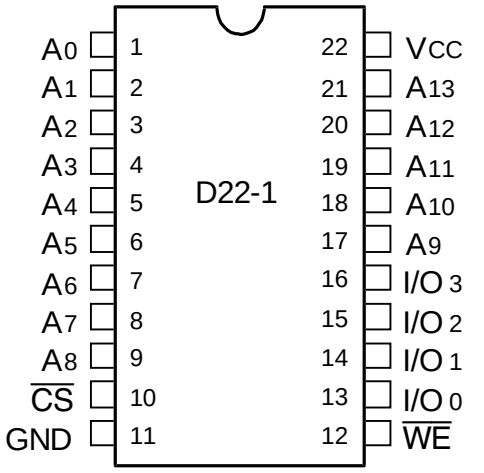
## Pin Configuration




2989 drw 02

**DIP**
**Top View**

## Pin Descriptions

| Name | Description |
|---|---|
| $A_0$ - $A_{13}$ | Address Inputs |
| $\overline{CS}$ | Chip Select |
| $\overline{WE}$ | Write Enable |
| $I/O_0$ - $I/O_3$ | Data Input/Output |
| $V_{CC}$ | Power |
| GND | Ground |

2989 tbl 01

## Truth Table(1)

| Mode | $\overline{CS}$ | $\overline{WE}$ | I/O | Power |
|---|---|---|---|---|
| Standby | H | X | High-Z | Standby |
| Read | L | H | $D_{OUT}$ | Active |
| Write | L | L | $D_{IN}$ | Active |

2989 tbl 02

**NOTE:**
1. H = $V_{IH}$, L = $V_{IL}$, X = don't care.

## Absolute Maximum Ratings(1)

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | -55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

2989 tbl 03

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Capacitance
### ($T_A$ = +25°C, f = 1.0MHz, Vcc = 0V)

| Symbol | Parameter(1) | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{OUT}$ = 0V | 6 | pF |

2989 tbl 04

**NOTE:**
1. This parameter is determined by device characterization, but is not production tested.

## Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | — | 6.0 | V |
| $V_{IL}$ | Input Low Voltage | -0.5(1) | — | 0.8 | V |

2989 tbl 05

**NOTE:**
1. $V_{IL}$ (min.) = –3.0V for pulse width less than 20ns,once per cycle.

## Recommended Operating Temperature and Supply Voltage

| Grade | Temperature | GND | Vcc |
|---|---|---|---|
| Military | -55°C to +125°C | 0V | 5V ± 10% |

2989 tbl 06

# DC Electrical Characteristics

## (Vcc = 5.0V ± 10%)

| Symbol | Parameter | Test Conditions | IDT7188S | | IDT7188L | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $\|I_{LI}\|$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = GND to $V_{CC}$ | — | 10 | — | 5 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | — | 10 | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 10mA, $V_{CC}$ = Min. | — | 0.5 | — | 0.5 | V |
| | | $I_{OL}$ = 8mA, $V_{CC}$ = Min. | — | 0.4 | — | 0.4 | |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4mA, $V_{CC}$ = Min. | 2.4 | — | 2.4 | — | V |

2989 tbl 07

# DC Electrical Characteristics(1)

## (Vcc = 5V ± 10%, VLC = 0.2V, VHC = Vcc - 0.2V)

| Symbol | Parameter | Power | 7188S25 7188L25 | 7188S35 7188L35 | 7188S45 7188L45 | 7188S55 7188L55 | 7188S70 7188L70 | 7188S85 7188L85 | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Operating Power Supply Current $\overline{CS}$ = $V_{IL}$, Outputs Open $V_{CC}$ = Max., f = 0(2) | S | 105 | 105 | 105 | 105 | 105 | 105 | mA |
| | | L | 80 | 80 | 80 | 80 | 80 | 80 | |
| $I_{CC2}$ | Dynamic Operating Current $\overline{CS}$ = $V_{IL}$, Outputs Open $V_{CC}$ = Max., f = $f_{MAX}$(2) | S | 155 | 140 | 140 | 140 | 140 | 140 | mA |
| | | L | 120 | 115 | 110 | 110 | 110 | 105 | |
| $I_{SB}$ | Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ $V_{IH}$, Outputs Open $V_{CC}$ = Max., f = $f_{MAX}$(2) | S | 60 | 50 | 50 | 50 | 50 | 50 | mA |
| | | L | 40 | 40 | 35 | 35 | 35 | 35 | |
| $I_{SB1}$ | Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ $V_{HC}$, $V_{CC}$ = Max., $V_{IN}$ ≥ $V_{HC}$ or $V_{IN}$ ≤ $V_{LC}$, f = 0(2) | S | 20 | 20 | 20 | 20 | 20 | 20 | mA |
| | | L | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | |

2989 tbl 08

**NOTES:**
1. All values are maximum guaranteed values.
2. At f = $f_{MAX}$ address and data inputs are cycling at the maximum frequency of read cycles of 1/$t_{RC}$. f = 0 means no input lines change.

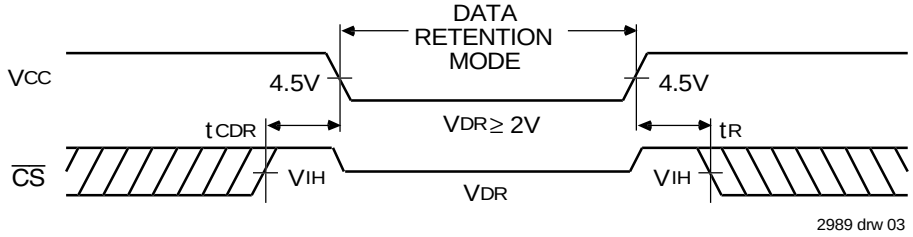
## Data Retention Characteristics
### (L Version Only) ($V_{HC}$ = Vcc - 0.2V)

| Symbol | Parameter | Test Condition | Min. | Typ.(1) Vcc @ 2.0V | Typ.(1) Vcc @ 3.0V | Max. Vcc @ 2.0V | Max. Vcc @ 3.0V | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{DR}$ | Vcc for Data Retention | — | 2.0 | — | — | — | — | V |
| $I_{CCDR}$ | Data Retention Current | $\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ | — | 10 | 15 | 600 | 900 | µA |
| $t_{CDR}$(3) | Chip Deselect to Data Retention Time | | 0 | — | — | — | — | ns |
| $t_R$(3) | Operation Recovery Time | | $t_{RC}$(2) | — | — | — | — | ns |
| $\|I_{LI}\|$(3) | Input Leakage Current | | — | — | — | 2 | 2 | µA |

2989 tbl 09

**NOTES:**
1. $T_A$ = +25°C.
2. $t_{RC}$ = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

## Low Vcc Data Retention Waveform

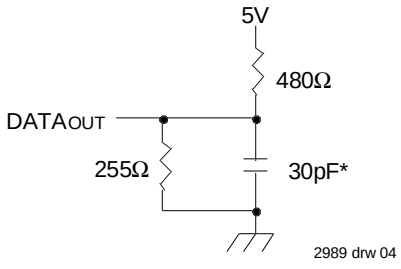



2989 drw 03

## AC Test Conditions

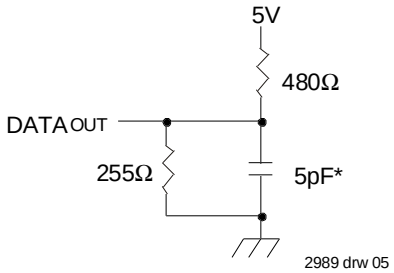
| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| AC Test Load | See Figures 1 and 2 |

2989 tbl 10




2989 drw 04

**Figure 1. AC Test Load**




2989 drw 05

**Figure 2. AC Test Load (for $t_{HZ}$, $t_{LZ}$, $t_{WZ}$, $t_{OHZ}$ and $t_{OW}$)**

*Includes scope and jig capacitances

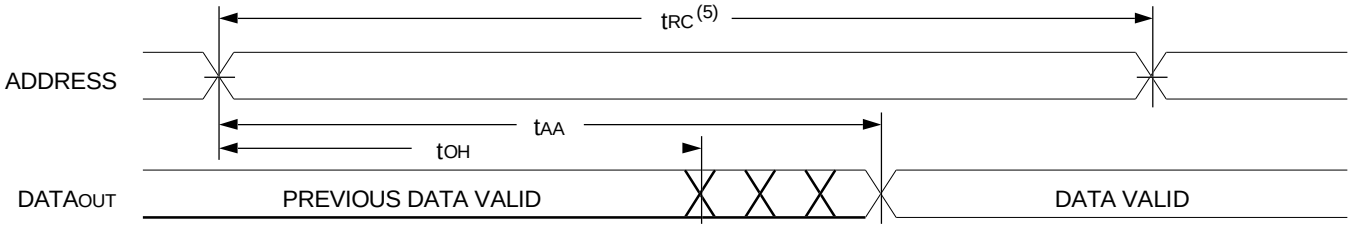
## AC Electrical Characteristics (Vcc = 5.0V ± 10%)

| Symbol | Parameter | 7188S25 7188L25 | | 7188S35 7188L35 | | 7188S45 7188L45 | | 7188S55 7188L55 | | 7188S70 7188L70 | | 7188S85 7188L85 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 25 | — | 35 | — | 45 | — | 55 | — | 70 | — | 85 | — | ns |
| $t_{AA}$ | Address Access Time | — | 25 | — | 35 | — | 45 | — | 55 | — | 70 | — | 85 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 25 | — | 35 | — | 45 | — | 55 | — | 70 | — | 85 | ns |
| $t_{OH}$ | Output Hold from Address Change | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{LZ}$(1) | Output Select to Output in Low-Z | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{HZ}$(1) | Chip Deselect to Output in High-Z | — | 10 | — | 14 | — | 14 | — | 20 | — | 25 | — | 30 | ns |
| $t_{PU}$(1) | Chip Select to Power Up Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}$(1) | Chip Deselect to Power Down Time | — | 25 | — | 35 | — | 45 | — | 55 | — | 70 | — | 85 | ns |

2989 tbl 11

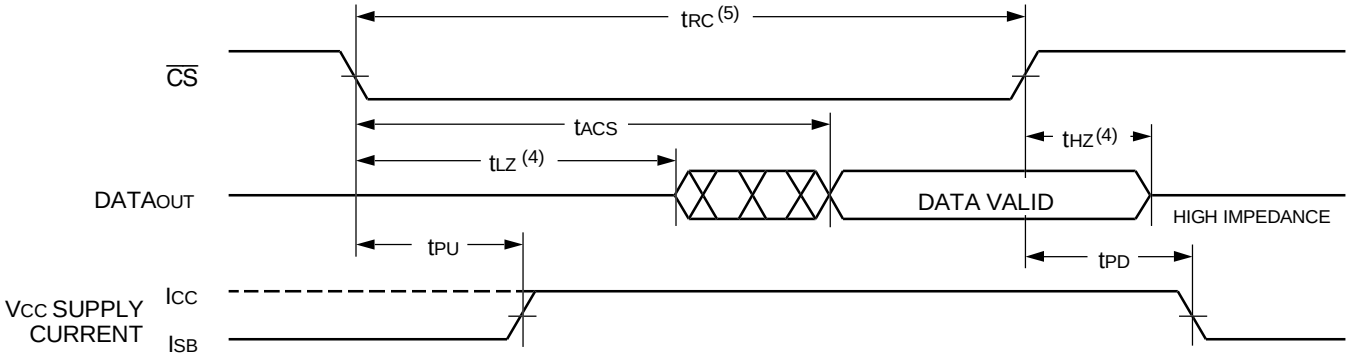
**NOTE:**
1. This parameter is guaranteed by device characterization but is not production tested.

## Timing Waveform of Read Cycle No. 1(1,2)




2989 drw 06

## Timing Waveform of Read Cycle No. 2(1,3)




2989 drw 07

**NOTES:**
1. $\overline{WE}$ is HIGH for Read cycle.
2. $\overline{CS}$ is LOW for Read cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state voltage.
5. All Read cycle timings are referenced from the last valid address to the first transitioning address.

## AC Electrical Characteristics (Vcc = 5.0V ± 10%)

| Symbol | Parameter | 7188S25 7188L25 | | 7188S35 7188L35 | | 7188S45 7188L45 | | 7188S55 7188L55 | | 7188S70 7188L70 | | 7188S85 7188L85 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **Write Cycle** | | | | | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 20 | — | 30 | — | 40 | — | 50 | — | 60 | — | 75 | — | ns |
| $t_{CW}$ | Chip Select to End-of-Write | 20 | — | 25 | — | 35 | — | 50 | — | 60 | — | 75 | — | ns |
| $t_{AW}$ | Address Valid to End-of-Write | 20 | — | 25 | — | 35 | — | 50 | — | 60 | — | 75 | — | ns |
| $t_{AS}$ | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WP}$ | Write Pulse Width | 20 | — | 25 | — | 35 | — | 50 | — | 60 | — | 75 | — | ns |
| $t_{WR}$ | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{DW}$ | Data Valid to End-of-Write | 13 | — | 15 | — | 20 | — | 25 | — | 30 | — | 35 | — | ns |
| $t_{DH}$ | Data Hold Time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{WZ}$[1] | Write Enable to Output in High-Z | — | 7 | — | 10 | — | 15 | — | 25 | — | 30 | — | 40 | ns |
| $t_{OW}$[1] | Output Active from End-of-Write | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |

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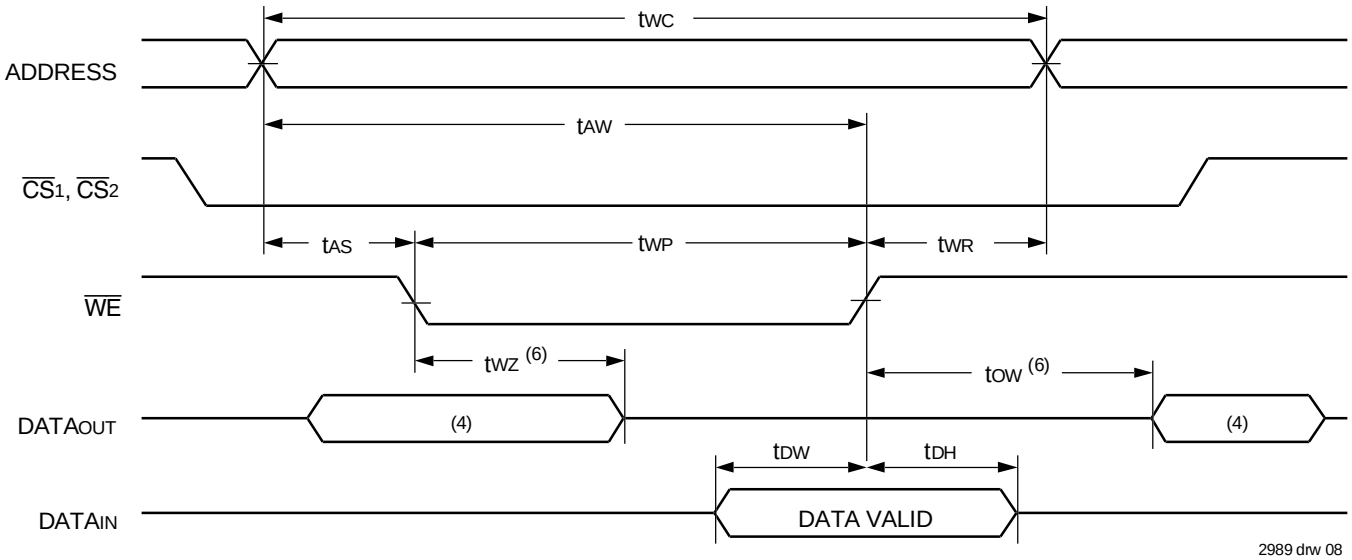
**NOTE:**
1. This parameter is guaranteed by device characterization.

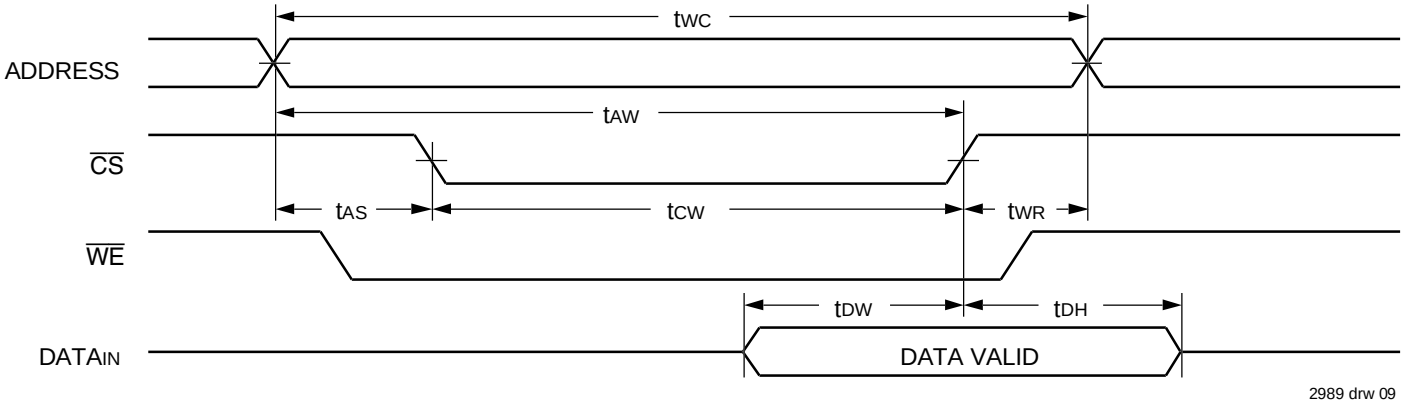
## Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)[1,2,3]




2989 drw 08

**NOTES:**
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap ($t_{WP}$) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $t_{WR}$ is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals should not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.

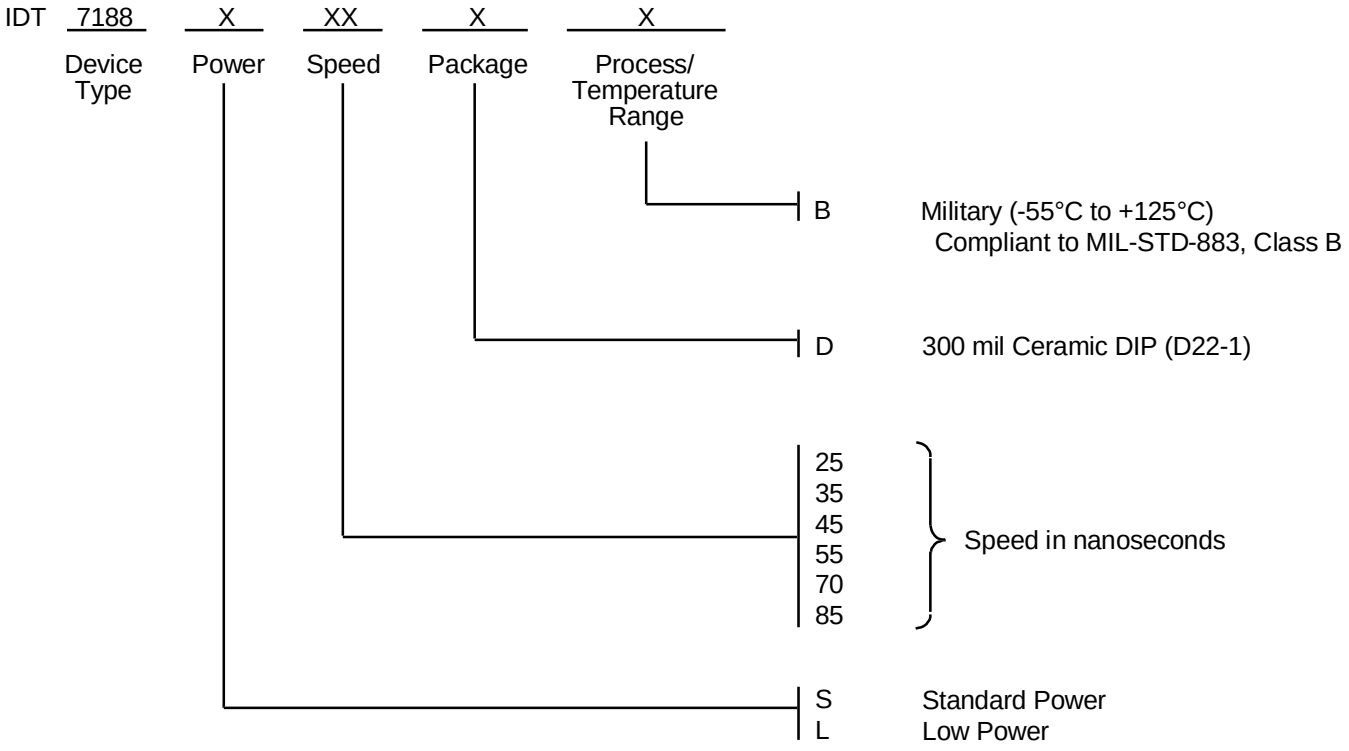
## Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)[1,2,3,5]




2989 drw 09

**NOTES:**
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap ($t_{WP}$) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $t_{WR}$ is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals should not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.

## Ordering Information

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# Datasheet Document History

| | | |
|---|---|---|
| 11/xx/99 | | Updated to new format |
| | Pg. 2, 3, 4 | Removed commercial temperature data |
| | Pg. 8 | Added Datasheet Document History |
| 08/09/00 | | Not recommended for new designs |
| 02/01/01 | | Removed "Not recommended for new designs" |

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