Current Output/ Serial Input, 16-/14-Bit DAC

AD5543/AD5553

FEATURES
16-Bit Resolution AD5543
14-Bit Resolution AD5553
±1 LSB DNL
±2 LSB INL for AD5543
±1 LSB INL for AD5553
Low Noise 12 nV/√Hz
Low Power, I_{DD} = 10 μA
0.5 μs Settling Time
4Q Multiplying Reference-Input
2 mA Full-Scale Current ± 20%, with V_{REF} = 10 V
Built-in RFB Facilitates Voltage Conversion
3-Wire Interface
Ultracompact MSOP-8 and SOIC-8 Packages

APPLICATIONS
Automatic Test Equipment
Instrumentation
Digitally Controlled Calibration
Industrial Control PLCs

GENERAL DESCRIPTION

The AD5543/AD5553 are precision 16-/14-bit, low power, current output, small form factor digital-to-analog converters. They are designed to operate from a single 5 V supply with a ±10 V multiplying reference.

The applied external reference V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) facilitates the R-2R and temperature tracking for voltage conversion when combined with an external op amp.

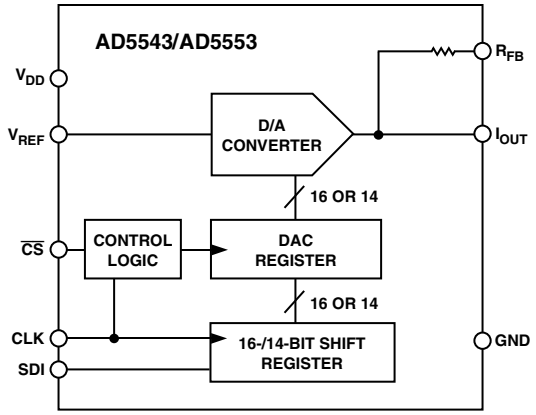
A serial-data interface offers high speed, 3-wire microcontroller compatible inputs using serial data in (SDI), clock (CLK), and chip select ($\overline{CS}$).

The AD5543/AD5553 are packaged in ultracompact (3 mm × 4.7 mm) MSOP-8 and SOIC-8 packages.

REV. A

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FUNCTIONAL BLOCK DIAGRAM



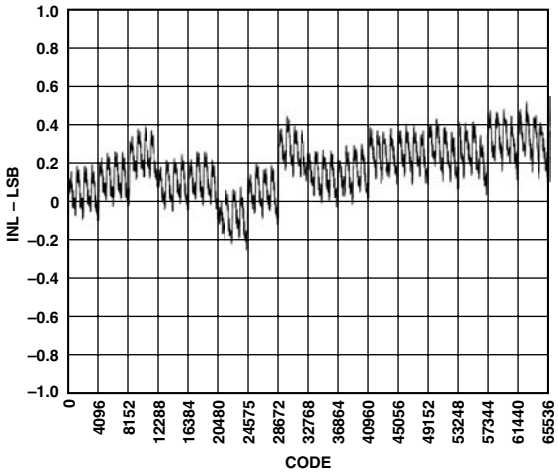


Figure 1. Integral Nonlinearity Error

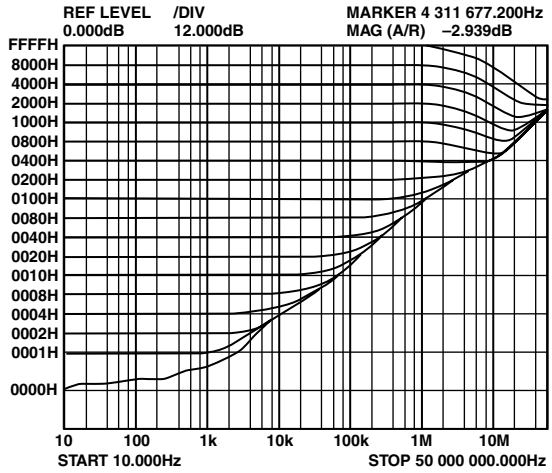


Figure 2. Reference Multiplying Bandwidth

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
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AD5543/AD5553–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_{DD} = 5 V ± 10%, V_{SS} = 0 V, I_{OUT} = Virtual GND, GND = 0 V, V_{REF} = 10 V, T_A = Full operating temperature range, unless otherwise noted.)

Parameter	Symbol	Condition	5 V ± 10%	Unit
STATIC PERFORMANCE[1]				
Resolution	N	1 LSB = $V_{REF}/2^{16}$ = 153 μV when V_{REF} = 10 V AD5543	16	Bits
		1 LSB = $V_{REF}/2^{14}$ = 610 μV when V_{REF} = 10 V AD5553	14	Bits
Relative Accuracy	INL	Grade: AD5553C	±1	LSB max
		Grade: AD5543B	±2	LSB max
Differential Nonlinearity	DNL	Monotonic	±1	LSB max
Output Leakage Current	I_{OUT}	Data = 0000_H, T_A = 25°C	10	nA max
		Data = 0000_H, T_A = T_A max	20	nA max
Full-Scale Gain Error	G_{FSE}	Data = $FFFF_H$	±1/±4	mV typ/max
Full-Scale Tempco[2]	TCV_{FS}		1	ppm/°C typ
REFERENCE INPUT				
V_{REF} Range	V_{REF}		–15/+15	V min/max
Input Resistance	R_{REF}		5	kΩ typ[3]
Input Capacitance[2]	C_{REF}		5	pF typ
ANALOG OUTPUT				
Output Current	I_{OUT}	Data = $FFFF_H$ for AD5543	2	mA typ
		Data = $3FFF_H$ for AD5553		
Output Capacitance[2]	C_{OUT}	Code Dependent	200	pF typ
LOGIC INPUTS AND OUTPUT				
Logic Input Low Voltage	V_{IL}		0.8	V max
Logic Input High Voltage	V_{IH}		2.4	V min
Input Leakage Current	I_{IL}		10	μA max
Input Capacitance[2]	C_{IL}		10	pF max
INTERFACE TIMING[2, 4]				
Clock Input Frequency	f_{CLK}		50	MHz
Clock Width High	t_{CH}		10	ns min
Clock Width Low	t_{CL}		10	ns min
$\overline{CS}$ to Clock Setup	t_{CSS}		0	ns min
Clock to $\overline{CS}$ Hold	t_{CSH}		10	ns min
Data Setup	t_{DS}		5	ns min
Data Hold	t_{DH}		10	ns min
SUPPLY CHARACTERISTICS				
Power Supply Range	$V_{DD\ RANGE}$		4.5/5.5	V min/max
Positive Supply Current	I_{DD}	Logic Inputs = 0 V	10	μA max
Power Dissipation	P_{DISS}	Logic Inputs = 0 V	0.055	mW max
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = ±5%	0.006	%/% max
AC CHARACTERISTICS[4]				
Output Voltage Settling Time	t_S	To ±0.1% of Full Scale,	0.5	μs typ
		Data = 0000_H to $FFFF_H$ to 0000_H for AD5543		
		Data = 0000_H to $3FFF_H$ to 0000_H for AD5553		
Reference Multiplying BW	BW	V_{REF} = 5 V p-p, Data = $FFFF_H$	4	MHz typ
DAC Glitch Impulse	Q	V_{REF} = 0 V, Data = $7FFF_H$ to 8000_H for AD5543	7	nV-s typ
		Data = $1FFF_H$ to 2000_H for AD5553		
Feedthrough Error	V_{OUT}/V_{REF}	Data = 0000_H, V_{REF} = 100 mV rms, same channel	–65	dB
Digital Feedthrough	Q	$\overline{CS}$ = 1, and f_{CLK} = 1 MHz	7	nV-s typ
Total Harmonic Distortion	THD	V_{REF} = 5 V p-p, Data = $FFFF_H$, f = 1 kHz	–85	dB typ
Output Spot Noise Voltage	e_N	f = 1 kHz, BW = 1 Hz	12	nV/√Hz

NOTES

[1]All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The AD5543 R_{FB} terminal is tied to the amplifier output. The op amp +IN is grounded and the DAC I_{OUT} is tied to the op amp –IN. Typical values represent average readings measured at 25°C.

[2]These parameters are guaranteed by design and are not subject to production testing.

[3]All ac characteristic tests are performed in a closed-loop system using an AD841 I-to-V converter amplifier.

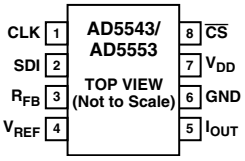
[4]All input control signals are specified with t_R = t_F = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . –0.3 V, +8 V
V_{REF} to GND . . . . . –18 V, +18 V
Logic Inputs to GND . . . . . –0.3 V, +8 V
$V(I_{OUT})$ to GND . . . . . –0.3 V, V_{DD} + 0.3 V
Input Current to Any Pin except Supplies . . . . . ±50 mA
Package Power Dissipation . . . . . $(T_J Max – T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
8-Lead Surface Mount (MSOP-8) . . . . . 150°C/W
8-Lead Surface Mount (SOIC-8) . . . . . 100°C/W
Maximum Junction Temperature (T_J Max) . . . . . 150°C
Operating Temperature Range
Models B, C . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature
RN-8, RM-8 (Vapor Phase, 60 sec) . . . . . 215°C
RN-8, RM-8 (Infrared, 15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION
MSOP and SOIC-8



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	CLK	Clock Input. Positive-edge triggered, clocks data into shift register.
2	SDI	Serial Register Input. Data loads directly into the shift register MSB first. Extra leading bits are ignored.
3	R_{FB}	Internal Matching Feedback Resistor. Connects to external op amp for voltage output.
4	V_{REF}	DAC Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance versus code.
5	I_{OUT}	DAC Current Output. Connects to inverting terminal of external precision I-to-V op amp for voltage output.
6	GND	Analog and Digital Ground
7	V_{DD}	Positive Power Supply Input. Specified range of operation 5 V ± 10%.
8	$\overline{CS}$	Chip Select. Active low digital input. Transfers shift-register data to DAC register on rising edge. See Truth Table for operation.

ORDERING GUIDE*

Model	INL (LSB)	RES (LSB)	Temperature Range	Package Description	Package Option	Marking
AD5543BR	±2	16	–40°C to +85°C	SOIC-8	RN-8	AD5543
AD5543BRM	±2	16	–40°C to +85°C	MSOP-8	RM-8	DXB
AD5553CRM	±1	14	–40°C to +85°C	MSOP-8	RM-8	DUC

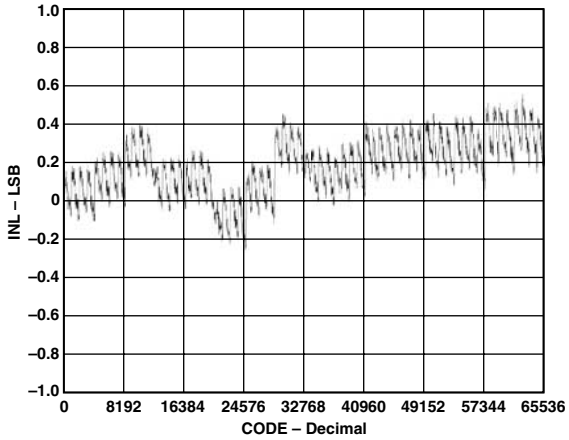
*The AD5543 contains 1040 transistors. The die size measures 55 mil × 73 mil, 4,015 sq. mil.

CAUTION

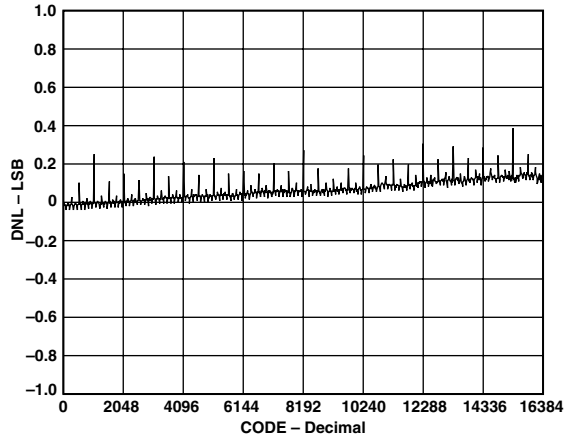
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5543/AD5553 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



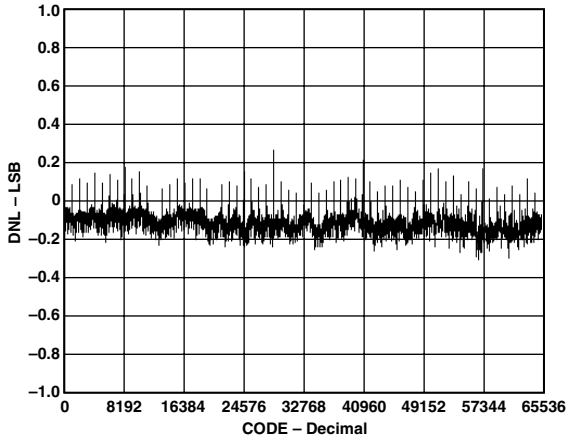
AD5543/AD5553–Typical Performance Characteristics



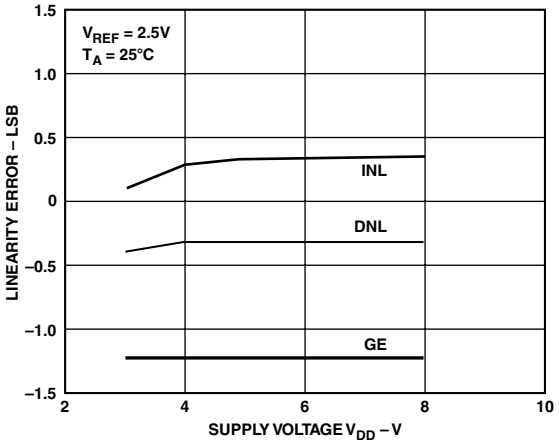
TPC 1. AD5543 Integral Nonlinearity Error



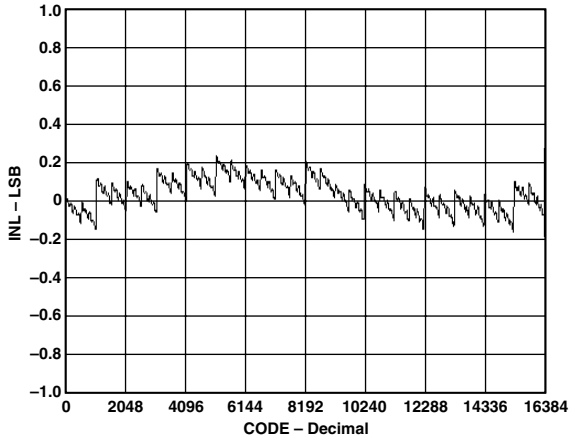
TPC 4. AD5553 Differential Nonlinearity Error



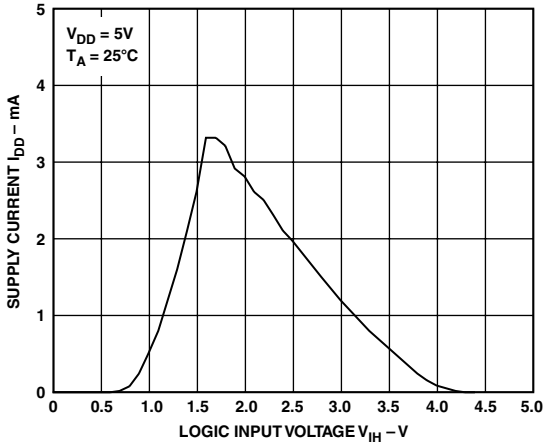
TPC 2. AD5543 Differential Nonlinearity Error



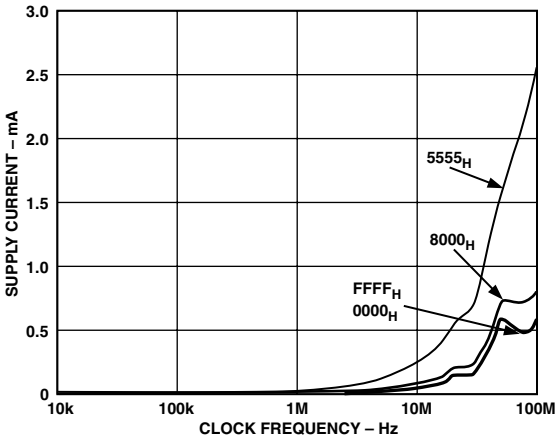
TPC 5. Linearity Errors vs. V_{DD}



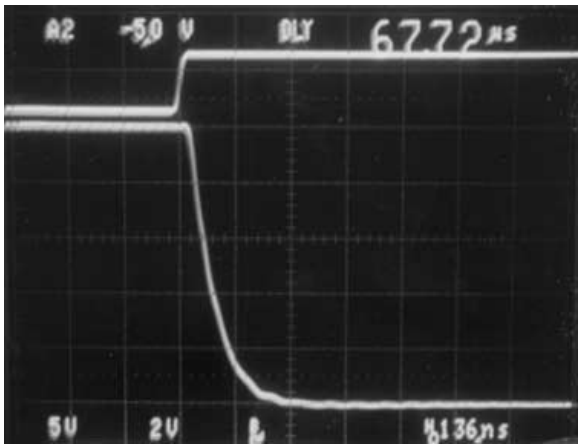
TPC 3. AD5553 Integral Nonlinearity Error



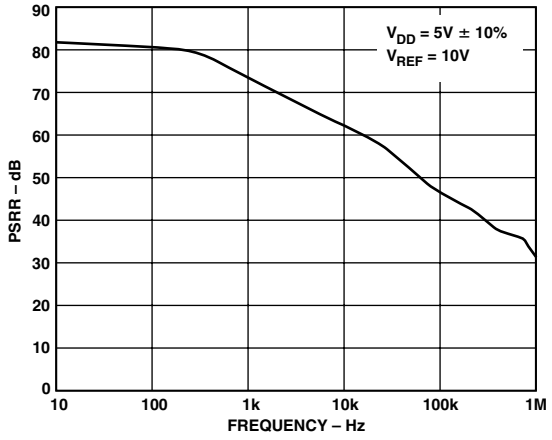
TPC 6. Supply Current vs. Logic Input Voltage



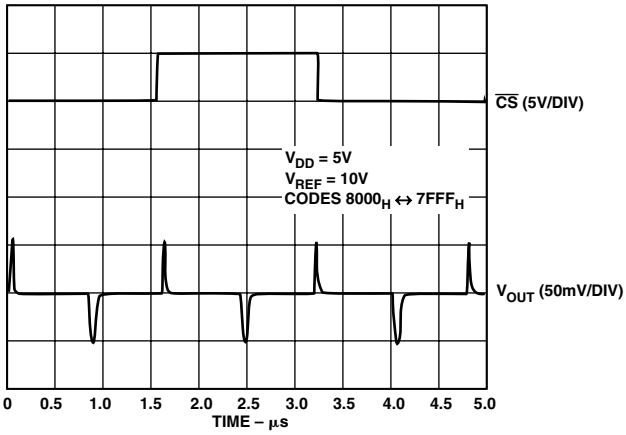
TPC 7. AD5543 Supply Current vs. Clock Frequency



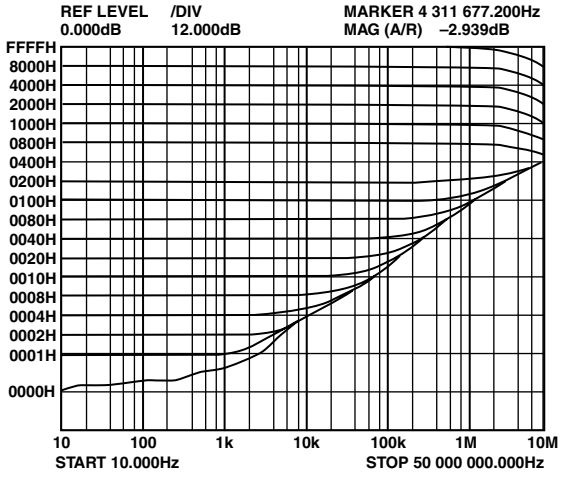
TPC 10. Settling Time



TPC 8. Power Supply Rejection vs. Frequency



TPC 11. Midscale Transition and Digital Feedthrough



TPC 9. Reference Multiplying Bandwidth

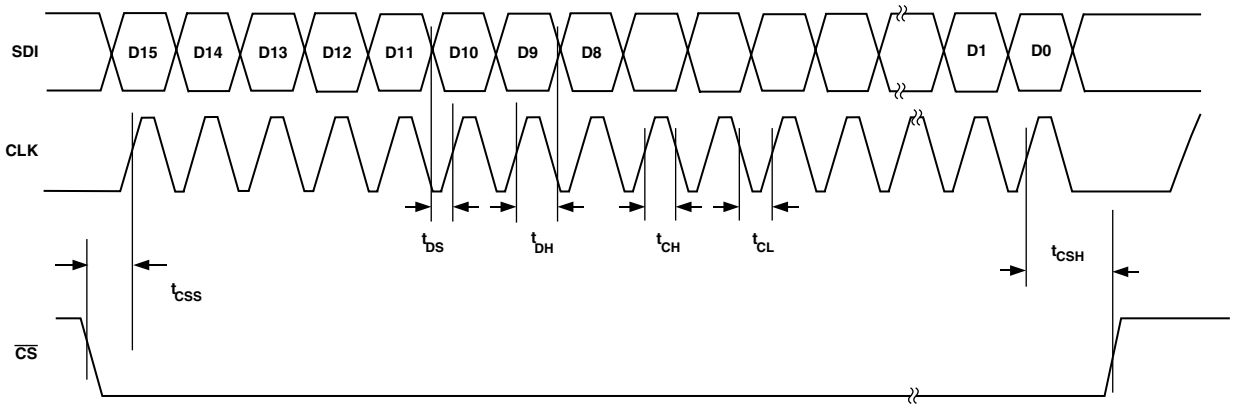


Figure 3a. AD5543 Timing Diagram

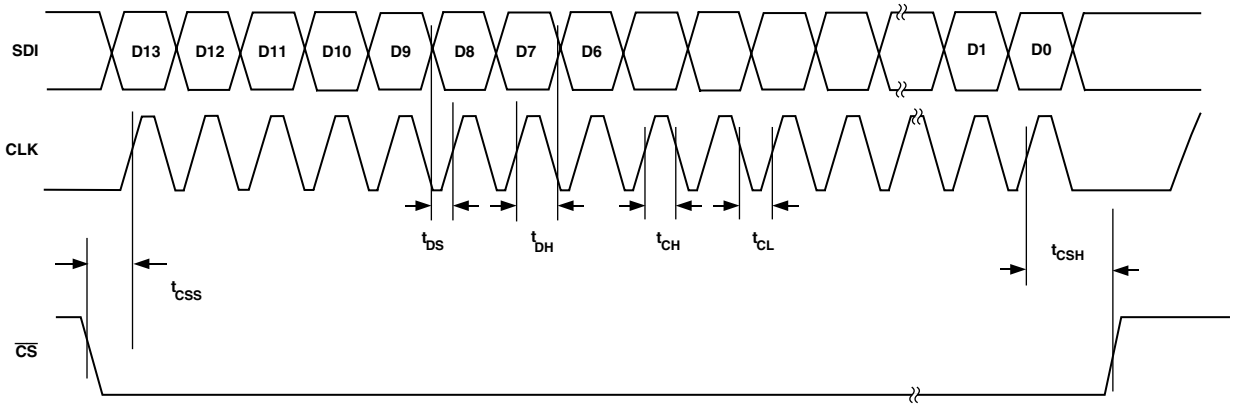


Figure 3b. AD5553 Timing Diagram

Table I. Control-Logic Truth Table

CLK	$\overline{CS}$	Serial Shift Register Function	DAC Register
X	H	No Effect	Latched
↑+	L	Shift Register Data Advanced One Bit	Latched
X	H	No Effect	Latched
X	↑+	Shift Register Data Transferred to DAC Register	New Data Loaded from Serial Register

↑+ positive logic transition; X Don't Care

Table II. AD5543 Serial Input Register Data Format; Data is Loaded in the MSB-First Format

	MSB														LSB	
Bit Position	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data-Word	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table III. AD5553 Serial Input Register Data Format; Data is Loaded in the MSB-First Format

	MSB												LSB	
Bit Position	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data-Word*	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

*A full 16-bit data-word can be loaded into the AD5553 serial input register, but only the last 14 bits entered will be transferred to the DAC register when $\overline{CS}$ returns to logic high.

CIRCUIT OPERATION

The AD5543/AD5553 contains a 16-/14-bit, current output, digital-to-analog converter, a serial input register, and a DAC register. Both converters use a 3-wire serial data interface.

D/A Converter Section

The DAC architecture uses a current steering R-2R ladder design. Figure 4 shows the typical equivalent DAC structure. The DAC contains a matching feedback resistor for use with an external op amp, (see Figure 5). With R_{FB} and I_{OUT} terminals connected to the op amp output and inverting node respectively, a precision voltage output can be achieved as:

$$V_{OUT} = -V_{REF} \times D / 65{,}536 \ (AD5543) \quad (1)$$

$$V_{OUT} = -V_{REF} \times D / 16{,}384 \ (AD5553) \quad (2)$$

Note that the output voltage polarity is opposite to the V_{REF} polarity for dc reference voltages.

These DACs are designed to operate with either negative or positive reference voltages. The V_{DD} power pin is only used by the internal logic to drive the DAC switches' ON and OFF states.

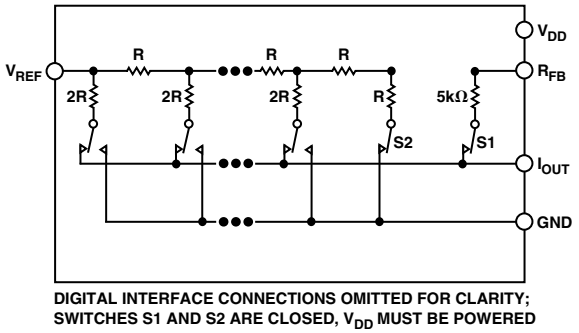


Figure 4. Equivalent R-2R DAC Circuit

Note that a matching switch is used in series with the internal 5 kΩ feedback resistor. If users attempt to measure RFB, power must be applied to V_{DD} to achieve continuity.

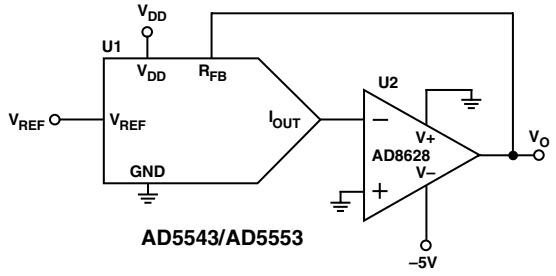


Figure 5. Voltage Output Configuration

These DACs are also designed to accommodate ac reference input signals. The AD5543 accommodates input reference voltages in the range of –12 V to +12 V. The reference voltage inputs exhibit a constant nominal input resistance value of 5 kΩ, ±30%. The DAC output (I_{OUT}) is code-dependent, producing various resistances and capacitances. External amplifier choice should take into account the variation in impedance generated by the AD5543 on the amplifier's inverting input node. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. To maintain good analog performance, power supply bypassing of 0.01 µF to 0.1 µF ceramic or chip capacitors in parallel with a 1 µF tantalum capacitor is recommended. Due to degradation of power supply rejection ratio in frequency, users must avoid using switching power supplies.

SERIAL DATA INTERFACE

The AD5543/AD5553 uses a 3-wire ($\overline{CS}$, SDI, CLK) serial data interface. New serial data is clocked into the serial input register in a 16-bit data-word format for AD5543. The MSB is loaded first. Table II defines the 16 data-word bits. Data is placed on the SDI pin and clocked into the register on the positive clock edge of CLK, subject to the data setup and hold time requirements specified in the interface timing specifications. Only the last 16 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin is strobed to transfer the serial register data to the DAC register. Since most microcontrollers output serial data in 8-bit bytes, two data bytes can be written to the AD5543/AD5553. After loading the serial register, the rising edge of $\overline{CS}$ transfers the serial register data to the DAC register; during this strobe, the CLK should not be toggled. For the AD5553, with 16-bit clock cycles, the two LSBs are ignored.

ESD Protection Circuits

All logic-input pins contain back-biased ESD protection Zener diodes connected to ground (GND) and V_{DD} as shown in Figure 6.

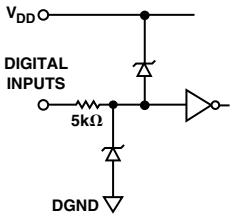


Figure 6. Equivalent ESD Protection Circuits

PCB Layout and Power Supply Bypassing

It is a good practice to employ compact, minimum lead length PCB layout design. The leads to the input should be as short as possible to minimize IR drop and stray inductance.

It is also essential to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low-ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance and filter out low frequency ripple

The PCB metal traces between V_{REF} and R_{FB} should also be matched to minimize gain error.

APPLICATIONS

Stability

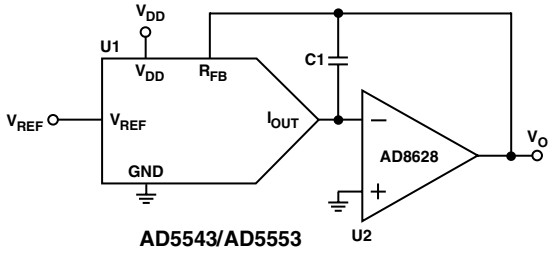


Figure 7. Optional Compensation Capacitor for Gain Peaking Prevention

In the I-to-V configuration, the I_{OUT} of the DAC and the inverting node of the op amp must be connected as close as possible, and proper PCB layout technique must be employed. Since every code change corresponds to a step function, gain peaking may occur if the op amp has limited GBP and there is excessive parasitic capacitance at the inverting node.

An optional compensation capacitor C1 can be added for stability as shown in Figure 7. C1 should be found empirically but 20 pF is generally adequate for the compensation.

Positive Voltage Output

To achieve the positive voltage output, an applied negative reference to the input of the DAC is preferred over the output inversion through an inverting amplifier because of the resistor's tolerance errors. To generate a negative reference, the reference can be level-shifted by an op amp such that the V_{OUT} and GND pins of the reference become the virtual ground and –2.5 V respectively, (see Figure 8).

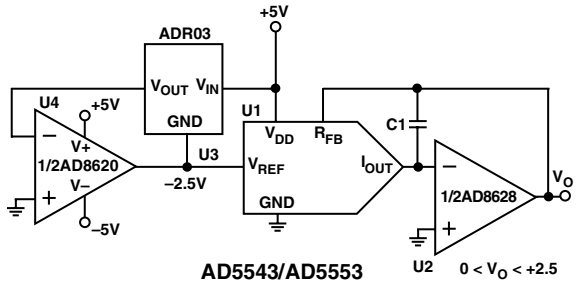


Figure 8. Positive Voltage Output Configuration

Bipolar Output

The AD5543/AD5553 is inherently a 2-quadrant multiplying D/A converter. That is, it can easily be set up for unipolar output operation. The full-scale output polarity is the inverse of the reference input voltage.

In some applications, it may be necessary to generate the full 4-quadrant multiplying capability or a bipolar output swing. This is easily accomplished by using an additional external amplifier U4 configured as a summing amplifier (see Figure 9). In this circuit, the second amplifier U4 provides a gain of 2 that increases the output span magnitude to 5 V. Biasing the external amplifier with a 2.5 V offset from the reference voltage results in a full 4-quadrant multiplying circuit. The transfer equation of this circuit shows that both negative and positive output voltages are created as the input data (D) is incremented from code zero (V_{OUT} = –2.5 V) to midscale (V_{OUT} = 0 V) to full-scale (V_{OUT} = +2.5 V).

$$V_{OUT} = (D / 32{,}768 - 1) \times V_{REF} \quad (AD5543) \tag{3}$$

$$V_{OUT} = (D / 16{,}384 - 1) \times V_{REF} \quad (AD5553) \tag{4}$$

For AD5543, the resistance tolerance becomes the dominant error of which users should be aware.

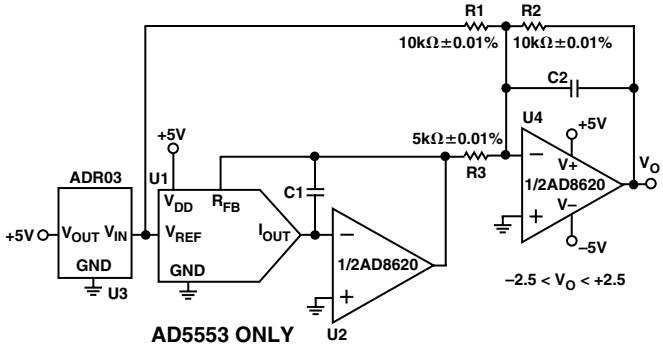


Figure 9. Four-Quadrant Multiplying Application Circuit

Programmable Current Source

Figure 10 shows a versatile V-I conversion circuit using an improved Howland Current Pump. In addition to the precision current conversion it provides, this circuit enables a bidirectional current flow and high voltage compliance. This circuit can be used in 4 to 20 mA current transmitters with up to 500 Ω of load. In Figure 10, it can be shown that if the resistor network is matched, the load current is:

$$I_L = \frac{(R2 + R3)/R1}{R3} \times V_{REF} \times D \quad (5)$$

*R*3 in theory can be made small to achieve the current needed within the U3 output current driving capability. This circuit is versatile such that AD8510 can deliver ±20 mA in both directions and the voltage compliance approaches 15 V, which is limited mainly by the supply voltages of U3. However, users must pay attention to the compensation. Without C1, it can be shown that the output impedance becomes:

$$Z_O = \frac{R1'\,R3(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \quad (6)$$

If the resistors are perfectly matched, Z_O is infinite, which is desirable, and behaves as an ideal current source. On the other hand, if they are not matched, Z_O can be either positive or negative. Negative can cause oscillation. As a result, C1 is needed to prevent the oscillation. For critical applications, C1 could be found empirically, but typically falls in the range of few pF.

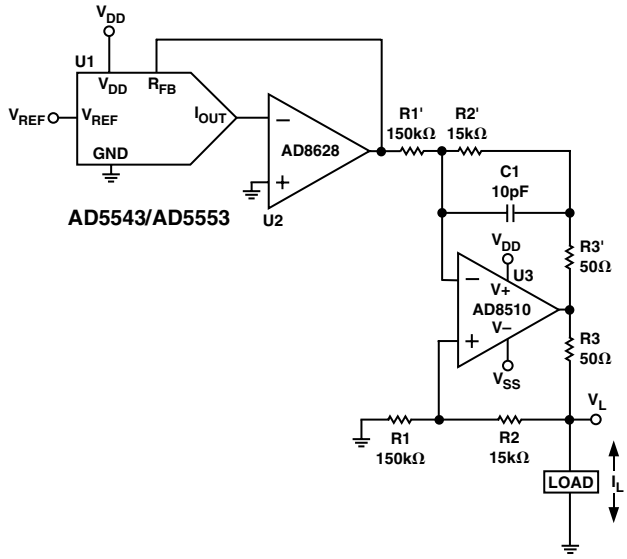
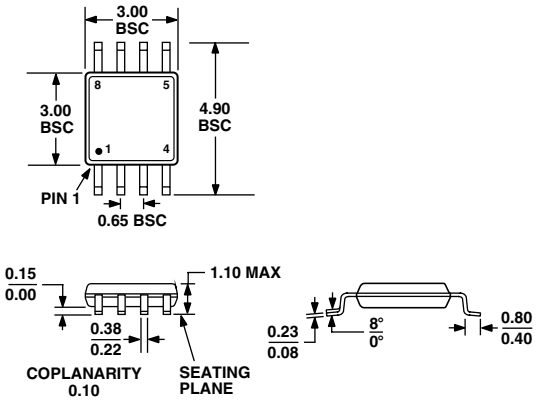


Figure 10. Programmable Current Source with Bidirectional Current Control and High Voltage Compliance Capabilities

OUTLINE DIMENSIONS

8-Lead microSOIC Package [MSOP]
(RM-8)

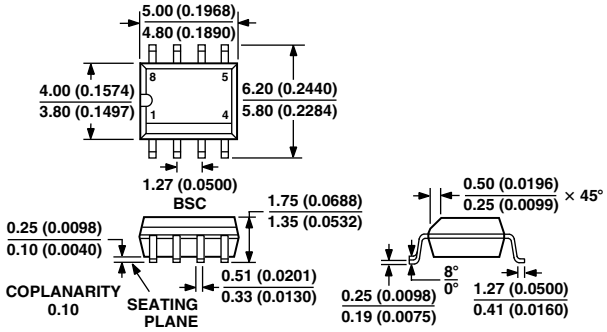
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(RN-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

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2/03—Data Sheet changed from REV. 0 to REV. A.	
Changes to ORDERING GUIDE	3

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