*Preliminary*

*128K X 32 Bit Synchronous High Speed SRAM with Burst Counter and Pipelined Data Output*

## Document Title

**128K X 32 Bit Synchronous High Speed SRAM with Burst Counter and Pipelined Data Output**

## Revision History

| Rev. No. | History | Issue Date | Remark |
|---|---|---|---|
| 1.0 | Initial issue | November, 1997 | Preliminary |
| 1.1 | Change pin 14 description from VCC to NC<br>Change package type from 100-pin TQFP to 100-pin LQFP | June 17, 1998 | |
| 2.0 | Change fast access times from 4.5/5/5.5 ns to 4.2/4.5/5.0 ns | August 27, 1998 | |
| 2.1 | Modify 100-pin LQFP symbol y dimensions -<br>Max. in mm : 0.08 → 0.1<br>Max. in inches : 0.003 → 0.004 | December 31, 1998 | |

Preliminary

# 128K X 32 Bit Synchronous High Speed SRAM with Burst Counter and Pipelined Data Output

## Features

- Fast access times: 4.2/4.5/5.0 ns (143/133/100 MHz)
- Single +3.3V+10% or +3.3V-5% power supply
- Separate +2.5V+0.4V/-0.12V isolated output buffer
- 3.3V tolerant inputs
- Synchronous burst function
- Individual Byte Write control and Global Write
- Registered output for pipelined applications
- Three separate chip enables allow wide range of options for CE control, address pipelining
- Selectable BURST mode
- SLEEP mode (ZZ pin) provided
- Available in 100-pin LQFP package

## General Description

The A63G7332 is a high-speed, low-power SRAM containing 4,194,304 bits of bit synchronous memory, organized as 131,072 words by 32 bits.

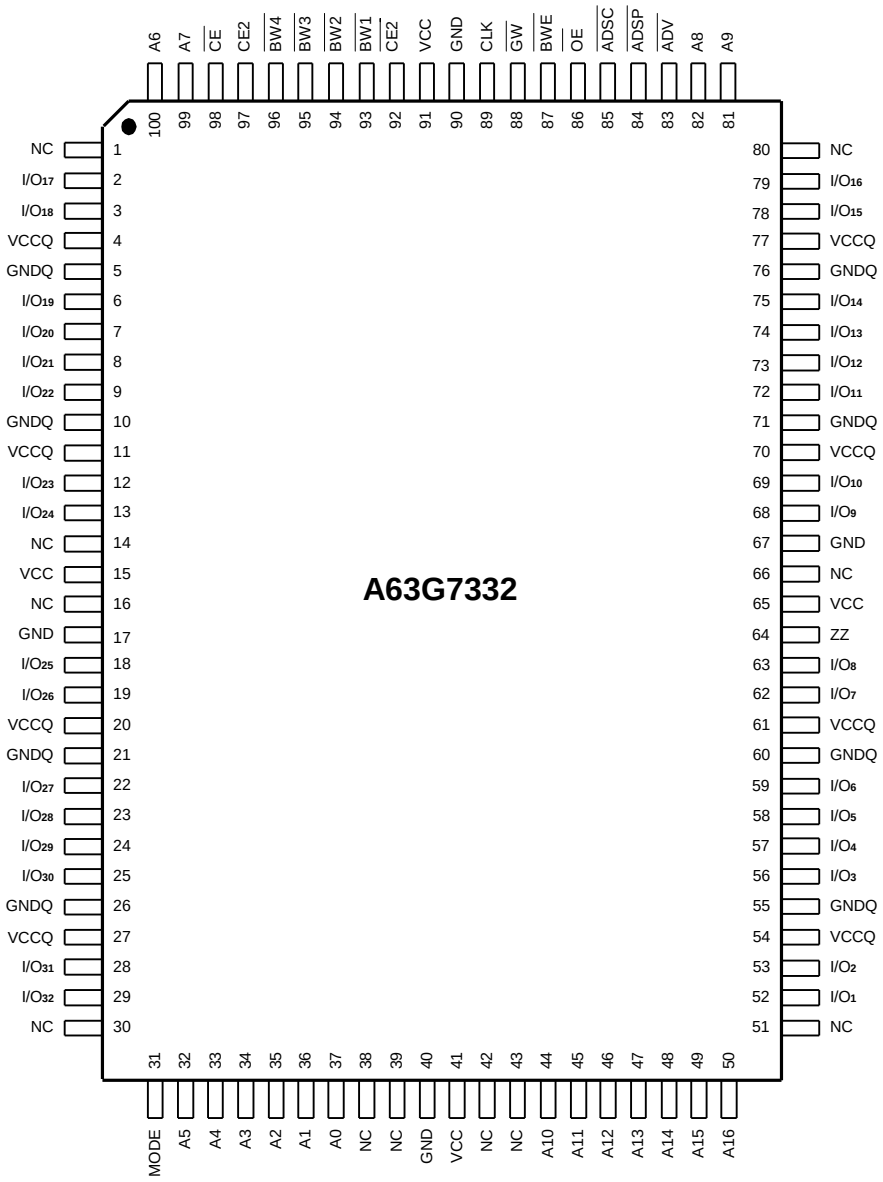
The A63G7332 combines advanced synchronous peripheral circuitry, 2-bit burst control, input registers, output registers and a 128K X 32 SRAM core to provide a wide range of data RAM applications.

The positive edge triggered single clock input (CLK) controls all synchronous inputs passing through the registers. Synchronous inputs include all addresses (A0 - A16), all data inputs ($I/O_1$ - $I/O_{32}$), active LOW chip enable ($\overline{CE}$), two additional chip enables (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$), byte write enables ($\overline{BWE}$, $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) and Global Write ($\overline{GW}$). Asynchronous inputs include output enable ($\overline{OE}$), clock (CLK), BURST mode (MODE) and SLEEP mode (ZZ).

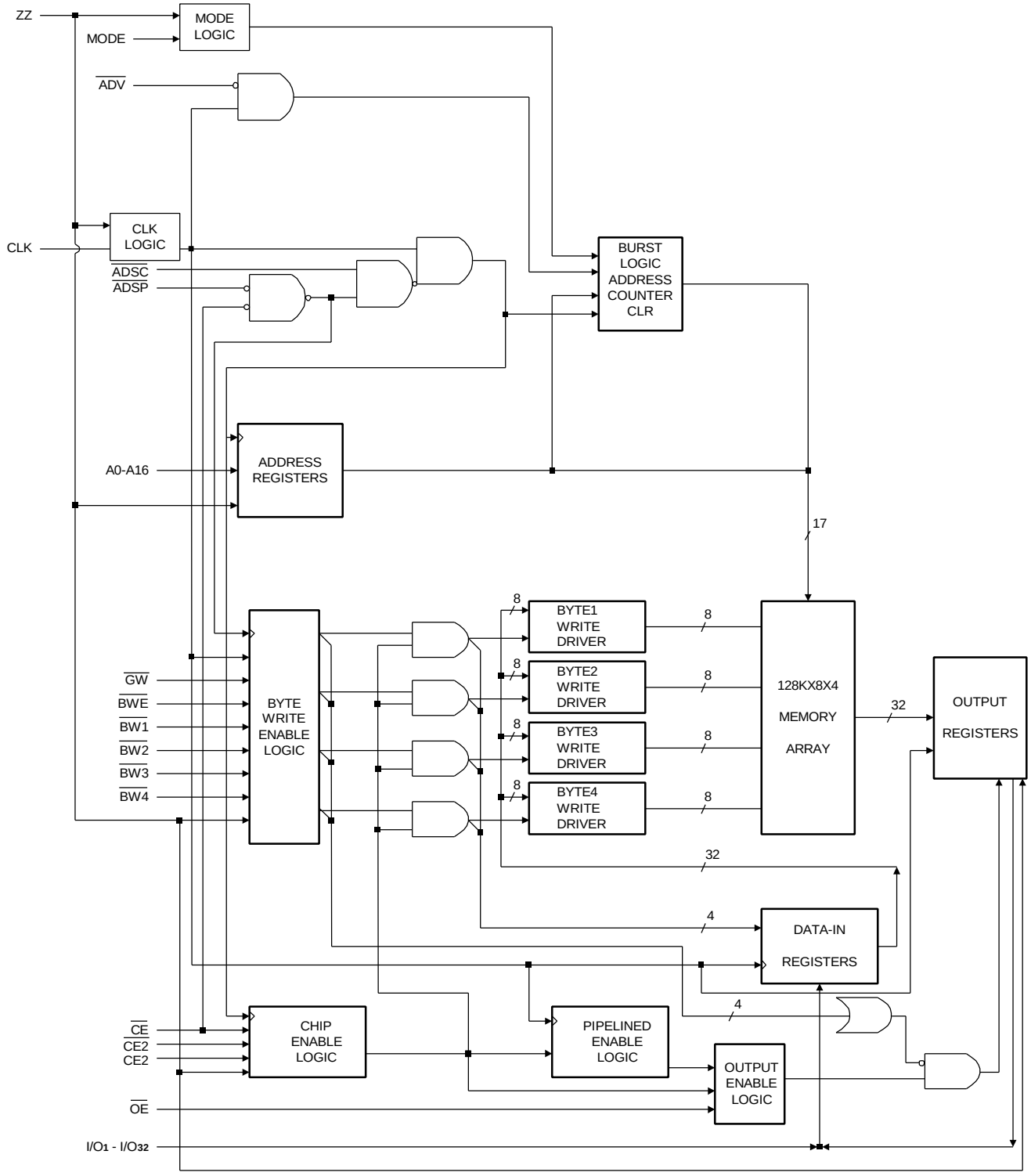
Burst operations can be initiated with either the address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pin. Subsequent burst sequence burst addresses can be internally generated by the A63G7332 and controlled by the burst advance ($\overline{ADV}$) pin. Write cycles are internally self-timed and synchronous with the rising edge of the clock (CLK).

This feature simplifies the write interface. Individual Byte enables allow individual bytes to be written. $\overline{BW1}$ controls $I/O_1$ - $I/O_8$, $\overline{BW2}$ controls $I/O_9$ - $I/O_{16}$, $\overline{BW3}$ controls $I/O_{17}$ - $I/O_{24}$, and $\overline{BW4}$ controls $I/O_{25}$ - $I/O_{32}$, all on the condition that $\overline{BWE}$ is LOW. $\overline{GW}$ LOW causes all bytes to be written.

## Pin Configuration



## Block Diagram



## Pin Description

| Pin No. | Symbol | Description |
|---|---|---|
| 32 - 37, 44 - 50, 81, 82, 99, 100 | A0 - A16 | Address Inputs |
| 89 | CLK | Clock |
| 87, 93 - 96 | $\overline{BWE}$, $\overline{BW1}$ - $\overline{BW4}$ | Byte Write Enables |
| 88 | $\overline{GW}$ | Global Write |
| 86 | $\overline{OE}$ | Output Enable |
| 92, 97, 98 | $\overline{CE2}$, CE2, $\overline{CE}$ | Chip Enables |
| 83 | $\overline{ADV}$ | Burst Address Advance |
| 84 | $\overline{ADSP}$ | Processor Address Status |
| 85 | $\overline{ADSC}$ | Controller Address Status |
| 31 | MODE | Burst Mode: HIGH or NC (Interleaved burst)<br>LOW (Linear burst) |
| 64 | ZZ | Asynchronous Power-Down (Snooze): HIGH (Sleep)<br>LOW or NC (Wake up) |
| 2, 3, 6 - 9, 12, 13, 18, 19, 22 - 25, 28, 29, 52, 53, 56 - 59, 62, 63, 68, 69, 72 - 75, 78, 79 | $I/O_1$- $I/O_{32}$ | Data Inputs/Outputs |
| 1,14,16, 30, 38, 39, 42, 43, 51, 66, 80 | NC | No Connection |
| 14, 15, 41, 65, 91 | VCC | Power Supply |
| 17, 40, 67, 90 | GND | Ground |
| 4, 11, 20, 27, 54, 61, 70, 77 | VCCQ | Isolated Output Buffer Supply |
| 5, 10, 21, 26, 55, 60, 71, 76 | GNDQ | Isolated Output Buffer Ground |

**Synchronous Truth Table (See Notes 1 Through 5)**

| Operation | Address Used | $\overline{CE}$ | $\overline{CE2}$ | CE2 | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{WRITE}$ | $\overline{OE}$ | CLK | I/O Operation |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselected Cycle, Power-down | NONE | H | X | X | X | L | X | X | X | L-H | High-Z |
| Deselected Cycle, Power-down | NONE | L | X | L | L | X | X | X | X | L-H | High-Z |
| Deselected Cycle, Power-down | NONE | L | H | X | L | X | X | X | X | L-H | High-Z |
| Deselected Cycle, Power-down | NONE | L | X | L | H | L | X | X | X | L-H | High-Z |
| Deselected Cycle, Power-down | NONE | L | H | X | H | L | X | X | X | L-H | High-Z |
| READ Cycle, Begin Burst | External | L | L | H | L | X | X | X | L | L-H | Dout |
| READ Cycle, Begin Burst | External | L | L | H | L | X | X | X | H | L-H | High-Z |
| WRITE Cycle, Begin Burst | External | L | L | H | H | L | X | L | X | L-H | Din |
| READ Cycle, Begin Burst | External | L | L | H | H | L | X | H | L | L-H | Dout |
| READ Cycle, Begin Burst | External | L | L | H | H | L | X | H | H | L-H | High-Z |
| READ Cycle, Continue Burst | Next | X | X | X | H | H | L | H | L | L-H | Dout |
| READ Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | L-H | High-Z |
| READ Cycle, Continue Burst | Next | H | X | X | X | H | L | H | L | L-H | Dout |
| READ Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | L-H | High-Z |
| WRITE Cycle, Continue Burst | Next | X | X | X | H | H | L | L | X | L-H | Din |
| WRITE Cycle, Continue Burst | Next | H | X | X | X | H | L | L | X | L-H | Din |
| READ Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | L | L-H | Dout |
| READ Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | L-H | High-Z |
| READ Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | L | L-H | Dout |
| READ Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | L-H | High-Z |
| WRITE Cycle, Suspend Burst | Current | X | X | X | H | H | H | L | X | L-H | Din |
| WRITE Cycle, Suspend Burst | Current | H | X | X | X | H | H | L | X | L-H | Din |

Notes: 1. X = "Disregard", H = Logic High, L = Logic Low.

2. $\overline{WRITE}$ = L means:
   1) Any $\overline{BWx}$ ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, or $\overline{BW4}$) and $\overline{BWE}$ are low or
   2) $\overline{GW}$ is low.
3. All inputs except $\overline{OE}$ must be synchronized with setup and hold times around the rising edge (L-H) of CLK.
4. For write cycles that follow read cycles, $\overline{OE}$ must be HIGH before the input data request setup time and held HIGH throughout the input data hold time.
5. $\overline{ADSP}$ LOW always initiates an internal Read at the L-H edge of CLK. A Write is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. Refer to the Write timing diagram for clarification.

**Write Truth Table**

| Operation | $\overline{GW}$ | $\overline{BWE}$ | $\overline{BW1}$ | $\overline{BW2}$ | $\overline{BW3}$ | $\overline{BW4}$ |
|---|---|---|---|---|---|---|
| READ | H | H | X | X | X | X |
| READ | H | L | H | H | H | H |
| WRITE Byte 1 | H | L | L | H | H | H |
| WRITE all bytes | H | L | L | L | L | L |
| WRITE all bytes | L | X | X | X | X | X |

### Linear Burst Address Table (MODE = LOW)

| First Address (External) | Second Address (Internal) | Third Address (Internal) | Fourth Address (Internal) |
|---|---|---|---|
| X . . . X00 | X . . . X01 | X . . . X10 | X . . . X11 |
| X . . . X01 | X . . . X10 | X . . . X11 | X . . . X00 |
| X . . . X10 | X . . . X11 | X . . . X00 | X . . . X01 |
| X . . . X11 | X . . . X00 | X . . . X01 | X . . . X10 |

### Interleaved Burst Address Table (MODE = HIGH or NC)

| First Address (External) | Second Address (Internal) | Third Address (Internal) | Fourth Address (Internal) |
|---|---|---|---|
| X . . . X00 | X . . . X01 | X . . . X10 | X . . . X11 |
| X . . . X01 | X . . . X00 | X . . . X11 | X . . . X10 |
| X . . . X10 | X . . . X11 | X . . . X00 | X . . . X01 |
| X . . . X11 | X . . . X10 | X . . . X01 | X . . . X00 |

### Absolute Maximum Ratings*

Power Supply Voltage (VCC) . . . . . -0.5V to +4.6V
Voltage Relative to GND for any Pin Except VCC (Vin, Vout) . . . . . -0.5V to VCC +0.5V
Power Dissipation ($P_D$) . . . . . 2W
Operating Temperature (Topr) . . . . . 0°C to 70°C
Storage Temperature (Tbias) . . . . . -10°C to 85 °C
Storage Temperature (Tstg) . . . . . -55°C to 125°C

### *Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

### Recommended DC Operating Conditions

(0°C ≤ $T_A$ ≤ 70°C, VCC = 3.3V+10% or 3.3V-5%, VCCQ = +2.5V+0.4V/-0.125V, unless otherwise noted)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| VCC | Supply Voltage (Operating Voltage Range) | 3.1 | 3.3 | 3.6 | V | |
| VCCQ | Isolated Input Buffer Supply | 2.375 | 2.5 | 2.9 | V | |
| GND | Supply Voltage to GND | 0.0 | - | 0.0 | V | |
| $V_{IH}$ | Input High Voltage | 1.7 | - | VCC+0.3 | V | 1, 2 |
| $V_{IHQ}$ | Input High Voltage | 1.7 | - | VCC+0.3 | V | |
| $V_{IL}$ | Input Low Voltage | -0.3 | - | 0.7 | V | 1, 2 |

## DC Electrical Characteristics

(0°C ≤ $T_A$ ≤ 70°C, VCC = 3.3V+10% or 3.3V-5%, VCCQ = +2.5V+0.4V/-0.125V, unless otherwise noted)

| Symbol | Parameter | Min. | Max. | Unit | Test Conditions | Note |
|---|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | - | ±2.0 | μA | All inputs $V_{IN}$ = GND to VCC | |
| $\|I_{LO}\|$ | Output Leakage Current | - | ±2.0 | μA | $\overline{OE}$ = $V_{IH}$, Vout = GND to VCC | |
| $I_{CC1}$ | Supply Current | - | 300 | mA | Device selected; VCC = max.<br>Iout = 0mA, all inputs = $V_{IH}$ or $V_{IL}$<br>Cycle time = $t_{KC}$ min. | 3, 11 |
| $I_{SB1}$ | Standby Current | - | 25 | mA | Device deselected; VCC = max.<br>All inputs are fixed.<br>All inputs ≥ VCC - 0.2V<br>or ≤ GND + 0.2V<br>Cycle time = $t_{KC}$ min. | 11 |
| $I_{SB2}$ | | - | 10 | mA | ZZ ≥ VCC - 0.2V | |
| $V_{OL}$ | Output Low Voltage | - | 0.7 | V | $I_{OL}$ = 2.0 mA | |
| | | - | 0.4 | V | $I_{OL}$ = 1.0 mA | |
| $V_{OH}$ | Output High Voltage | 1.7 | - | V | $I_{OH}$ = -2.0 mA | |
| | | 2.0 | - | V | $I_{OH}$ = -1.0 mA | |

## Capacitance

| Symbol | Parameter | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 3 | 4 | pF | $T_A$ = 25 C; f = 1MHz<br>VCC = 3.3V |
| $C_{I/O}$ | Input/Output Capacitance | 4 | 5 | pF | |

* These parameters are sampled and not 100% tested.

**AC Characteristics** (0°C ≤ $T_A$ ≤ 70°C, VCC = 3.3V+10% or 3.3V-5%)

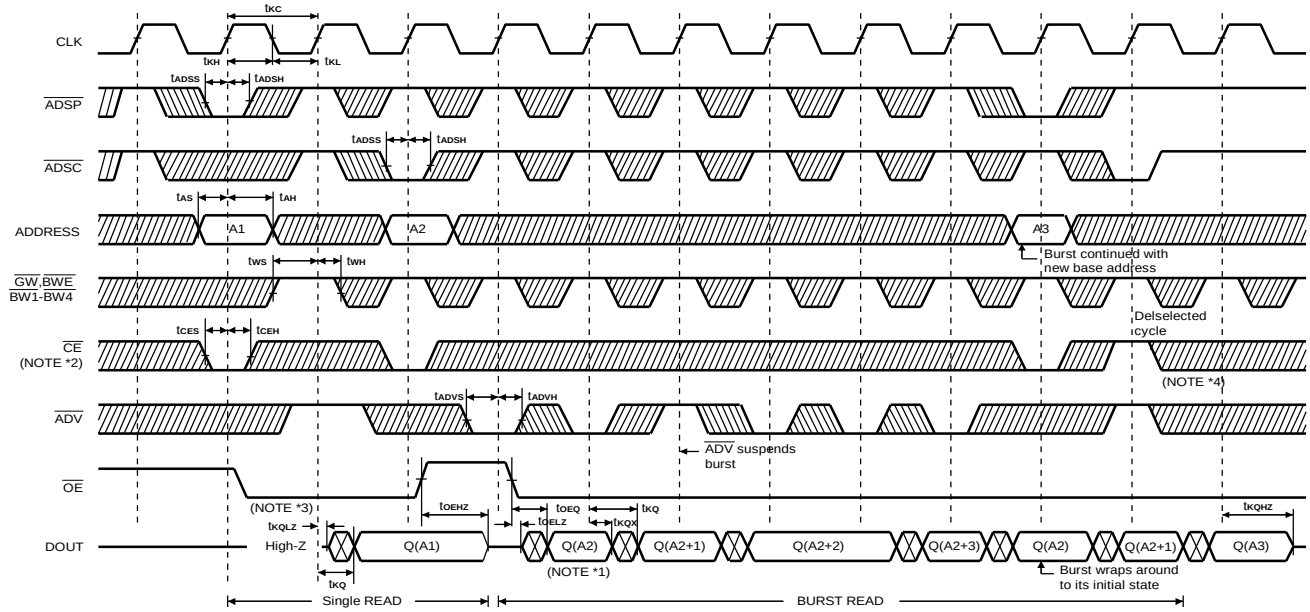
| Symbol | Parameter | -4.2 | | -4.5 | | -5.0 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $t_{KC}$ | Clock Cycle Time | 7 | - | 7.5 | - | 10 | - | ns | |
| $t_{KH}$ | Clock High Time | 1.9 | - | 1.9 | - | 3.2 | - | ns | |
| $t_{KL}$ | Clock Low Time | 1.9 | - | 1.9 | - | 3.2 | - | ns | |
| $t_{KQ}$ | Clock to Output Valid | - | 4.2 | - | 4.5 | - | 5.0 | ns | |
| $t_{KQX}$ | Clock to Output Invalid | 1.5 | - | 1.5 | - | 1.5 | - | ns | |
| $t_{KQLZ}$ | Clock to Output in Low-Z | 1.5 | - | 1.5 | - | 1.5 | - | ns | 5, 6 |
| $t_{KQHZ}$ | Clock to Output in High-Z | 1.5 | 4.2 | 1.5 | 4.5 | 1.5 | 5.0 | ns | 5, 6 |
| $t_{OEQ}$ | $\overline{OE}$ to Output Valid | - | 4.2 | - | 4.5 | - | 5.0 | ns | 8 |
| $t_{OELZ}$ | $\overline{OE}$ to Output in Low-Z | 0 | - | 0 | - | 0 | - | ns | 5, 6 |
| $t_{OEHZ}$ | $\overline{OE}$ to Output in High-Z | - | 4.2 | - | 4.5 | - | 5.0 | ns | 5, 6 |
| Setup Times | | | | | | | | | |
| $t_{AS}$ | Address | 2.0 | - | 2.0 | - | 2.0 | - | ns | 7, 9 |
| $t_{ADSS}$ | Address Status ( $\overline{ADSC}$ , $\overline{ADSP}$ ) | 2.0 | - | 2.0 | - | 2.0 | - | ns | 7, 9 |
| $t_{ADVS}$ | Address Advance ( $\overline{ADV}$ ) | 2.0 | - | 2.0 | - | 2.0 | - | ns | 7, 9 |
| $t_{WS}$ | Write Signals ( $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$ ) | 2.0 | - | 2.0 | - | 2.0 | - | ns | 7, 9 |
| $t_{DS}$ | Data-in | 2.0 | - | 2.0 | - | 2.0 | - | ns | 7, 9 |
| $t_{CES}$ | Chip Enable ( $\overline{CE}$ , CE2, $\overline{CE2}$ ) | 2.0 | - | 2.0 | - | 2.0 | - | ns | 7, 9 |

**AC Characteristics (continued)**

| Symbol | Parameter | -4.2 | | -4.5 | | -5.0 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Hold Times | | | | | | | | | |
| $t_{AH}$ | Address | 0.5 | - | 0.5 | - | 0.5 | - | ns | 7, 9 |
| $t_{ADVH}$ | Address Status ( $\overline{ADSC}$ , $\overline{ADSP}$ ) | 0.5 | - | 0.5 | - | 0.5 | - | ns | 7, 9 |
| $t_{AAH}$ | Address Advance ( $\overline{ADV}$ ) | 0.5 | - | 0.5 | - | 0.5 | - | ns | 7, 9 |
| $t_{WH}$ | Write Signal ( $\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$ ) | 0.5 | - | 0.5 | - | 0.5 | - | ns | 7, 9 |
| $t_{DH}$ | Data-in | 0.5 | - | 0.5 | - | 0.5 | - | ns | 7, 9 |
| $t_{CEH}$ | Chip Enable ( $\overline{CE}$ , CE2, $\overline{CE2}$ ) | 0.5 | - | 0.5 | - | 0.5 | - | ns | 7, 9 |

Notes:
1. All voltages refer to GND.
2. Overshoot: $V_{IH} \le +4.6V$ for $t \le t_{KC}/2$.
   Undershoot: $V_{IH} \ge -0.7V$ for $t \le t_{KC}/2$.
   Power-up: $V_{IH} \le +3.6$ and $VCC \le 3.1V$ for $t \le 200ms$
3. $I_{CC}$ is given with no output current. $I_{CC}$ increases with greater output loading and faster cycle times.
4. Test conditions assume the output loading shown in Figure 1, unless otherwise specified.
5. For output loading, $C_L$ = 5pF, as shown in Figure 2. Transition is measured ±150mV from steady state voltage.
6. At any given temperature and voltage condition, $t_{KQHZ}$ is less than $t_{KQLZ}$ and $t_{OEHZ}$ is less than $t_{QELZ}$.
7. A WRITE cycle is defined by at least one Byte Write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ( $\overline{ADSC}$ or $\overline{ADV}$ LOW) or $\overline{ADSP}$ LOW for the required setup and hold times.
8. $\overline{OE}$ has no effect when a Byte Write enable is sampled LOW.
9. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and the chip is enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW to remain enabled.
10. The load used for $V_{OH}$, $V_{OL}$ testing is shown in Figure 2. AC load current is higher than the given DC values. AC I/O curves are available upon request.
11. "Device Deselected" means device is in POWER-DOWN mode, as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
12. MODE pin has an internal pulled-up, and ZZ pin has an internal pulled-down. All of then exhibit an input leakage current of 10μA.
13. Snooze (ZZ) input is recommended that users plan for four clock cycles to go into SLEEP mode and four clocks to emerge from SLEEP mode to ensure no data is lost.

## Timing Waveforms




**Read Timing**

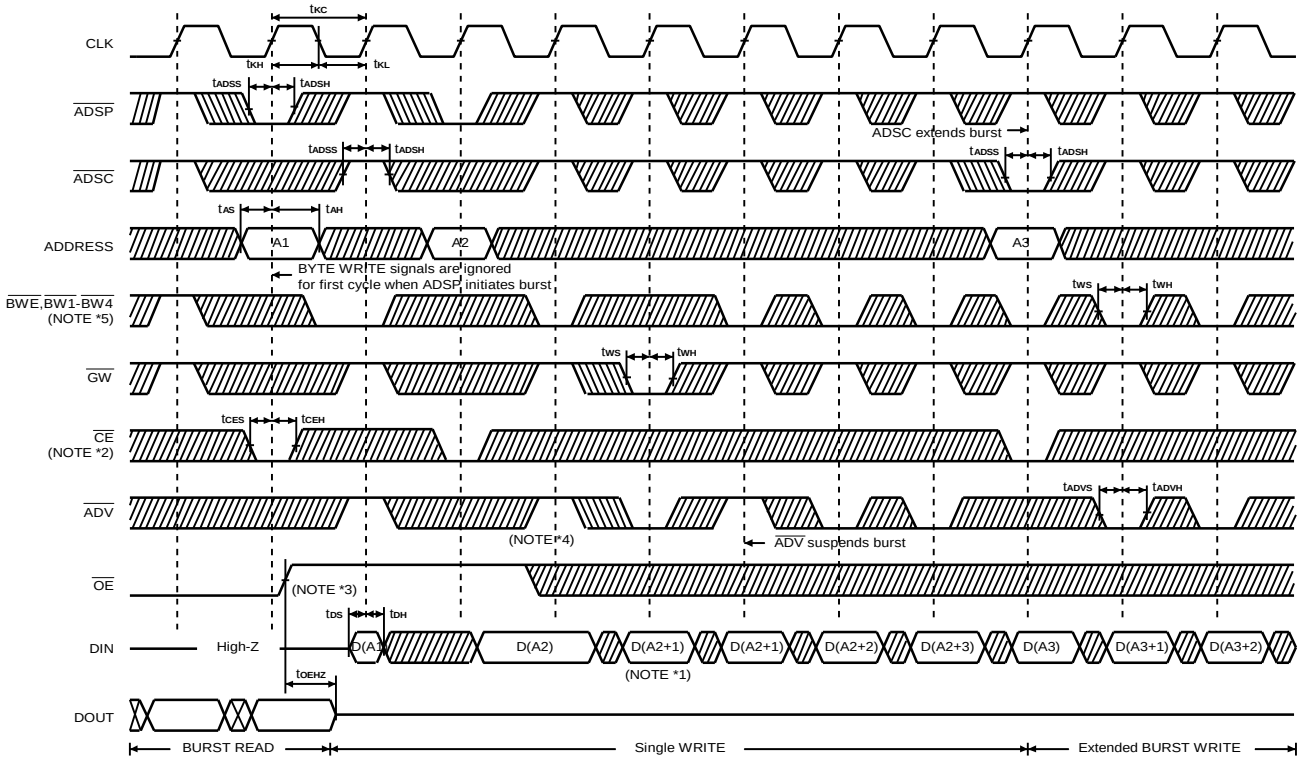
Notes:

*1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the internal burst address immediately following A2.

*2. Timing for $\overline{CE2}$ and CE2 is identical to that for $\overline{CE}$. As shown in this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

*3. Timing shown assumes that the device was not enabled before entering this sequence. $\overline{OE}$ does not cause Q to be driven until after the rising edge of the following clock.

## Timing Waveforms (continued)




**Write Timing**

Notes: *1. D(A2) refers to output from address A2. D(A2+1) refers to output from the internal burst address immediately following A2.

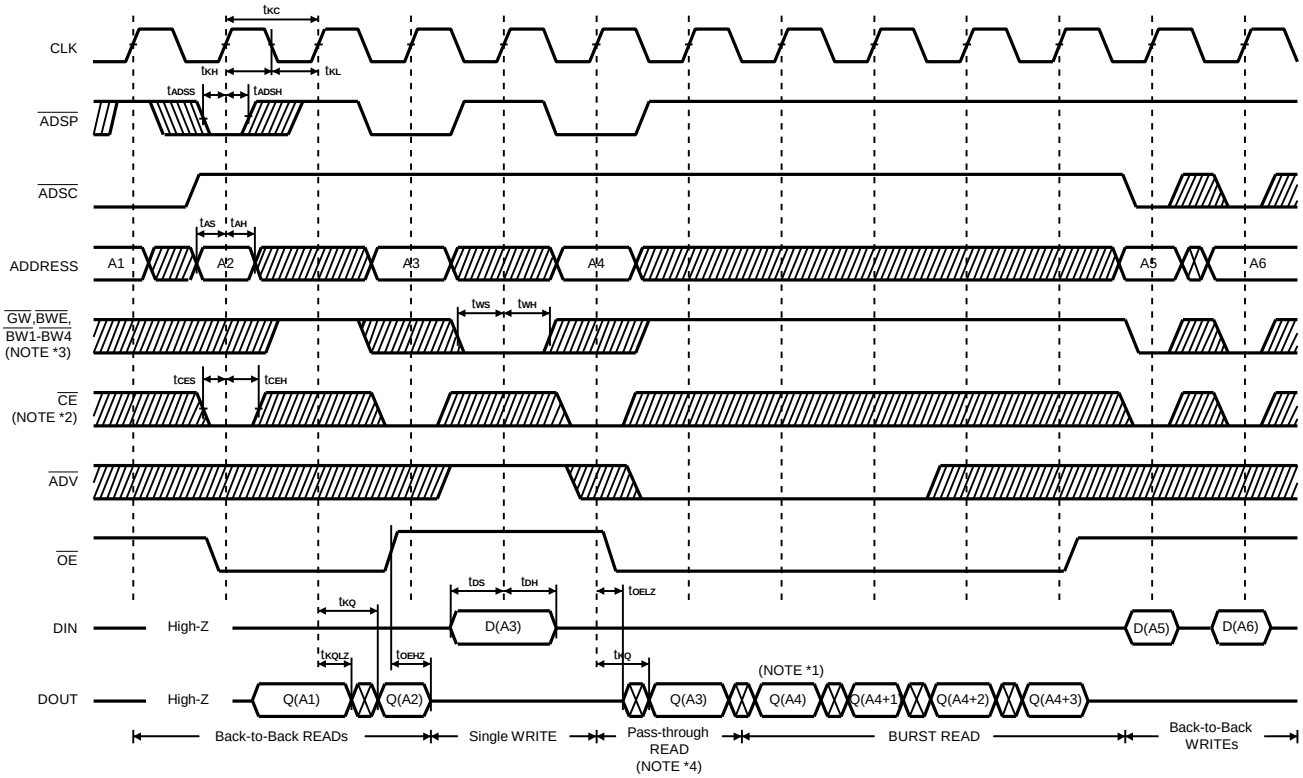
*2. Timing for $\overline{CE2}$ and CE2 is identical to that for $\overline{CE}$. As shown in the above diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

*3. $\overline{OE}$ must be HIGH before the input data setup, and held HIGH throughout the data hold period. This prevents input/output data contention for the period prior to the time Byte Write enable inputs are sampled.

*4. $\overline{ADV}$ must be HIGH to permit a Write to the loaded address.

*5. Byte Write enables are decided by means of a Write truth table.

## Timing Waveforms (continued)




**Read/Write Timing**

Notes:

*1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the internal burst address immediately following A4.

*2. Timing for $\overline{CE2}$ and CE2 is identical to that for $\overline{CE}$. As shown in this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

*3. Byte Write enables are decided by means of a Write truth table.

*4. Pass-through occurs when data is first written, then Read in sequence.

### AC Test Conditions

| | |
|---|---|
| Input Pulse Levels | GND to 2.5V |
| Input Rise and Fall Times | 1.5ns |
| Input Timing Reference Levels | 1.25V |
| Output Reference Levels | 1.25V |
| Output Load | See Figures 1 and 2 |

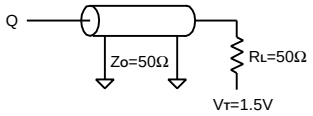



**Figure 1. Output Load Equivalent**

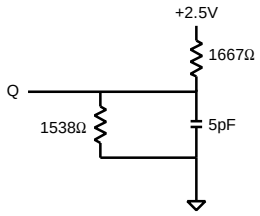



**Figure 2. Output Load Equivalent**

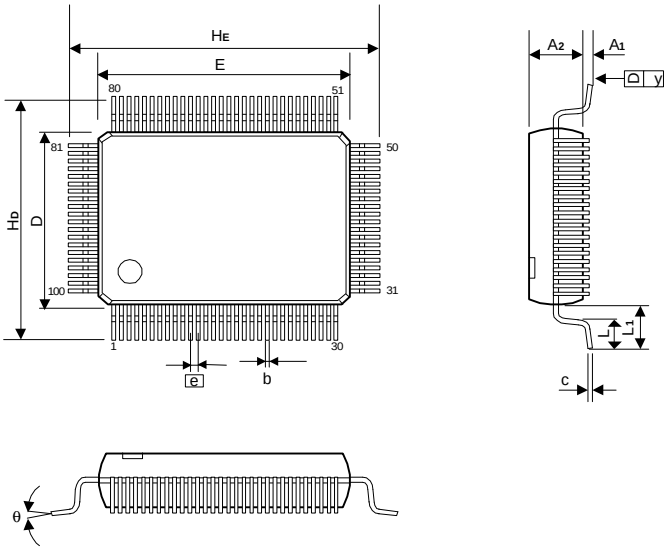
## Ordering Information

| Part No. | Access Times (ns) | Package |
|---|---|---|
| A63G7332E-4.2 | 4.2 | 100L LQFP |
| A63G7332E-4.5 | 4.5 | 100L LQFP |
| A63G7332E-5 | 5.0 | 100L LQFP |

## Package Information

### LQFP 100L Outline Dimensions

unit: inches/mm




| Symbol | Dimensions in inches | | | Dimensions in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| $A_1$ | 0.002 | - | - | 0.05 | - | - |
| $A_2$ | 0.053 | 0.055 | 0.057 | 1.35 | 1.40 | 1.45 |
| b | 0.011 | 0.013 | 0.015 | 0.27 | 0.32 | 0.37 |
| c | 0.005 | - | 0.008 | 0.12 | - | 0.20 |
| $H_E$ | 0.860 | 0.866 | 0.872 | 21.85 | 22.00 | 22.15 |
| E | 0.783 | 0.787 | 0.791 | 19.90 | 20.00 | 20.10 |
| $H_D$ | 0.624 | 0.630 | 0.636 | 15.85 | 16.00 | 16.15 |
| D | 0.547 | 0.551 | 0.555 | 13.90 | 14.00 | 14.10 |
| e | 0.026 BSC | | | 0.65 BSC | | |
| L | 0.018 | 0.024 | 0.030 | 0.45 | 0.60 | 0.75 |
| $L_1$ | 0.039 REF | | | 1.00 REF | | |
| y | - | - | 0.004 | - | - | 0.1 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |

**Notes:**
1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
   Total in excess of the b dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.