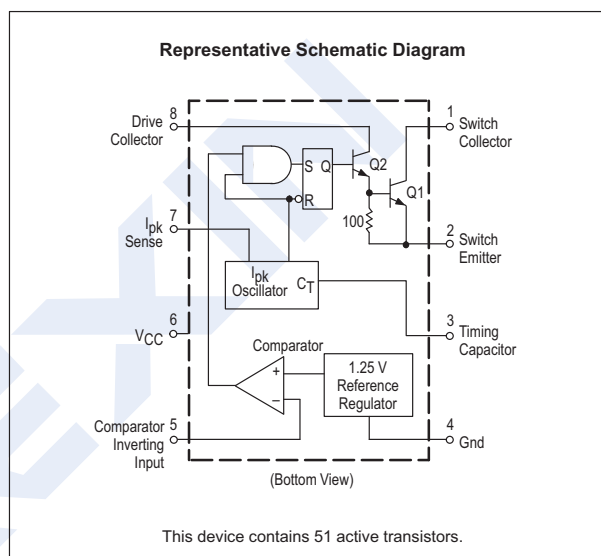
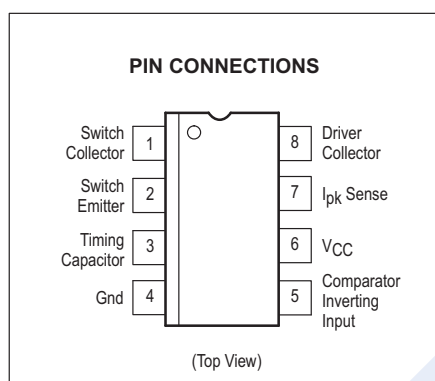
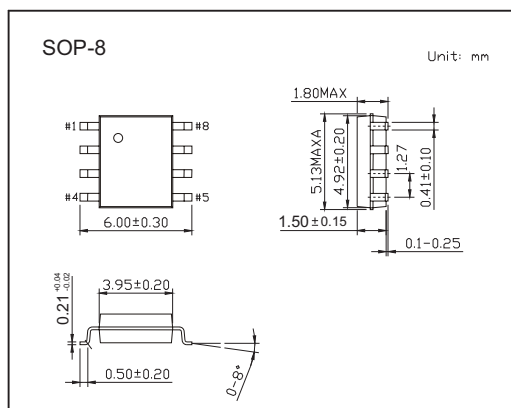


DC-to-DC Converter Control Circuits

KM34064

■ Features

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.2 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference



■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	40	V
Comparator Input Voltage Range	V_{IR}	-0.3 to +40	
Switch Collector Voltage	$V_{C(\text{switch})}$	40	
Switch Emitter Voltage ($V_{Pin\ 1} = 40\text{ V}$)	$V_{E(\text{switch})}$	40	
Switch Collector to Emitter Voltage	$V_{CE(\text{switch})}$	40	
Driver Collector Voltage	$V_{C(\text{driver})}$	40	
Driver Collector Current (Note 1)	$I_{C(\text{driver})}$	100	mA
Switch Current	I_{SW}	1.2	A
SOP8 Package, D Suffix $T_A = 25^\circ\text{C}$	P_D	625	mW
Thermal Resistance	$R_{\theta JA}$	160	$^\circ\text{C/W}$
Operating Junction Temperature	T_J	+150	$^\circ\text{C}$
Operating Ambient Temperature Range	T_A	0 to +70	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to 150	

NOTES: 1. Maximum package power dissipation limits must be observed.

2. ESD data available upon request.

DC-to-DC Converter Control Circuits

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■ ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = T_{\text{low}}$ to T_{high} [Note 3], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency ($V_{\text{Pin } 5} = 0\text{ V}$, $C_T = 1.0\text{ nF}$, $T_A = 25\text{ }^\circ\text{C}$)	f_{osc}	24	33	42	kHz
Charge Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $T_A = 25\text{ }^\circ\text{C}$)	I_{chg}	24	35	42	μA
Discharge Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $T_A = 25\text{ }^\circ\text{C}$)	I_{dischg}	140	220	260	μA
Discharge to Charge Current Ratio (Pin 7 to V_{CC} , $T_A = 25\text{ }^\circ\text{C}$)	$I_{\text{dischg}}/I_{\text{chg}}$	5.2	6.5	7.5	—
Current Limit Sense Voltage ($I_{\text{chg}} = I_{\text{dischg}}$, $T_A = 25\text{ }^\circ\text{C}$)	$V_{\text{ipk(sense)}}$	250	300	350	mV
OUTPUT SWITCH (Note 4)					
Saturation Voltage, Darlington Connection (Note 5) ($I_{\text{SW}} = 1.0\text{ A}$, Pins 1, 8 connected)	$V_{\text{CE(sat)}}$	—	1.0	1.3	V
Saturation Voltage, Darlington Connection ($I_{\text{SW}} = 1.0\text{ A}$, $R_{\text{pin } 8} = 82\text{ }\Omega$ to V_{CC} , Forced $\beta \approx 20$)	$V_{\text{CE(sat)}}$	—	0.45	0.7	V
DC Current Gain ($I_{\text{SW}} = 1.0\text{ A}$, $V_{\text{CE}} = 5.0\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$)	h_{FE}	50	75	—	—
Collector Off-State Current ($V_{\text{CE}} = 40\text{ V}$)	$I_{\text{C(off)}}$	—	0.01	100	μA
COMPARATOR					
Threshold Voltage $T_A = 25\text{ }^\circ\text{C}$ $T_A = T_{\text{low}}$ to T_{high}	V_{th}	1.225 1.21	1.25 —	1.275 1.29	V
Threshold Voltage Line Regulation ($V_{CC} = 3.0\text{ V}$ to 40 V)	Reg_{line}	—	1.4	6.0	mV
Input Bias Current ($V_{\text{in}} = 0\text{ V}$)	I_{IB}	—	−20	−400	nA
TOTAL DEVICE					
Supply Current ($V_{CC} = 5.0\text{ V}$ to 40 V , $C_T = 1.0\text{ nF}$, Pin 7 = V_{CC} , $V_{\text{Pin } 5} > V_{\text{th}}$, Pin 2 = Gnd, remaining pins open)	I_{CC}	—	—	4.0	mA

NOTES: 3. $T_{\text{low}} = 0\text{ }^\circ\text{C}$, $T_{\text{high}} = 70\text{ }^\circ\text{C}$

4. Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
5. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ($\leq 300\text{ mA}$) and high driver currents ($\geq 30\text{ mA}$), it may take up to 2.0 for it to come out of saturation. This condition will shorten the off time at frequencies $\geq 30\text{ kHz}$, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended:

$$\text{Forced } \beta \text{ of output switch: } \frac{\text{IC output}}{\text{IC driver} - 7.0\text{ mA}} \geq 10$$

*The $100\text{ }\Omega$ resistor in the emitter of the driver requires about 7 mA before the output switch conducts.

■ Marking

Marking	34064
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DC-to-DC Converter Control Circuits

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Figure 1. Output Switch On-Off Time versus Oscillator Timing Capacitor

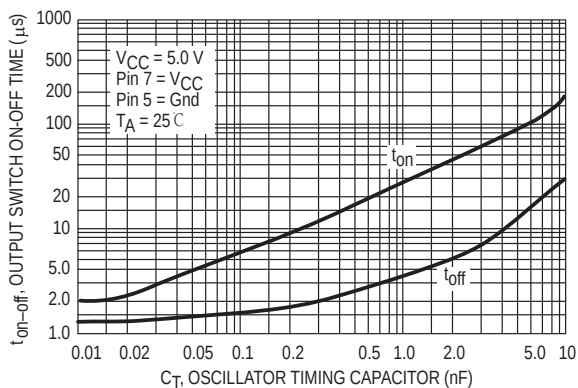


Figure 2. Timing Capacitor Waveform

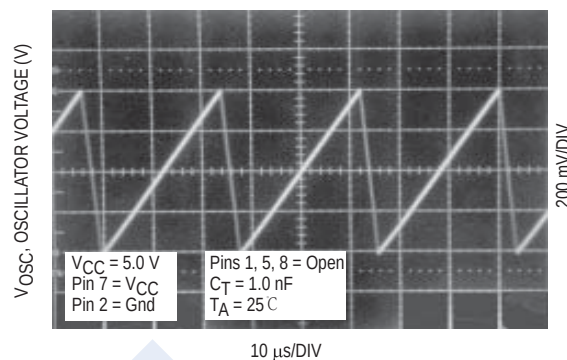


Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

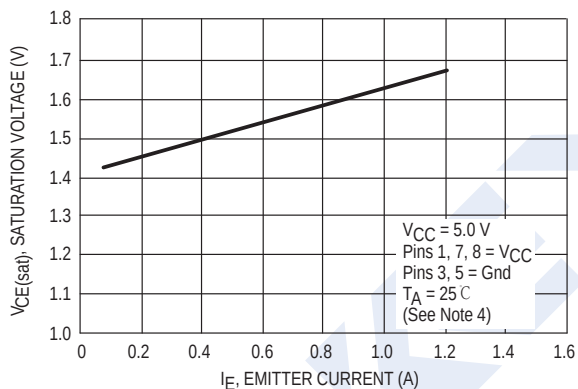


Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

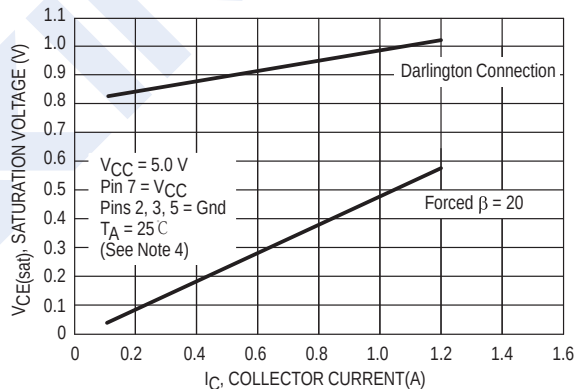


Figure 5. Current Limit Sense Voltage versus Temperature

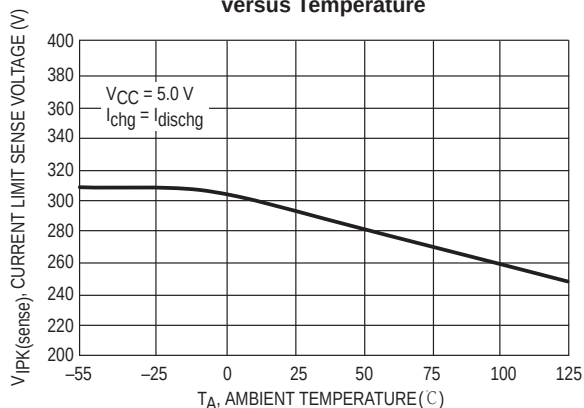
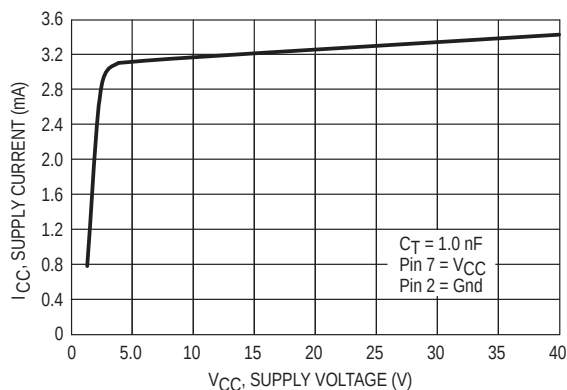


Figure 6. Standby Supply Current versus Supply Voltage

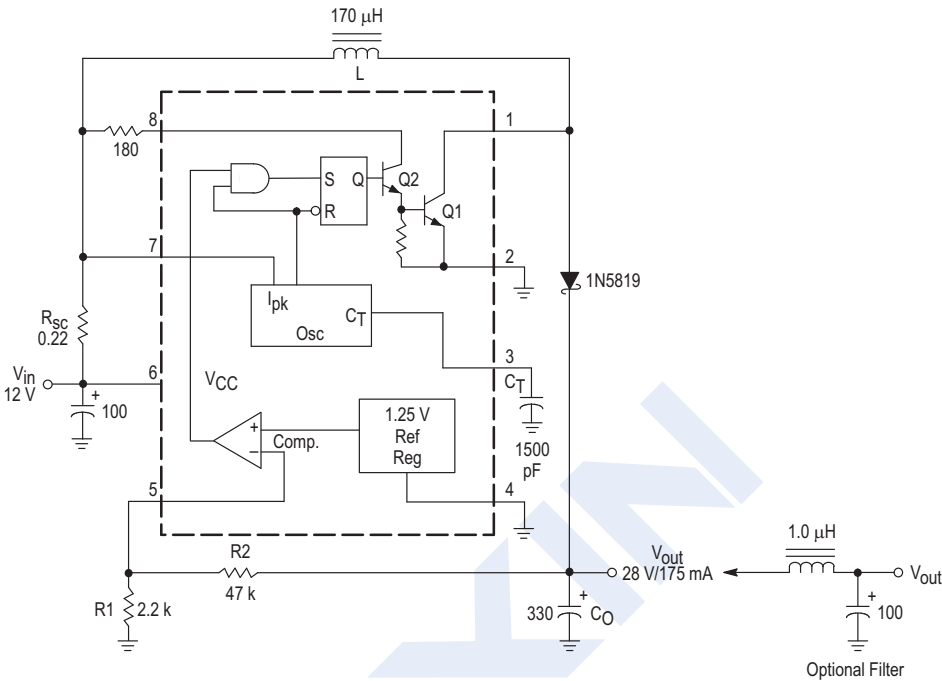


NOTE: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

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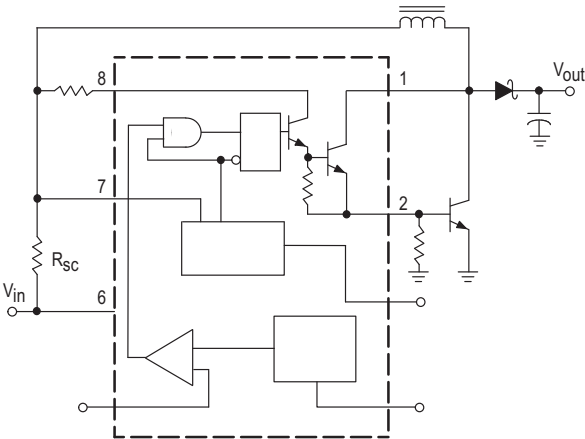
Figure 7. Step-Up Converter



Test	Conditions	Results
Line Regulation	$V_{in} = 8.0 \text{ V to } 16 \text{ V}$, $I_O = 175 \text{ mA}$	$30 \text{ mV} \pm 0.05\%$
Load Regulation	$V_{in} = 12 \text{ V}$, $I_O = 75 \text{ mA to } 175 \text{ mA}$	$10 \text{ mV} \pm 0.017\%$
Output Ripple	$V_{in} = 12 \text{ V}$, $I_O = 175 \text{ mA}$	400 mVpp
Efficiency	$V_{in} = 12 \text{ V}$, $I_O = 175 \text{ mA}$	87.7%
Output Ripple With Optional Filter	$V_{in} = 12 \text{ V}$, $I_O = 175 \text{ mA}$	40 mVpp

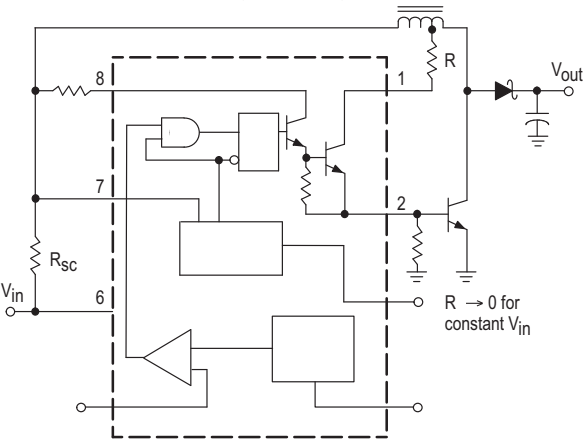
Figure 8. External Current Boost Connections for I_C Peak Greater than 1.2 A

8a. External NPN Switch



8b. External NPN Saturated Switch

(See Note 5)

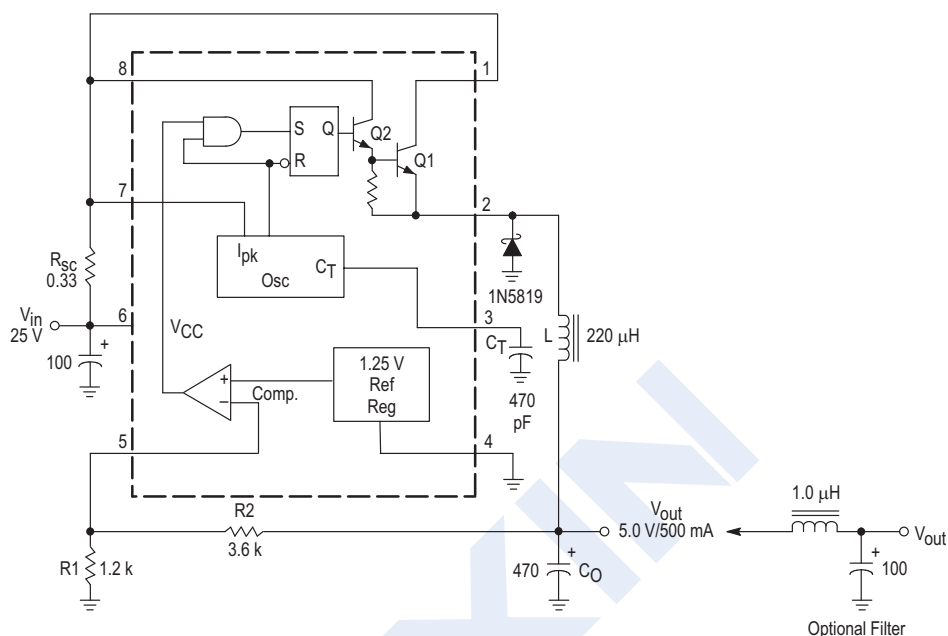


NOTE: 5. If the output switch is driven into hard saturation (non-Darlington configuration) at low switch currents ($\leq 300 \text{ mA}$) and high driver currents ($\geq 30 \text{ mA}$), it may take up to $2.0 \mu\text{s}$ to come out of saturation. This condition will shorten the off time at frequencies $\geq 30 \text{ kHz}$, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non-Darlington configuration is used, the following output drive condition is recommended.

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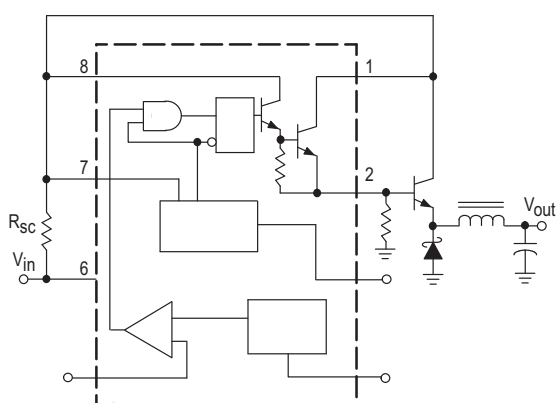
Figure 9. Step-Down Converter



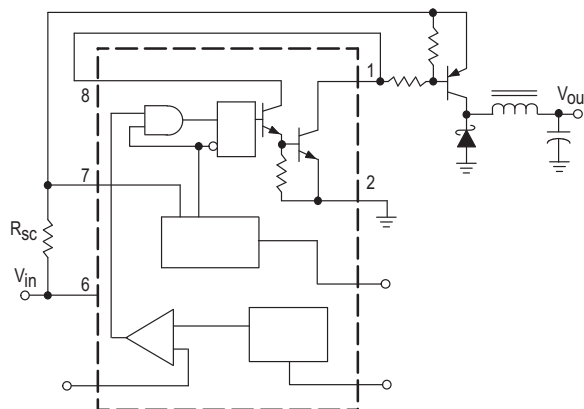
Test	Conditions	Results
Line Regulation	$V_{in} = 15\text{ V to } 25\text{ V}$, $I_O = 500\text{ mA}$	$12\text{ mV} \pm 0.12\%$
Load Regulation	$V_{in} = 25\text{ V}$, $I_O = 50\text{ mA to } 500\text{ mA}$	$3.0\text{ mV} \pm 0.03\%$
Output Ripple	$V_{in} = 25\text{ V}$, $I_O = 500\text{ mA}$	120 mVpp
Short Circuit Current	$V_{in} = 25\text{ V}$, $R_L = 0.1\ \Omega$	1.1 A
Efficiency	$V_{in} = 25\text{ V}$, $I_O = 500\text{ mA}$	83.7%
Output Ripple With Optional Filter	$V_{in} = 25\text{ V}$, $I_O = 500\text{ mA}$	40 mVpp

Figure 10. External Current Boost Connections for I_C Peak Greater than 1.2 A

10a. External NPN Switch

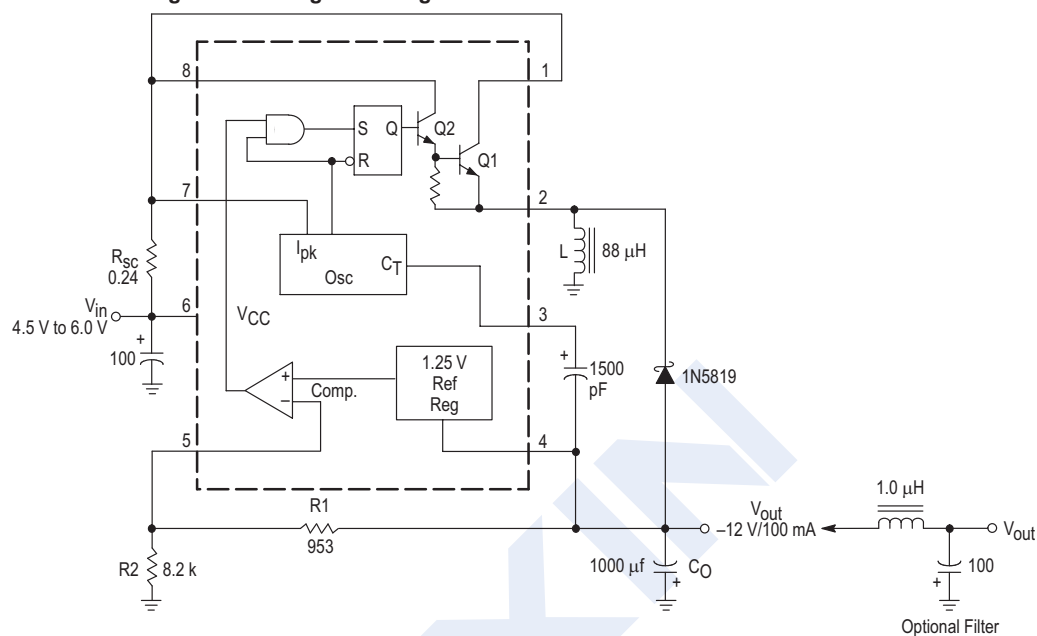


10b. External PNP Saturated Switch



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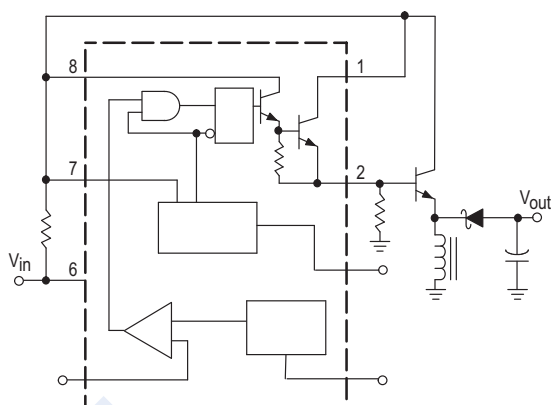
Figure 11. Voltage Inverting Converter



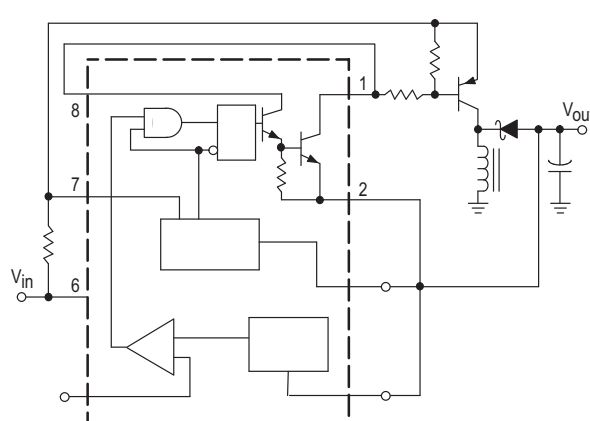
Test	Conditions	Results
Line Regulation	$V_{in} = 4.5 \text{ V to } 6.0 \text{ V}$, $I_O = 100 \text{ mA}$	$3.0 \text{ mV} \pm 0.012\%$
Load Regulation	$V_{in} = 5.0 \text{ V}$, $I_O = 10 \text{ mA to } 100 \text{ mA}$	$0.022 \text{ V} \pm 0.09\%$
Output Ripple	$V_{in} = 5.0 \text{ V}$, $I_O = 100 \text{ mA}$	500 mVpp
Short Circuit Current	$V_{in} = 5.0 \text{ V}$, $R_L = 0.1 \Omega$	910 mA
Efficiency	$V_{in} = 5.0 \text{ V}$, $I_O = 100 \text{ mA}$	62.2%
Output Ripple With Optional Filter	$V_{in} = 5.0 \text{ V}$, $I_O = 100 \text{ mA}$	70 mVpp

Figure 12. External Current Boost Connections for I_C Peak Greater than 1.2 A

12a. External NPN Switch



12b. External PNP Saturated Switch



DC-to-DC Converter Control Circuits

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Figure 13. Design Formula Table

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk}(\text{switch})$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$	$2I_{out(max)}$	$2I_{out(max)} \left(\frac{t_{on}}{t_{off}} + 1 \right)$
R_{sc}	$0.3/I_{pk}(\text{switch})$	$0.3/I_{pk}(\text{switch})$	$0.3/I_{pk}(\text{switch})$
$L(\text{min})$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk}(\text{switch})} \right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk}(\text{switch})} \right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk}(\text{switch})} \right) t_{on(max)}$
C_O	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk}(\text{switch})(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.

V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} - Nominal input voltage.

V_{out} - Desired output voltage, $|V_{out}| = 1.25 \left(1 + \frac{R_2}{R_1} \right)$

I_{out} - Desired output current.

f_{min} - Minimum desired output switching frequency at the selected values of V_{in} and I_O .

$V_{ripple(pp)}$ - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.