MAX3243E 具有 ±15kV IEC ESD 保护功能的 3V 至 5.5V 多通道 RS-232 线路驱动器/接收器

1 特性

- 用于 IBM™ PC/AT™ 串行端口的单芯片和单电源接口
- 为 RS-232 总线引脚提供 ESD 保护
  - ±15kV 人体放电模型 (HBM)
  - ±8kV IEC61000-4-2，接触放电
  - ±15kV IEC61000-4-2，气隙放电
- 符合或超出 TIA/EIA-232-F 和 ITU V.28 标准的要求
- 由 3V 至 5.5V V_{CC} 电源供电
- 始终有效同相接收器输出 (ROUT2B)
- 旨在以高达 500kbit/s 的数据速率传输数据
- 低待机电流：1 µA（典型值）
- 外部电容器：4 × 0.1 µF
- 接受 5V 逻辑输入及 3.3V 电源
- 旨在可与 maxim MAX3243E 互换
- 串行鼠标驱动能力
- 自动断电功能，在没有检测到有效 RS-232 信号时禁用驱动器输出
- 封装选项包括塑料小外形封装 (DW)、紧缩小外形封装 (DB) 和薄型紧缩小外形 (PW) 封装

2 应用

- 电池供电型系统
- 有线网络
- 数据中心和企业级计算
- 电池供电型系统
- 笔记本电脑
- 便携式计算机
- 掌上电脑
- 手持设备

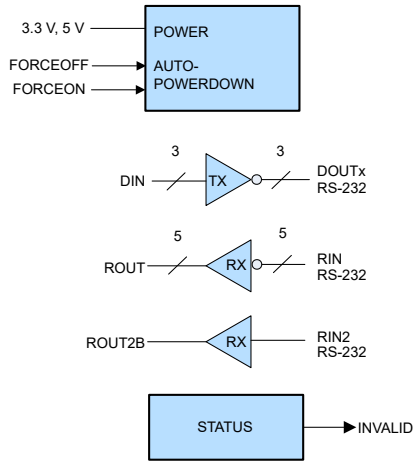
3 说明

MAX3243E 器件由三个线路驱动器、五个线路接收器和一个双电荷泵电路组成，在串行端口连接引脚上具有 ±15kV ESD（HBM 和 IEC61000-4-2，空气间隙放电）和 ±8kV ESD（IEC61000-4-2，接触放电）保护。该器件符合 TIA/EIA-232-F 的要求并在异步通信控制器与串行端口连接器之间提供电气接口。这种驱动器和接收器的组合可满足对在 IBM PC/AT 中使用的典型串行端口的需求或与之兼容。电荷泵和四个小型外部电容器支持由 3V 至 5.5V 单电源供电。另外，该器件包括一个始终有效同相输出 (ROUT2B)，这使得使用振铃指示的应用能够在器件断电的情况下发送数据。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
MAX3243E	SSOP (DB) (28)	10,20 mm × 5,30 mm
	SOIC (DW) (28)	17,90 mm × 7,50 mm
	TSSOP (PW) (28)	9,70mm × 4,40mm
	VQFN (RHB) (32)	5,00mm × 5,00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版电路

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (September 2011) to Revision E (October 2022)	Page
• 添加了*器件信息表*、*ESD 等级*、*ESD 等级 - IEC 规格*、*热性能信息*、*详细说明*、*电源建议*、*布局*、*器件和文档支持*以及*机械、封装和可订购信息*	1
• 删除了“订购信息”表	1
• 在整个数据表中 250kBit/s 至：500kbit/s (在*声明*中)	1
• Changed the I_{CC} Supply current auto-powerdown disabled MAX value from 1 mA to 1.2 mA in the *Electrical Characteristics*	7

Changes from Revision C (February 2009) to Revision D (September 2011)	Page
• Deleted "VALID RIN RS-232 LEVEL" from INPUTS	13
• Deleted "ROUT2B is active" RECEIVER STATUS and combined ROUT outputs	13
• Added table "Outputs ROUT2B and $\overline{\text{INVALID}}$" defining truth for ROUT2B and INVALID outputs.	13

5 说明 (续)

该器件以高达 250kbit/s 的数据信号传输速率运行，驱动器输出压摆率最高为 30V/μs。

MAX3243EC 器件的额定工作温度范围为 0°C 至 70°C。MAX3243EI 器件的额定工作温度范围为 –40°C 至 85°C。

6 Pin Configuration and Functions

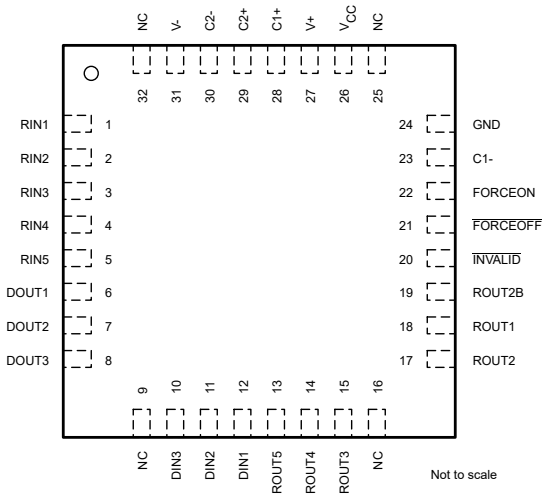


图 6-1. RHB Package, 32 Pin (VQFN), Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	RIN1	I	RS-232 receiver inputs
2	RIN2		
3	RIN3		
4	RIN4		
5	RIN5		
6	DOUT1	O	RS-232 driver outputs
7	DOUT2		
8	DOUT3		
9	NC	—	Not connected internally
10	DIN3	I	Driver inputs
11	DIN2		
12	DIN1		
13	ROUT5	O	Receiver outputs
14	ROUT4		
15	ROUT3		
16	NC	—	Not connected internally
17	ROUT2	O	Receiver outputs
18	ROUT1		
19	ROUT2B	O	Always-active noninverting receiver output
20	$\overline{\text{INVALID}}$	O	Invalid Output Pin
21	$\overline{\text{FORCEOFF}}$	I	Auto Powerdown Control input (Refer to Truth Table)
22	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
23	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
24	GND	—	Ground
25	NC	—	Not connected internally
26	V_{CC}	—	3-V to 5.5-V supply voltage

表 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminals of the voltage-doubler charge-pump capacitors
29	C2+	—	
30	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
31	V-	—	Negative charge pump output voltage
32	NC	—	Not connected internally

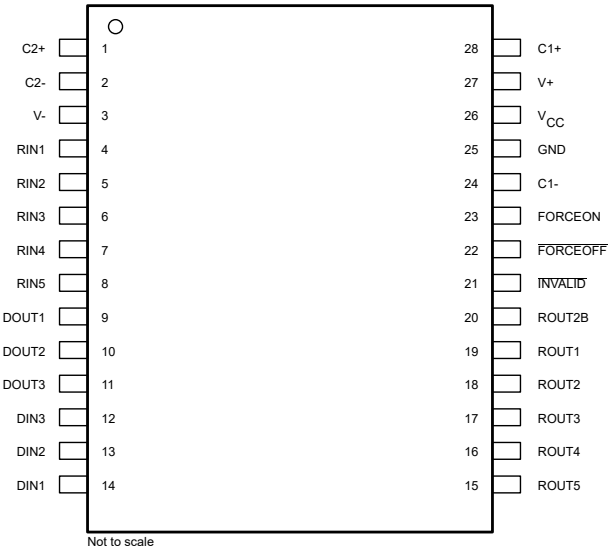


图 6-2. DB, DW, or PW Package, 28 Pin (SSOP, SOIC, TSSOP), Top View

表 6-2. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the voltage-doubler charge-pump capacitor
2	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
3	V-		Negative charge pump output voltage
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active noninverting receiver output;
21	$\overline{\text{INVALID}}$	O	Invalid Output Pin
22	$\overline{\text{FORCEOFF}}$	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
25	GND	—	Ground
26	V_{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.3	6	V
V+	Positive output supply voltage range(2)		–0.3	7	V
V–	Negative output supply voltage range(2)		0.3	–7	V
V+ – V–	Output supply voltage difference(2)			13	V
V_I	Input voltage range	Driver ($\overline{FORCEOFF}$, FORCEON)	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage range	Driver	–13.2	13.2	V
		Receiver ($\overline{INVALID}$)	–0.3	V_{CC} + 0.3	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 DOUT1/2/3, RIN1/2/3/4/5 pins(1)	±15,000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge (1)	RIN1, RIN2, RIN3, RIN4, RIN5, DOUT1, DOUT2 and DOUT3 pins	±8,000	V
		IEC 61000-4-2 Air-gap Discharge (1)		±15,000	

(1) For DB, PW and RHB package only: A minimum of 1-µF capacitor between V_{CC} and GND is required to meet the specified IEC 61000-4-2 rating.

7.4 Recommended Operating Conditions

See 图 10-1 (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{FORCEOFF}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature		MAX3243EC	0		70	°C
			MAX3243EI	–40		85	

(1) Test conditions are C1 – C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2 – C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

7.5 Thermal Information

THERMAL METRIC[1]		{DB} (SSOP) 28 PINS	{DW} (SOIC) 28 PINS	{PW} (TSSOP) 28 PINS	{RHB} (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.1	59.0	70.3	34.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	28.8	21.0	25.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	30.3	29.2	14.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	7.8	1.3	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.0	30.0	28.8	14.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	5.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] (see 图 10-1)

PARAMETER			TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
I_I	Input leakage current	$\overline{FORCEOFF}$, FORCEON			±0.01	±1	μA
I_{CC}	Supply current (T_A = 25°C)	Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC} For DB, PW and RHB package		0.3	1.2	mA
		Auto-powerdown disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC} For DW package		0.3	1	mA
		Powered off	No load, $\overline{FORCEOFF}$ at GND		1	10	μA
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded, All DIN are grounded		1	10	

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

7.7 Driver Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 图 10-1)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND			5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND			–5	–5.4		V
V_O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC}, 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA			±5			V
I_{IH}	High-level input current	$V_I = V_{CC}$				±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND				±0.01	±1	μA
V_{hys}	Input hysteresis						±1	V
I_{OS}	Short-circuit output current(3)	V_{CC} = 3.6 V,	V_O = 0 V				±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V					
r_o	Output resistance	V_{CC}, V+, and V– = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND,	V_O = ±12 V,	V_{CC} = 0 to 5.5 V			±25	μA

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

7.8 Receiver, Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 图 10-1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OH} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})			0.5		V
I_{off}	Output leakage current (except ROUT2B)	$\overline{FORCEOFF}$ = 0 V		±0.05	±10	μA
r_i	Input resistance	V_I = ±3 V or ±25 V	3	5	7	kΩ

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

7.9 Auto-Powerdown Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 8-5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{IT-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = -1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		0.4	V

7.10 Driver Switching Characteristics

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 图 10-1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	C_L = 1000 pF, One DOUT switching,	R_L = 3 kΩ See 图 8-1	250	500		kbit/s
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ, See 图 8-2		100		ns
SR(tr)	Slew rate, transition region (see 图 8-1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ, PRR = 250 kbit/s	C_L = 150 pF to 1000 pF	6		30	V/μs
			C_L = 150 pF to 2500 pF	4		30	

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V + 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

7.11 Receiver Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	TYP(2)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 图 8-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output		150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 图 8-4	200	ns
t_{dis}	Output disable time		200	ns
$t_{sk(p)}$	Puse skew(3)	See 图 8-3	50	ns

(1) Test conditions are C1 – C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 – C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

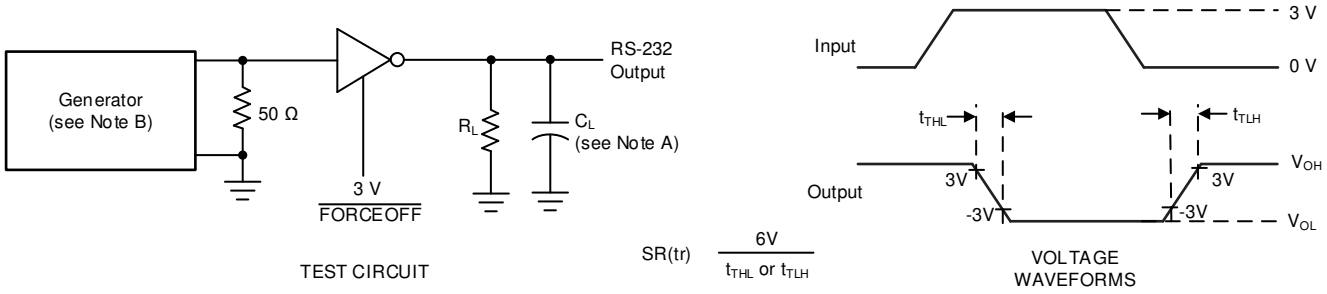
7.12 Auto-Powerdown Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 图 8-5)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	V_{CC} = 5 V	1	μs
$t_{invalid}$	Propagation delay time, high- to low-level output	V_{CC} = 5 V	30	μs
t_{en}	Supply enable time	V_{CC} = 5 V	100	μs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

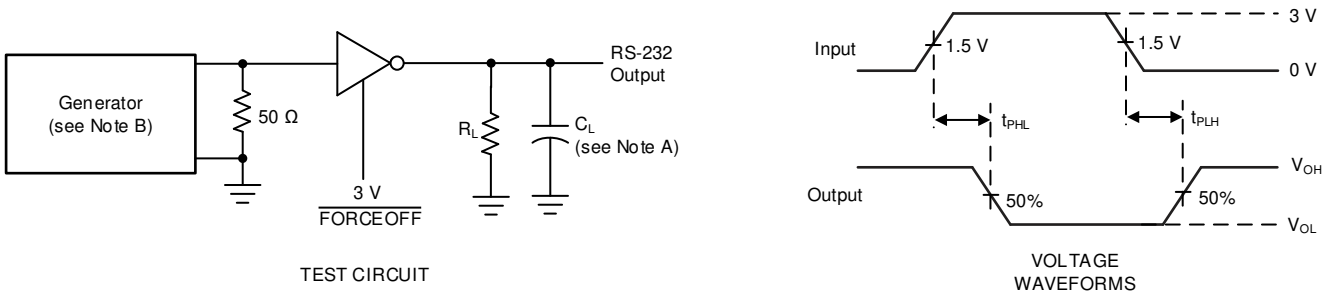
8 Parameter Measurement Information



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns.

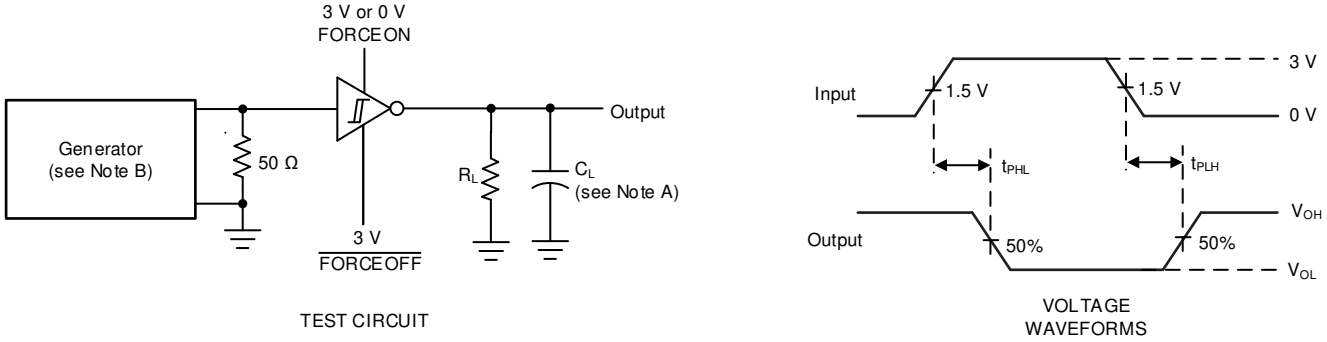
图 8-1. Driver Slew Rate



A. C_L includes probe and jig capacitance

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns.

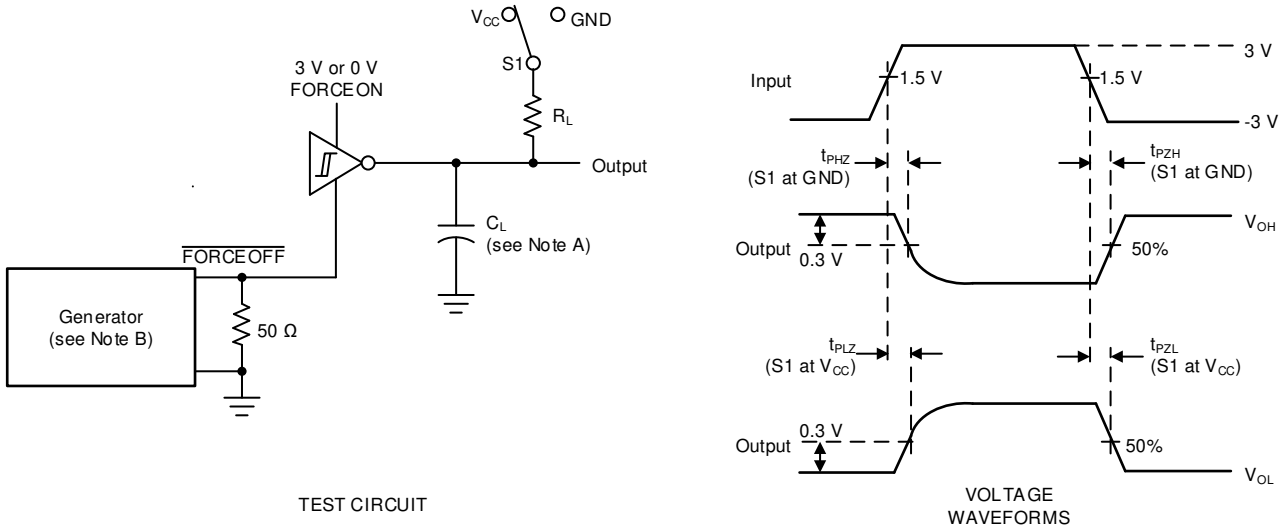
图 8-2. Driver Pulse Skew



A. C_L includes probe and jig capacitance

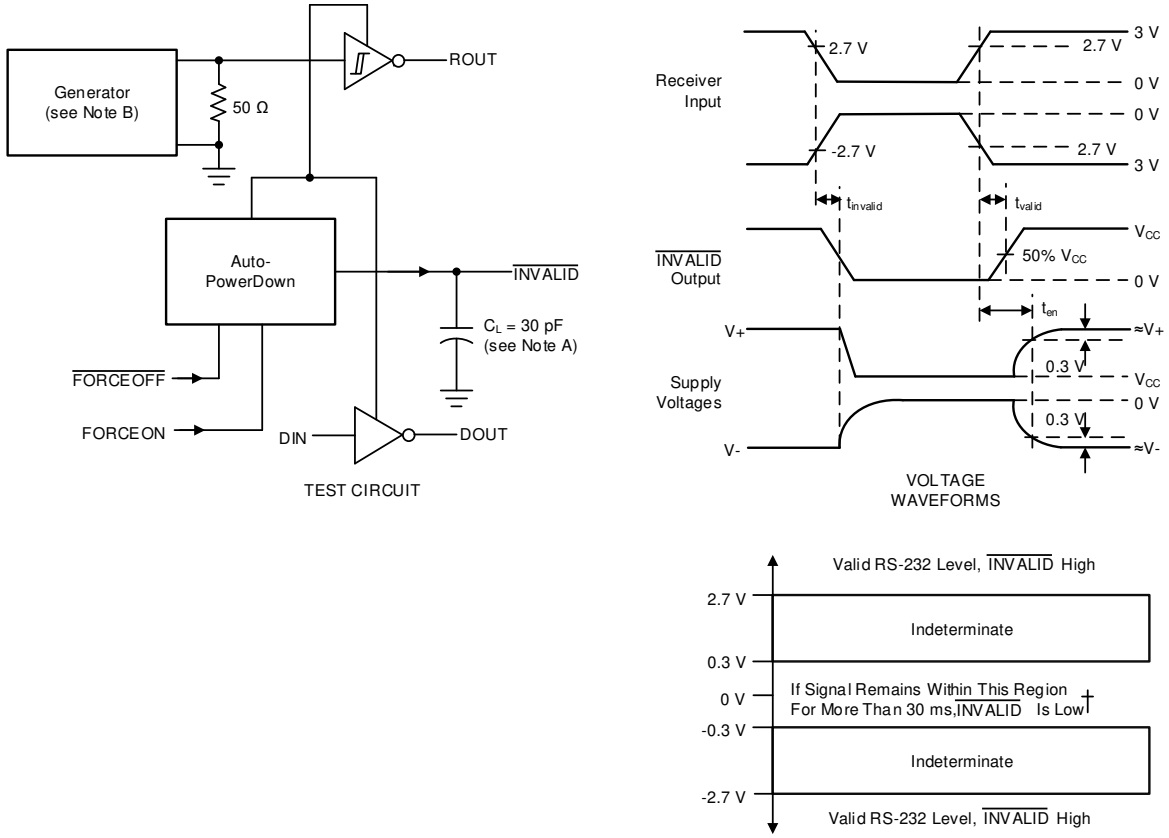
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns.

图 8-3. Receiver Propagation Delay Times



A. C_L includes probe and jig capacitance
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

图 8-4. Receiver Enable and Disable Times



A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50 % duty cycle, $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns.

图 8-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

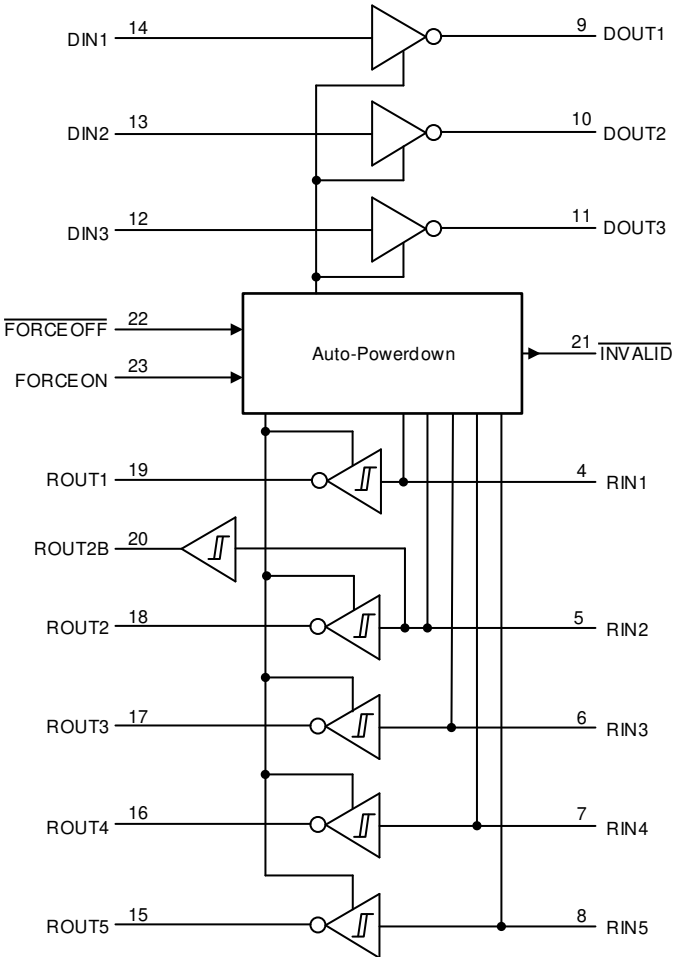
9 Detailed Description

9.1 Overview

The MAX3243E device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ±8-kV ESD (IEC61000-4-2, Contact Discharge) protection on serial-port connection pins. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector.

The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/μs driver output slew rate.

9.2 Functional Block Diagram



9.3 Feature Description

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If $\overline{\text{FORCEOFF}}$ is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high, and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V or has been between –0.3 V and 0.3 V for less than 30 μs. $\overline{\text{INVALID}}$ is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 μs. Refer to Figure 8-5 for receiver input levels.

9.4 Device Functional Modes

Figure 9-1 through 9-3 show the device functional modes.

表 9-1. Each Driver

INPUTS(1)				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
X	L	H	No	Z	Powered off by auto-powerdown feature

表 9-2. Each Receiver

INPUTS(1)			OUTPUT	RECEIVER STATUS
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation with auto-powerdown disabled/enabled
H	X	H	L	
Open	X	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

表 9-3. Outputs ROUT2B and $\overline{\text{INVALID}}$

INPUTS(1)				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{INVALID}}$	ROUT2B	
Yes	L	X	X	H	L	Always active
Yes	H	X	X	H	H	
Yes	Open	X	X	H	L	
No	Open	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

10 Application and Implementation

备注

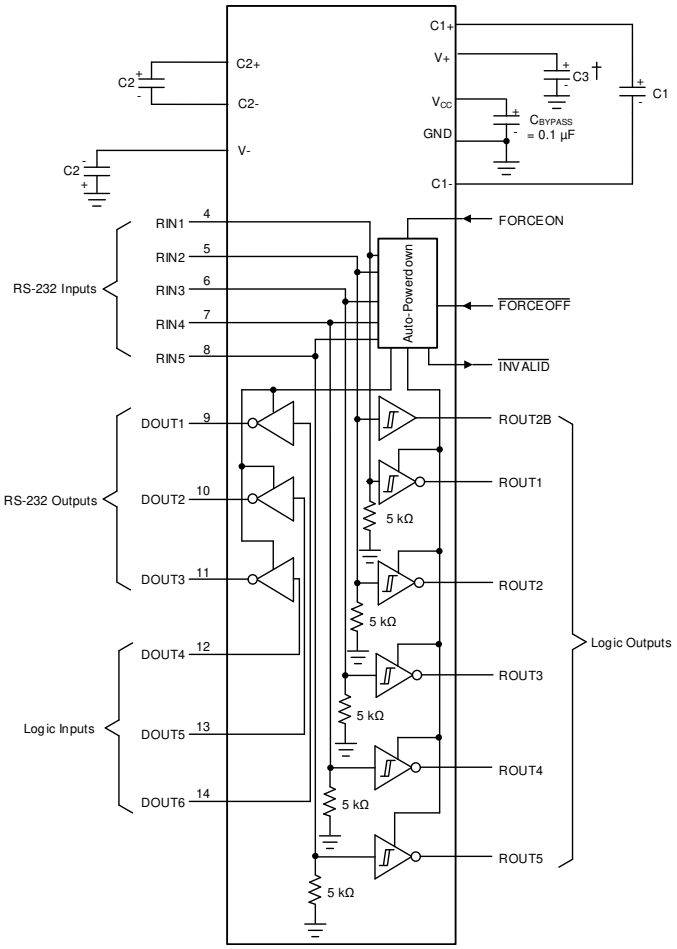
以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

For proper operation, add capacitors as shown in 图 10-1. Pins 12 through 23 connect to UART or general purpose logic lines. RS-232 lines on Pins 4 through 11 connect to a connector or cable.

10.2 Typical Application

Three driver and five receiver channels are supported for full duplex transmission with hardware flow control. The five 5-kΩ resistors are internal to the MAX3243E.



† C3 can be connected to V_{CC} or GND

A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

图 10-1. Typical Operating Circuit and Capacitor Values

10.2.1 Design Requirements

For this design example, use the values in 表 10-1.

- V_{CC} minimum is 3 V and maximum is 5.5 V.
- Maximum recommended bit rate is 250 kbps.

表 10-1. V_{CC} vs Capacitor Values

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

10.2.2 Detailed Design Procedure

MAX3243E has integrated charge-pump that generates positive and negative rails needed for RS-232 signal levels. Main design requirement is that charge-pump capacitor terminals must be connected with recommended capacitor values. Charge-pump rail voltages and device supply pin must be properly bypassed with ceramic capacitors.

10.2.2.1 ESD Protection

TI MAX3243E devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15-kV in all states: normal operation, shutdown, and powered down. The MAX3243E devices are designed to continue functioning properly after an ESD occurrence without any latchup.

The MAX3243E devices have three specified ESD limits on the driver outputs and receiver inputs, with respect to GND:

- ±15-kV Human Body Model (HBM)
- ±15-kV IEC61000-4-2, Air-Gap Discharge (formerly IEC1000-4-2)
- ±8-kV IEC61000-4-2, Contact Discharge

10.2.2.1.1 ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

10.2.2.1.2 Human Body Model (HBM)

The Human Body Model of ESD testing is shown in 图 10-2, while 图 10-3 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5k-Ω resistor.

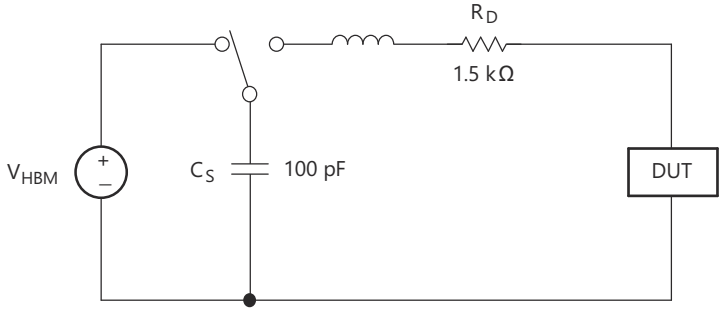


图 10-2. HBM ESD Test Circuit

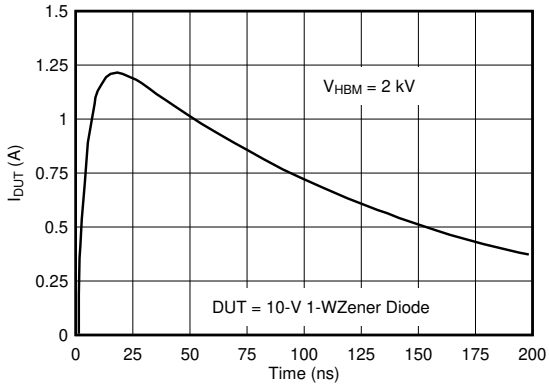


图 10-3. Typical HBM Current Waveform

10.2.2.1.3 IEC61000-4-2 (Formerly Known as IEC1000-4-2)

Unlike the HBM, MM, and CDM, ESD tests that apply to component level integrated circuits, the IEC61000-4-2 is a system-level ESD testing and performance standard that pertains to the end equipment. The MAX3243E device is designed to enable the manufacturer in meeting the highest level (Level 4) of IEC61000-4-2 ESD protection with no further need of external ESD protection circuitry. The more stringent IEC test standard has a higher peak current than the HBM, due to the lower series resistance in the IEC model.

图 10-4 shows the IEC61000-4-2 model, and 图 10-5 shows the current waveform for the corresponding ±8-kV Contact-Discharge (Level 4) test. This waveform is applied to a probe that has been connected to the DUT. On the other hand, the corresponding ±15-kV (Level 4) Air-Gap Discharge test involves approaching the DUT with an already energized probe.

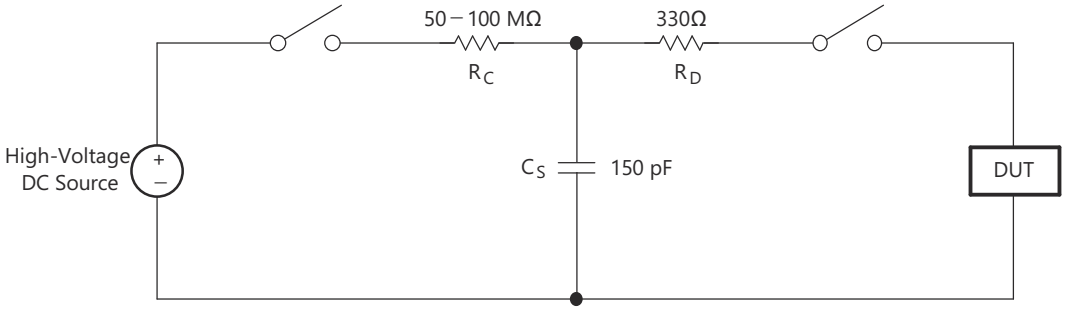


图 10-4. Simplified IEC61000-4-2 ESD Test Circuit

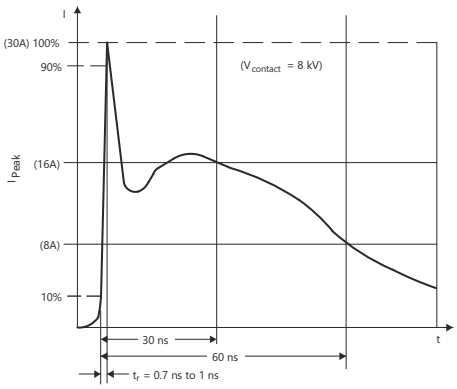


图 10-5. Typical Current Waveform of IEC61000-4-2 ESD Generator

10.2.2.1.4 Machine Model

The Machine Model (MM) ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test is no longer as pertinent to the RS-232 pins.

10.3 Power Supply Recommendations

The V_{CC} voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins. V_{CC} must be between 3 V and 5.5 V.

10.4 Layout

As shown in Layout Example, charge-pump and supply voltage capacitors must be located very close to device pins. Non-polarized ceramic capacitors are recommended. If polarized tantalum or electrolytic capacitors are used, they should be connected as per Typical Operating Circuit and Capacitor Values.

10.4.1 Layout Example

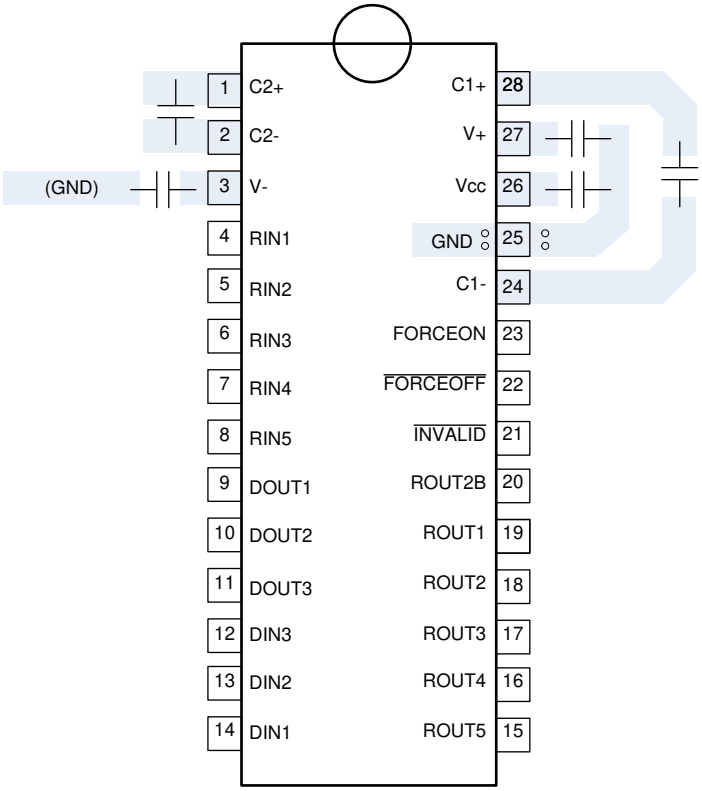


图 10-6. Example Layout

Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.3 Trademarks

IBM™ and PC/AT™ are trademarks of International Business Machines Corporation.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3243ECDB	LIFEBUY	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243EC	
MAX3243ECDBG4	LIFEBUY	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243EC	
MAX3243ECDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243EC	Samples
MAX3243ECDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243EC	Samples
MAX3243ECDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3243EC	Samples
MAX3243ECPW	LIFEBUY	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP243EC	
MAX3243ECPWE4	LIFEBUY	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP243EC	
MAX3243ECPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP243EC	Samples
MAX3243ECPWRG4	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP243EC	Samples
MAX3243ECRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	MP243E	Samples
MAX3243EIDB	LIFEBUY	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI	
MAX3243EIDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI	Samples
MAX3243EIDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI	Samples
MAX3243EIDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI	Samples
MAX3243EIDWRG4	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3243EI	Samples
MAX3243EIPW	LIFEBUY	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP243EI	
MAX3243EIPWE4	LIFEBUY	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP243EI	
MAX3243EIPWG4	LIFEBUY	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP243EI	
MAX3243EIPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP243EI	Samples
MAX3243EIPWRE4	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP243EI	Samples
MAX3243EIPWRG4	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP243EI	Samples
MAX3243EIRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MR243E	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3243EIRHBRG4	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MR243E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

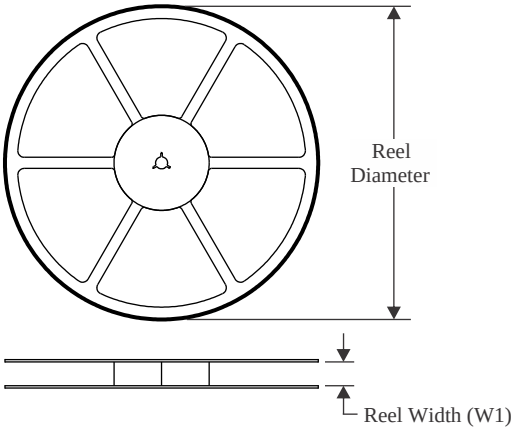
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

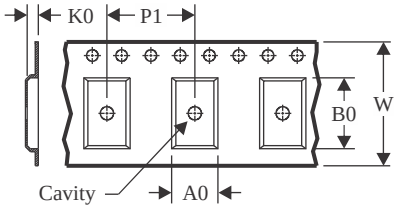
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

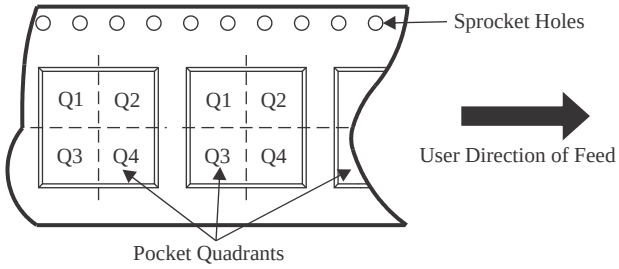


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

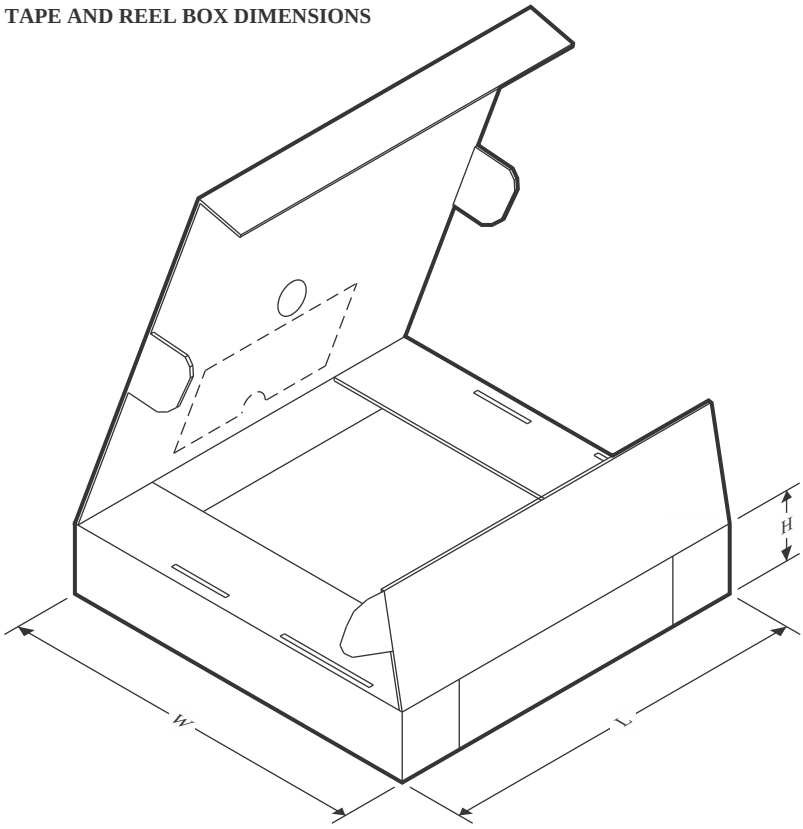
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3243ECDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MAX3243ECDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX3243ECPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MAX3243ECRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
MAX3243EIDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MAX3243EIDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MAX3243EIPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MAX3243EIRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

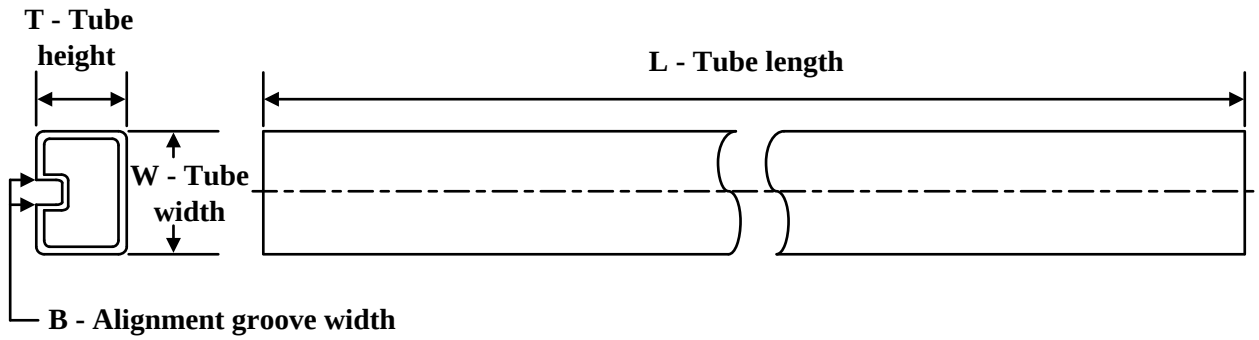
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3243ECDBR	SSOP	DB	28	2000	356.0	356.0	35.0
MAX3243ECDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MAX3243ECPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
MAX3243ECRHBR	VQFN	RHB	32	3000	356.0	356.0	35.0
MAX3243EIDBR	SSOP	DB	28	2000	356.0	356.0	35.0
MAX3243EIDWR	SOIC	DW	28	1000	350.0	350.0	66.0
MAX3243EIPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
MAX3243EIRHBR	VQFN	RHB	32	3000	356.0	356.0	35.0

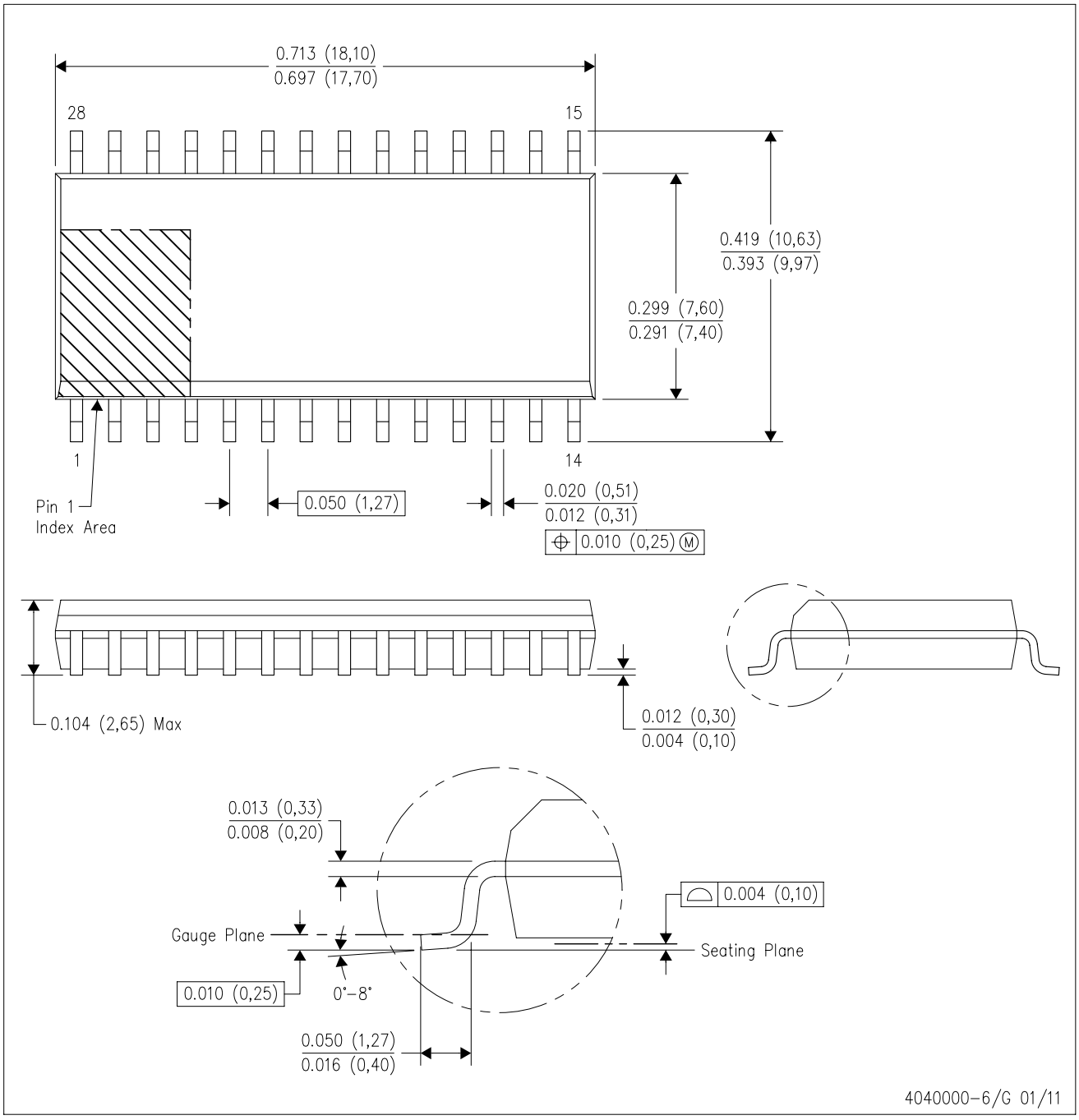
TUBE



*All dimensions are nominal

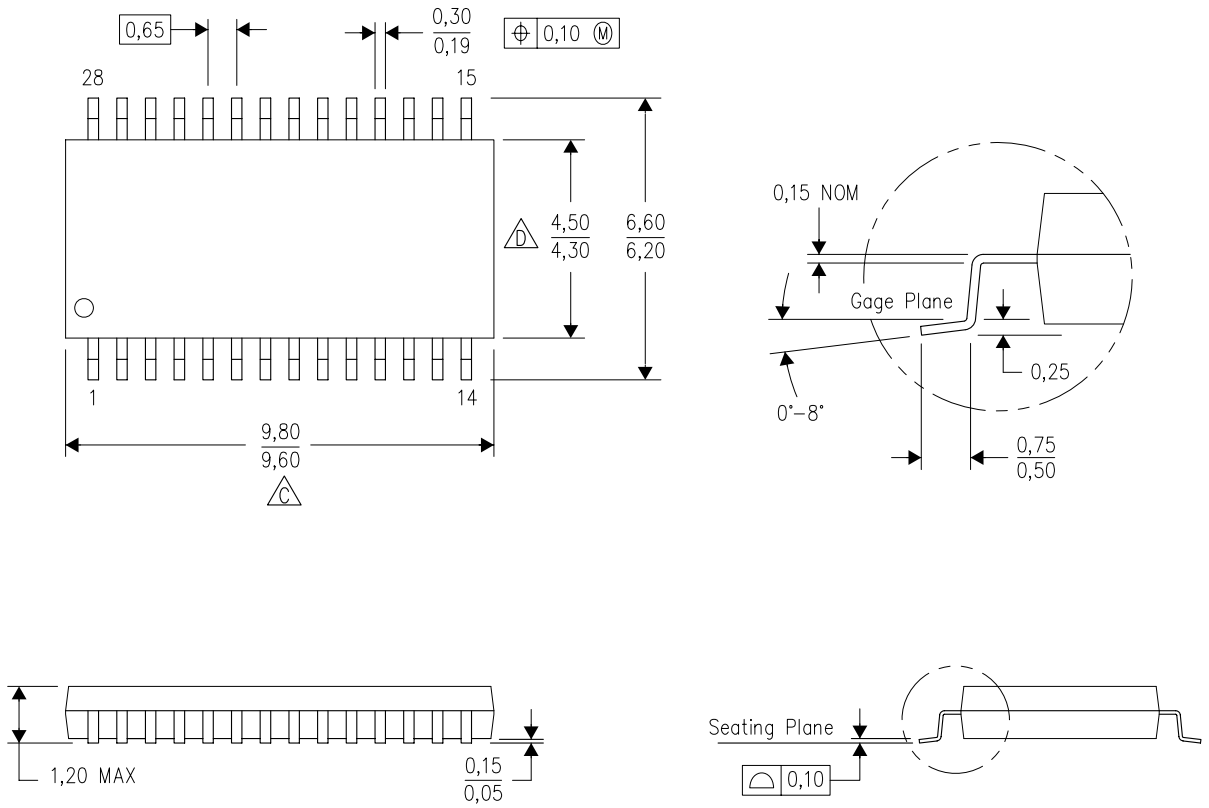
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MAX3243ECDB	DB	SSOP	28	50	530	10.5	4000	4.1
MAX3243ECDBG4	DB	SSOP	28	50	530	10.5	4000	4.1
MAX3243ECDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
MAX3243ECPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243ECPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243ECPWE4	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243ECPWE4	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243EIDB	DB	SSOP	28	50	530	10.5	4000	4.1
MAX3243EIDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
MAX3243EIPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243EIPW	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243EIPWE4	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243EIPWE4	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243EIPWG4	PW	TSSOP	28	50	530	10.2	3600	3.5
MAX3243EIPWG4	PW	TSSOP	28	50	530	10.2	3600	3.5

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

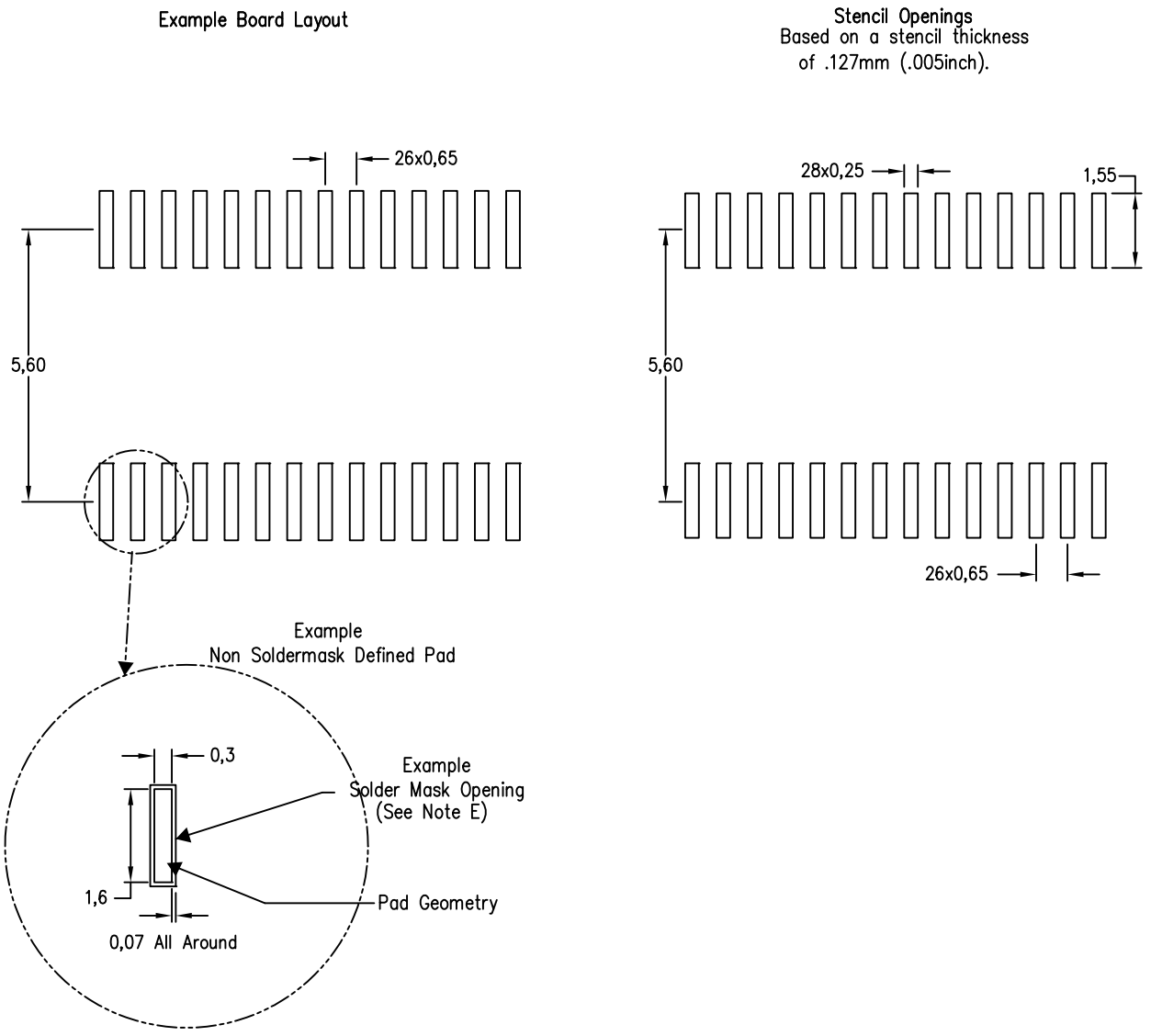
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



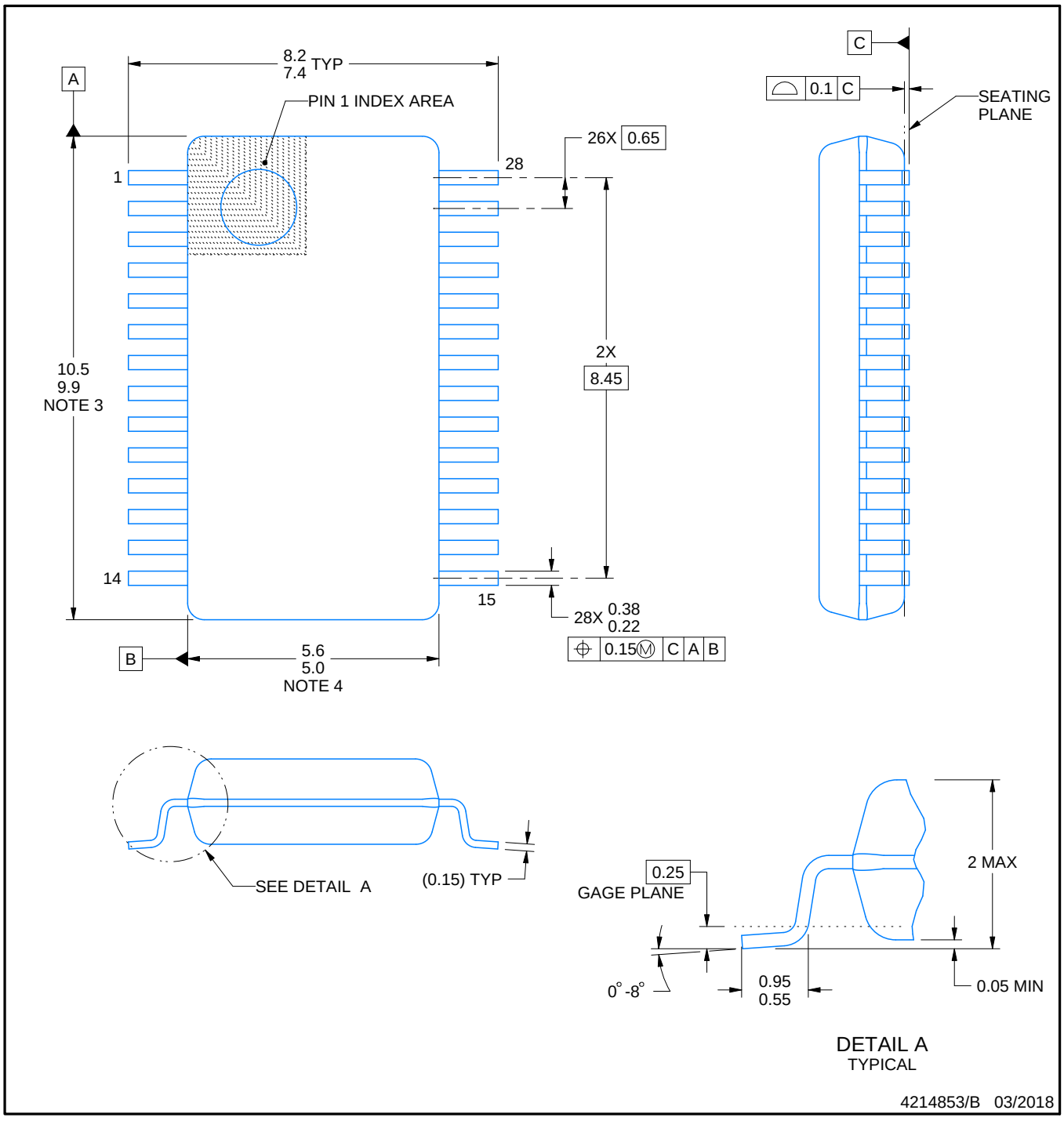
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DB0028A

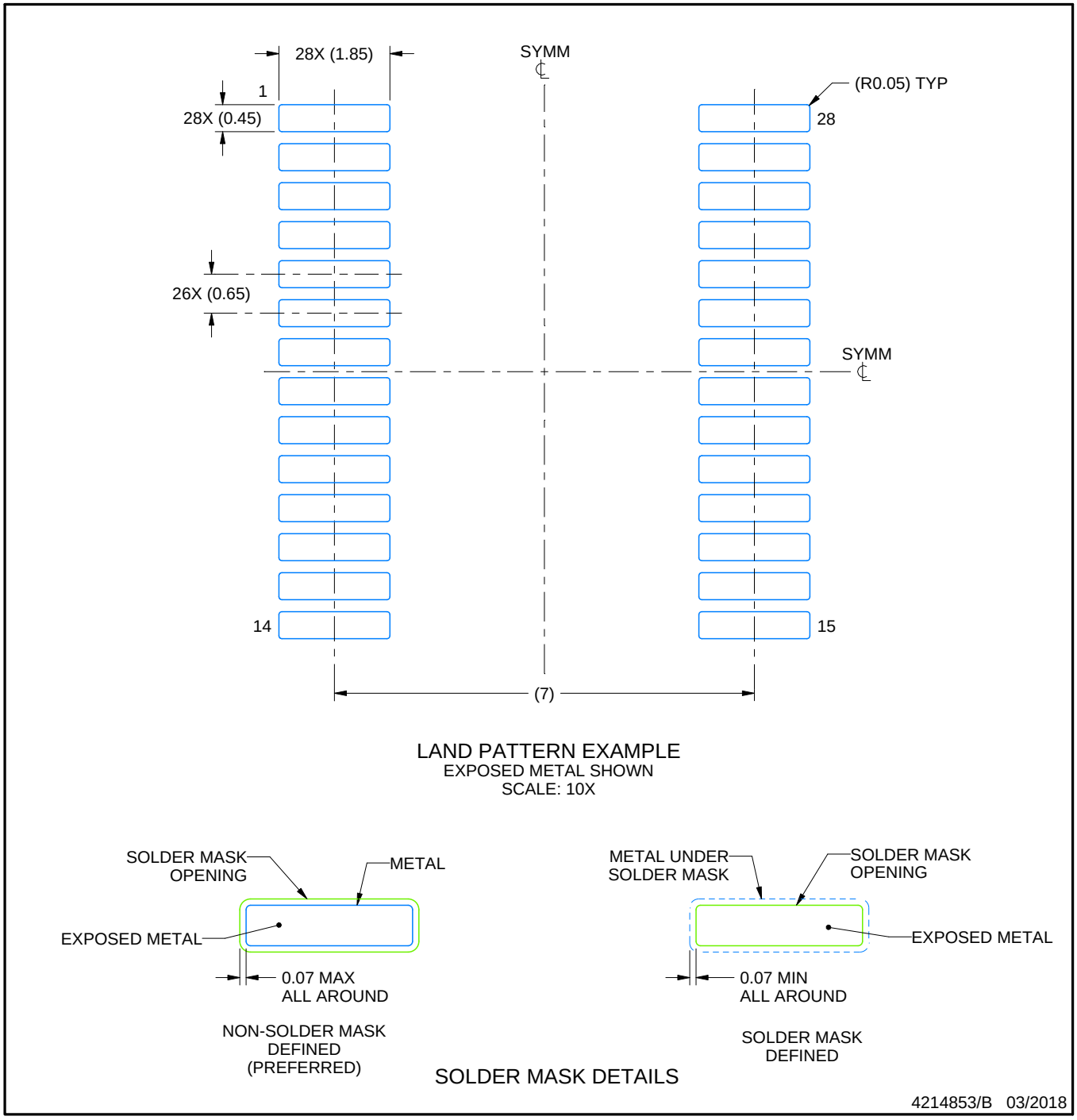
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



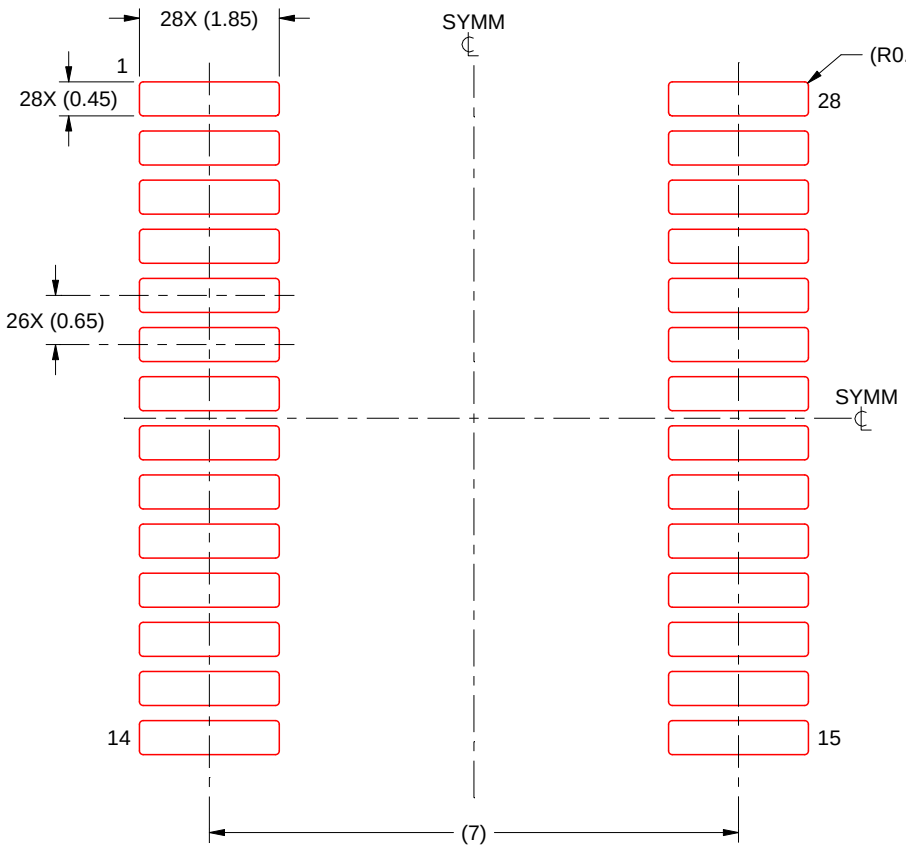
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

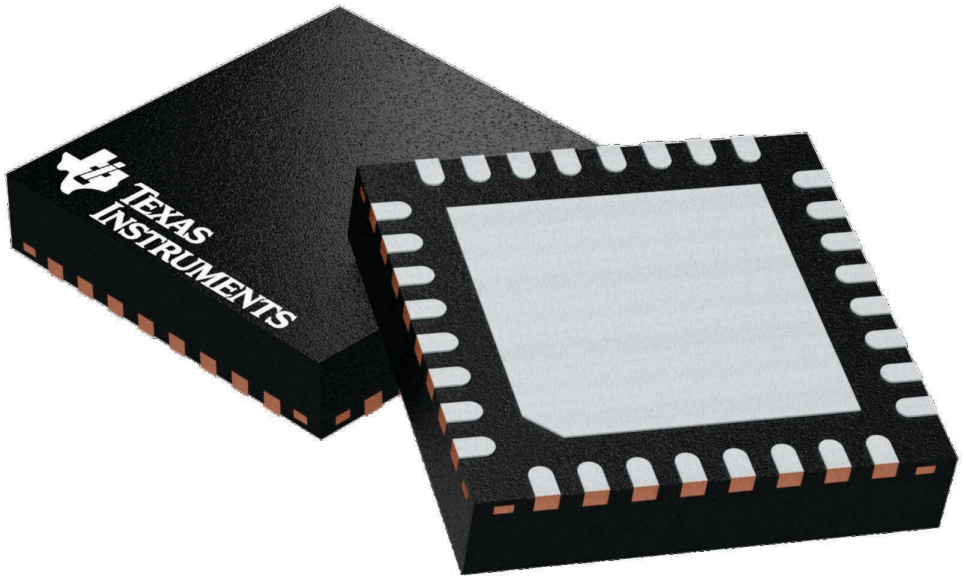
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

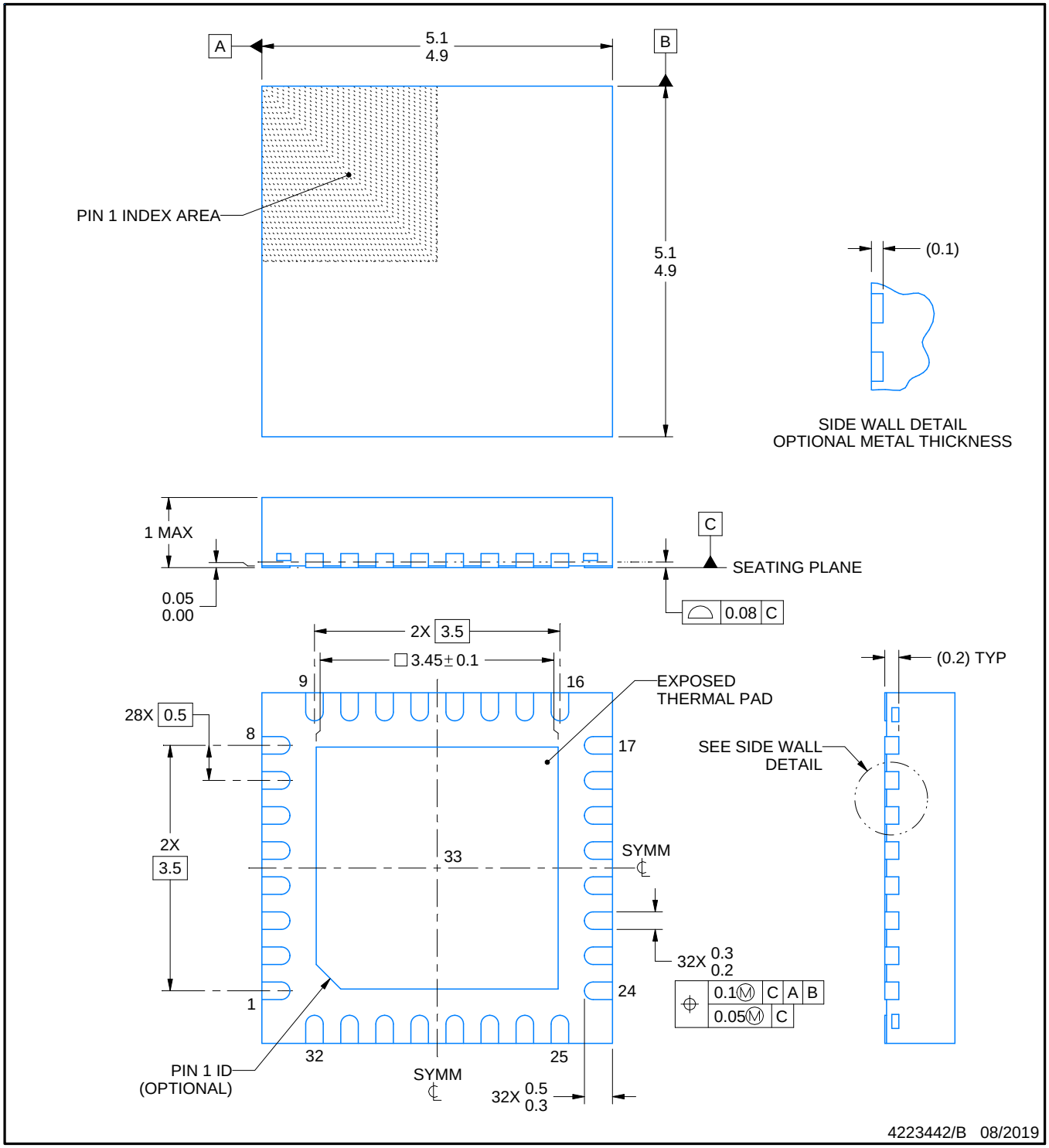
4224745/A

RHB0032E

PACKAGE OUTLINE

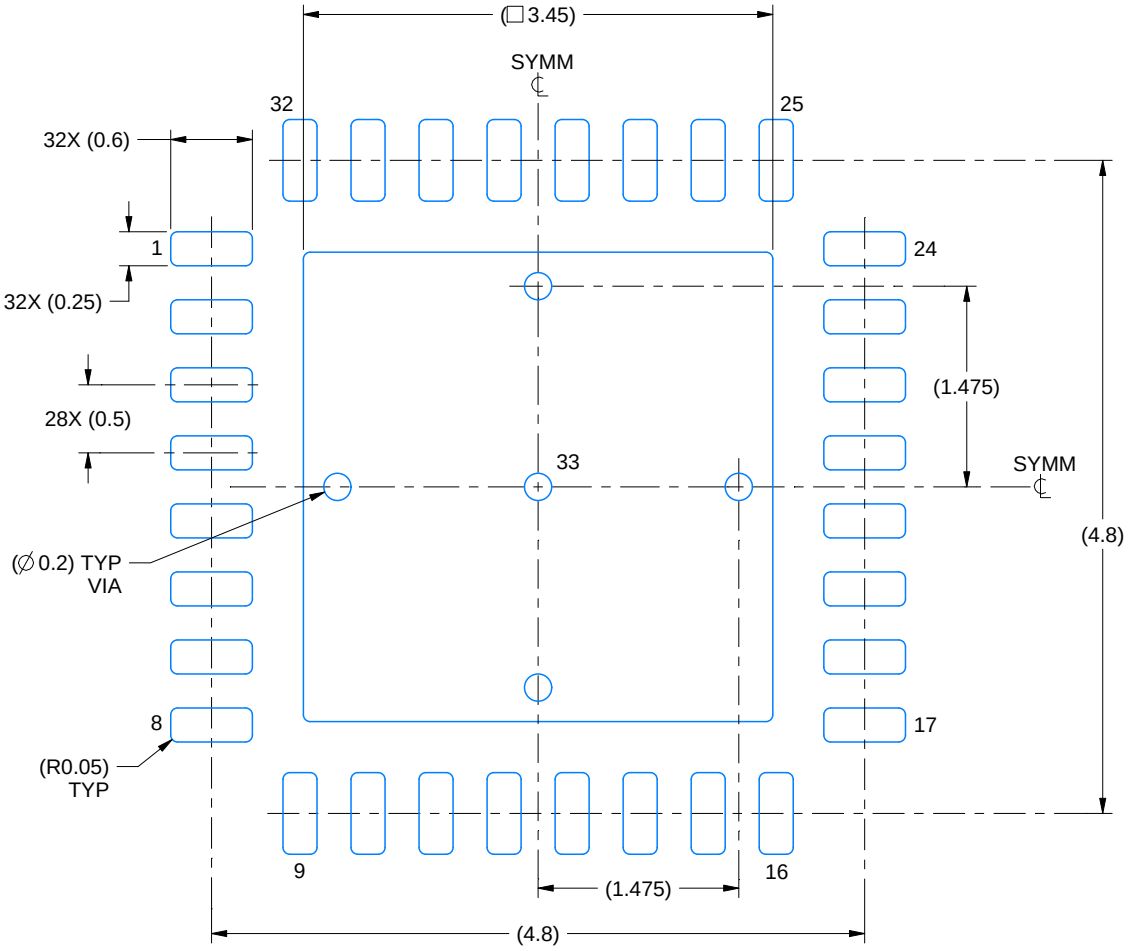
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

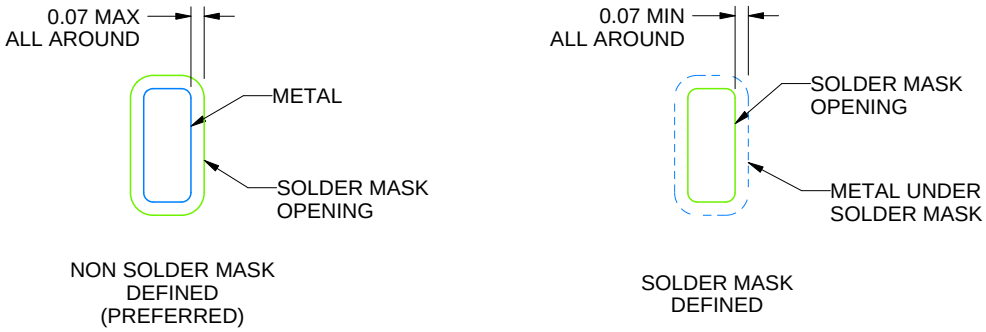


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

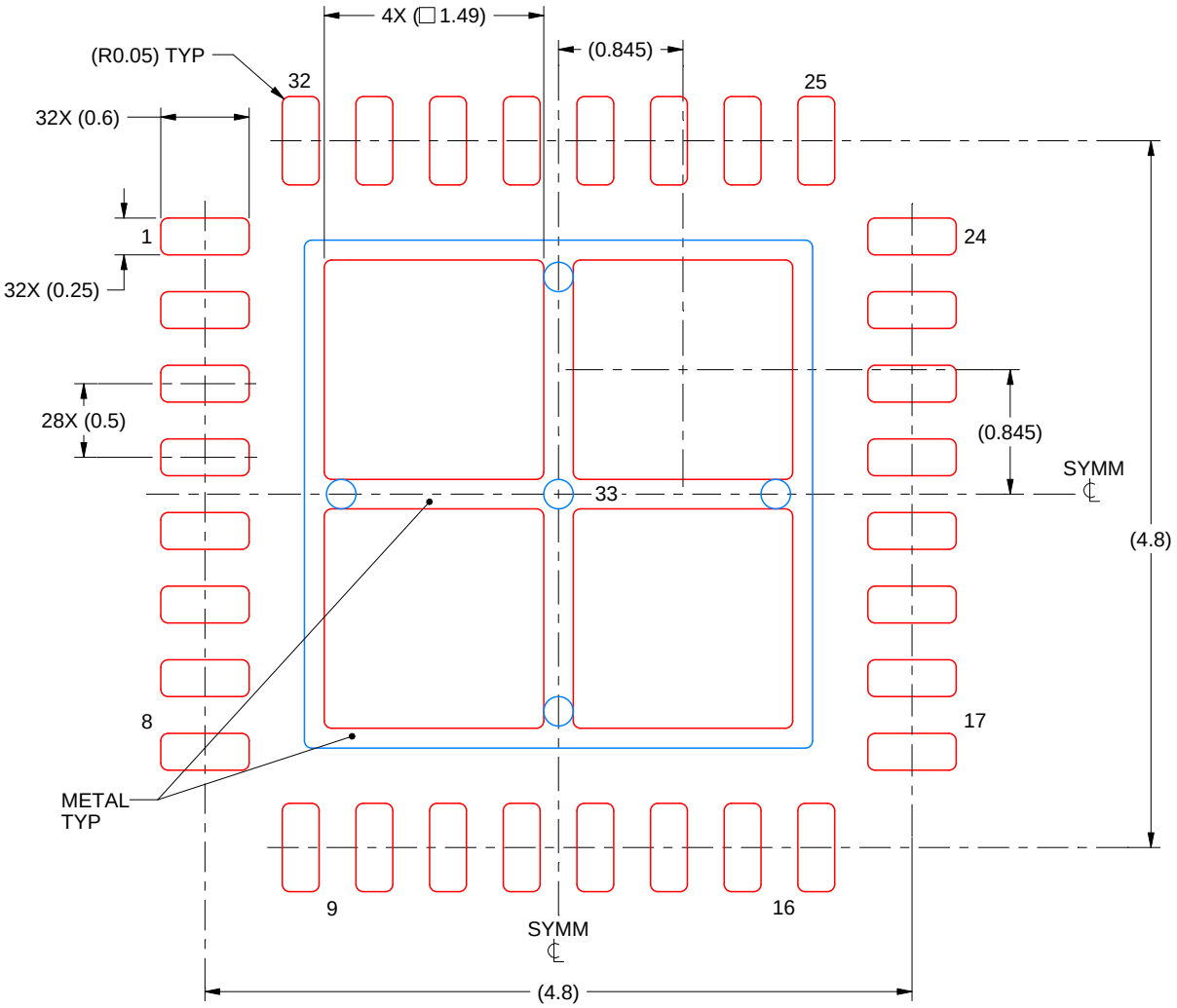


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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